32-bit RISC Microcontroller

TXZ Family

Reference manual
Trimming Circuit
(TRM-A)

Revision 3.0

2018-04

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related document

Document name
Clock Control and Operation Mode
32-bit Timer Event Counter

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of two or more same kind of units and channels in same register name in the Register List.

  In case of unit, "x" means A, B, and C ..
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2..
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

CG	Clock control and Operation Mode
TRM	Trimming circuit

The TXZ™ family has the trimming function to adjust the frequency of the internal high speed oscillator.

1. Outlines

The trimming circuit (TRM) can adjust the frequency for a internal oscillator.
The lists of functions are as follows.

Function Classification	Function	Operation
Frequency adjustment of the internal oscillator	Target oscillator	Internal High Speed Oscillator 1 (IHOSC1)
	Adjustment range	Coarse trimming -18.8 to +30.4 % (Average 0.8 % step) Fine trimming -0.8 to +0.7 % (0.1 % step)
	Monitor function	The reading of the initial trimming level is possible
Protection	Protection function	Incorrect writing is prevented.

2. Configuration

The configuration of the trimming circuit is shown as follows.

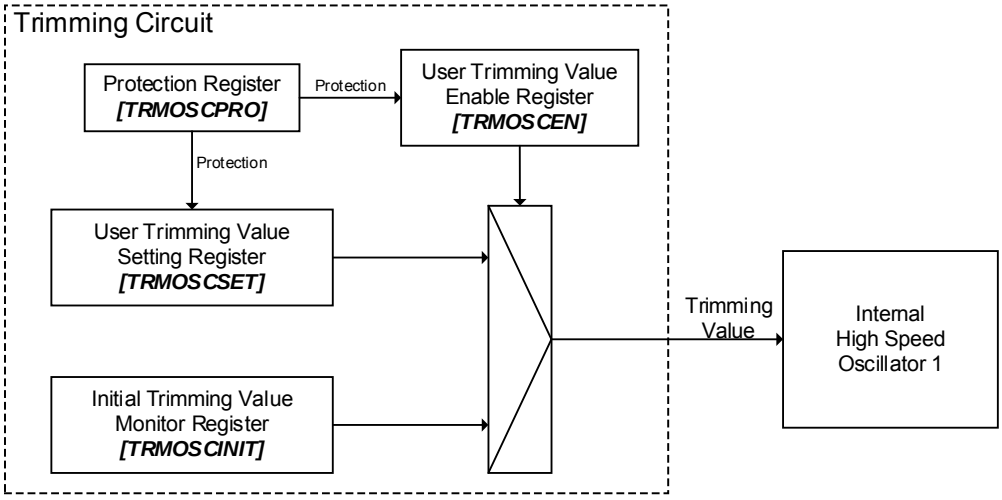

Figure 2.1 Trimming circuit Configuration

3. Function and Operation

The Internal High Speed Oscillator 1 (IHOSC1) for the system clocks can adjust frequency by the trimming circuit (TRM). The initial trimming level monitor register (***[TRMOSCINIT]***) can confirm the value that a factory trimmed before shipment.

When you use TRM, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A(***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B(***[CGFSYSENB]***,***[CGFSYSMENB]***), and fc supply stop registers (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in Reference manual.

3.1. Adjustment

As for ***[TRMOSCSET]*** (user trimming value setting register) and ***[TRMOSCEN]*** (user trimming value enabling register), the protection is carried out after reset. And the writing is forbidden. In order to write in, please write "0xC1" in ***[TRMOSCPRO]*** <PROTECT> (protection register), and remove the protection.

The adjustment of the frequency is made by fine trimming and coarse trimming. Please set the trimming value in <TRIMSETC>/<TRIMSETF> of the user trimming level setting register(***[TRMOSCSET]***).

When ***[TRMOSCEN]*** <TRIMEN> is set to "1", the trimming value is updated in a user trimming value from an initial trimming value.

Oscillating frequency is varied by change of temperature or power supply voltage, the stress from the outside, etc. Therefore, please perform trimming before operation in which the accuracy of frequency is needed, or regularly.

3.2. Adjustment Range

About the adjustment range, the fine trimming is available for the adjustment of 16 steps. Please perform the setup by ***[TRMOSCSET]***<TRIMSETF[3:0]>. In addition, the coarse trimming is available for the adjustment of 64 steps. Please perform the setup by ***[TRMOSCSET]***<TRIMSETC[5:0]>.

Please refer to "Table 3.1 Adjustment range of the fine trimming (Sampled value)" and "Table 3.2 Adjustment range of the coarse trimming (Sampled value) " for the range of adjustment.

Table 3.1 Adjustment range of the fine trimming (Sampled value)

Fine Trimming			
+ Value		- Value	
<TRIMSETF[3:0]>	Frequency Change (typ.)	<TRIMSETF[3:0]>	Frequency Change (typ.)
0111	0.7%	1111	-0.1%
0110	0.6%	1110	-0.2%
0101	0.5%	1101	-0.3%
0100	0.4%	1100	-0.4%
0011	0.3%	1011	-0.5%
0010	0.2%	1010	-0.6%
0001	0.1%	1001	-0.7%
0000	0%	1000	-0.8%

Table 3.2 Adjustment range of the coarse trimming (Sampled value)

Coarse Trimming			
+ Value		- Value	
<TRIMSETC[5:0]>	Frequency Change (typ.)	<TRIMSETC[5:0]>	Frequency Change (typ.)
011111	30.4%	111111	-0.8%
011110	29.1%	111110	-1.5%
011101	27.8%	111101	-2.2%
011100	26.6%	111100	-2.9%
011011	25.4%	111011	-3.5%
011010	24.2%	111010	-4.2%
011001	23.0%	111001	-4.9%
011000	21.8%	111000	-5.5%
010111	20.8%	110111	-6.2%
010110	19.7%	110110	-6.8%
010101	18.6%	110101	-7.4%
010100	17.6%	110100	-8.1%
010011	16.5%	110011	-8.7%
010010	15.4%	110010	-9.3%
010001	14.5%	110001	-9.9%
010000	13.5%	110000	-10.5%
001111	12.5%	101111	-11.0%
001110	11.5%	101110	-11.6%
001101	10.7%	101101	-12.2%
001100	9.7%	101100	-12.7%
001011	8.8%	101011	-13.2%
001010	8.0%	101010	-13.8%
001001	7.1%	101001	-14.3%
001000	6.2%	101000	-14.8%
000111	5.4%	100111	-15.4%
000110	4.6%	100110	-15.9%
000101	3.8%	100101	-16.3%
000100	3.0%	100100	-16.9%
000011	2.2%	100011	-17.3%
000010	1.5%	100010	-17.8%
000001	0.7%	100001	-18.3%
000000	0.0%	100000	-18.8%

4. Registers

The trimming registers for the Internal High Speed Oscillator 1 (IHOSC1) are described below.

4.1. List of Registers

The trimming control registers and their addresses for the Internal High Speed Oscillator 1 (IHOSC1) are shown as follows:

Peripheral function		Channel/Unit	Base address		
			TYPE 1	TYPE 2	TYPE3
Trimming Circuit	TRM	-	0x400F3200	0x400E3100	0x40083100

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register Name		Base Address (Base+)
Protection Register	***[TRMOSCPRO]***	0x0000
User Trimming Value Enable Register	***[TRMOSCEN]***	0x0004
Initial Trimming Value Monitor Register	***[TRMOSCINIT]***	0x0008
User Trimming Value Setting Register	***[TRMOSCSET]***	0x000C

4.2. Register Description

4.2.1. *[TRMOSCPRO]* (Protection Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Read as “0”
7:0	PROTECT[7:0]	0x00	R/W	Protect control 0xC1: Protect function release. Other than 0xC1: Protect set

4.2.2. *[TRMOSCEN]* (User Trimming Value Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as “0”
0	TRIMEN	0	R/W	User trimming value enable control 0: Disabled (Use initial trimming value) 1: Enabled (Use user trimming value)

4.2.3. *[TRMOSCINIT]* (Initial Trimming Value Monitor Register)

Bit	Bit Symbol	After Reset	Type	Function
31:14	-	0	R	Read as “0”
13:8	TRIMINITC[5:0]	Indeterminate	R	Initial coarse trimming value. The coarse trimming value at the time of shipment can be read.
7:4	-	0	R	Read as “0”
3:0	TRIMINITF[3:0]	Indeterminate	R	Initial fine trimming value. The fine trimming value at the time of shipment can be read.

4.2.4. *[TRMOSCSET]* (User Trimming Value Setting Register)

Bit	Bit Symbol	After Reset	Type	Function
31:14	-	0	R	Read as “0”
13:8	TRIMSETC[5:0]	0x00	R/W	Coarse trimming value setting. Sets a coarse trimming value.
7:4	-	0	R	Read as “0”
3:0	TRIMSETF[3:0]	0x0	R/W	Fine trimming value setting. Sets a fine trimming value.

5. Usage Example

5.1. Internal oscillation frequency trimming using 32-bit Timer Event Counter (T32A)

The capture function of the T32A can be used to measure frequencies of the Internal High Speed Oscillator 1.
For more information about the T32A, please refer to "32-bit Timer Event Counter" of the reference manual.

5.1.1. Input of Reference Clock to T32AxINAx Pin

The prescaler output (ΦT0) is set to the count clock of the T32A. And the internal high speed oscillator is selected.
The reference clock is input to the T32AxINAx pin. Using the pulse width measurement function, the up counter value is captured on the rising edge of the reference clock.
The trimming value is calculated with the difference between the frequency of the captured reference clock and the frequency of the input reference clock.

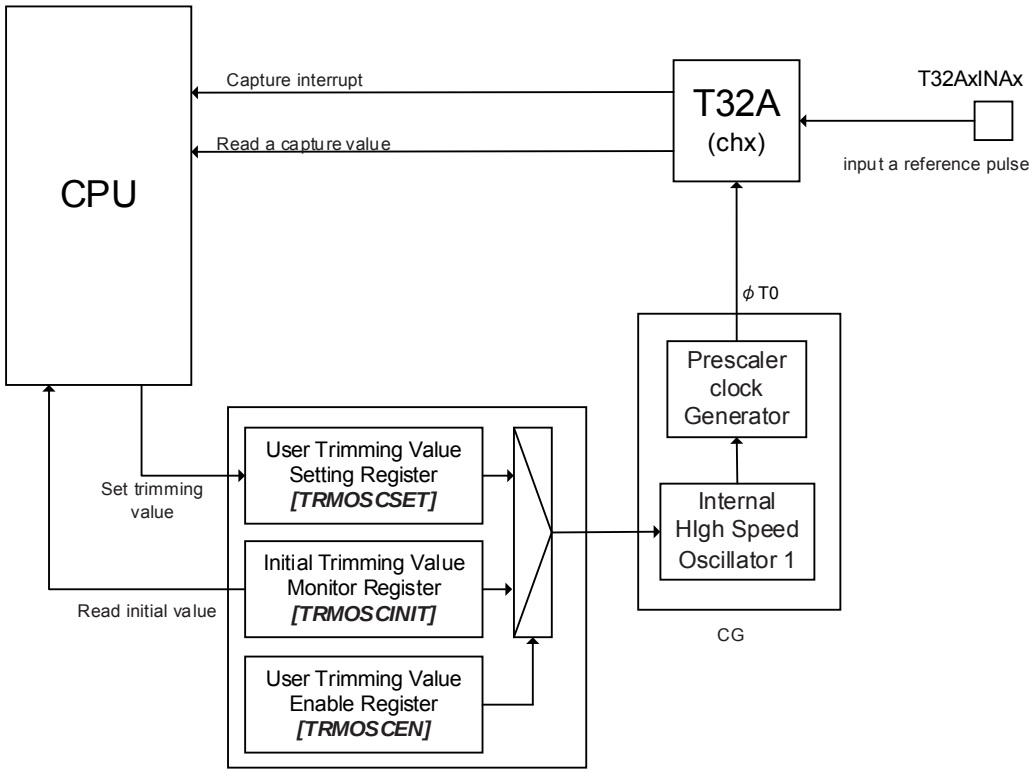

Figure 5.1 Example : Input of Reference Clock to T32AxINAx Pin

A trimming level calculation and a setting example:

<Conditions>
- Reference clock frequency: 10Hz (Input clock to the T32AxINAx pin)
- Prescaler value: 1/16 (ΦT0 fc = Internal High Speed Oscillator 1 frequency)
- Prescaler division value in T32A: 1/1 (Capture trigger clock)
- Input to the T32AxINAx pin: Capture setting (CAPA0:Rising edge is selected)

(1) In the case of pulse width calculated value = 0xD6D8 (= 55000), it is at the one cycle of the reference signal.:
The frequency of the Internal High Speed Oscillator 1 is calculated as follows.

$$\text{Internal high speed oscillator 1 frequency} = \frac{1}{(1 / \text{Reference clock frequency}) / (\text{Pulse width calculated value}) / (1 / \text{Prescaler value})}$$

$$= \frac{1}{(1/10\ \text{Hz}) \ / \ (55000) \ / \ (1 / (1/16))}$$

$$= 8.8\ \text{MHz}$$

(2) The difference from the target frequency (10 MHz) of the oscillator 1 of the internal high speed is calculated.

- Frequency deviation (%) = 1 - ((Preadjustment frequency) / (Reference clock frequency))
  = 1 - (8.8 MHz / 10 MHz)
  = 0.12 = 12.0 %

(3) The fine and coarse trimming values are selected in Table 3.1 and Table 3.2, respectively: the total trimming values should be 12.0 % which is the calculated frequency deviation (%). Those values should be set to the User Trimming Value Setting Register (***[TRMOSCSET]***).

- Coarse trimming value: +12.6% * TRIMSETC[5:0] = 001110
- Fine trimming value: - 0.6% * TRIMSETF[3:0] = 1010

(4) The user trimming level is output to Internal High Speed Oscillator 1 by setting "1" to the ***[TRMOSCEN]*** <TRIMEN> after having set a trimming value.

(5) By the result, when retrimming is necessity, please repeat and perform the above mentioned operation. However, while ***[TRMOSCEN]*** <TRIMEN> has been "1", please perform.

Please write the data other than "0xC1" in protection control register ***[TRMOSCPRO]*** <PROTECT> after the end of trimming, and enable the protection function.

5.1.2. Input of fs on ch4 in Timer A

As for the following explanation, fs is connected to the internal trigger input of the T32A ch4 timer A, and the timer A output is the example connected to the internal trigger input of the timer B.

The fs is chosen as the internal trigger input of the timer A of T32A ch4, and the count clock of the timer A is set to the internal trigger (fs). By matching the count value(n) of the timer register A1 with the counter, invert the timer output A to create the reference signal (= fs / 2n).The output of ch4 of timer A is connected to ch4 of timer B. The count clock of timer B of T32A ch4 sets it to the prescaler output and, as φT0, chooses a internal high speed oscillation. In addition, timer B sets it for a pulse width measurement function and captures the value of the up counter in rising edge of the standard signal from timer A.

The trimming value is calculated with the difference between the frequency of the captured reference clock and the frequency of the input reference clock.

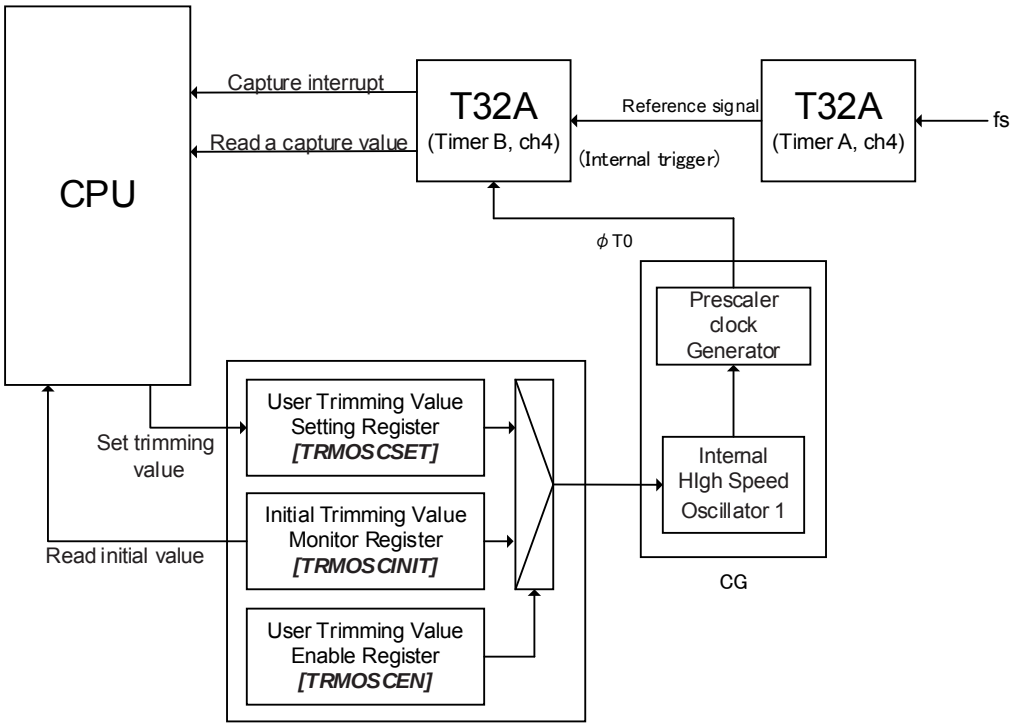

Figure 5.2 Example : Input of fs on ch4 in Timer A

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2017-09-08	First release
2.0	2018-02-27	Conventions: Revised 3.1. Adjustment Corrected: “<TRMSETC>”→” <TRIMSETC>” Corrected: “<TRMSETF>”→” <TRIMSETF>” 3.2. Adjustment Range Corrected: “<TRMSETC[5:0]>”→” <TRIMSETC[5:0]>” Corrected: “<TRMSETF[3:0]>”→” <TRIMSETF[3:0]>” 4.1. List of Registers Deleted: Headline “Function name” Corrected: Base address of TYPE2 “0x400F3100”→” 0x400E3100” Corrected: Note sentences “The base address type・・・・” →” Channel/Unit and Base address type・・・” 4.3. ***[TRMOSCEN]*** (User Trimming Value Enable Register) Corrected: Bit Symbol “TRMEN”→”TRIMEN” 4.4. ***[TRMOSCINIT]*** (Initial Trimming Value Monitor Register) Corrected: Bit Symbol “TRMINITC[5:0]”→” TRIMINITC[5:0]” Corrected: Bit Symbol “TRMINITF[3:0]”→” TRIMINITF[3:0]” 4.5. ***[TRMOSCSET]*** (User Trimming Value Setting Register) Corrected: Bit Symbol “TRMSETC[5:0]”→” TRIMSETC[5:0]” Corrected: Bit Symbol “TRMSETF[3:0]”→” TRIMSETF[3:0]” 5.1.1. Input of Reference Clock to T32AxINAx Pin Corrected: (3) Description “TRMSETC[5:0]”→” TRIMSETC[5:0]” “TRMSETF[3:0]”→” TRIMSETF[3:0]” Corrected: (4)(5) Description “<TRMEN>”→”<TRIMEN>”
3.0	2018-04-11	4.1 List of Registers Added base address of TYPE3 4.2 Detail of Register Modified 4.2 to 4.2.1, 4.3 to 4.2.2, 4.4 to 4.2.3, 4.5 to 4.2.4

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