32-bit RISC Microcontroller

TXZ/TXZ+ Family

Reference Manual
Advanced Encoder Input Circuit
(A-ENC-A)

Revision 2.3

2022-05

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

A-PMD	Advanced Programmable Motor Control Circuit
ADC	Analog to Digital Converter
BLDC	Brushless DC (Motor)
BEMF	Back Electromotive Force
CCW	Counter Clockwise
CW	Clockwise
PMD+	Programmable Motor Control Circuit Plus
PWM	Pulse Width Modulation

1. Outlines

The advanced encoder input circuit (A-ENC) can operate as an input circuit of one channel (ENCxA/ENCxB/ENCxZ) per 1 unit. Below, the list of functions is shown.

Function classification	Function	Functional Description
Sensor input	Encoder mode	It is the mode which connects and uses an AB or ABZ type incremental form encoder. In the combination of an Input Signal, a rotating direction is judged and count-up/down operation is carried out for every rotational edge.
	Sensor mode (Event count)	It is the mode which connects and uses the Hall IC (U, V, W) of a 2-phase or a 3-phase circuit. Whenever it detects the edge of U, V, and W of a Hall IC, count-up/down operation of a pulse is performed. In the combination of an Input Signal, a rotating direction is judged and count-up/down operation is carried out.
	Sensor mode (Timer count)	It is the mode which connects and uses the Hall IC (U, V, W) of a 2-phase or a 3-phase circuit. Measure the interval of edge detection of U, V, W of Hall IC. The rotation direction can be judged by a combination of input signals. The commutation trigger to the Programmable Motor Control Circuit (PMD) in sync with edge detection is generable. In a PWM synchronous sampling, it can respond to sensorless control of the brushless DC (BLDC) motor of a square-wave mode.
	Sensor mode (Phase count)	It is the mode which connects and uses the Hall IC (U, V, W) of a 2-phase or a 3-phase circuit. 16-bit counter operation is carried out with the clock of arbitrary frequency, and the interval of edge detection of U, V, and W of a Hall IC can be measured. A rotating direction can be judged in the combination of Input signals. Up/down operation can be chosen.
General purpose timer	Timer mode	It is the mode which can be used as 32 bit timers which operate by fsys. Capture by an ENCxZ input can be performed.
Phase counter	Phase counter mode (Phase measurement)	It is the mode which measures the phase at the time of the edge detection of an ENCxZ input, with a 16-bit counter which operates with the clock of arbitrary frequency. Interrupt generating by a comparison function can be performed.
	Phase counter mode (Phase difference measurement)	With the 16-bit counter which operates with the clock of arbitrary frequency, the phase difference between a general-purpose timer output and an ENCxZ input can be measured.
Noise Canceller	Input circuit	The sampling with a fsys dividing clock or the sampling in sync with a PWM signal can be performed. Noise cancel width can be chosen.

Table 1.1 Signal input pin

Signal name		Encoder A, B, Z	Hall sensor U, V, W
Connecting terminal	ENCxA	A	U
	ENCxB	B	V
	ENCxZ	Z	W

2. Configuration

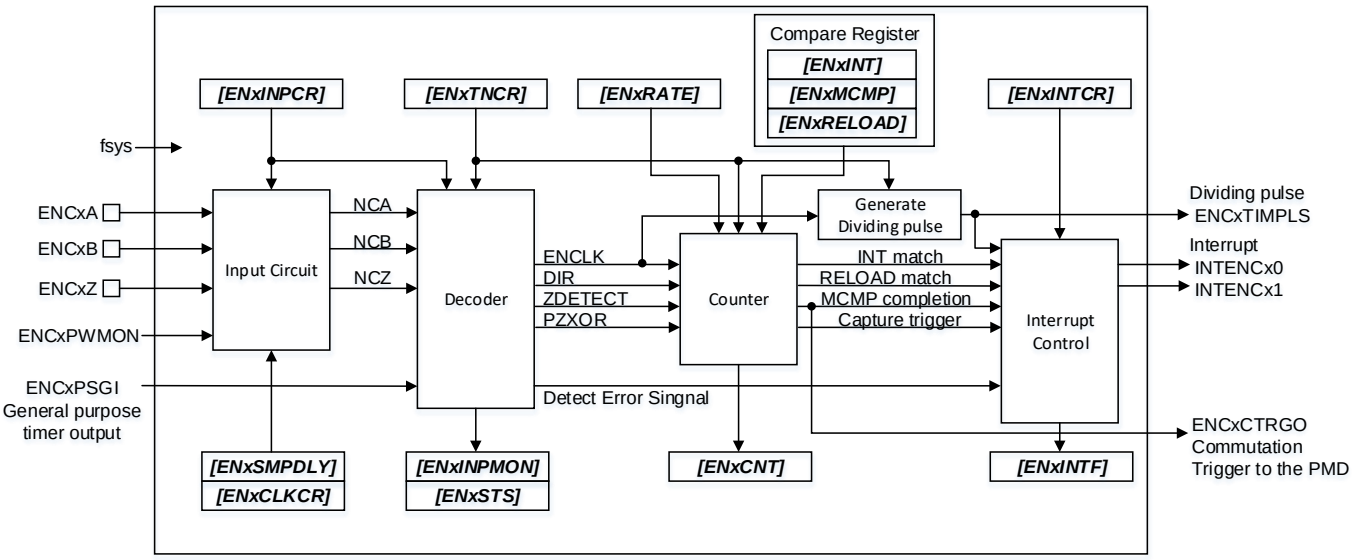


Figure 2.1 A-ENC Block Diagram

Table 2.1 List of Signals

No	Symbol	Signal name	I/O	Related Reference manual
1	fsys	System clock	Input	Clock Control and Operation Mode
2	ENCxA	Encoder input A pin	Input	Product Information
3	ENCxB	Encoder input B pin	Input	Product Information
4	ENCxZ	Encoder input Z pin	Input	Product Information
5	ENCxPWMON	PWM signal for sampling	Input	Product Information
6	ENCxCTRGO	The commutation trigger to the PMD	Output	Product Information
7	ENCxPSGI	General purpose timer output signal	Input	Product Information
8	ENCxTIMPLS	Divided pulse signal	Output	Product Information
9	INTENCx0	Encoder input interrupt 0	Output	Exception, Product Information
10	INTENCx1	Encoder input interrupt 1	Output	Exception

3. Function and Operation

3.1. Clock Supply

When using A-ENC, set an applicable clock enable bit to "1" (Clock supply) in clock supply and stop register A for fsys (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), clock supply and stop register B for fsys (***[CGFSYSENB]*** and ***[CGFSYSMENB]***), clock supply and stop register C for fsys (***[CGFSYSMENC]***), and clock supply and stop register for fc (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

3.2. Operation Mode

The operation mode is determined with ***[ENxTNCR]***<MODE[2:0]>, <P3EN>, and <ZEN>. They are 13 types in total. The fields should not be set to other combinations.

The following table lists the operation mode settings:

Table 3.1 Setting of operation mode

[ENxTNCR]			Input pin	Mode
<MODE[2:0]>	<ZEN>	<P3EN>		
000	0	0	ENCxA, ENCxB	Encoder mode (without the ENCxZ)
	1		ENCxA, ENCxB, ENCxZ	Encoder mode (use of the ENCxZ)
001	0	0	ENCxA, ENCxB	Sensor mode (event count and the 2-phase input)
		1	ENCxA, ENCxB, ENCxZ	Sensor mode (event count and the 3-phase input)
010	0	0	ENCxA, ENCxB	Sensor mode (timer count and the 2-phase input)
		1	ENCxA, ENCxB, ENCxZ	Sensor mode (timer count and the 3-phase input)
011	0	0	-	Timer mode
	1		ENCxZ	Timer mode (use of the ENCxZ)
110	0	0	ENCxA, ENCxB	Sensor mode (phase count and the 2-phase input)
		1	ENCxA, ENCxB, ENCxZ	Sensor mode (phase count and the 3-phase input)
111	0	0	-	Phase counter mode (phase measurement)
	1		ENCxZ	Phase counter mode (phase measurement and use of the ENCxZ)
	1	1	ENCxZ	Phase counter mode (phase difference measurement and use of the ENCxZ)

3.2.1. Encoder Mode

The A-ENC supports the high-speed position sensor (phase determination) that determines the phase input from the incremental encoder (AB encoder or ABZ encoder).

- Rotational edge detection is performed, a divided pulse is output, and an interrupt can be generated.
- Rotational edge pulses are counted and an interrupt can be generated at the specified counter value.
- Determines the rotational direction.
- Up/down count (controlled by the rotational direction)
- Sets the range of counts.
- Sets the rotational direction for the detection.
- An abnormal error detection flag is available.

(1) The ENCxZ input is enabled. (***[ENxTNCR]***<ZEN>=1)

[ENxRELOAD]<RELOADH[15:0]>=0x0380, ***[ENxINT]***<INTH[15:0]>=0x0002

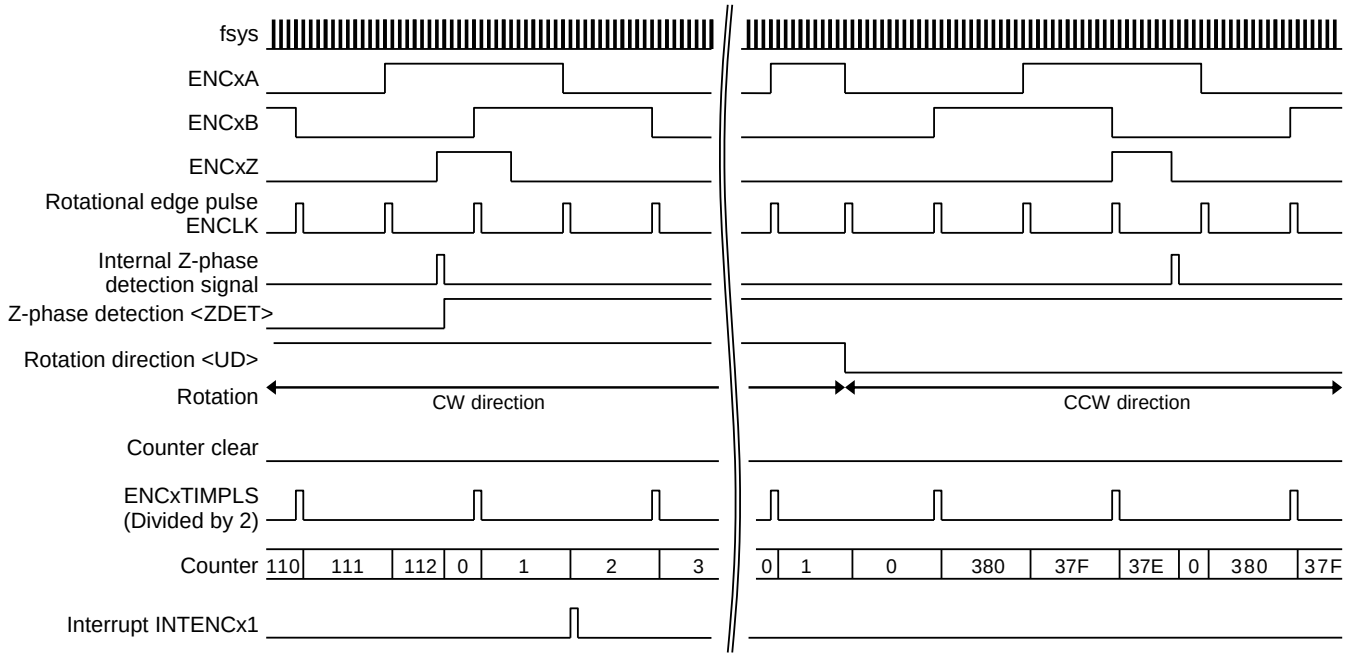


Figure 3.1 ENCxZ input enabled (*[ENxTNCR]*<ZEN>=1)

(2) The ENCxZ input is disabled. (***[ENxTNCR]***<ZEN>=0)

[ENxRELOAD]<RELOADH[15:0]>=0x0380, ***[ENxINT]***<INTH[15:0]>=0x0002

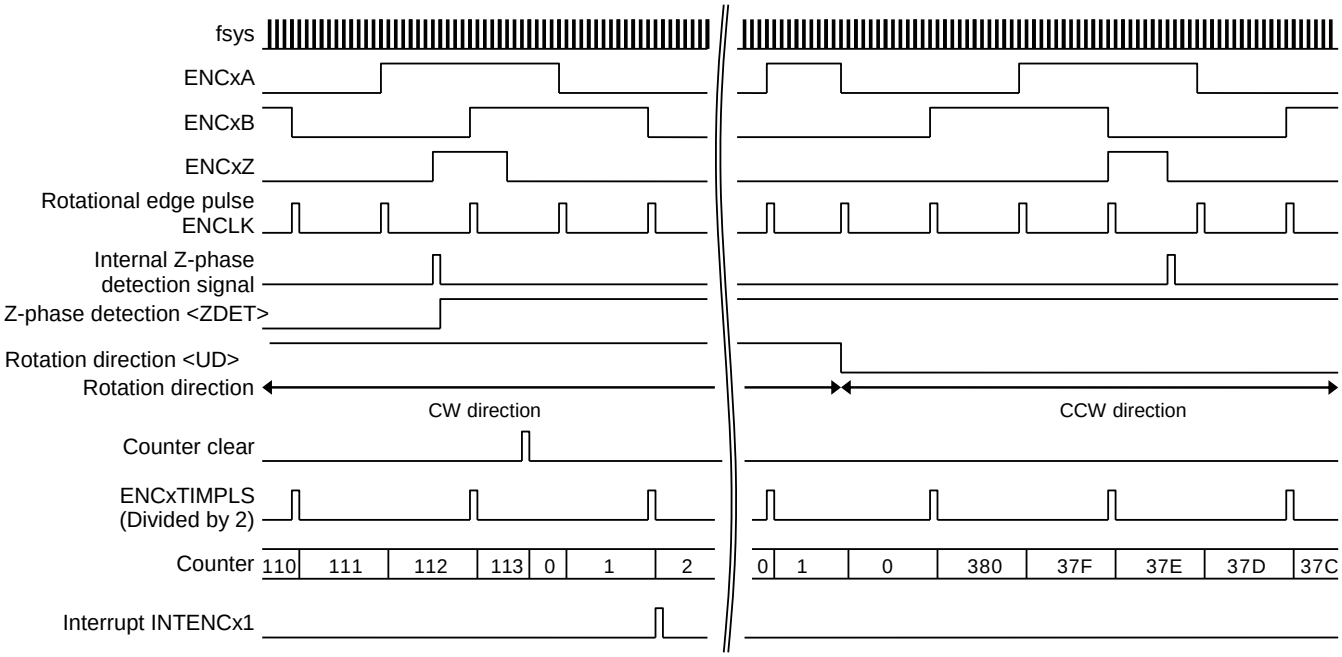


Figure 3.2 ENCxZ input is disabled (*[ENxTNCR]*<ZEN>=0)

In encoder mode, the incremental encoder inputs should be connected to the ENCxA, ENCxB, and ENCxZ pins. The encoder multiplies the ENCxA and the ENCxB signals by 4 to count the rotational edge pulses.

During the CW rotation (i.e., ENCxA has the 90-degree phase lead to ENCxB), the counter counts up; when the value of the counter reaches the value of <RELOADH>, the counter is cleared to "0x0000" on the next ENCLK.

During the CCW rotation (i.e., ENCxA has the 90-degree phase lag to ENCxB), the counter counts down; when the value of the counter reaches "0x0000", the counter is set to the value of <RELOADH> on the next ENCLK.

Additionally, when <ZEN>=1, the counter is cleared to "0x0000" on the rising edge of ENCxZ during the CW rotation and on the falling edge of ENCxZ during the CCW rotation. If the ENCLK matches ENCxZ detection timing, the counter is cleared to "0x0000" without increment or decrement.

When "1" is written to ***[ENxTNCR]***<ENCLR>, the counter is cleared to "0x0000".

[ENxSTS]<UD> is set to "1" during the CW rotation and is cleared to "0" during the CCW rotation.

The detection direction (CW direction or CCW direction) can be set with ***[ENxTNCR]***<DECMD[1:0]>. Except when <DECMD>=00, a rotational edge is detected based on the comparison between the input status (***[ENxINPMON]***<DETMONA>, <DETMONB>, <DETMONZ>) at the previously detected edge and the current input value.

ENCxTIMPLS is a division of ENCLK, and the division ratio is selected by ***[ENxTNCR]***<ENDEV>.

When ***[ENxINTCR]***<CMPIE>=1, if the value of <INTH> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE>=1, if the value of ***[ENxMCMP]***<MCMPH[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

However, when <ZEN>=1, a match interrupt does not occur during ***[ENxSTS]***<ZDET>=0. After the encoder input is enabled, if the A-ENC detects the first ENCxZ, <ZDET> is set to "1".

<ZDET> and ***[ENxSTS]***<UD> are cleared to "0" when ***[ENxTNCR]***<ENRUN>=0.

3.2.2. Sensor Mode

The counter supports low-speed position sensing (zero-cross determination) to deal 2-phase Hall sensor input and 3-phase Hall sensor input. There are three modes, event count mode, timer count mode, and phase count mode.

In timer count mode or phase count mode, when a BLDC motor is driven on rectangular waveforms from the PMD, the A-ENC can perform zero-cross detection of an induced voltage using PWM synchronous sampling. (BEMF Detection Control)

3.2.2.1. Event Count

The counter counts using rotational edge detection.

- Rotational edge detection is performed, a divided pulse is output, and an interrupt can be generated.
- Rotational edge pulses are counted and an interrupt can be generated at the specified counter value.
- Determines the rotational direction.
- Sets up- or down count (controls by the determination of rotational direction).
- Specifies the rotational detection direction.
- Abnormal error detection flag

(1) 3-phase decoding (***[ENxTNCR]***<P3EN>=1)

[ENxINT]<INTH[15:0]>=0x0002

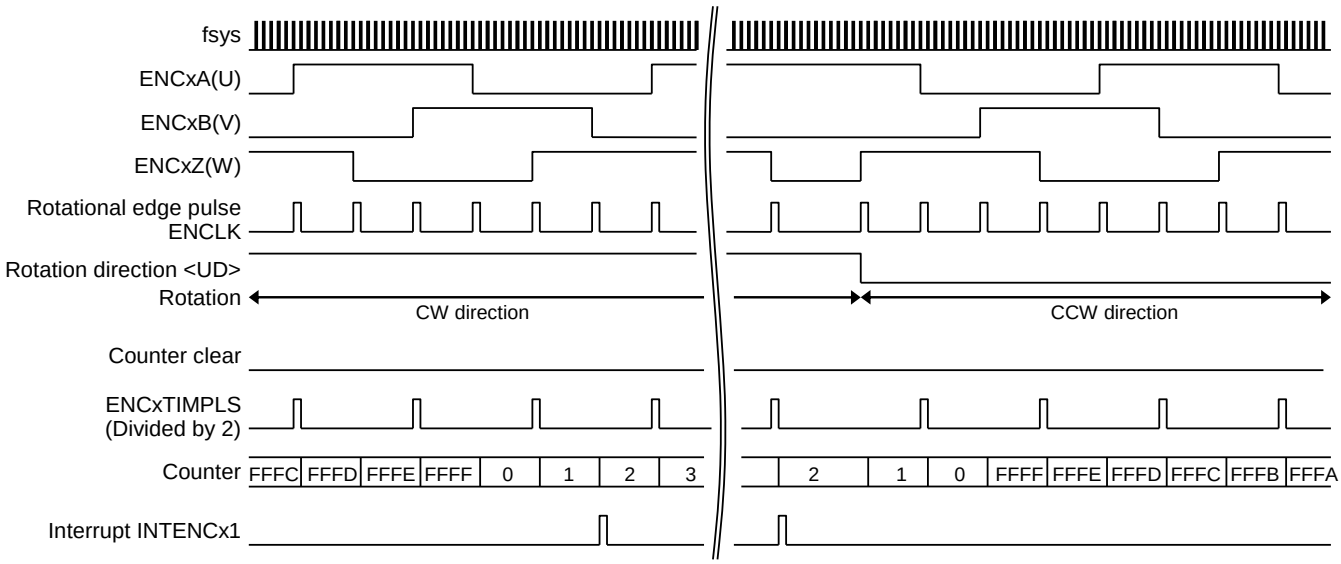


Figure 3.3 3-phase decoding (*[ENxTNCR]*<P3EN>=1)

(2) 2-phase decoding (***[ENxTNCR]***<P3EN>=0)

[ENxINT]<INTH[15:0]>=0x0002

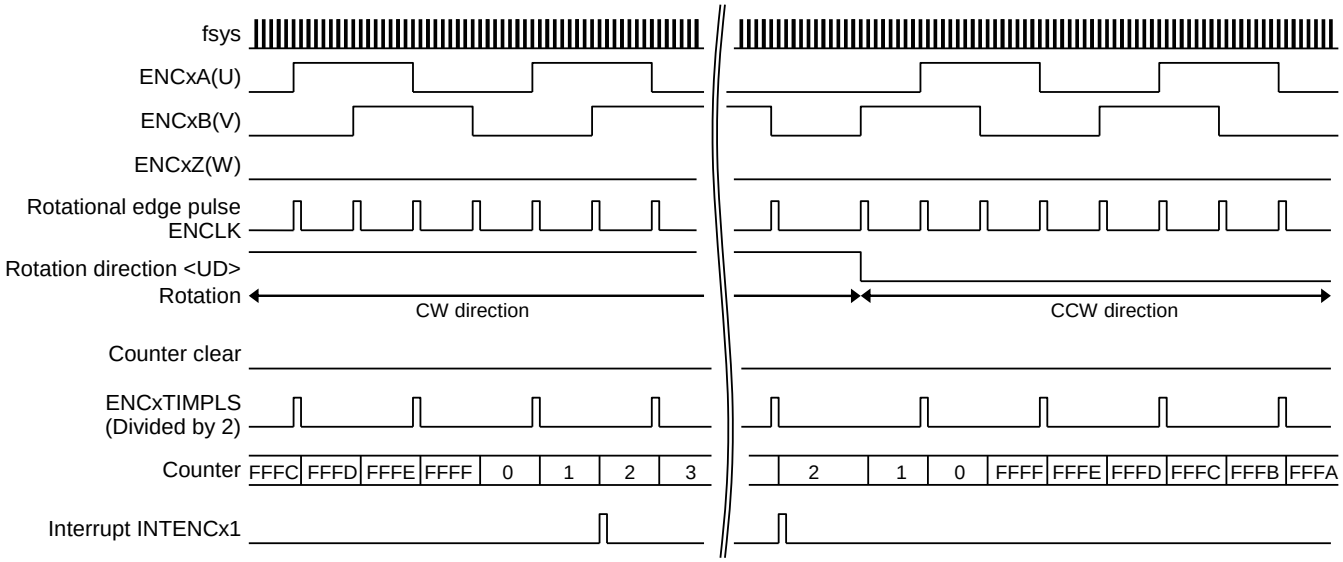


Figure 3.4 2-phase decoding (*[ENxTNCR]*<P3EN>=0)

Hall sensor inputs (U, V, and W) should be connected to ENCxA, ENCxB, and ENCxZ. When <P3EN>=0, the counter multiplies a 2-phase input (ENCxA or ENCxB) by 4; when <P3EN>=1, the counter multiplies a 3-phase input (ENCxA, ENCxB, or ENCxZ) by 6. After that, the counter counts the Rotational edge pulse.

During the CW rotation (i.e., ENCxA has 90-degree (2-phase input) or 120-degree (3-phase input) phase lead to ENCxB channel), the counter performs up counting. When the value of the counter reaches "0xFFFF", the counter is cleared to "0x0000" on the next ENCLK.

During the CCW rotation (i.e., ENCxA has 90-degree (2-phase input) or 120-degree (3-phase input) phase lag to ENCxB), the counter performs down counting. When the value of the counter reaches "0x0000", the counter is set to "0xFFFF" on the next ENCLK.

When "1" is written to ***[ENxTNCR]***<ENCLR>, the counter is cleared to "0x0000".

When the CW rotation is detected, ***[ENxSTS]***<UD> is set to "1". When the CCW rotation is detected, ***[ENxSTS]*** <UD> is cleared to "0".

The detection direction (CW direction or CCW direction) can be set with ***[ENxTNCR]***<DECMD[1:0]>. Except when <DECMD>=00, a rotational edge is detected based on the comparison between the input status (***[ENxINPMON]***<DETMONA>, <DETMONB>, <DETMONZ>) at the previously detected edge and the current input value.

ENCxTIMPLS is a division of ENCLK, and the division ratio is selected by ***[ENxTNCR]***<ENDEV>.

When ***[ENxINTCR]***<CMPIE>=1, if the value of <INTH> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE>=1, if the value of <MCMPH> and the counter value become equal, an INTENCx1 interrupt occurs.

3.2.2.2. Timer Count

(1) 3-phase decoding (***[ENxTNCR]***<P3EN>=1)

[ENxINT]<INTH[15:0]><INTL[15:0]>=0x00000002

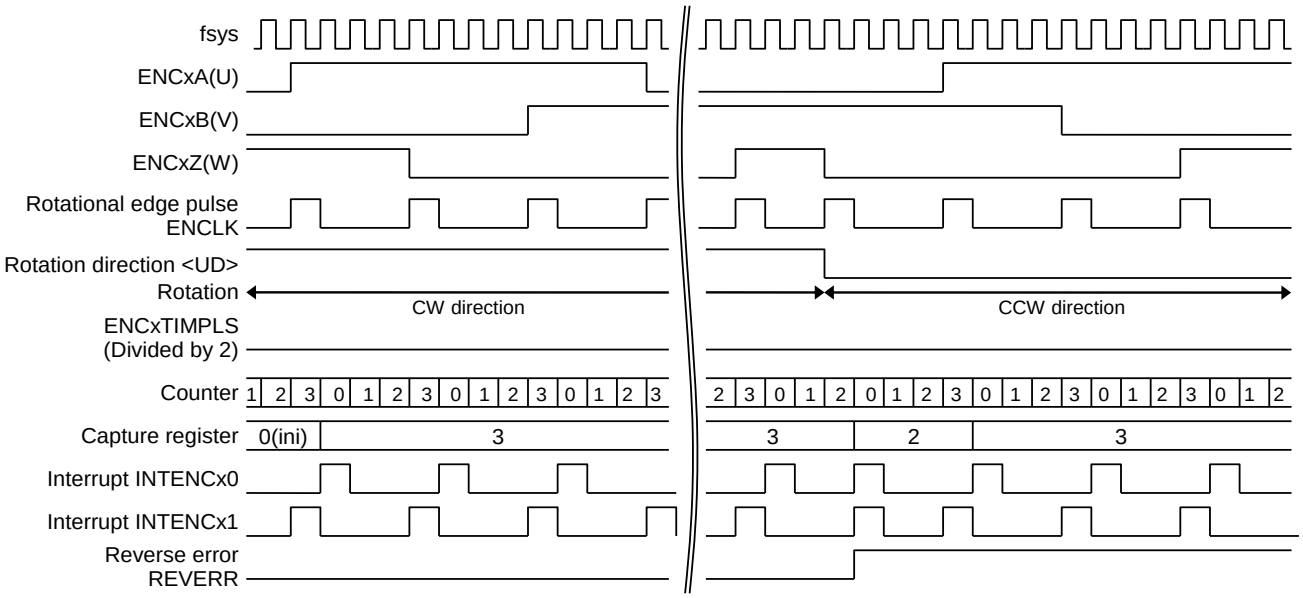


Figure 3.5 3-phase decoding (*[ENxTNCR]*<P3EN>=1)

(2) 2-phase decoding (***[ENxTNCR]***<P3EN>=0)

[ENxINT]<INTH[15:0]><INTL[15:0]>=0x00000002

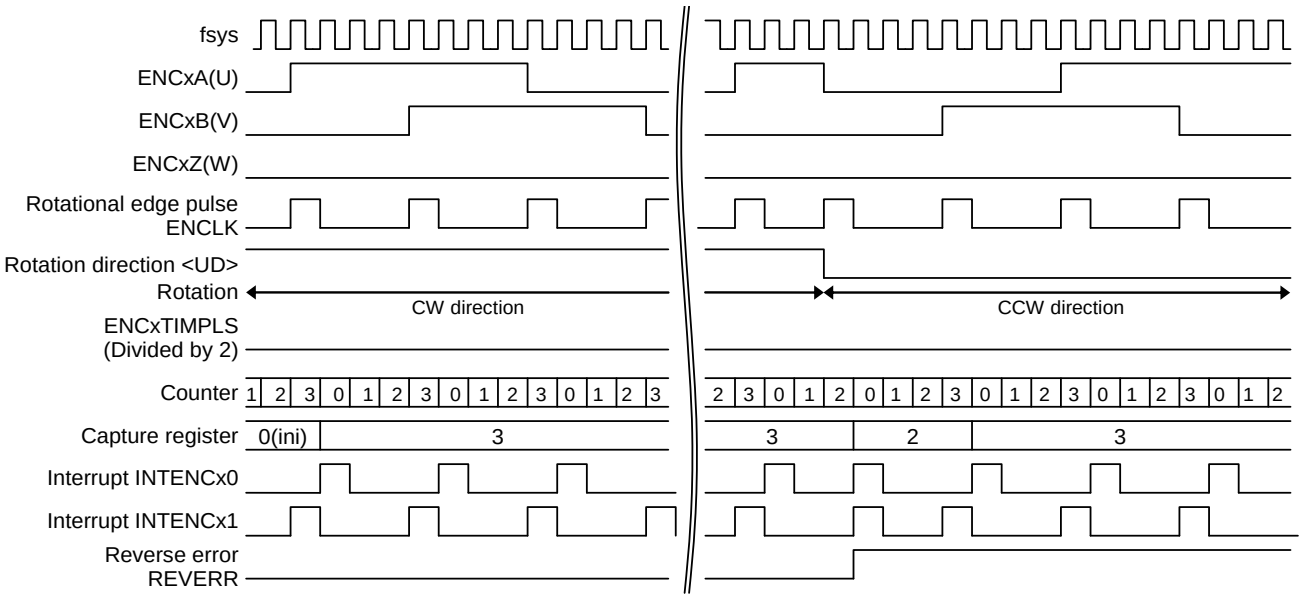


Figure 3.6 2-phase decoding (*[ENxTNCR]*<P3EN>=0)

Hall sensor inputs (U, V, and W) should be connected to ENCxA, ENCxB, and ENCxZ. When <P3EN>=0, the counter multiplies a 2-phase input (ENCxA or ENCxB) by 4; when <P3EN>=1, the counter multiplies a 3-phase input (ENCxA, ENCxB, or ENCxZ) by 6. After that, the counter generates a 4-fold or 6-fold rotational edge pulse (ENCLK).

The counter always performs up counting and is cleared to "0x00000000" on ENCLK. When "1" is written to ***[ENxTNCR]***<ENCLR>, the counter is cleared to "0x00000000".

The counter value is captured on ENCLK. The captured value can be read from the ***[ENxCNT]*** register.

When "1" is written to ***[ENxTNCR]***<SFTCAP>, the counter value is captured. The timing of capturing can be specified by the user. The captured value can be read from the ***[ENxCNT]*** register.

The value of the ***[ENxCNT]*** register (captured value) is maintained regardless of the value of ***[ENxTNCR]*** <ENRUN>.

When the CW rotation is detected, ***[ENxSTS]***<UD> is set to "1". When the CCW rotation is detected, ***[ENxSTS]*** <UD> is cleared to "0". When <ENRUN>=0, <UD> is cleared to "0". If the rotational direction is reversed, ***[ENxSTS]***<REVERR> is set to "1". This flag is cleared upon reading.

The detection direction (CW direction or CCW direction) can be set with ***[ENxTNCR]***<DECMD[1:0]>.
Except when <DECMD>=00, a rotational edge is detected based on the comparison between the input status ***[ENxINPMON]***<DETMONA><DETMONB><DETMONZ> at the previously detected edge and the current input value.

When ***[ENxINTCR]***<RLDIE>=1, if the value of ***[ENxRELOAD]***<RELOADH[15:0]><RELOADL[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<CMPIE>=1, if the value of ***[ENxINT]***<INTH[15:0]><INTL[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE>=1, if the value of ***[ENxMCMP]***<MCMPH[15:0]><MCMPL[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs. When ***[ENxTNCR]***<MCMPMD>=1, if the counter value is the value of <MCMPH> or more, an INTENCx1 interrupt occurs.

3.2.2.3. Phase Count

(1) 3-phase decoding (***[ENxTNCR]***<P3EN>=1)

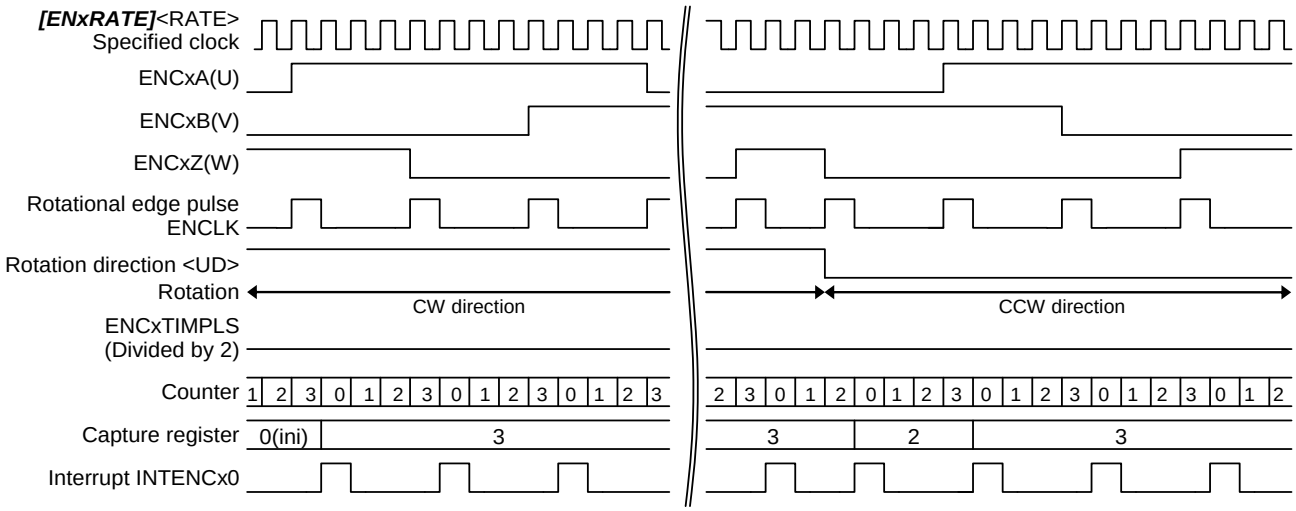


Figure 3.7 3-phase decoding (*[ENxTNCR]*<P3EN>=1)

(2) 2-phase decoding (***[ENxTNCR]***<P3EN>=0)

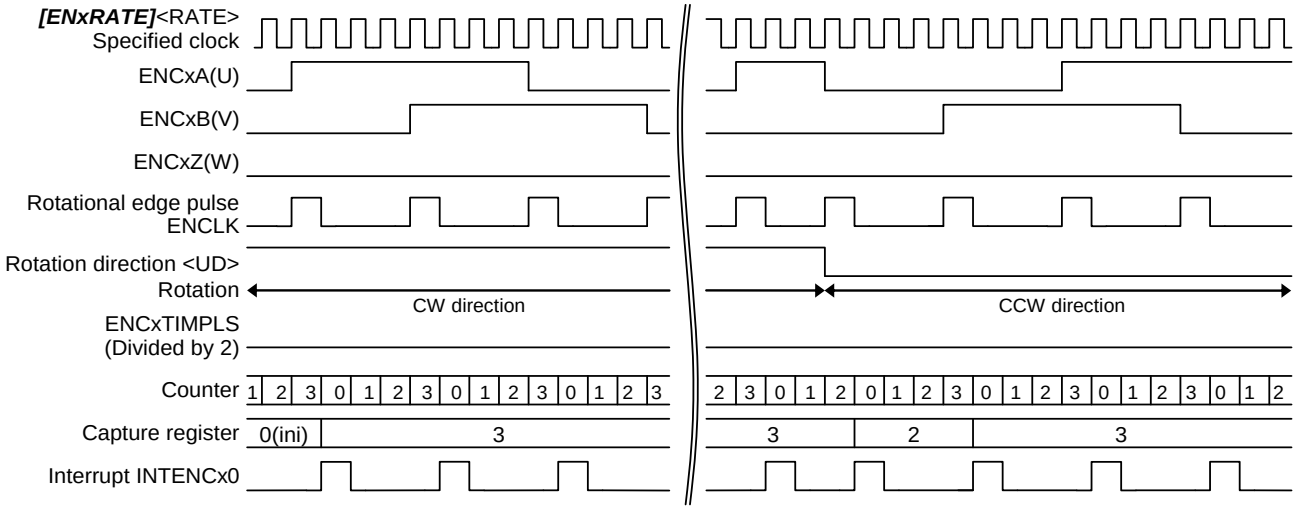


Figure 3.8 2-phase decoding (*[ENxTNCR]*<P3EN>=0)

Hall sensor inputs (U, V, and W) should be connected to ENCxA, ENCxB, and ENCxZ. When <P3EN>=0, the counter multiplies a 2-phase input (ENCxA or ENCxB) by 4; when <P3EN>=1, the counter multiplies a 3-phase input (ENCxA, ENCxB, or ENCxZ) by 6. After that, the counter generates a 4-fold or 6-fold rotational edge pulse (ENCLK).

The counter can be set to up/down count by the <UDMD> setting and the ***[ENxRATE]*** register setting at the specified frequency. When the counter is set to up count, if the value of the counter and the value of <RELOADH> become equal, the counter is cleared to "0x0000". When the counter is set to down count, if the value of the counter reaches "0x0000", the counter is set to the value of <RELOADH>.

When "1" is written to <ENCLR>, the counter is cleared to "0x0000".

When <TOVMD>=1, the counter stops at the value of <RELOADH>.

The counter value is captured on ENCLK. The captured value can be read from the ***[ENxCNT]*** register.

When "1" is written to <SFTCAP>, the counter value is captured. The timing of capturing can be specified by the user. The captured value can be read from the ***[ENxCNT]*** register.

The value of the ***[ENxCNT]*** register (captured value) is maintained regardless of the value of <ENRUN>.

When the CW rotation is detected, <UD> is set to "1". When the CCW rotation is detected, <UD> is cleared to "0". When <ENRUN>=0, <UD> is cleared to "0".

The detection direction (CW direction or CCW direction) can be set with ***[ENxTNCR]***<DECMD[1:0]>. Except when <DECMD>=00, a rotational edge is detected based on the comparison between the input status ***[ENxINPMON]***<DETMONA><DETMONB><DETMONZ> at the previously detected edge and the current input value.

When ***[ENxINTCR]***<CMPIE>=1, if the value of ***[ENxINT]***<INTH[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE>=1, if the value of ***[ENxMCMP]***<MCMPH[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

3.2.3. Timer Mode

This mode can be used as a general-purpose 32-bit timer.

- 32-bit up counter (counts using the fsys clock)
- Counter clear control (software clear, compare match clear, and external trigger)
- A match interrupt occurs using the compare function.
- Capture functions: external trigger capture (interrupt can be generated), software capture

(1) The ENCxZ input is enabled. (***[ENxTNCR]***<ZEN>=1)

[ENxINT]<INTH[15:0]><INTL[15:0]>=0x00000006

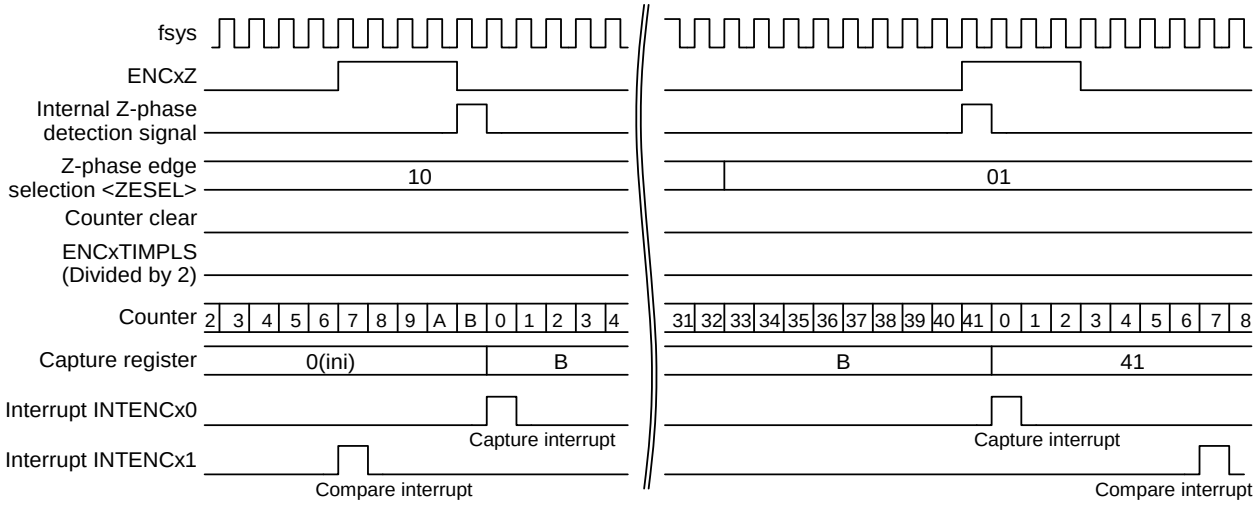


Figure 3.9 ENCxZ input is enabled. (*[ENxTNCR]*<ZEN>=1)

(2) The ENCxZ input is disabled. (***[ENxTNCR]***<ZEN>=0)

[ENxINT]<INTH[15:0]><INTL[15:0]>=0x00000006

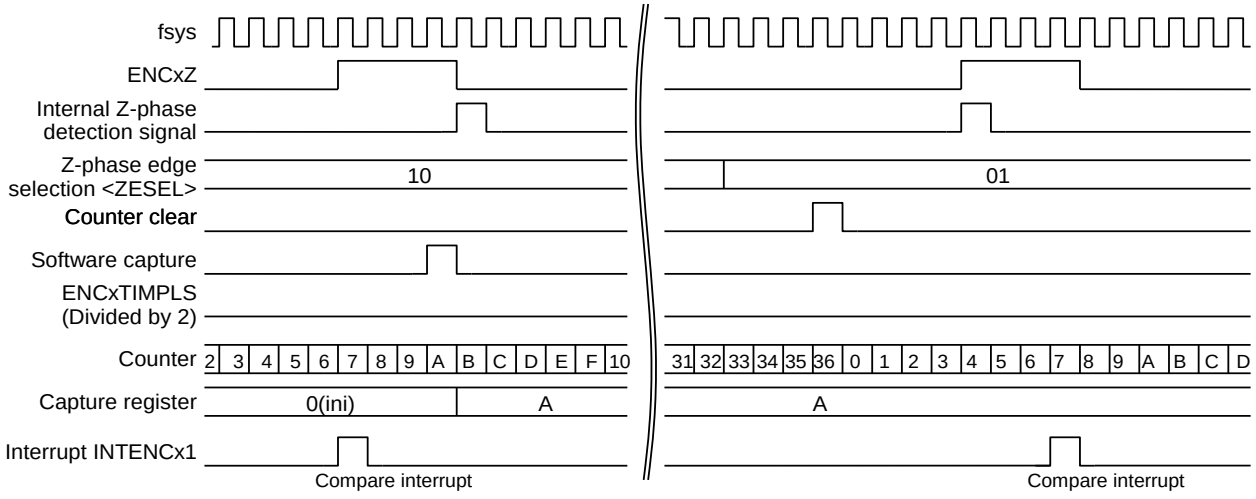


Figure 3.10 ENCxZ input is disabled. (*[ENxTNCR]*<ZEN>=0)

When <ZEN>=1, a ENCxZ input can work as the external trigger. When <ZEN>=0, the external trigger is not used.

The counter always performs up counting.

When "1" is written to ***[ENxTNCR]***<ENCLR>, the counter is cleared to "0x00000000".

When <ZEN>=1, if ***[ENxTNCR]***<ZESEL> is set to "01", the counter is cleared on the rising edge of the ENCxZ. When <ZESEL>=10, the counter is cleared on the falling edge of the ENCxZ. When <ZESEL>=11, the counter is cleared on the both edge of the ENCxZ.

When the ENCxZ edge is detected, the counter value is captured. The captured value can be read from the ***[ENxCNT]*** register.

When "1" is written to ***[ENxTNCR]***<SFTCAP>, the counter value is captured. The timing of capturing can be specified by the user. The captured value can be read from the ***[ENxCNT]*** register.

The value of the ***[ENxCNT]*** register (captured value) is maintained regardless of the value of ***[ENxTNCR]*** <ENRUN>. The clearing event of the captured value is only a reset.

When ***[ENxINTCR]***<RLDIE>=1, the value of ***[ENxRELOAD]***<RELOADH[15:0]>, <RELOADL[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<CMPIE>=1, the value of ***[ENxINT]***<INTH[15:0]>, <INTL[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE>=1, the value of ***[ENxMCMP]***<MCMPH[15:0]>, <MCMPL[15:0]> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxTNCR]***<MCMPMD>=1, if the counter value is ***[ENxMCMP]***<MCMPH[15:0]>, <MCMPL[15:0]> or more, an INTENCx1 interrupt occurs.

3.2.4. Phase Counter Mode

3.2.4.1. Phase Measurement

This mode can be used as a 16-bit counter that can be controlled at the specified frequency.

- Up/down count control is available.
- Sets the compare function and match interrupt.
- Clears and captures the counter using a ENCxZ input, and then occurs an interrupt.

(1) The ENCxZ input is enabled. (***[ENxTNCR]***<ZEN>=1)
[ENxINT]<INTH[15:0]>=0x0006

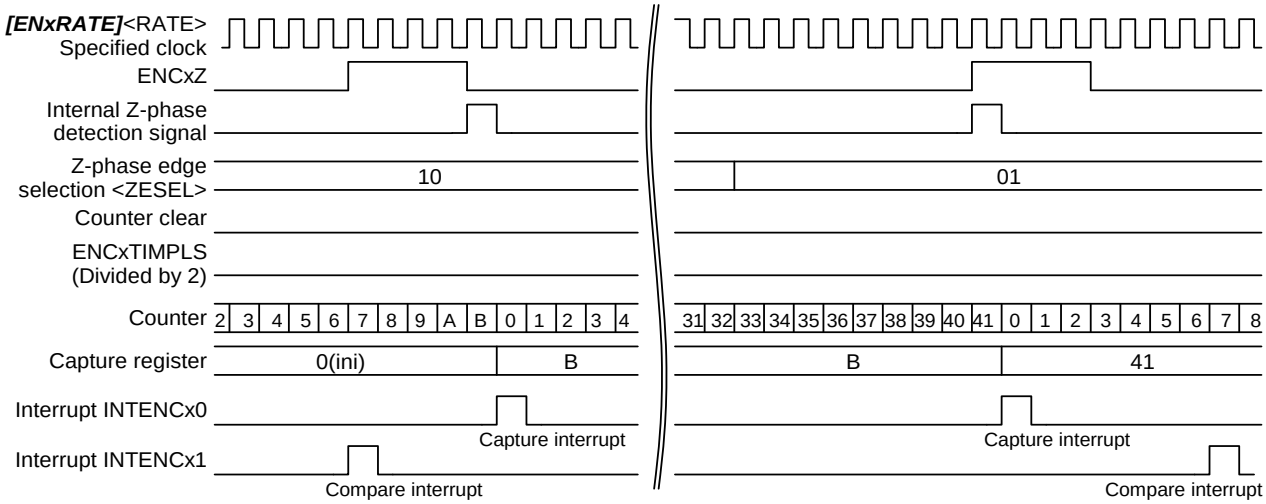


Figure 3.11 ENCxZ input is enabled (*[ENxTNCR]*<ZEN>=1)

(2) The ENCxZ input is disabled. (***[ENxTNCR]***<ZEN>=0)
[ENxINT]<INTH[15:0]>=0x0006

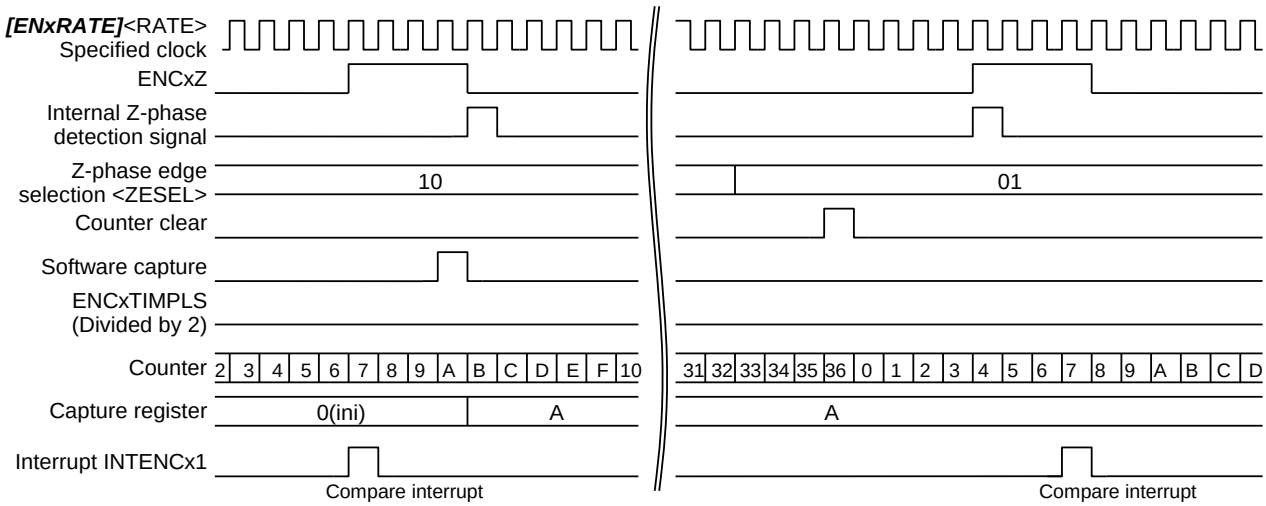


Figure 3.12 ENCxZ input is disabled (*[ENxTNCR]*<ZEN>=0)

When <ZEN>=1, a ENCxZ input can work as the external trigger. When <ZEN>=0, the external trigger is not used.

The counter controls up/down counting with the ***[ENxTNCR]***<UDMD> and the ***[ENxRATE]*** registers at the specified frequency.

When the counter performs up counting, if the value of the counter becomes equal to the value of ***[ENxRELOAD]*** <RELOADH[15:0]>, the counter is cleared to "0x0000".

When the counter preforms down counting, if the value of the counter reaches "0x0000", the counter is set to the value of ***[ENxRELOAD]***<RELOADH>.

When ***[ENxTNCR]***<TOVMD>=1, the counter stops at the value of ***[ENxRELOAD]***<RELOADH>.

When "1" is written to ***[ENxTNCR]***<ENCLR>, the counter is cleared to "0x0000".

When <ZEN>=1, if ***[ENxTNCR]***<ZESEL>=01, the counter is cleared to "0x0000" on the rising edge of the ENCxZ; if <ZESEL>=10, the counter is cleared to "0x0000" on the falling edge of the ENCxZ; if <ZESEL>=11, the counter is cleared to "0x0000" on the both edges.

When an edge of the ENCxZ is detected, the counter value is captured. The captured value can be read from the ***[ENxCNT]*** register.

When "1" is written to ***[ENxTNCR]***<SFTCAP>, the counter value is captured. Capturing can be performed at the specified timing. The captured valued can be read from the ***[ENxCNT]*** register.

The value of the ***[ENxCNT]*** register (captured value) is maintained regardless of the value of ***[ENxTNCR]*** <ENRUN>. The clearing event of the captured value is only a reset.

When ***[ENxINTCR]***<CMPIE>=1, if the value of ***[ENxINT]***<INTH> and the counter value become equal, an INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE>=1, if the value of ***[ENxMCMP]***<MCMPH> and the counter value become equal, an INTENCx1 interrupt occurs.

3.2.4.2. Phase Difference Measurement

In phase counter mode, when <P3EN>=<ZEN>=1, the counter enters phase difference measurement mode. In this mode, the up/down counter is controlled with the general purpose timer output (ENCxPSGI) and the ENCxZ input.

- When the general purpose timer output and the ENCxZ input are equal, the counter operation is set to up counting. When the general purpose timer output and the ENCxZ input are not equal, the counter operation is set to down counting.

- The value of the counter is captured on the edge of the general purpose timer output. At this time the counter can be cleared and an interrupt can be generated.

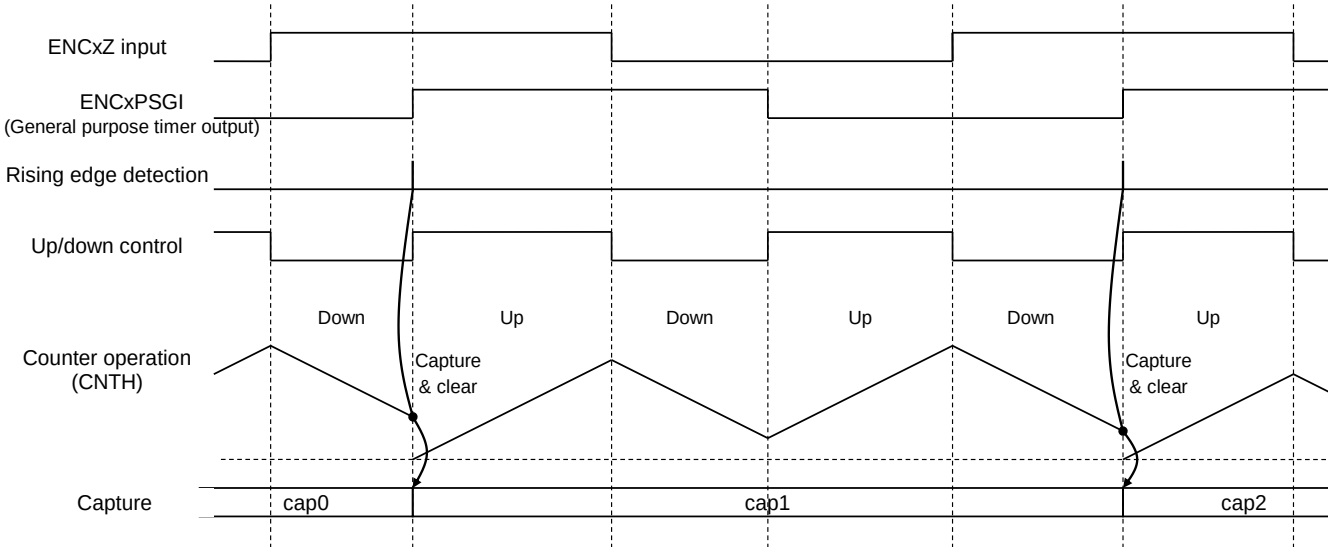


Figure 3.13 Operation in phase counter mode (phase difference measurement)

When an edge of the general purpose timer output (ENCxPSGI) signal is detected, the counter is captured and cleared. At this time, the detection edge is set with ***[ENxTNCR]***<ZESEL>. When "1" is written to ***[ENxTNCR]***<ENCLR>, the counter is cleared to "0x0000".

The captured value indicates the phase difference between the ENCxZ input and the general purpose timer output (ENCxPSGI) signal. The standard value (captured value is "0x0000") is assumed that the phase difference between the ENCxZ input and the general purpose timer output (ENCxPSGI) signal is 1/4 cycle.

3.3. Function Description in Each Circuit

3.3.1. Input Circuit

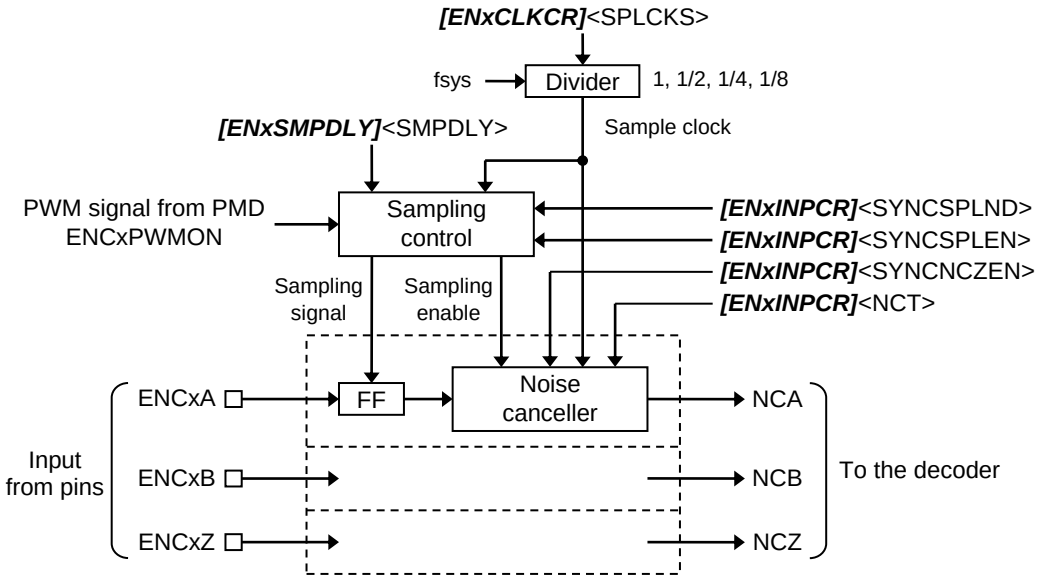


Figure 3.14 Configuration of input circuit

The input circuit samples the inputs from the pins (ENCxA, ENCxB, ENCxZ) on the specified sampling signal to reduce the noise using the digital noise canceller.

3.3.1.1. Sample Clock

The sample clock can be selected from fsys, fsys/2, fsys/4, or fsys/8 with ***[ENxCLKCR]***<SPLCKS>.

3.3.1.2. Sampling Mode

(1) Continuous sampling (***[ENxINPCR]***<SYNCSPLEN>=0)

In continuous sampling, the input circuit samples the input clock on sample clocks.

(2) PWM synchronous sampling (***[ENxINPCR]***<SYNCSPLEN>=1)

In PWM synchronous sampling, the input circuit samples the input clock synchronously with PWM signals from the PMD.

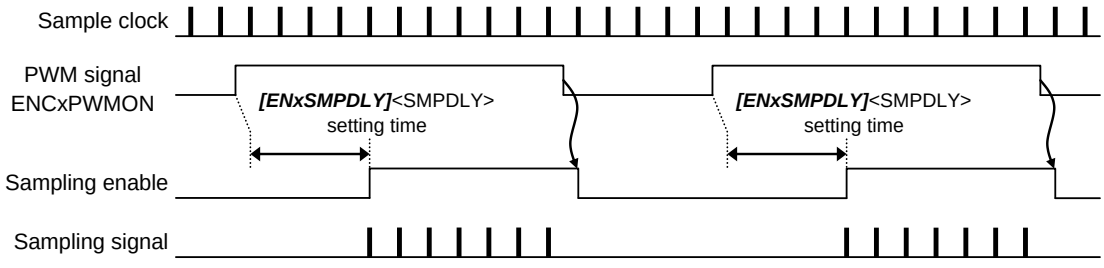
- PWM-on period sampling (***[ENxINPCR]***<SYNCSPLND>=0)
  In PWM-on period sampling, the input circuit samples the input signal on the specified sample clock selected with ***[ENxCLKCR]***<SPLCKS> for the PWM-on period.

  The PWM on-delay setting can be set with ***[ENxSMPDLY]***<SMPDLY> when the input circuit samples an on-delay period.

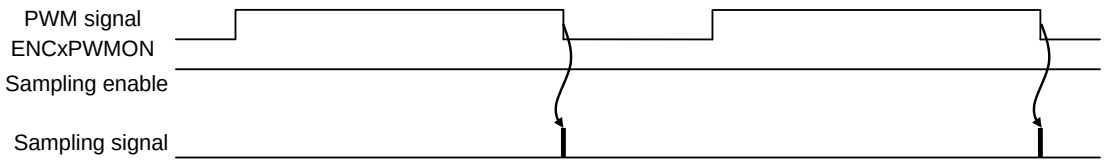
  Start delay time = <SMPDLY> × Sample clock cycle

  Note: After enabling ENC(after changing ***[ENxTNCR]***<ENRUN> from "0" to "1"), the first delay time may not match the value of <SMPDLY>.

- PWM off-edge sampling (***[ENxINPCR]***<SYNCSPLND>=1)
  ENCxPWMON signal serves as a sampling signal, and the input circuit samples the input signal on the off-edge of ENCxPWMON signal.



(a) PWM on-period sampling



(b) PWM off-edge sampling

Figure 3.15 PWM synchronous sampling

3.3.1.3. Noise Cancelling

(1) Continuous sampling (***[ENxINPCR]***<SYNCSPLEN>=0)

A noise cancelling time can be set with ***[ENxINPCR]***<NCT[6:0]>. A noise cancelling time can be calculated as follows:

Noise cancelling time = <NCT> × Sample clock cycle

Note: When <NCT> is set to "0", noise cancelling is disabled.

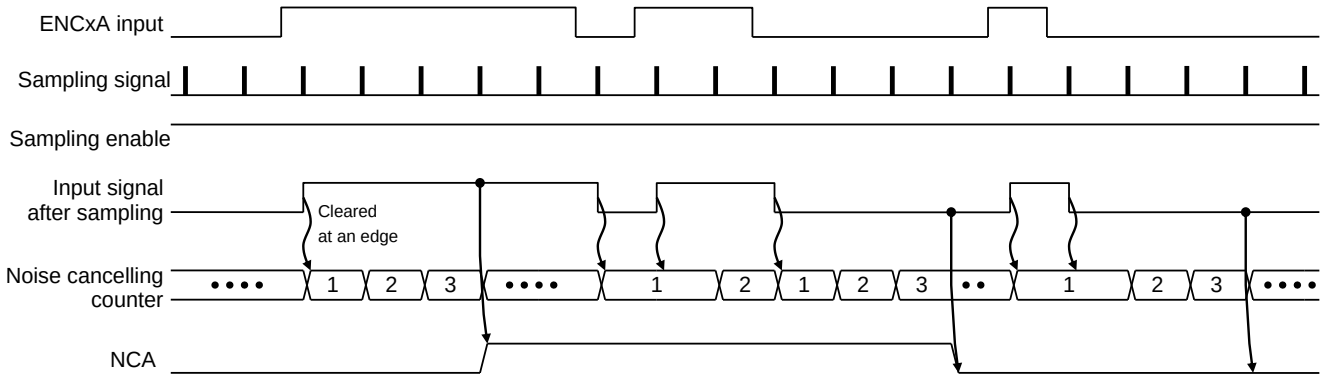


Figure 3.16 Noise cancelling (Continuous, <NCT>=3)

(2) Sampling in the PWM-on period (***[ENxINPCR]***<SYNCSPLEN>=1)

- Noise cancelling timer stops during the "Low" period of sampling signal (***[ENxINPCR]***<SYNCNCZEN>=0)
- Noise cancelling timer is cleared during the "Low" period of sampling signal (***[ENxINPCR]***<SYNCNCZEN>=1)

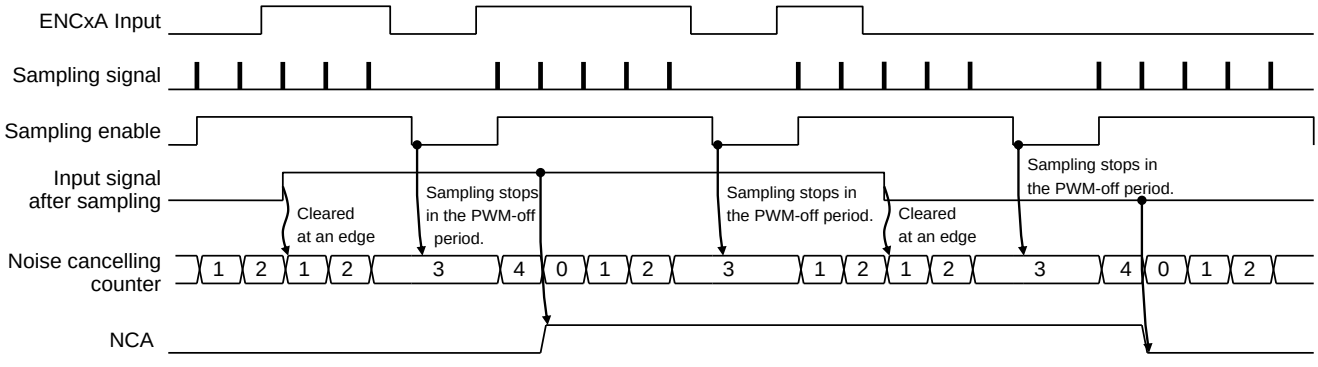


Figure 3.17 Noise cancelling (Sampling in the PWM-on period. Noise cancelling timer stops in the PWM-off period. <NCT>=4)

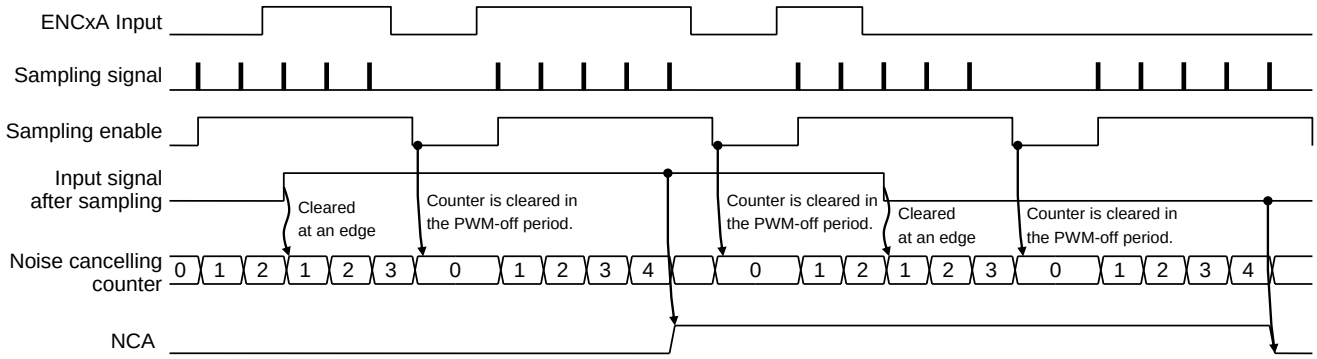


Figure 3.18 Noise cancelling (Sampling in the PWM-on period. Noise cancelling timer is cleared in the PWM-off period. <NCT>=4)

3.3.2. Decoder

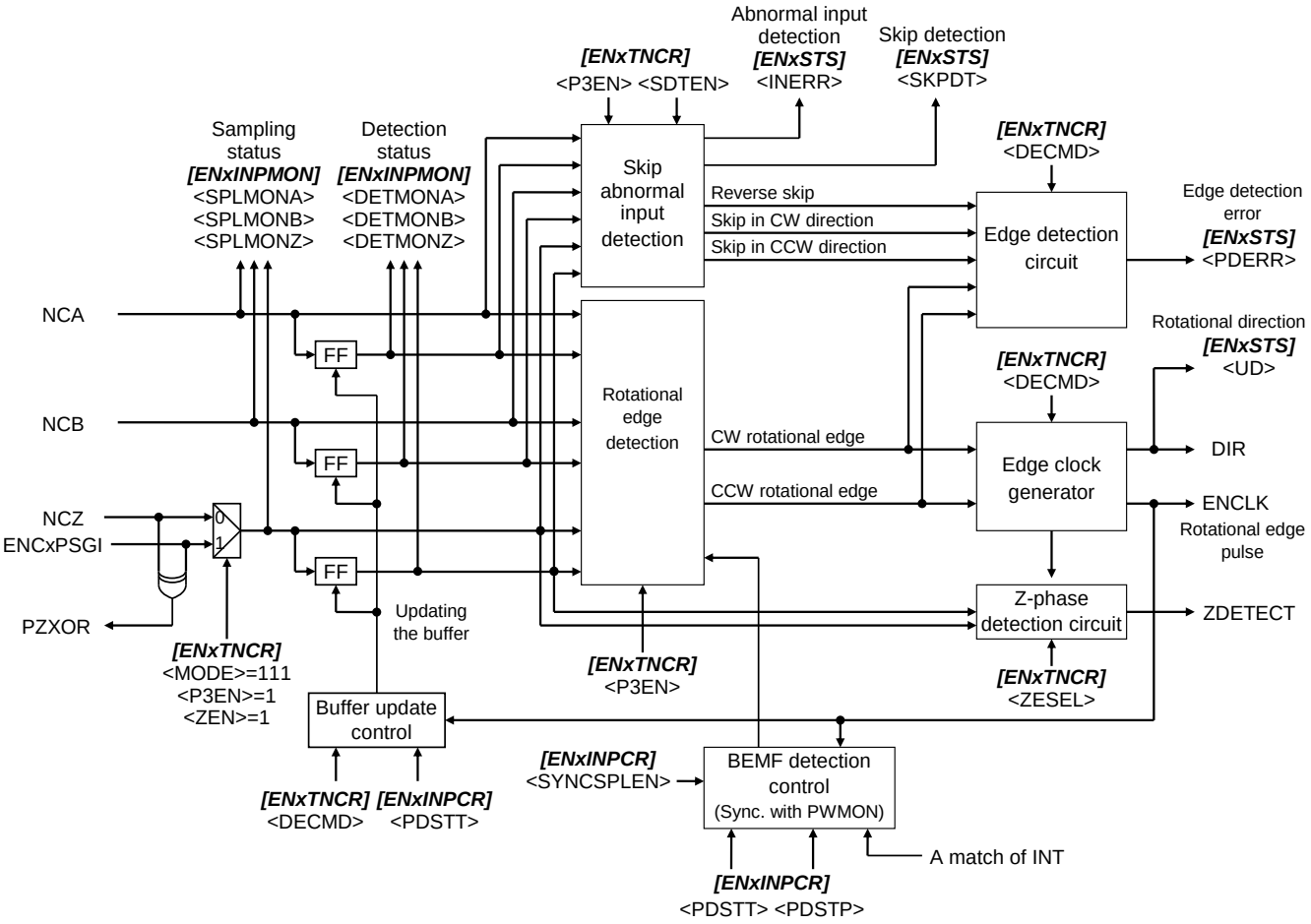


Figure 3.19 Configuration of the decoder

The decoder detects a rotational edge and rotational direction from 2-phase or 3-phase inputs after noise cancelling. It also detects the ENCxZ in the encoder mode, and the edge of ENCxZ signal in the timer mode and the phase counter mode.

3.3.2.1. Rotational Edge Detection and Direction Signal Generation

(1) 2-phase decoding (***[ENxTNCR]***<P3EN>=0)

Supports encoder mode and sensor mode (2-phase input).
In 2-phase decoding, four input pattern variations (rotational edge) are detected.

For the inputs in CW direction, when a rotational edge of (1) → (2), (2) → (3), (3) → (4), or (4) → (1) is detected, the status of ***[ENxSTS]***<UD> is "1".

For the inputs in CCW direction, when a rotational edge of (4) → (3), (3) → (2), (2) → (1), or (1) → (4) is detected, the status of ***[ENxSTS]***<UD> is "0".

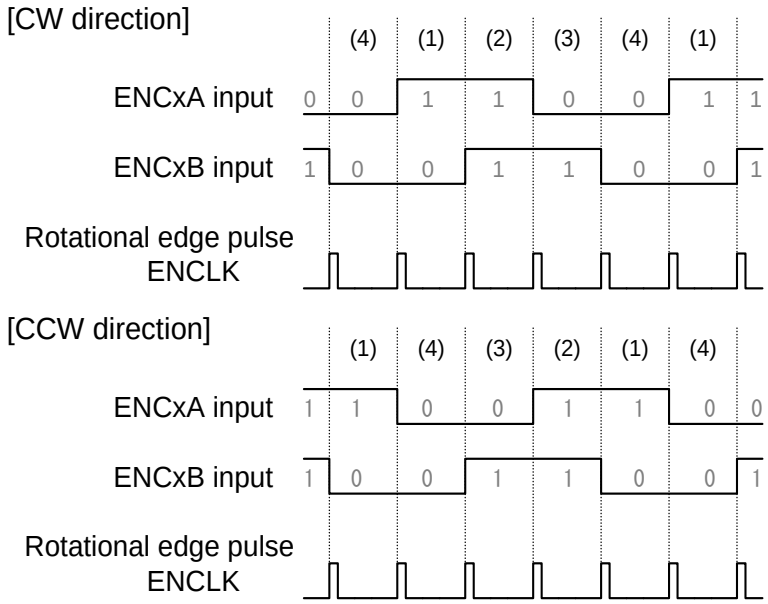


Figure 3.20 Waveforms of 2-phase decoding

(2) 3-phase decoding (***[ENxTNCR]***<P3EN>=1)

Available only in sensor mode (3-phase input).
3-phase decoding detects variations of 6 input patterns (rotational edge).

For inputs in CW direction, when a rotational edge of (1) → (2), (2) → (3), (3) → (4), (4) → (5), (5) → (6), or (6) → (1). The status of ***[ENxSTS]***<UD> is set to "1".

For inputs in CCW direction, when a rotational edge of (6) → (5), (5) → (4), (4) → (3), (3) → (2), (2) → (1), or (1) → (6), the status of ***[ENxSTS]***<UD> is set to "0".

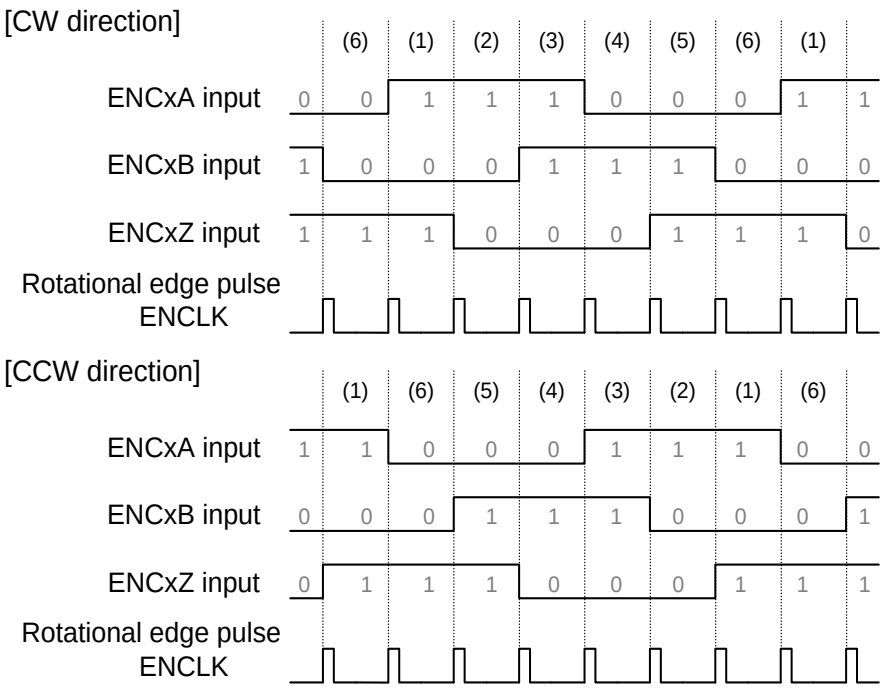


Figure 3.21 Waveforms of 3-phase decoding

3.3.2.2. Z-input Detection Circuit

The decoder detects an edge of the ENCxZ input.

- Encoder mode
  The decoder detects a rising edge in CW direction and detects a falling edge in CCW direction.

- Timer mode and Phase counter mode
  The decoder selects a detection edge either from a rising edge, falling edge, or both edges with ***[ENxTNCR]***<ZESEL>.

3.3.2.3. Skip Detection and Abnormal Input Detection

(1) Skip detection

Skip detection is enabled when ***[ENxTNCR]***<SDTEN>=1.

- Combination of skip detection in 2-phase decoding (***[ENxTNCR]***<P3EN>=0)

  Reverse skip detection: (1) → (3), (2) → (4), (3) → (1), (4) → (2)

- Combination of skip detection in 3-phase decoding (***[ENxTNCR]***<P3EN>=1)

  Skip detection in CW direction: (1) → (3), (2) → (4), (3) → (5), (4) → (6), (5) → (1), (6) → (2)
  Skip detection in CCW direction: (1) → (5), (2) → (6), (3) → (1), (4) → (2), (5) → (3), (6) → (4)
  Reverse skip detection: (1) → (4), (4) → (1), (2) → (5), (5) → (2), (3) → (6), (6) → (3)

- Combination that skip detection flag (***[ENxSTS]***<SKPDT>) is set to "1"

  In Sensor mode (event count, timer count);
  Skip detection in CW direction: (1) → (3), (2) → (4), (3) → (5), (4) → (6), (5) → (1), (6) → (2)
  Skip detection in CCW direction: (1) → (5), (2) → (6), (3) → (1), (4) → (2), (5) → (3), (6) → (4)

(2) Abnormal input detection

In sensor mode (event count, timer count, or phase count), if an edge detection of which three inputs are all "0" or all "1" in 3-phase decoding, is detected, the encoder determines these inputs are abnormal. If an abnormal input is detected, ***[ENxSTS]***<INERR> is set to "1".

3.3.2.4. Edge Detection Error Detection

The encoder determines an error when a direction that is not the specified direction with ***[ENxTNCR]***<DECMD> is detected. An edge detection error detection is one of the interrupt events. ***[ENxSTS]***<PDERR> is set to "1", when an error is detected.

- Skip detection is disabled. (***[ENxTNCR]***<SDTEN>=0)

  During the CW rotational edge detection (***[ENxTNCR]***<DECMD>=01):
  an error occurs when a rotational edge of CCW direction is detected.

  During the CCW rotational edge detection (***[ENxTNCR]***<DECMD>=10):
  an error occurs when a rotational edge of CW direction is detected.

- Skip detection is enabled. (***[ENxTNCR]***<SDTEN>=1)

  During the CW rotational edge detection (***[ENxTNCR]***<DECMD>=01):
  an error occurs when a skip in CCW direction, a reverse skip,
  or rotational edge of CCW direction is detected.

  During the CCW rotational edge detection (***[ENxTNCR]***<DECMD>=10):

an error occurs when a skip in CW direction, a reverse skip, or rotational edge of CW direction is detected.

3.3.2.5. Buffer Update Control

When ***[ENxTNCR]***<DECMD>=00, the buffer is always enabled. In this case, rotational edge detection and skip detection are determined by the variations of input signals.

If <DECMD> is set to other than "00", buffer updating is only performed when a rotational edge is detected. Therefore, the buffers (***[ENxINPMON]*** <DETMONA>, <DETMONB> and <DETMONZ>) have stored the input state at the previous rotational edge detection. The edge detection and skip detection are determined by comparing the buffer values (***[ENxINPMON]*** <DETMONA>, <DETMONB> and <DETMONZ>) with the current input values (***[ENxINPMON]***<SPLMONA>, <SPLMONB> and <SPLMONZ>).

3.3.2.6. BEMF Detection Control

In sensor mode (timer count and phase count), BEMF detection control is enabled when ***[ENxINPCR]*** <SYNCSPLEN>=1 (PWM synchronous sampling). It can stop (suspend) or start (restart) the rotational edge detection.

This control is used when position detection is performed on the induced voltage of the BLDC motor driven on rectangular waveforms generated by the PMD (position sensorless control).

(1) Starting the rotational edge detection

- Command operation: Write "1" to ***[ENxINPCR]***<PDSTT>
- Event operation: An INT compare match from the counter circuit

(2) Stopping the rotational edge detection

- Command operation: Write "1" to ***[ENxINPCR]***<PDSTP>
- Event operation: A rotational edge is detected.

3.3.3. Counter

The counter circuit consists of the clock generator, counter, compare function, and capture function. Usable functions vary depending on the operation mode.

3.3.3.1. Encoder Mode and Sensor Mode (Event Count)

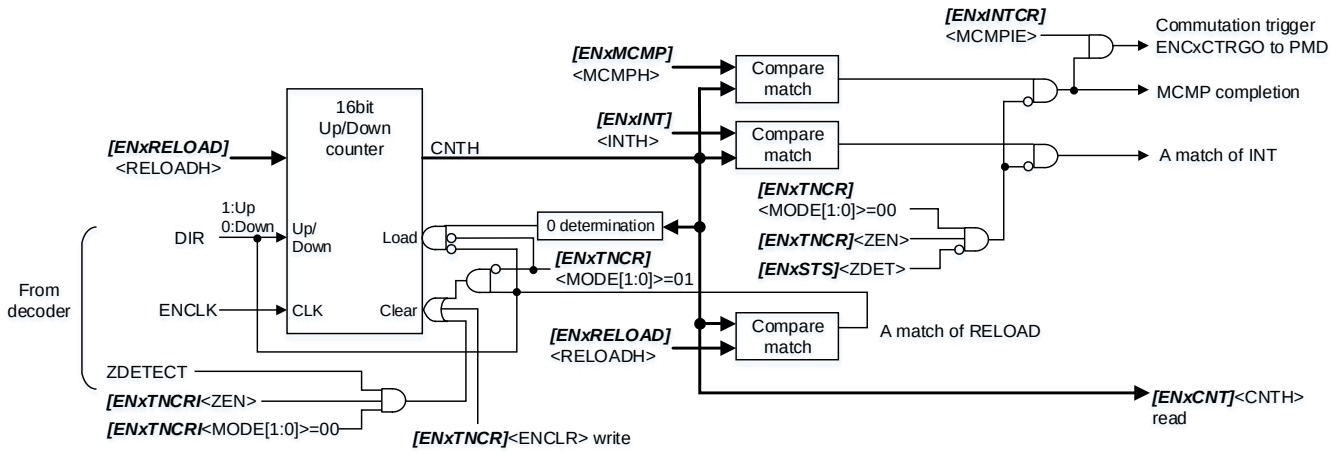


Figure 3.22 Configuration of the counter (encoder mode and sensor mode (event count))

The counter circuits use a rotational edge pulse (ENCLK) from the decoder, a 16-bit up/down counter operating on rotational direction signal (DIR), and three types of compare functions: <RELOADH>, <INTH>, and <MCMPH>.

In encoder mode, the counter is cleared by a match of RELOAD compare during the CW rotation.
When a CCW rotation is used, if the counter is determined as "0x0000", the value of the <RELOADH> is loaded to the counter.

In encoder mode, when ENCxZ is enabled (***[ENxTNCR]***<ZEN>=1), a match signal of INT compare and MCMP compare are ignored during when the encoder input is enabled (***[ENxTNCR]***<ENRUN>=1) to when an edge of the first ENCxZ is detected.

The value of the up/down counter can be read by the counter register (***[ENxCNT]***). When ***[ENxINTCR]*** <MCMPIE>=1, a MCMP completion signal serves as a commutation trigger for the PMD.

3.3.3.2. Sensor Mode (Timer count) or Timer Mode

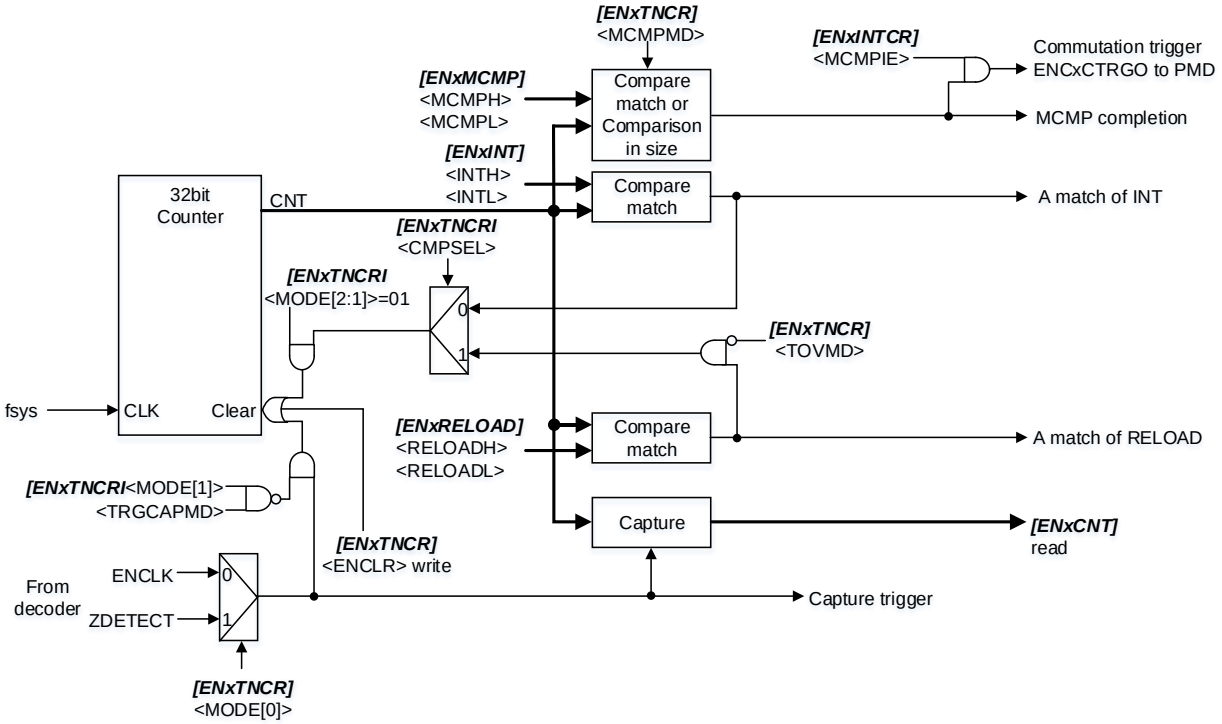


Figure 3.23 Configuration of the counter (sensor mode (timer count) or timer mode)

The counter consists of the 32-bit counter operating on the system clock (fsys), three-types of the compare functions (RELOAD, INT, and MCMP), and the capture function.

The MCMP compare function can select the selection type from match compare and compare in size. When comparison in size is selected (***[ENxTNCR]***<MCMPMD>=1), comparison starts by setting the ***[ENxMCMP]*** register. If the conditions are met, a MCMP completion signal is output and comparison finishes.

The counter is cleared by a match of INT compare or RELOAD compare in timer mode.

In sensor mode (timer count), the counter is captured and cleared when a rotational edge is detected (ENCLK). In timer mode, the counter is captured and cleared when a Z-edge is detected (ZDETECT). The captured value can be read by reading the counter register (***[ENxCNT]***).

When ***[ENxINTCR]***<MCMPIE>=1, a MCMP completion signal serves as a commutation trigger signal for the PMD.

3.3.3.3. Sensor Mode (Phase count) or Phase Counter Mode

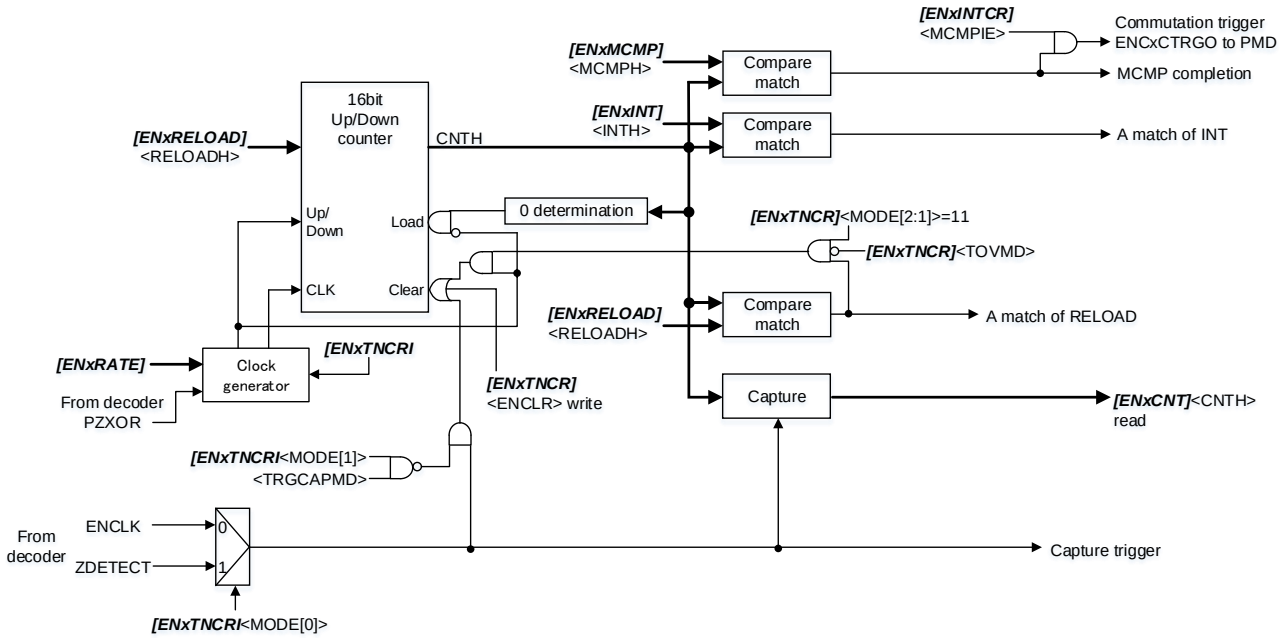


Figure 3.24 Configuration of the counter (sensor mode (phase count), and phase counter mode)

The counter consists of the clock generator specified with ***[ENxRATE]***, a 16-bit up/down counter operating on the clock signal and direction signal from the clock generator, three-types of compare match comparators (<RELOADH>, <INTH>, and <MCMPH>), and capture function.

The counter clock is specified with the ***[ENxRATE]*** register at the specified rate.

The up/down counter is specified with ***[ENxTNCR]***<UDMD>. However, in phase counter mode (phase difference measurement) (***[ENxTNCR]***<MODE>=111, <ZEN>=1, <P3EN>=1), up / down control is performed with the PZXOR signal

When the counter is set to up counting, the counter is cleared by a match of RELOAD compare. When the counter is set to down counting, if the counter is determined as "0x0000", the value of the <RELOADH> is loaded to the counter.

In sensor mode (phase count), the counter is captured and cleared when a rotational edge is detected on ENCLK. In phase counter mode, the counter is captured and cleared when a Z-edge is detected (ZDETECT). The captured value can be read by reading the counter register (***[ENxCNT]***).

When ***[ENxINTCR]***<MCMPIE>=1, a MCMP completion signal serves as a commutation trigger signal for the PMD.

3.3.4. Interrupt Control

The counter outputs two types of interrupts among the 6 types of interrupt events. An interrupt is enabled to output with the interrupt control register (***[ENxINTCR]***) according to the interrupt event. An interrupt event can be checked with an interrupt flag (***[ENxINTF]***).

The interrupt flag register (***[ENxINTF]***) is set by the occurrence of the interrupt event, and the flag is cleared by reading the register.

Table 3.2 List of interrupt events

Interrupt event	Description	Mode	Interrupt enable *[ENxINTCR]*	Event flag *[ENxINTF]*	Interrupt output
Divided pulse	When a rotational edge pulse is divided by 1 to 128 with ***[ENxTNCR]***<ENDEV>, this interrupt is sent.	Encoder mode Sensor mode (event count)	<TPLSIE>	<TPLSF>	INTENCx0
Capture	When the value of the counter is captured due to the external trigger (ENCxZ input), this interrupt is sent.	Timer mode Phase counter mode	<CAPIE>	<CAPF>	INTENCx0
	When the value of the counter is captured due to ENCLK, this interrupt is sent.	Sensor mode (timer count, phase count)			
Detection error	When an edge detection error (***[ENxSTS]*** <PDERR>) or the skip detection (***[ENxSTS]*** <SKPDT>) occurs, this interrupt is sent.	Encoder mode Sensor mode (event count, timer count and phase count)	<ERRIE>	<ERRF>	INTENCx0
A match of INT	When the value of the ***[ENxINT]*** register matches the counter value, this interrupt is sent.	All modes	<CMPIE>	<INTCPF>	INTENCx1
A match of RELOAD	When the value of the ***[ENxRELOAD]*** register matches the counter value, this interrupt is sent.	Sensor mode (timer count and phase count) Timer mode Phase counter mode (phase measurement)	<RLDIE>	<RLDCPF>	INTENCx1
MCMP completion	When ***[ENxTNCR]*** <MCMPMD>=0, if the ***[ENxMCMP]*** register matches the counter value, this interrupt is sent. When <MCMPMD>=1, if the counter value is the value of the ***[ENxMCMP]*** register or more, this interrupt is sent.	Sensor mode (timer count) Timer mode	<MCMPIE>	<MCMPF>	INTENCx1
	When the value of the ***[ENxMCMP]*** register matches the counter value, this interrupt is sent.	Encoder mode Sensor mode (event count and phase count) Phase counter mode			

Table 3.3 Interrupt events of each mode

Mode	Interrupt event
Encoder Mode	Divided pulse, Detection error, A match of INT, MCMP completion
Sensor Mode (event count)	Divided pulse, Detection error, A match of INT, MCMP completion
Sensor Mode (timer count)	Capture, Detection error, A match of INT, A match of RELOAD, MCMP completion
Sensor Mode (phase count)	Capture, Detection error, A match of INT, A match of RELOAD, MCMP completion
Timer Mode	Capture, A match of INT, A match of RELOAD, MCMP completion
Phase Counter Mode	Capture, A match of INT, A match of RELOAD, MCMP completion

4. Registers

4.1. Register List

The following table lists the control registers and their addresses:

Peripheral function		Channel/Unit	Base Address
			TYPE1
Advanced Encoder Input Circuit	A-ENC	ch0	0x400F7000

Register Name		Address (Base+)
ENC Control Register	***[ENxTNCR]***	0x0000
RELOAD Compare Register	***[ENxRELOAD]***	0x0004
INT Compare Register	***[ENxINT]***	0x0008
Counter Register	***[ENxCNT]***	0x000C
MCMP Compare Register	***[ENxMCMP]***	0x0010
Phase Count Rate Register	***[ENxRATE]***	0x0014
Status Register	***[ENxSTS]***	0x0018
Input Process Control Register	***[ENxINPCR]***	0x001C
Sample Delay Register	***[ENxSMPDLY]***	0x0020
Input Monitor Register	***[ENxINPMON]***	0x0024
Sample Clock Control Register	***[ENxCLKCR]***	0x0028
Interrupt Control Register	***[ENxINTCR]***	0x002C
Interrupt Flag Register	***[ENxINTF]***	0x0030

Note: The registers which can be updated in operation are ***[ENxTNCR]***<SFTCAP>, <ENRUN>, and <ENCLR>, and ***[ENxINPCR]***<PDSTP> and <PDSTT>.
The other registers should not be updated in operation.

4.2. Details of Registers

When describing the register function for each operation mode, it is explained after showing the operation mode in [xx mode].

4.2.1. *[ENxTNCR]* (ENC Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:29	-	0	R	Read as "0".
28	CMPSEL	0	R/W	[Timer mode] Counter clear condition. 0: A match of the ***[ENxINT]*** register 1: A match of the ***[ENxRELOAD]*** register
27:26	UDMD[1:0]	00	R/W	[Sensor mode (phase count), Phase counter mode (phase measurement)] Sets the up/down count setting. 00: Up count 01: Down count 10,11: Sets to up or down count setting with the ***[ENxRATE]*** register When this field is set to "10" or "11", if ***[ENxRATE]*** < 0, the counter is set to down count setting. If ***[ENxRATE]*** ≥ 0, the counter is set to up count setting.
25	TOVMD	0	R/W	Sets the counter operation when the ***[ENxRELOAD]*** register matches the value of the counter (timeout operation setting). [Sensor mode (timer count)] 0: Counting continues. 1: Counting stops. When the counter stops, the match should be cleared by software to restart the counter. [Timer mode, Sensor mode (phase count), Phase counter mode (phase measurement)] 0: The counter is cleared and counting continues. 1: Counting stops When the counter stops, the match should be cleared by software to restart the counter. [Encoder mode] Regardless of the <TOVMD> setting, when the motor drives on CW direction, the counter is cleared and counting continues, when the motor drives on CCW direction, counting continues. [Sensor mode (event count)] This bit is not used for a match of RELOAD.
24	MCMPMD	0	R/W	[Sensor mode (timer count), or Timer mode] Compare mode for the ***[ENxMCMP]*** register. 0: Compare match (***[ENxMCMP]*** = counter value) 1: Comparison in size (***[ENxMCMP]*** ≤ counter value) Set <MCMPMD> to "0" except in sensor mode (timer count) or timer mode.

Bit	Bit Symbol	After reset	Type	Function
23:22	DECMD[1:0]	00	R/W	[Encoder mode or Sensor mode] Sets the detection direction for the decoder. 00: CW or CCW edge detection Detects the variation of input signals (ENCxA, ENCxB, and ENCxZ). 01: CW edge detection Detects the variation of the input signal from the previous state on rotational edge detection to the current state. (The result of detection is maintained.) 10: CCW edge detection Detects the variation of the input signal from the previous state on rotational edge detection to the current state. (The result of detection is maintained.) 11: CW or CCW edge detection Detects the variation of the input signal from the previous state on rotational edge detection to the current state. (The result of detection is maintained.) Set <DECMD> to "00" in timer mode or phase counter mode.
21	SDTEN	0	R/W	[Encoder mode or Sensor mode] Sets skip detection. 0: Detection is disabled. 1: Detection is enabled. For details, refer to "3.3.2.3.Skip Detection and Abnormal Input Detection".
20	-	0	R	Read as "0".
19:17	MODE[2:0]	000	R/W	Sets the operation mode. 000: Encoder mode 001: Sensor mode (event count) 010: Sensor mode (timer count) 011: Timer mode 100: Reserved 101: Reserved 110: Sensor mode (phase count) 111:Phase counter mode In Phase counter mode, when <ZEN>=<P3EN>=1, the operation mode becomes "phase difference measurement". There are 13 operation modes. The operation mode is determined by <MODE>, <P3EN>, and <ZEN> (Refer to "Table 3.1 Setting of operation mode").
16	P3EN	0	R/W	[Sensor mode] Sets the decoding mode (2-phase/3-phase input selection) 0: 2-phase decoding 1: 3-phase decoding [Phase counter mode (phase difference measurement)] Set <P3EN> and <ZEN> to "1". [Encoder mode, Timer mode, or Phase counter mode (phase measurement)] Set <P3EN> to "0". (Refer to "Table 3.1 Setting of operation mode").
15:13	-	0	R	Read as "0".

Bit	Bit Symbol	After reset	Type	Function
12	TRGCAPMD	0	R/W	[Sensor mode (timer count or phase count), Timer mode, or Phase counter mode] Trigger capture operation selection 0: Capturing and clearing the counter 1: Only capturing Selects the capture operation at rotational edge detection in sensor mode (timer count or phase count). Selects the capture operation when the ENCxZ input is enabled in timer mode or phase counter mode. When software capturing is used, the counter is not cleared. [Encoder mode and Sensor mode (event count)] Capture is not performed.
11	SFTCAP	0	W	[Sensor mode (timer count, phase count), Timer mode, or Phase counter mode] Performs software capturing. 1: Captures the value of the counter. When this bit to "1", the value of the counter is captured. To obtain the captured value, read the ***[ENxCNT]*** register. Writing "0" has no meaning. Read as "0". [Encoder mode and Sensor mode (event count)] Write as "0".
10	ENCLR	0	W	Clears the counter. 1: Clear When this bit to "1", the counter is cleared to "0". After the counter is cleared, the counter restarts operation. Writing "0" has no meaning. Read as "0". <SFTCAP> and <ENCLR> should not be set to "1" at the same time.
9:8	ZESEL[1:0]	00	R/W	[Timer mode or Phase counter mode] Selects the detection edge when the ENCxZ input is enabled. (The ENCxZ input/the ENCxPSGI input) 00: Reserved 01: A rising edge is detected. 10: A falling edge is detected. 11: Both edges are detected. In the phase counter mode (phase difference measurement), the detection target is the ENCxPSGI input.
7	ZEN	0	R/W	[Encoder mode, Timer mode, or Phase counter mode (phase measurement)] Enables/disables Z-phase input. 0: The ENCxZ input is disabled. 1: The ENCxZ input is enabled. [Phase counter mode (phase difference measurement)] Set <P3EN> and <ZEN> to "1". [Sensor mode] Set <ZEN> to "0". (Refer to "Table 3.1 Setting of operation mode").
6	ENRUN	0	R/W	Enables/disables the encoder input circuit. 0: Disabled 1: Enabled When <ENRUN>=1, <ZDET> is cleared to "0" and the encoder input circuit is also enabled. When <ENRUN>=0, the encoder input circuit is disabled.
5:3	-	0	R	Read as "0".

Bit	Bit Symbol	After reset	Type	Function
2:0	ENDEV[2:0]	000	R/W	[Encoder mode, or Sensor mode (event count)] Sets the ratio of a divided output (ENCxTIMPLS) of a rotational edge pulse. According to this setting, a rotational edge pulse is divided and this pulse is used as an interrupt event. 000: divided by 1 001: divided by 2 010: divided by 4 011: divided by 8 100: divided by 16 101: divided by 32 110: divided by 64 111: divided by 128 [Sensor mode (timer count and phase count), Timer mode, and Phase counter mode] There is no division output.

Note: When setting <ENRUN>=1, do not change other bits at the same time. Operation settings other than <ENRUN> must be set before setting <ENRUN>=1.

4.2.2. *[ENxRELOAD]* (RELOAD Compare Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	RELOADH[15:0]	0x0000	R/W	[Encoder mode] Sets the maximum value of the counter. ***[ENxTNCR]***<ZEN>=1: Set "Number of input pulses per rotation × 4". ***[ENxTNCR]***<ZEN>=0: Set "Number of input pulses per rotation" × 4 -1" [Sensor mode (phase count) or Phase counter mode] Sets the maximum value (count range per rotation) of the counter. [Sensor mode (timer count) or Timer mode] This field is used as the register to compare with the counter. If a match occurs, an interrupt occurs. Sets the upper 16 bits of 32 bits for comparison. [Sensor mode (event count)] This field is not used.
15:0	RELOADL[15:0]	0x0000	R/W	[Sensor mode (timer count) or Timer mode] Sets the lower 16 bits for 32-bit comparison. [Others] This field is not used.

4.2.3. *[ENxINT]* (INT Compare Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	INTH[15:0]	0x0000	R/W	[Encoder mode or Sensor mode (event count)] Sets the value on 16 bits for comparison with the counter. When the counter matches the value of <INTH>, an INT match signal occurs. At this time, an interrupt can be generated. [Sensor mode (timer count) or Timer mode] Sets the value on 32 bits for comparison with the counter. Sets the upper 16 bits of 32 bits to <INTH> for comparison. When the counter matches the value of <INTH>, an INT match signal occurs. At this time, an interrupt can be generated. [Sensor mode (phase count) or Phase counter mode] Sets the value on 16 bits for comparison with the counter. When the counter matches the value of <INTH>, an INT match signal occurs. At this time, an interrupt can be generated.
15:0	INTL[15:0]	0x0000	R/W	[Sensor mode (timer count) or Timer mode] Sets the lower 16 bits for 32-bit comparison. [Others] This field is not used.

Note) In sensor mode (phase count, timer count), it is used for BEMF control (Refer to "3.3.2.6.BEMF Detection Control").

4.2.4. *[ENxCNT]* (Counter Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	CNTH[15:0]	0x0000	R	[Encoder mode or Sensor mode (event count)] Read the counter value of a rotational edge pulse. [Sensor mode (timer count or phase count)] Read the captured value at rotational edge detection/at the ENCxZ input edge detection or software capture. [Timer mode or Phase counter mode (phase measurement)] Read the captured value at the ENCxZ input edge detection or the software capture. [Sensor mode (timer count) or Timer mode] Read the value of the upper 16 bits at 32-bit capturing. [Phase counter mode (phase difference measurement)] Read the captured value at the software capture or the ENCxPSGI signal edge detection.
15:0	CNTL[15:0]	0x0000	R	[Encoder mode, Sensor mode (event count or phase count), or Phase counter mode] This field is not used. [Sensor mode (timer count) or Timer mode] Read the value of the lower 16 bits at 32-bit capturing.

4.2.5. *[ENxMCMP]* (MCMP Compare Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	MCMPH[15:0]	0x0000	R/W	[Sensor mode (timer count) or Timer mode] Sets the value on 32 bits for comparison with the counter. Set this field to the upper 16 bits of 32 bits for comparison. An interrupt can be generated. Comparison in size (***[ENxTNCR]***<MCMPMD>=1) An MCMP completion signal is output when ***[ENxMCMP]*** ≤ a counter value is established. In this mode, one completion signal is output in each time the register is written. Compare match mode (***[ENxTNCR]***<MCMPMD>=0) An MCMP completion signal is output when ***[ENxMCMP]*** = a counter value is established. [Except Sensor mode (timer count) or Timer mode] Sets the value on 16 bits for comparison with the counter. An interrupt can be generated. An MCMP completion signal is output when ***[ENxMCMP]***<MCMPH> = a counter value. When ***[ENxINTCR]***<MCMPIE> is enabled, a commutation trigger signal is output to the PMD.
15:0	MCMPL[15:0]	0x0000	R/W	[Sensor mode (timer count) or Timer mode] Set this field to the lower 16 bits of 32 bits for comparison. [Others] This field is not used.

4.2.6. *[ENxRATE]* (Phase Count Rate Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	RATE[15:0]	0x0000	R/W	[Sensor mode (phase count) or Phase counter mode] Set the count frequency of the counter. Clock frequency generation: fsys × <RATE> /2^{16} Depending on the ***[ENxTNCR]***<UDMD> setting, the value of <RATE> can be specified as a signed bit or unsigned bit. If the value of <RATE> is negative, the counter counts down. <UDMD>=0x: Unsigned, 0 or more/less than 1.0 (0x0000 to 0xFFFF) <UDMD>=1x: Signed, -0.5 or more/less than 0.5 (0x8000 to 0x7FFF, two's complement) When <RATE>=0x0000, ***[ENxCNT]*** does not count. [Encoder mode, Sensor mode (event count and timer count), and Timer mode] Unused.

4.2.7. *[ENxSTS]* (Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14	REVERR	0	R	[Sensor mode (timer count)] Sets the flag at inversion of <UD> when the both edges are detected. (Note1) (Note2) 0: - 1: An inversion of <UD> is detected. When ***[ENxTNCR]***<ENRUN>=0, this bit is set to "0". After <ENRUN> is set to "1", the flag that shows inversion is not set at the first rotating edge pulse (ENCLK).
13	UD	0	R	[Encoder mode or Sensor mode (event count, timer count, or phase count)] Determination state of the rotation direction. 0: CCW (Counterclockwise) 1: CW (Clockwise) When the motor rotates to CW direction, this bit is "1". When the motor rotates to CCW direction, this bit is "0". If ***[ENxTNCR]***<ENRUN>=0, "0" is always set.
12	ZDET	0	R	[Encoder mode] Detects passing of the ENCxZ input. 0: A ENCxZ input is not detected after the encoder input has been enabled. 1: A ENCxZ input is detected. This bit is cleared when ***[ENxTNCR]***<ENRUN>=0.
11:3	-	0	R	Read as "0".
2	SKPDT	0	R	**[Sensor mode (event count, timer count)]** Detects a skip detection flag when skip detection is enabled. (Note1) 0: Undetected 1: A skip is detected.
1	PDERR	0	R	[Encoder mode, Sensor mode (event count, timer count, or phase count)] Detects an edge detection error flag. (Note1) 0: Undetected 1: An error is detected.
0	INERR	0	R	[Sensor mode (event count, timer count, or phase count)] Detects an abnormal input error. (Note1) 0: No abnormal error 1: Abnormal error This bit is set to "1" when all 3-phase inputs on 3-phase decoding are "Low" or "High".

Note1: The flag is cleared by reading this register.

Note2: After the mode transition, make sure to read this register first to clear the flag.

4.2.8. *[ENxINPCR]* (Input Process Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:15	-	0	R	Read as "0".
14:8	NCT	0x00	R/W	Sets the noise cancel time. (Note1) Setting range: 0 to 127 (0x00 to 0x7F) Cancel time: Setting value × Sample clock cycle (with the ***[ENxCLKCR]***<SPLCKS> setting) When this field is set to "0x00", noise cancelling does not operate. The sampling clock in PWM-off edge sample mode is a PWM signal.
7	PDSTP	0	W	[Sensor mode (timer count or phase count)] Sets the rotational edge detection stop command at PWM synchronous sampling. (BEMF detection control) 0: - 1: Stops rotational edge detection When this bit is set to "1", rotational edge detection is stopped. Writing "0" has no meaning. Read as "0". Do not set <PDSTP> and <PDSTT> to "1" at the same time.
6	PDSTT	0	W	[Sensor mode (timer count or phase count)] Sets the rotational edge detection start command at PWM synchronous sampling. (BEMF detection control) 0: - 1: Starts rotational edge detection When this bit is set to "1", rotational edge detection is started. Writing "0" has no meaning. Read as "0". Do not set <PDSTP> and <PDSTT> to "1" at the same time.
5:3	-	0	R	Read as "0".
2	SYNCNCZEN	0	R/W	Controls a noise cancel counter when sampling is performed in the PWM-on period. 0: The counter stops in the PWM-off period. 1: The counter stops and cleared in the PWM-off period. This setting is used to enable the PWM synchronous sampling (<SYNCSPLEN>=1) and to select the PWM sampling in the PWM-on period (<SYNCSPLND>=0).
1	SYNCSPLND	0	R/W	Selects the PWM synchronous sampling 0: Sampling in the PWM-on period 1: Sampling in the PWM-off edge This setting is enabled when the PWM synchrony sampling is enabled (<SYNCSPLEN>=1).
0	SYNCSPLEN	0	R/W	Enables the PWM synchronous sampling 0: Continuous sampling 1: PWM synchronous sampling(Note1) This bit enables the PWM synchronous sampling. (Note2) When <SYNCSPLEN> is set to "1" in sensor mode (timer count or phase count), BEMF detection control is enabled on decoding operation.

Note1: For the PWM synchronous sampling (<SYNCSPLEN>=1), set <NCT> to "1" or more.

Note2: For details of the PMD, refer to "Programmable Motor Control Circuit Plus" or "Advanced Programmable Motor Control Circuit" of the reference manual.

4.2.9. *[ENxSMPDLY]* (Sample Delay Register)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as "0".
7:0	SMPDLY[7:0]	0x00	R/W	Sampling start delay time Setting range: 0 to 255 (0x00 to 0xFF) Start delay time: <SMPDLY> setting value × Sampling cycle (with the ***[ENxCLKCR]***<SPLCKS> setting) Sets the sampling start delay time after the PWM-on edge, when the sampling in the PWM-on period is selected (***[ENxINPCR]***<SYNCSPLEN>=1, ***[ENxINPCR]***<SYNCSPLND>=0).

Note: After enabling ENC(after changing ***[ENxTNCR]***<ENRUN> from "0" to "1"), the first delay time may not match the value of <SMPDLY>.

4.2.10. *[ENxINPMON]* (Input Monitor Register)

Bit	Bit Symbol	After reset	Type	Function
31:7	-	0	R	Read as "0".
6	DETMONZ	0	R	Monitors the rotational edge detection status for NCZ. (Note1) (Note2) Stores the value of NCZ at rotational edge detection.
5	DETMONB	0	R	Monitors the rotational edge detection status for NCB. (Note1) (Note2) Stores the value of NCB at rotational edge detection.
4	DETMONA	0	R	Monitors the rotational edge detection status for NCA. (Note1) (Note2) Stores the value of NCA at rotational edge detection.
3	-	0	R	Read as "0".
2	SPLMONZ	0	R	Monitors the status of ENCxZ after noise cancelling. Stores the status of NCZ that is the ENCxZ input after noise cancelling.
1	SPLMONB	0	R	Monitors the status of ENCxB after noise cancelling. Stores the status of NCB that is the ENCxB input after noise cancelling.
0	SPLMONA	0	R	Monitors the status of ENCxA after noise cancelling. Stores the status of NCA that is the ENCxA input after noise cancelling.

Note1: When ***[ENxTNCR]***<DECMD>=00, this bit indicates the previous value of <SPLMONn>(n=A, B, Z).

Note2: This bit indicates the previous value of <SPLMONn>(n=A, B, Z) until the first rotational edge detection after changing ***[ENxTNCR]***<ENRUN> to "1" or writing "1" to ***[ENxINPCR]***<PDSTT>.

4.2.11. *[ENxCLKCR]* (Sample Clock Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as "0".
1:0	SPLCKS[1:0]	00	R/W	Sets the sampling frequency. 00: fsys 01: fsys/2 10: fsys/4 11: fsys/8 Sets the sampling frequency for the ENCxA input, the ENCxB input, and the ENCxZ input. On PWM synchronous sampling, this field is disabled, when off edge sampling is set (***[ENxINPCR]***<SYNCSPLEN>=1 and ***[ENxINPCR]***<SYNCSPLND>=1).

4.2.12. *[ENxINTCR]* (Interrupt Control Register)

Bit	Bit Symbol	After reset	Type	Function
31:6	-	0	R	Read as "0".
5	MCMPIE	0	R/W	Enables/disables a MCMP completion interrupt. 0: Disabled 1: Enabled When this bit to "1", an INTENCx1 occurs at MCMP completion.
4	RLDIE	0	R/W	Enables/disables a RELOAD interrupt. 0: Disabled 1: Enabled When this bit to "1", an INTENCx1 occurs when the counter matches the value of the RELOAD register. A RELOAD interrupt does not occur in encoder mode or sensor mode (event count).
3	CMPIE	0	R/W	Enables/disables a INT interrupt. 0: Disabled 1: Enabled When this bit to "1", an INTENCx1 occurs when the counter matches the value of the INT register.
2	ERRIE	0	R/W	Enables/disable a detection error interrupt. 0: Disabled 1: Enabled When this bit to "1", an edge detection error (***[ENxSTS]*** <PDERR>=1) occurs, or when a skip is detected (***[ENxSTS]*** <SKPDT>=1), an INTENCx0 occurs. An interrupt does not occur in timer mode or phase counter mode.
1	CAPIE	0	R/W	Enables/disable a capture trigger interrupt. 0: Disabled 1: Enabled When this bit to "1", if the value of the counter is captured due to the external trigger (an ENCxZ input) or the rotational edge pulse (ENCLK), an INTENCx0 occurs. An interrupt does not occur in encoder mode or sensor mode (event count).
0	TPLSIE	0	R/W	Enables/disable a rotational divided edge interrupt. 0: Disabled 1: Enabled When this bit to "1", an INTENCx0 occurs by rotational edge divided pulses. An interrupt occurs only in encoder mode and sensor mode (event count).

4.2.13. *[ENxINTF]* (Interrupt Flag Register)

Bit	Bit Symbol	After reset	Type	Function
31:6	-	0	R	Read as "0".
5	MCMPF	0	R	MCMP completion flag 0: No flag 1: The flag is generated.
4	RLDCPF	0	R	RELOAD match flag 0: No flag 1: The flag is generated. This bit is not set in encoder mode or sensor mode (event count).
3	INTCPF	0	R	INT match flag 0: No flag 1: The flag is generated.
2	ERRF	0	R	Detection error flag 0: No flag 1: The flag is generated. This bit is not set in timer mode or phase counter mode.
1	CAPF	0	R	Capture flag 0: No flag 1: The flag is generated. This bit is not set by soft capture. This bit is not set in encoder mode or sensor mode (event count).
0	TPLSF	0	R	Rotational edge divided pulse flag 0: No flag 1: The flag is generated. This bit is enabled in encoder mode or sensor mode (event count).

Note: Each flag is set by the occurrence of the event that was enabled, and it is cleared by reading. When ***[ENxTNCR]***<ENRUN>=0, each flag is set to "0".

5. Precaution for Usage

- Before the clock supply is shut down, it should be checked that A-ENC has stopped. And, before the operation mode is changed to the stop mode, it should be checked that A-ENC has stopped.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2017-09-08	First release

Revision	Date	Description
2.0	2018-02-28	- The entire document Z-input, Z signal, Encoder input Z, Z-phase→ENCxZ Encoder input A, A-phase→ENCxZ, Encoder input B, B-phase→ENCxB Encoder input U→ENCxA(U), Encoder input V→ENCxB(V) Encoder input W→ENCxZ(W) Figure: "DIR"→"Rotational direction <UD>" -"1. Outline" Table Encoder/Function Description: signal edge→rotational edge - "Table 2.1" "interruption"→"interrupt" - "3.2. Operation Mode" Added: The other combinations should not be set. - "Table 3.1" Title: Setting of mode→Setting of operation mode - "3.2.1. Encoder Mode" "3.2.2.1. Event Count": TIMPLS description modified - "3.2.2.3. Phase Count" Figure3.7, Figure 3.8: REVERR signal deleted Deleted: "If the rotational direction is reversed, ***[ENxSTS]***<REVERR> is set to "1". This flag is cleared upon reading."- "3.3.1.1.Sample Clock" <SPLCKS>→***[ENxCLKCR]***<SPLCKS> - "3.3.1.2. Sampling Mode" (2): Modified, Added note before "Figure 3.1": PWM signal→ENCxPWMON signal - "3.3.1.3. Noise Cancelling" (1) Title modified: Continuous sampling(***[ENxINPCR]***<SYNCSPLEN>=0) (2) Title modified: Sampling in the PWM-on period (***[ENxINPCR]***<SYNCSPLEN>=1) in the PWM off period→during the "Low" period of sampling signal - "3.3.2.1. Rotational Edge Detection and Direction Signal Generation " (1): sensor mode(by setting <P3EN>=0) → sensor mode(2-phase input) (2): sensor mode → sensor mode (3-phase input) in CCW →in CCW direction - "3.3.2.2. Z-input Detection Circuit" <ZESEL>→***[ENxTNCR]***<ZESEL> - "3.3.2.4. Edge Detection Error Detection" rotation→ rotational edge detection - "3.3.3.1. Encoder Mode and Sensor Mode (Event Count)" 2nd stage: rotation detection→ rotation 3rd stage: Z-phase is detected→first ENCxZ is detected - Table 3.2 Capture/Mode: Modified supported mode A match of RELOAD/Mode added:(phase measurement) - "4.1. Register List" Added note below table - "4.2.1." UDMD/Function: phase counter mode→ phase counter mode(phase measurement) "1x"→"10,11" TOVMD/Function: phase counter mode→ phase counter mode(phase measurement) SDTEN/Function: sensor mode→Encoder mode or sensor mode P3ENFunction: Added [Phase counter mode (phase difference count)], [Encoder mode, Timer mode, or phase counter mode (phase measurement)] ZESEL/Function: Added "In the phase difference count mode, the detection target is the PSGI input." ZEN/Function: phase counter mode→ phase counter mode (phase measurement) Added: [Phase counter mode (phase difference count)], [Sensor mode] Deleted notes below the table - "4.2.7." REVERR/Function: [Sensor mode (timer count or phase count)] → [Sensor mode (timer count)] Modified other ZDET/Function added: [Encoder mode] - "4.2.8." <PDSTP>, <PDSTT>/Function added: "Do not set "1" to <PDSTP> and <PDSTT> at the same time." Note2: "Programmable Motor Control Circuit"→"Programmable Motor Control Circuit Plus" or "Advanced Programmable Motor Control Circuit" - "4.2.9." Function: disable period→start delay time, Added note - "4.2.13." Added in note: When ***[ENxTNCR]***<ENRUN>=0, "0" is set.

Revision	Date	Description
2.1	2018-10-10	- Conventions Modified explanation of trademark - "1. Outlines" Function Description of Phase counter: "Interrupt request" →"Interrupt" - "2." Figure 2.1: "Encoder input circuit"→ "A-ENC", "Interrupt request"→"Interrupt" Table 2.1: "The PWM signal for a sampling"→"PWM signal for sampling" "Timer output signal in general"→"General purpose timer output signal" - "3." Changed term of "3.2.1.","3.2.2.1.","3.2.4.1.","3.2.4.2.","3.3.4.": "Interrupt request"→"Interrupt" - "3.1." Deleted "When attempting to stop supplying ---------- as well. - "3.3.1." Figure 3.14 Corrected "<SYNCSPLMD>"→"<SYNCSPLND>" - "3.3.1.2." Corrected "<SYNCSPLMD>"→"<SYNCSPLND>" - "3.3.3.3." Explanation, Figure 3.24: "***[ENxRATE]***<RATE>"→"***[ENxRATE]***" - "3.3.4." Table 3.2 Corrected "Sensor mode"→"Sensor mode (event count, timer count and phase count)" of Detection error. - "4.2.1." Added explanation to Function column of MODE[2: 0], P3EN, TRGCAPMD, SFTCAP, ENCLR, ZEN and ENDEV[2:0]. Note) was added. Modified Function column of TRGCAPMD: "z-input"→"ENCxZ input" - "4.2.4." Function column of CNTH[15:0]: "phase counter mode"→ "Phase counter mode (phase measurement)" Added explanation of "Phase counter mode (phase difference measurement)" - "4.2.6." Function column of RATE[15:0] Modified explanation of "<UDMD>=1x:" Added explanation of other mode. - "4.2.7." ZDET: "Z-input"→"ENCxZ input" - "4.2.8." Added register name to Function column of NCT. Corrected "<SYNCSPLMD>"→"<SYNCSPLND>" to Function column of SYNCNCZEN. Corrected "SYNCSPLMD"→"SYNCSPLND" of Bit Symbol column. - "4.2.9." Added register name to Function column of SMPDLY[7:0]. Corrected "<SYNCSPLMD>"→"<SYNCSPLND>" to Function column of SMPDLY[7:0]. - "4.2.11." Corrected "<SYNCSPLMD>"→"<SYNCSPLND>" to Function column of SPLCKS[1:0]. - "5." Added "5. Precaution for Usage" chapter - "RESTRICTIONS ON PRODUCT USE" Replaced

Revision	Date	Description
2.2	2020-10-19	- All over document Added bit field to bit symbol - Prefer Modified trademark term - Added TXZ+ family - "1.Outlines" Table 1.1: "Hole sensor"→"Hall sensor" - "3.1. Clock Supply" Added clock supply and stop register C for fsys - "3.2.Operation Mode" Table 3.1: "Phase count"→"Phase counter" - "3.2.1.Encoder Mode" "specified count value"→"specified counter value" (2): "<RELOAD>"→"<RELOADH>" - "3.2.2. Sensor Mode Added "(BEMF Detection Control)" - "3.2.2.1.Event Count" "specified count value"→"specified counter value" Figure 3.3: Changed the waveform of ENCxB, ENCxZ (2): "Hall sensor"→"Rotational edge" Added "(2-phase input) or 120-degree (3-phase input)" - "3.2.3.Timer Mode" Figure 3.10: Changed the waveform of Counter, Capture register - "3.2.4.1.Phase Measurement" Figure 3.12: Changed the waveform of Counter, Capture register - "3.3.1.2.Sampling Mode" Title of Figure 3.14: "PMN"→"PWM" - "3.3.1.3.Noise Cancelling" (1): "<SYNCSPLEN>=1"→"<SYNCSPLEN>=0" - "3.3.2. Decoder" Revised the second sentence. - "3.3.2.3.Skip Detection and Abnormal Input Detection" (1): Deleted "If a skip is detected, <SKPDT> is set to "1"." Added an item "Combination that skip detection flag (***[ENxSTS]***<SKPDT>) is set to "1"" - "3.3.2.4.Edge Detection Error Detection" Added "***[ENxSTS]***<PDERR> is set to "1", when an error is detected." 2nd term: "<SDETEN>" → "<SDTEN>" - "3.3.3.1.Encoder Mode and Sensor Mode (Event Count)" Figure 3.22: Added ZDETECT signal - "3.3.3.2.Sensor Mode (Timer count) or Timer Mode" Figure 3.23: Added <TOVMD> and <TRGCAPMD> - "3.3.3.3.Sensor Mode (Phase count) or Phase Counter Mode" Figure 3.24: Added <TOVMD> and <TRGCAPMD> "<MCMPEN>"→"<MCMPIE>" - "3.3.4.Interrupt Control" Table 3.2: "PDERR"→"***[ENxSTS]***<PDERR>" "SKPDT"→"***[ENxSTS]***<SKPDT>" "count value"→"counter value" - "4.1.Register List" Base address list: Revised the item row Register address list: "Address"→"Address (Base+)" - "4.2.Details of Registers" "4.2.1." to "4.2.13." Term line: "Description"→"Function" "4.2.1." DECMD/Function: "phase count mode"→"phase counter mode" SDTEN/Function: Added "For details, refer to "3.3.2.3. .."." Deleted "When a skip is detected, an error flag (..) is set." ZESEL/Function: "PSGI"→"ENCxPSGI" "4.2.2." RELOADH/Function: Separated the description of encoder mode by the setting of <ZEN> "4.2.3." INTH/Function: Deleted "This match signal can be used as a rotational edge detection start signal when the PWM synchronous sampling is enabled." to the sensor mode Added note "4.2.4." CNTH/Function: "count value"→"counter value" CNTL/Function: "phase count mode"→"phase counter mode" "4.2.5." MCMPH/Function: "<MCMPMD>"→"***[ENxTNCR]***<MCMPMD>" "4.2.7." REVERR/Function: Added "After <ENRUN> is set to "1", the inverted flag is not set at the first rotating edge pulse (ENCLK)." SKPDT/Function: Added "[Sensor mode (event count, timer count)]"

Revision	Date	Description
2.3	2022-05-16	- Figure 2.1 Added fsys - Table 2.1 Added fsys, Correction of errors - 3.2.2.2. Changed ***[ENxINT]***, ***[ENxRELOAD]***,***[ENxMCMP]*** from 16bit to 32bit notation, Changed 0x0000 to 0x00000000 - Figure 3.22 ZDETECT changed to "from decode". - Changed from "CTRGO" in Figure 3.22, Figure 3.23, and Figure 3.24 to "ENCxCTRGO". - Figure 3.23 Changed from "Comparison in size" to " Compare match or Comparison in size". Changed from "***[ENxTNCR]***<MODE[2:1]>=11" to "***[ENxTNCR]***<MODE[2:1]>=01" . - 4.2.2 Changed the function description of RELOADL[15:0] - 4.2.3 Changed the function description of INTL[15:0] - 4.2.5 Changed the function description of MCMPL[15:0]

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