Derating of the MOSFET Safe Operating Area

Description

This document discusses temperature derating of the MOSFET safe operating area.

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1. Introduction

The safe operating area SOA of a MOSFET is temperature-dependent. The safe operating area is specified at either T_c = 25°C or T_a = 25°C. Derating of the safe operating area is required according to the actual case temperature and ambient temperature of the operation in order to determine that the operating locus of the MOSFET is within the derated SOA boundary. This document discusses the temperature derating of the safe operating area.

2. What is the safe operating area?

The safe operating area is the voltage and current conditions over which a MOSFET operates without permanent damage or degradation. The MOSFET must not be exposed to conditions outside the safe operating area even for an instant. Conventionally, MOSFETs were known for the absence of secondary breakdown, which was a failure mode specific to bipolar transistors. The safe operating area of a MOSFET was bound only by the maximum drain-source voltage, the maximum drain current, and a thermal limit between them. However, due to device geometry scaling, recent MOSFETs exhibit secondary breakdown. It is therefore necessary to determine whether the operating locus of the MOSFET is within the safe operating area.

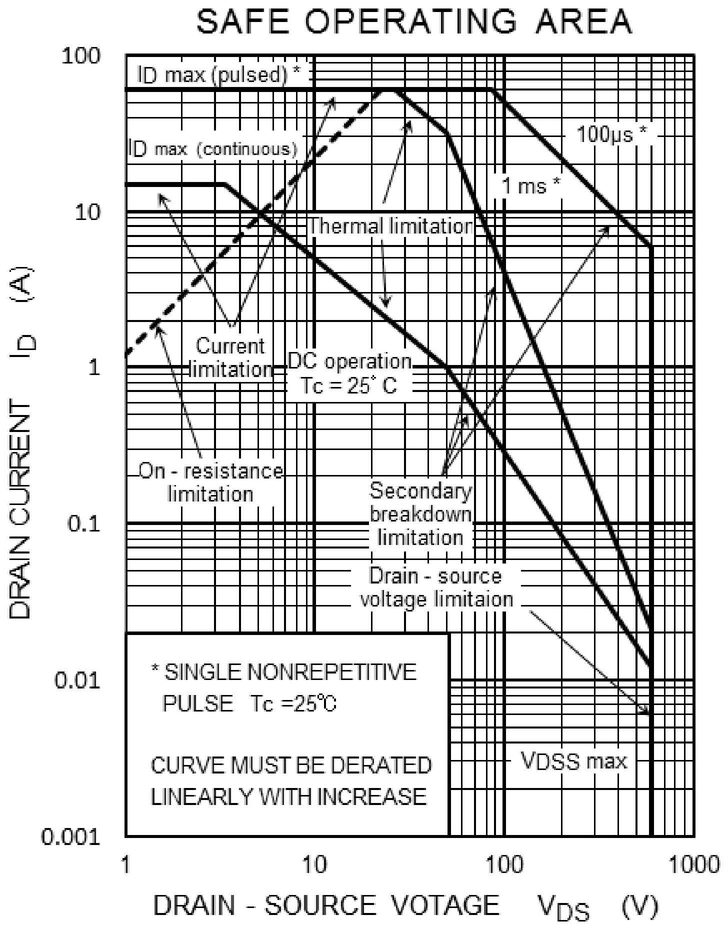

Figure 2.1 Safe operating area of a MOSFET

The safe operating area of a MOSFET is divided into the following five regions:

1. Thermal limitation

   This area is bound by the maximum power dissipation (P_D). In this area, P_D is constant and has a slope of -1 in a double logarithmic graph.

2. Secondary breakdown limitation

   With the shrinking device geometries, some MOSFETs have exhibited a failure mode resembling secondary breakdown in recent years. This area is bound by the secondary breakdown limit.

3. Current limitation

   This defines an area limited by the maximum drain current rating. The safe operating area is bound by I_D(max) for continuous-current (DC) operation and by I_{DP}(max) for pulsed operation.

4. Drain-source voltage limitation

   This defines an area bound by the drain-source voltage (V_{DSS}) limit.

5. On-state resistance limitation

   This defines an area that is theoretically limited by the on-state resistance ($R_{DS(ON)}$(max)) limit. I_D is equal to $V_{DS}/R_{DS(ON)}$(max).

3. Temperature derating of the safe operating area

The SOA is shown in Figure 2.1. For example, the power dissipation P_D with the derating at T_c= 100°C is calculated as follows. Figure 3.1 shows the P_D – T_c characteristics of a MOSFET. For example, $P_D(T_c = 100°C)$ is derated using Equation 3-1. $P_D(T_c = 100°C)$ is calculated to be 20 W as shown below. Note that Equation 3-1 applies to the area bound by the thermal limitation.

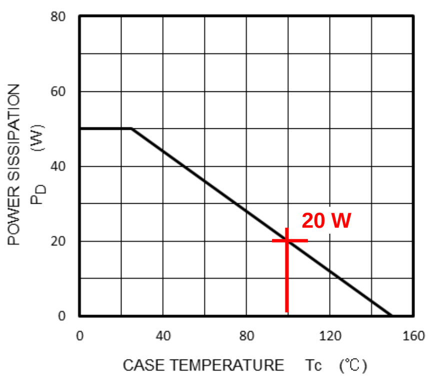

Figure 3.1 P_D – T_c characteristics

$$P_D = \frac{T_{ch(max)} - T_C}{T_{ch(max)} - 25} \times P_{D(max)}$$
$$= \frac{150 - 100}{150 - 25} \times 50$$
$$= 20(W) \qquad \cdots (3\text{-}1)$$

3.1. Derating of the T_c = 25°C (DC operation) line

In Figure 3.2, ① and ② are in the area bound by the thermal limitation. ① and ② lie on the iso-power line of P_D (max) = 50 W ($V_{DS} \times I_D$ = 50 W). At T_c = 100°C, The power dissipation is derated to a 20-W iso-power line derived from Figure 3.1. ①′ and ②′ can be calculated using Equation 3-3 and Equation 3-4 by derating V_{DS} at ① and I_D at ② to 40% using Equation 3-2.

$$d_T = \frac{P_D}{P_{D\,max}} \qquad \cdots \text{(3-2)}$$

$$V_{DS①'} = \frac{P_D}{I_{D\,max}} \cdot d_T = \frac{50}{15} \times 0.4 \approx 1.33\ \text{(V)}$$

$$I_{D②'} = \frac{P_D}{V_{DS}} \cdot d_T \qquad \cdots \text{(3-3)}$$

$$= \frac{50}{50} \times 0.4 = 0.4\ \text{(A)} \qquad \cdots \text{(3-4)}$$

The slope a of the line passing through ② and ③ can be calculated using Equation 3-5.

$$a = \frac{\log_{10} I_{D③} - \log_{10} I_{D②}}{\log_{10} V_{DS③} - \log_{10} V_{DS②}} = \frac{\log_{10} \frac{I_{D③}}{I_{DS②}}}{\log_{10} \frac{V_{DS③}}{V_{DS②}}} = \frac{\log_{10} \frac{0.012}{1}}{\log_{10} \frac{600}{50}} \approx -1.780 \qquad \cdots \text{(3-5)}$$

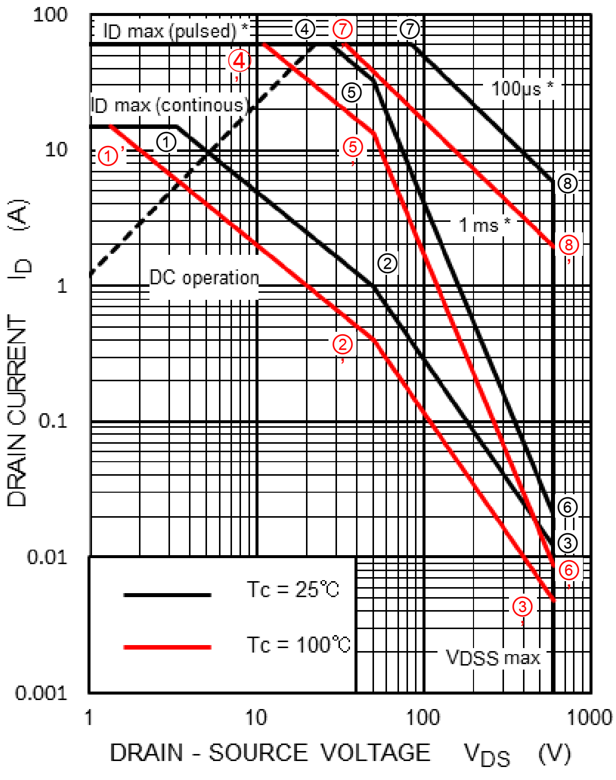

Figure 3.2 Temperature derating of the safe operating area

After derating, the line passes through ②′ with a slope of a. Therefore, I_D at ③′ can be calculated using Equation 3-6.

$$I_{D③'} = \left(\frac{V_{DS③'}}{V_{DS②'}}\right)^a \cdot I_{D②'} = \left(\frac{600}{50}\right)^{-1.780} \times 0.4 \approx 0.0048\ (A) \qquad \cdots \text{(3-6)}$$

3.2. Derating of the t_w = 1 ms line

The power dissipation at t_w = 1 ms, P_D(1 ms), is calculated to be roughly 1667 W from the transient thermal impedance curves shown in Figure 3.3. The points through which the derating lines for the thermal limitation at T_c = 100°C (④′ to ⑤′) and the secondary breakdown limitation (⑤′ to ⑥′) pass can be calculated in the same manner as for the T_c = 25°C (DC operation) line.

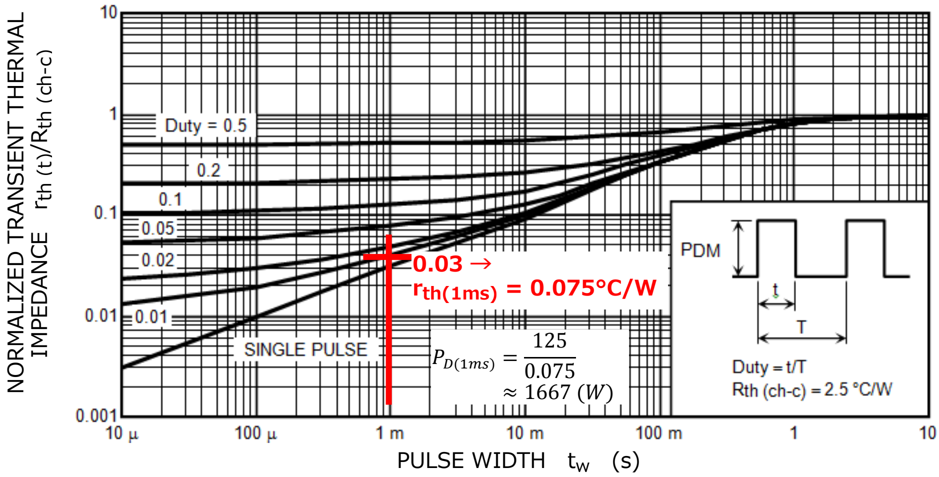

Figure 3.3 Transient thermal impedance curves

$$V_{DS④'} = \frac{P_{D(1ms)}}{I_{DP}} \cdot d_T = \frac{1667}{60} \times 0.4 \approx 11.1 \ (V) \qquad \cdots (3\text{-}7)$$

$$I_{D⑤'} = \frac{P_{D(1ms)}}{V_{DS⑤}} \cdot d_T = \frac{1667}{50} \times 0.4 \approx 13.3 \ (A) \qquad \cdots (3\text{-}8)$$

$$I_{D⑥'} = \left(\frac{V_{DS⑥'}}{V_{DS⑤'}}\right)^{a'} \cdot I_{D⑤'} = \left(\frac{600}{50}\right)^{-2.952} \times 13.3 \approx 0.0087 \ (A) \qquad \cdots (3\text{-}9)$$

3.3. Derating of the t_w = 100 μs line

The slope (a'') of this line is calculated to be roughly -1.196, which is outside the thermal limitation. $V_{DS⑦'}$ and $I_{D⑧'}$ can be calculated using Equation 3-10 and Equation 3-11, respectively:

$$V_{DS⑦'} = \frac{P_{D(100\mu s)}}{I_{DP}} \cdot d_T = \frac{5100}{60} \times 0.4 = 34\ (V) \quad \cdots (3\text{-}10)$$

$$I_{D⑧'} = \left(\frac{V_{DS⑧'}}{V_{DS⑦'}}\right)^{-a''} \cdot I_{D⑦'} = \left(\frac{600}{34}\right)^{-1.196} \times 60 \approx 1.94\ (A) \quad \cdots (3\text{-}11)$$

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