MOSFET Self-Turn-On Phenomenon

Description

When a rising voltage is applied sharply to a MOSFET between its drain and source, the MOSFET may turn on due to malfunction. This document describes the cause of this phenomenon and its countermeasures.

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1. Self-turn-on

1.1. What is self-turn-on?

For example, inverter and non-isolated synchronous rectification converter circuits consist of a bridge using MOSFETs. When the MOSFETs switch at high speed, a fast rising voltage is applied across the drain and source terminals of the MOSFET in the off state. Depending on the voltage change over time dv/dt, a voltage is induced at the gate input of the MOSFET according to the ratio between its gate-drain capacitance C_{gd} and gate-source capacitance C_{gs}. A current flowing to the gate resistor R_G via C_{gd} causes an excessive gate voltage.

The induced gate voltage exceeding the gate threshold voltage V_{th} leads to false turn-on of the MOSFET. This phenomenon is called self-turn-on.

Figure 1.1 shows a non-isolated synchronous rectification converter. When the MOSFET Q_1 turns on while the MOSFET Q_2 is off, a fast rising voltage (with a high dv/dt rate) is applied to Q_2. Figure 1.2 shows an inverter circuit configured as a bridge. If either one of the upper- or lower-arm MOSFETs (Q_1 or Q_2) turns on while the other one is off, a high-dv/dt voltage appears across the drain and source terminals of the MOSFET in the off state.

A self-turn-on event creates a short circuit between Q_1 and Q_2. This not only increases power losses, but also might permanently damage the devices.

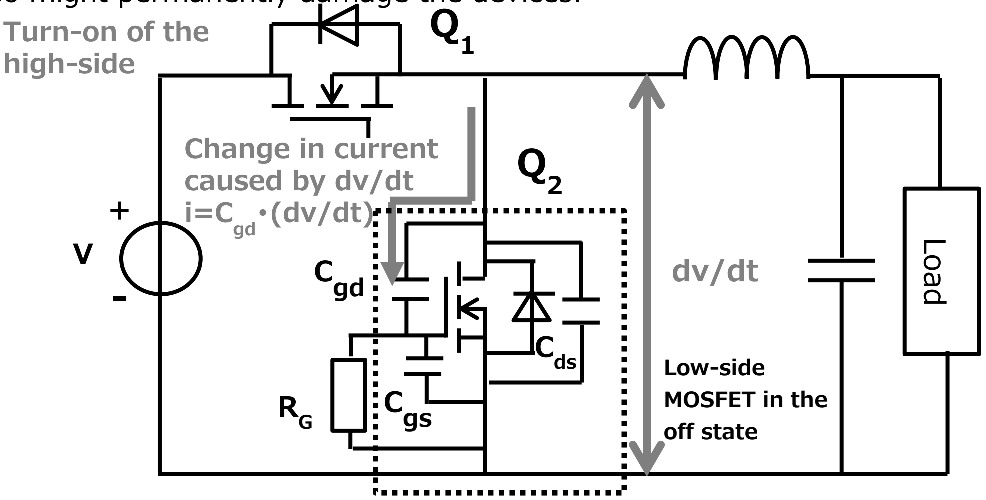

Figure 1.1 Non-isolated synchronous rectification converter

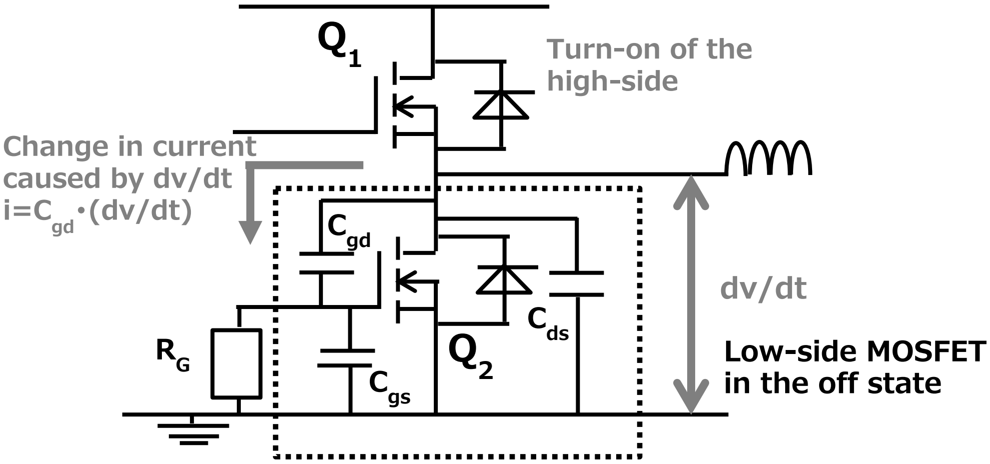

Figure 1.2 Inverter circuit configured as a bridge

1.2. Self-turn-on mechanism

When a voltage with a dv/dt ramp is applied to a MOSFET, a current flows through its gate-drain capacitance C_{gd}.

$$i = C_{gd}\frac{dv}{dt}$$

This current i induces a voltage across the gate and source terminals of the MOSFET, which is expressed as:

$$v_{GS} = R_G C_{gd}\frac{dv}{dt}\left\{1 - \exp\left(\frac{-t}{(C_{gs}+C_{gd})R_G}\right)\right\} \cdots\cdots\cdots (1)$$

(Here, the assumption is that the MOSFET capacitances, C_{gs} and C_{gd}, do not change with the voltage.)

The cause of self-turn-on depends on the length of the period during which a high-dv/dt voltage is applied across the drain and source terminals:

Phenomenon a: When the dv/dt period is shorter than (C_{gs}+ C_{gd})·R_G (i.e., when $t \ll (C_{gs}+C_{gd})\cdot R_G$)

Approximating the term $\exp\{-t/[(C_{gs}+C_{gd})\cdot R_G]\}$ in Equation (1) to $1-t/[(C_{gs}+C_{gd})\cdot R_G]$ gives the following:

(Maclaurin expansion at exp x using primary approximation exp x=1+x)

$$v_{GS} \approx \frac{C_{gd}}{(C_{gs}+C_{gd})}v(t) \cdots\cdots\cdots (2)$$

When a MOSFET switches at very high speed in switching applications such as non-isolated synchronous rectification converters, the resulting rise in its gate voltage can be calculated using Equation (2).

Phenomenon b: When the dv/dt period is longer than (C_{gs}+ C_{gd})·R_G (i.e., $t \gg (C_{gs}+C_{gd})\cdot R_G$)

Since $\exp\{-t/[(C_{gs}+C_{gd})\cdot R_G]\} \ll 1$, v_{GS} is approximated as follows:

$$v_{GS} \approx R_G C_{gd}\frac{dv}{dt} \cdots\cdots\cdots (3)$$

Self-turn-on occurs: 1) when v_{GS} calculated using Equation (2) or (3) exceeds the gate threshold voltage V_{th} of the MOSFET, or 2) when the sum of v_{GS} and the residual gate-source voltage that has been driving the gate exceeds V_{th}.

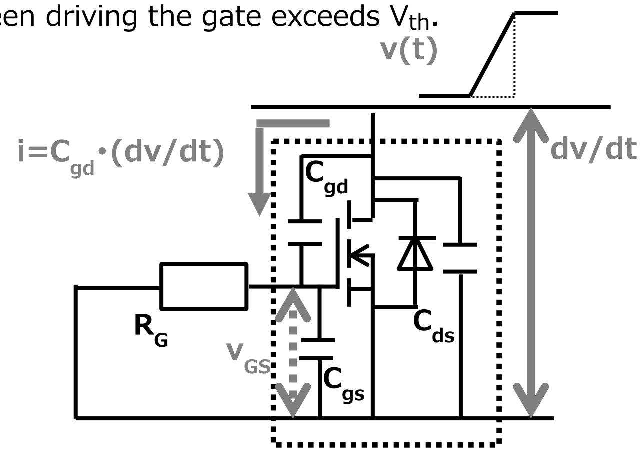

Figure 1.3 Circuit with a MOSFET

2. Simulation of self-turn-on

2.1. Non-isolated DC-DC converter

2.1.1. Method of checking for self-turn-on

Suppose that the MOSFET Q_2 in Figure 2.1 turns off after synchronous rectification mode (in the on state shown by #2) and that the following dead-time period overlaps the turn-on of the MOSFET Q_1. Then, a high-dv/dt voltage is applied to Q_2, causing self-turn-on. This is the mechanism of the MOSFET self-turn-on in a DC/DC converter.

The MOSFET self-turn-on occurs in a DC/DC converter as follows:

1. The MOSFET Q_1 turns on, causing a current to flow to L.
2. When the MOSFET Q_1 turns off, the energy accumulated on L flows back through the source and drain of the MOSFET Q_2. During this period, the low-side MOSFET Q_2 turns on, acting as a synchronous rectifier.
3. Next, the MOSFET Q_2 turns off. After a dead-time period, the MOSFET Q_1 turns on.

   This causes a high dv/dt voltage to be applied to the MOSFET Q_2.

   At this point in time, the gate and drain-source voltages and currents of the MOSFET Q_2 are measured.

(The gate current caused by the dv/dt ramp is calculated as $i_G \approx C_{gd} \cdot (dv/dt)$.)

(During the dead-time period from the turn-off of the MOSFET Q_2 to the turn-on of Q_1, a current flows through the body diode of the MOSFET Q_2. Synchronous rectification MOSFETs in motor applications operate in the same manner while a current flows back through the body diode.)

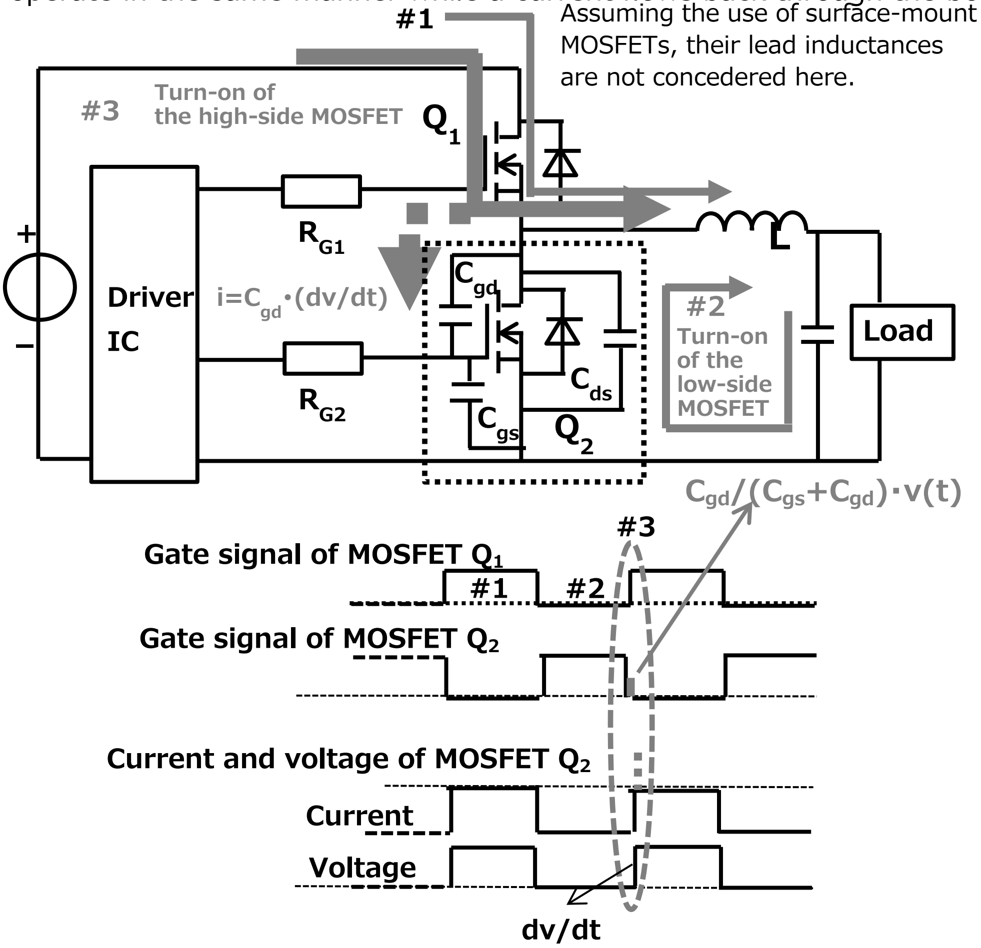

Figure 2.1 Simulation circuit model and simplified waveforms

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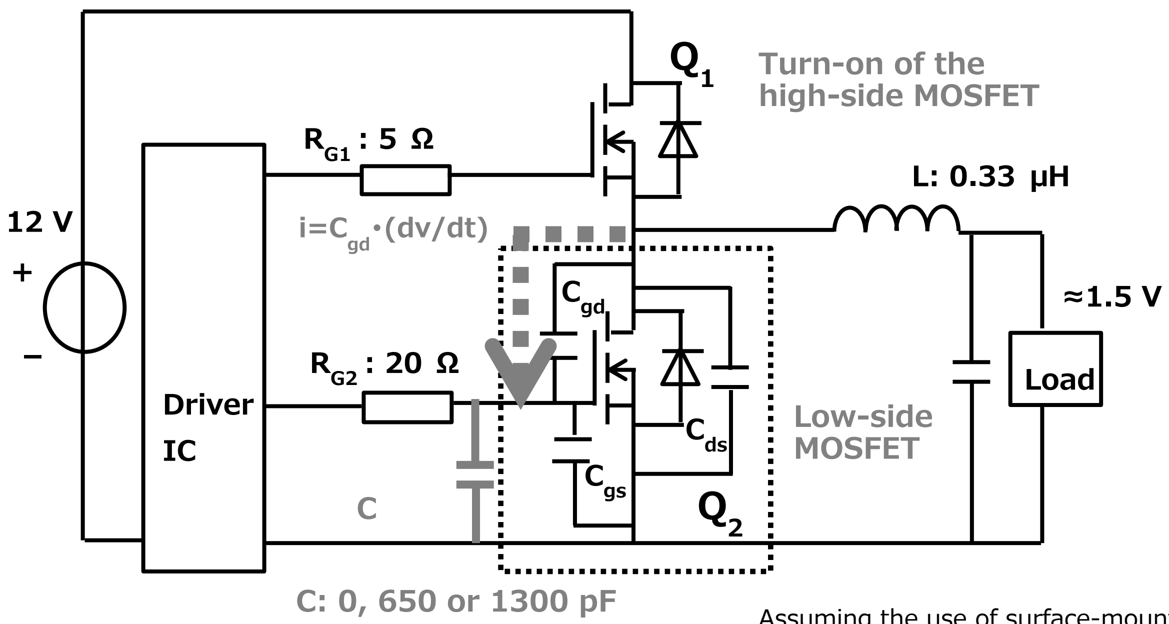
2.1.2. Adding an external gate-source capacitor to prevent self-turn-on

When a MOSFET switches at high speed, a voltage is induced according to the ratio between its gate-drain and gate-source capacitances. The induced voltage is superimposed on its gate voltage and might cause undesired self-turn-on. In our first simulation, the MOSFET used did not experience self-turn-on under typical conditions. So, we added a large gate resistor (R_{G2}=20 Ω) only to Q_2 to force a self-turn-on phenomenon to occur and then simulated the effect of an external gate-source capacitor. Because the MOSFETs in a DC/DC converter are driven at a very high frequency (300 to 500 kHz), the dead-time period from the turn-off of the MOSFET Q_2 to the turn-on of the MOSFET Q_1 is very short.

A simulation showed that the external gate-source capacitor is effective in reducing a rise in the gate voltage, $C_{gd}/(C_{gs}+C_{gd})\cdot v(t)$, which is a function of the ratio between gate-source and gate-drain capacitances. However, because the MOSFET Q_2 had a large gate resistor R_{G2}, the effect of the external gate-source capacitor was affected by a rise in the gate voltage due to $R_{G2}\cdot C_{gd}\cdot(dv/dt)$. The addition of a capacitor also increased the time required to discharge the gate charge after the MOSFET Q_2 turned off. As a result, the gate discharge current remained when the MOSFET Q_1 turned on, making Q_2 more susceptible to self-turn-on, contrary to our expectation. As demonstrated by this simulation, you should examine both the gate discharge time and the dead time when adding a capacitor between the gate and source terminals of a MOSFET for the purpose of self-turn-on prevention.

For accurate simulation, it is important to select appropriate devices and conditions.



MOSFET used
30 V/16 A
C_{iss}:1350 pF
C_{rss}:63 pF

Assuming the use of surface-mount MOSFETs, their lead inductances are not concedered here.

Figure 2.2a Simulation circuit model

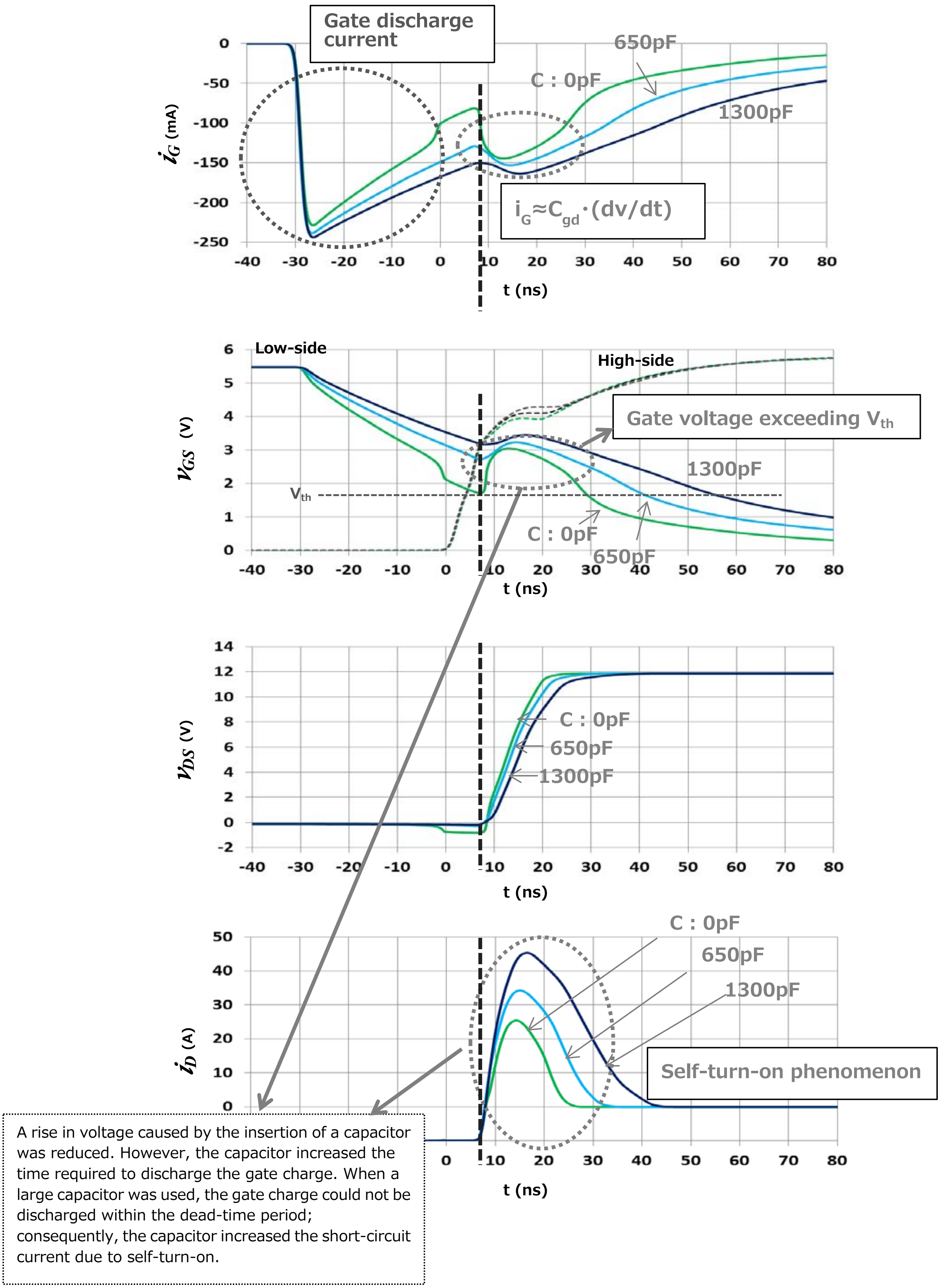


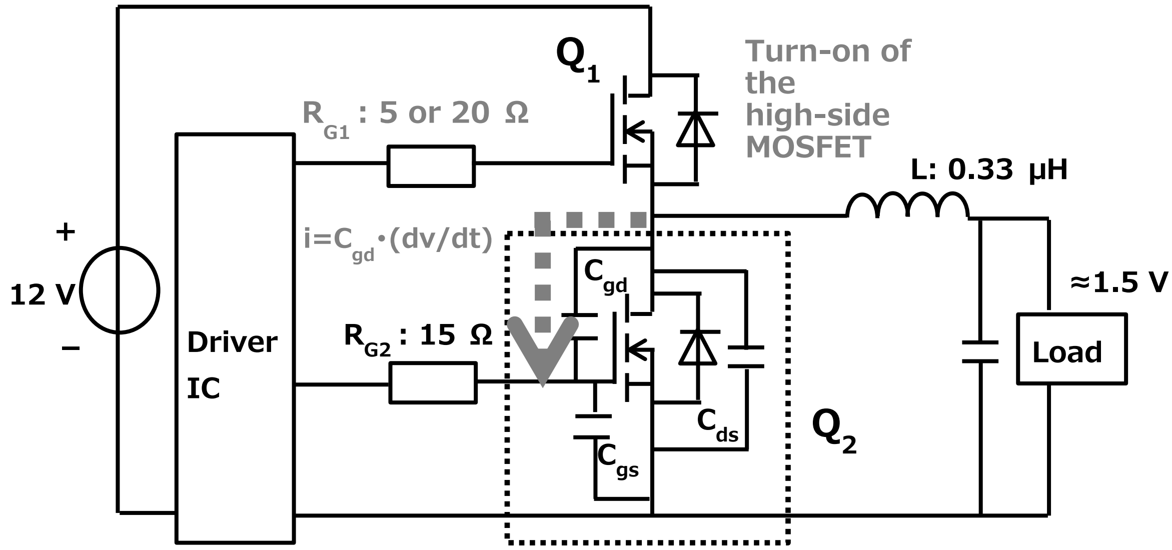
Figure 2.2b Waveforms of the circuit of Figure 2.2a

2.1.3. Changing the slope of the voltage-versus-time curve (dv/dt) to prevent self-turn-on

Next, we simulated the impact of the fast changing drain-source voltage (with a high dv/dt rate) on the MOSFET self-turn-on. (We intentionally selected simulation conditions that would cause self-turn-on.)

We experimented with different gate resistors R_{G1} for the high-side MOSFET Q_1 in order to change the dv/dt rate of the drain-source voltage of the MOSFET Q_2 and determined whether self-turn-on occurs as a result.

The voltage superimposed on the gate is expressed as $C_{gd}/(C_{gs}+C_{gd})\cdot v(t)$. A simulation showed that reducing the dv/dt rate of the drain-source voltage helped prevent self-turn-on. This is probably because when the dv/dt rate is small, t is outside the range of v(t) in which the equation is satisfied and v(t) became smaller as a result.



MOSFET used
30 V/16 A
C_{iss}:1350 pF
C_{rss}:63 pF

Assuming the use of surface-mount MOSFETs, their lead inductances are not considered here.

Figure 2.3a Simulation circuit model

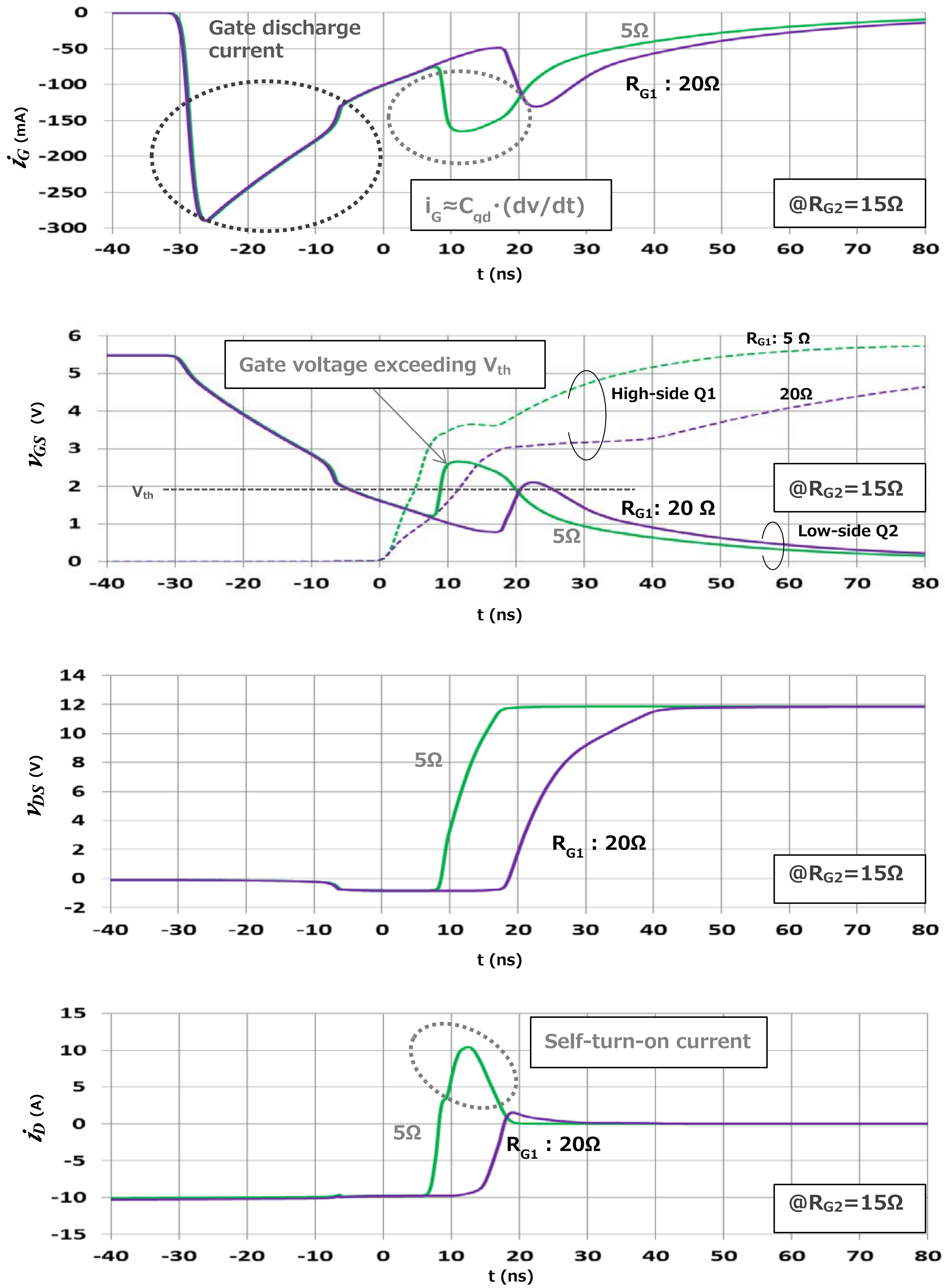


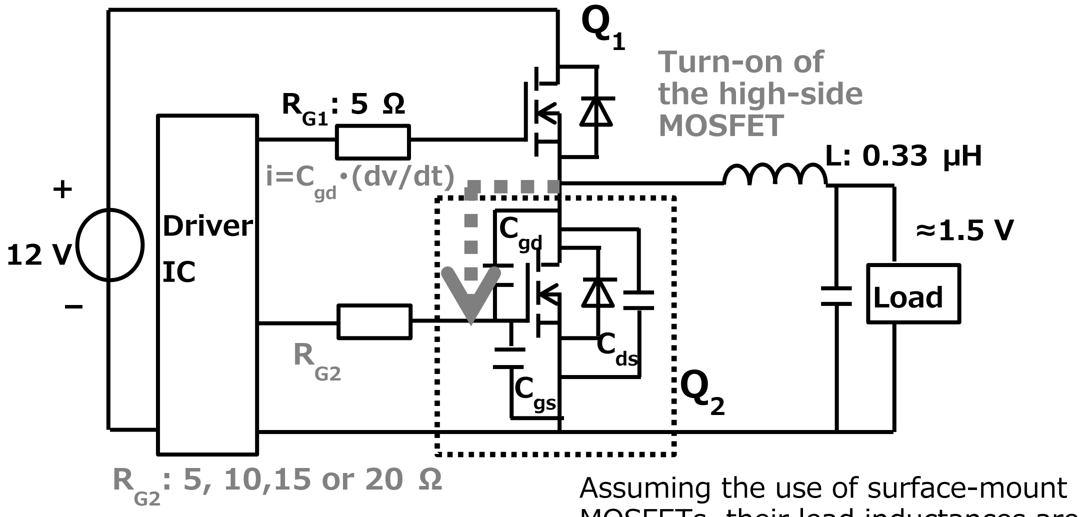
Figure 2.3b Waveforms of the circuit of Figure 2.3a

2.1.4. Effect of the gate resistor on self-turn-on

We simulated the occurrence of self-turn-on in the circuit shown in Figure 2.4a using different gate resistors R_{G2} for the low-side MOSFET Q_2. (We intentionally selected simulation conditions that would cause self-turn-on.)

Our simulation showed that the circuit with a larger gate resistor is more susceptible to self-turn-on. This is probably because the increase in the gate resistance caused the current and voltage resulting from the discharging of the gate charge persisted longer, offsetting the positive effect of the reduced dv/dt rate on the gate voltage. In reality, increasing the gate resistance did not significantly affect the gate current for the MOSFET Q_2 during the dv/dt period.

Because the MOSFETs in a real-world DC/DC converter switch at a very high frequency (300 to 500 kHz), a small gate resistor and a short dead-time period are typically used. Although we used a large gate resistor for this simulation in order to force self-turn-on to occur, such a large resistor is unlikely to be used in an actual DC/DC converter. In the event of self-turn-on, it will be difficult to work around the self-turn-on problem by adding an external gate resistor.



Assuming the use of surface-mount MOSFETs, their lead inductances are not considered here.

MOSFET used

30 V/16 A, C_{iss}:1350 pF, C_{rss}:63 pF

Figure 2.4a Simulation circuit model

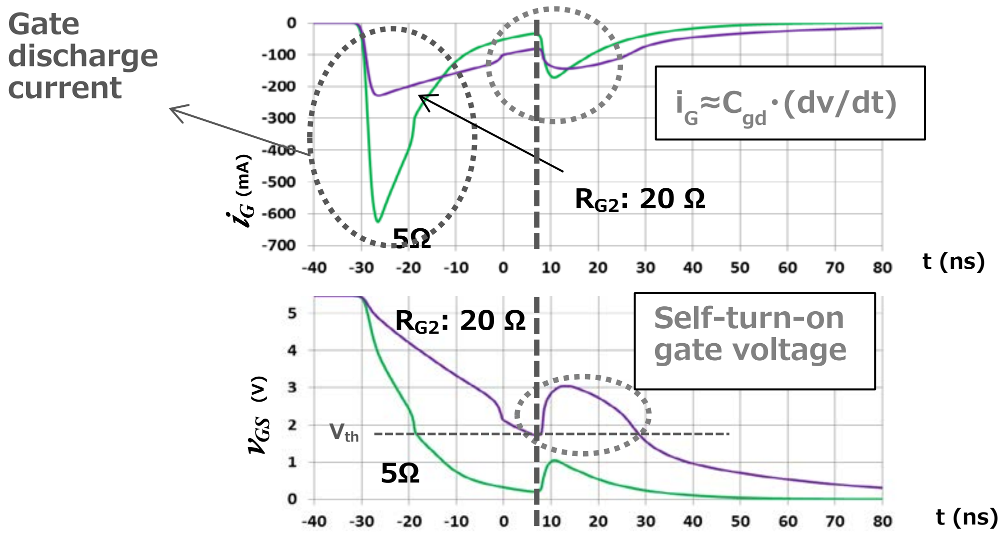


Figure 2.4b Gate current and voltage of the low-side MOSFET Q_2

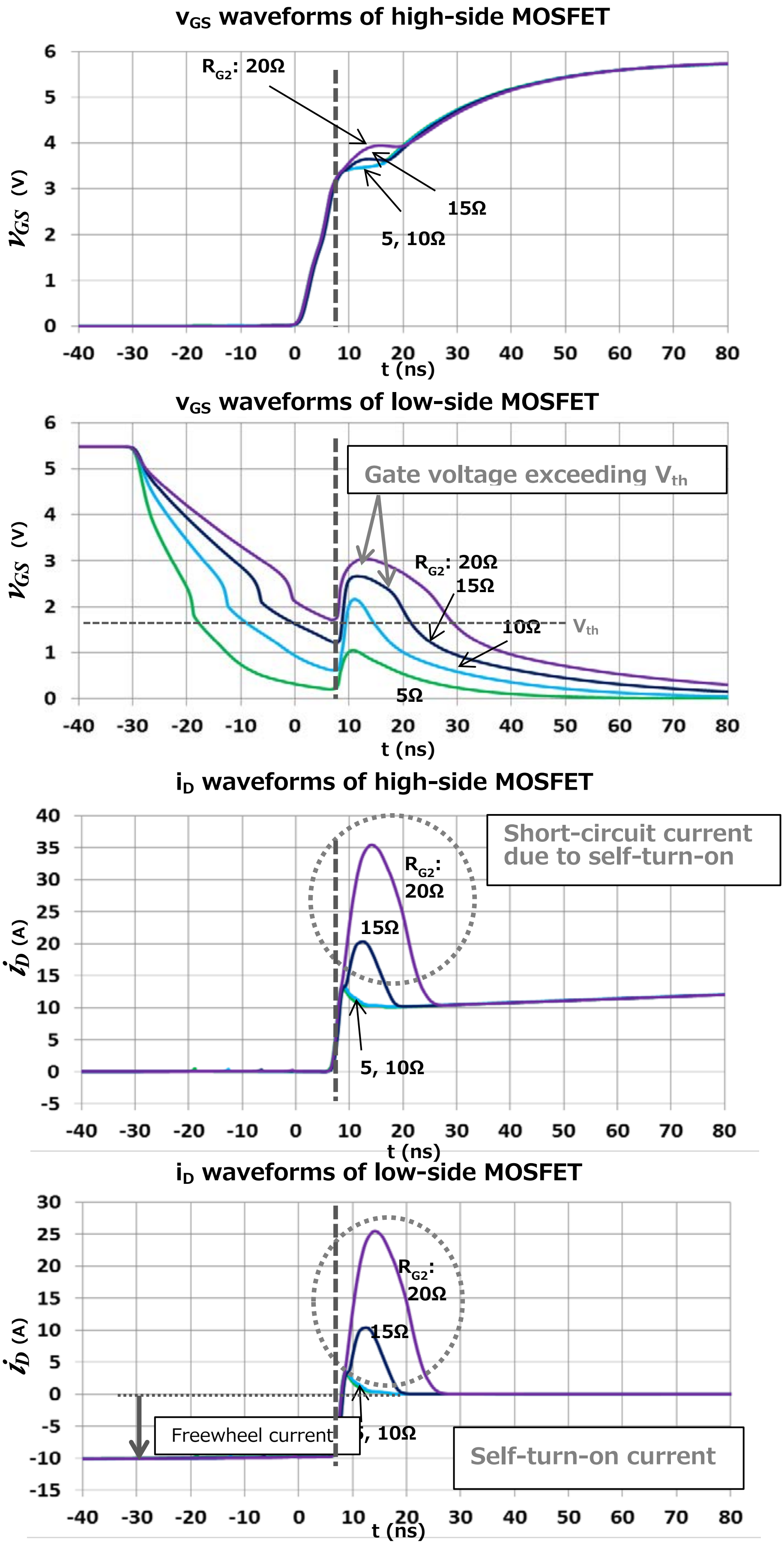


Figure 2.4c v_{GS} and i_D waveforms of the high-side and low-side MOSFETs

2.2. Inverter circuit configured as a bridge

2.2.1. Method of checking for self-turn-on

Figure 2.5 shows an inverter circuit configured as a bridge. When the MOSFET Q_1 in this circuit turns on, a high dv/dt voltage is applied across the drain and source terminals of the MOSFET Q_2. Consequently, a current flows to the gate resistor via the gate-drain capacitance C_{gd} of Q_2, lifting its gate voltage. As a result, the MOSFET Q_2 might falsely turn on.

The basic operation of the inverter circuit is shown in Figure 2.5. In a simulation, we applied a train of two pulses to the gate of the MOSFET Q_1 in order to examine the self-turn-on of the MOSFET Q_2 as follows:

1. The first gate pulse applied to the MOSFET Q_1 causes a current to flow to the inductor L.
2. When the MOSFET Q_1 turns off, this current flows back through the body diode of the MOSFET Q_2.
3. Upon application of the second gate pulse to Q_1, the body diode of Q_2 enters reverse recovery t_{rr} mode. Thereafter, a high-dv/dt drain-source voltage is applied Q_2. As a result, a current flows to the gate resistor R_{G2} for the MOSFET Q_2, lifting its gate voltage.

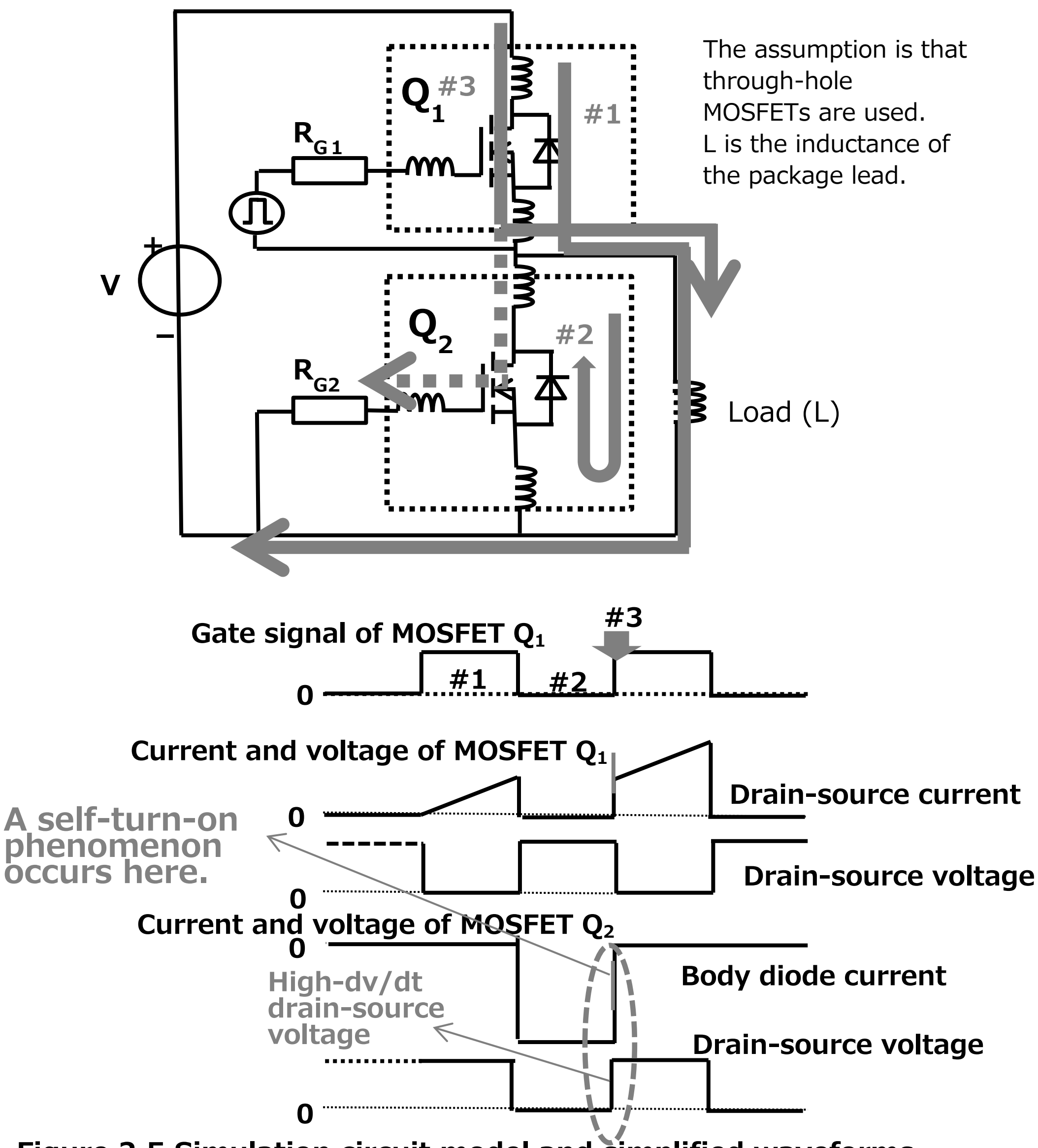
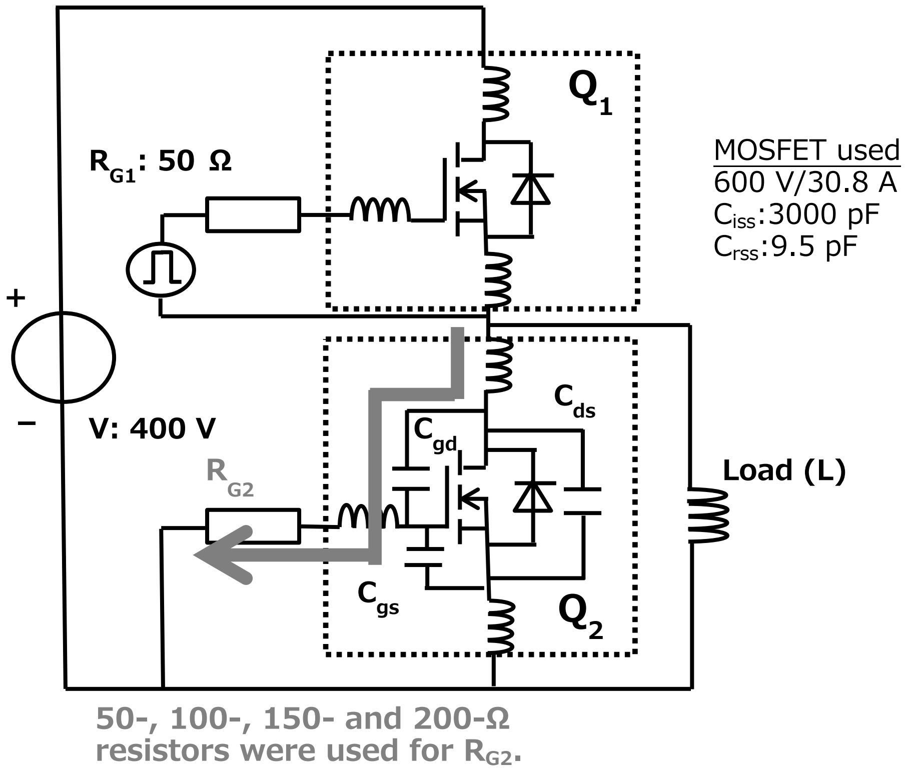


Figure 2.5 Simulation circuit model and simplified waveforms

2.2.2. Effect of the gate resistor on self-turn-on

In order to examine the effect of the gate resistor, we performed simulations, changing the value of the gate resistor R_{G2} for the MOSFET Q_2 (in the off state) in the range from 50 Ω to 200 Ω. The larger the gate resistance R_{G2}, the more susceptible the MOSFET becomes to self-turn-on. ($v_{GS}=R_G \cdot C_{gd} \cdot (dv/dt)$)

The current flowing to the gate of a MOSFET is limited by the associated gate resistor. The greater the gate resistance, the smaller the gate current. However, because voltage is the product of current and resistance, the greater the gate resistance, the greater the gate voltage becomes. Self-turn-on occurs when the gate voltage exceeds V_{th}. (We intentionally selected simulation conditions that would cause self-turn-on.)



The assumptions are that through-hole MOSFETs are used and that the package lead has an inductance of 2 nH.

Figure 2.6a Simulation circuit model

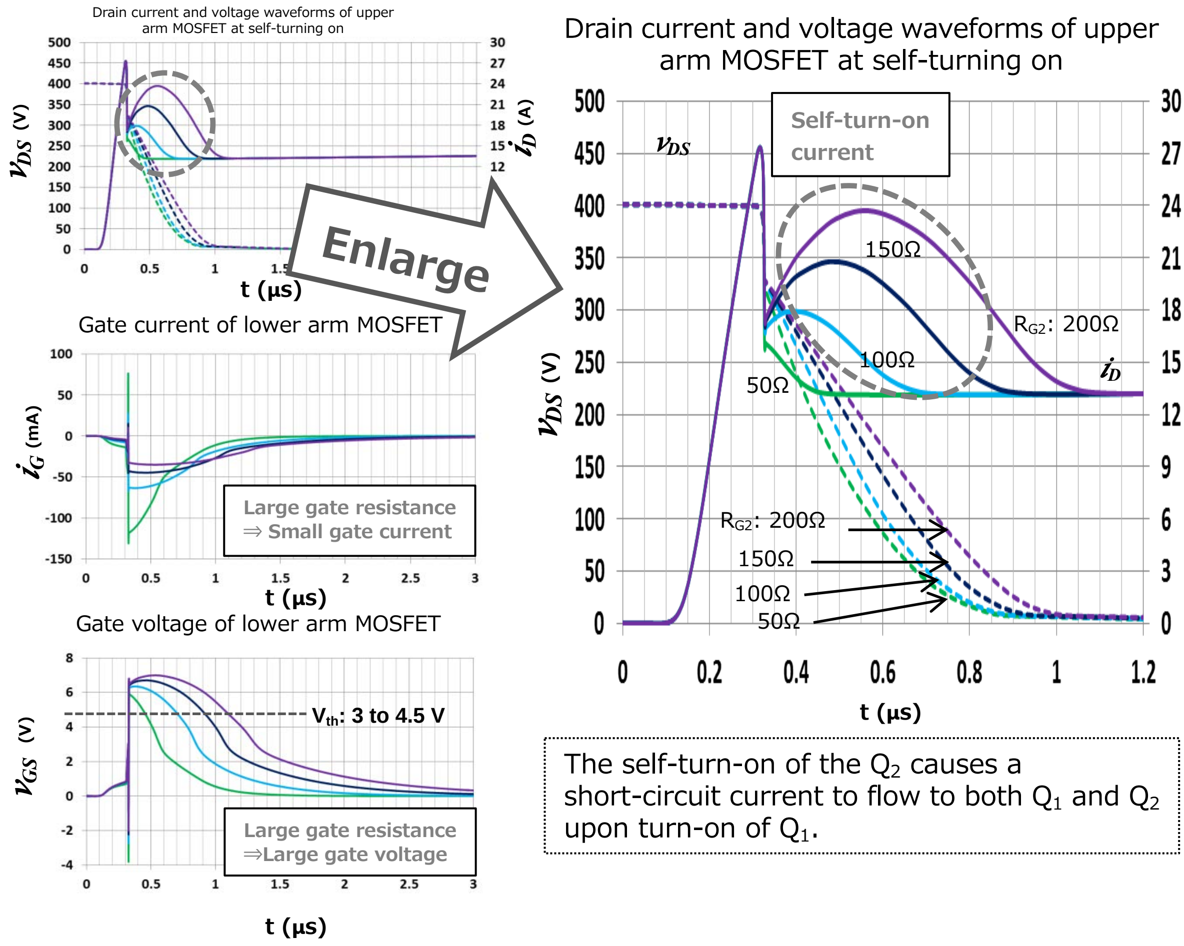
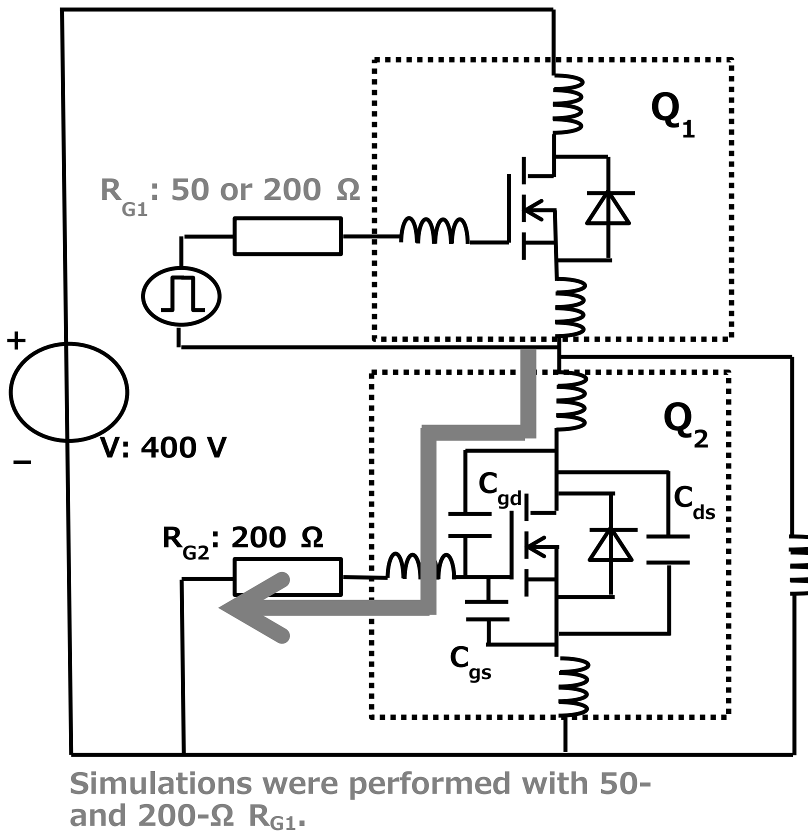


Figure 2.6b Turn-on curves

2.2.3. Effect of the slope of the voltage-versus-time curve (dv/dt) on self-turn-on

This section discusses the effect of the dv/dt rate of the drain-source voltage on self-turn-on. Since $v_{GS}=R_G \cdot C_{gd} \cdot (dv/dt)$, a rise in the gate voltage can be reduced by reducing dv/dt.
In order to adjust the dv/dt rate while the MOSFET Q_2 is in reverse recovery t_{rr} mode, the value of the gate resistor R_{G1} for the MOSFET Q_1 in the gate driver was changed under the conditions in which self-turn-on occurs (with a 200-Ω gate resistor connected to the MOSFET Q_2). The MOSFET Q_2 can be made less susceptible to self-turn-on by increasing the R_{G1} value to reduce the dv/dt rate. (We intentionally selected simulation conditions that would cause self-turn-on.)



MOSFET used
600 V/30.8 A
C_{iss}:3000 pF
C_{rss}:9.5 pF

The assumptions are that through-hole MOSFETs are used and that the package lead has an inductance of 2 nH.

Figure 2.7a Simulation circuit model

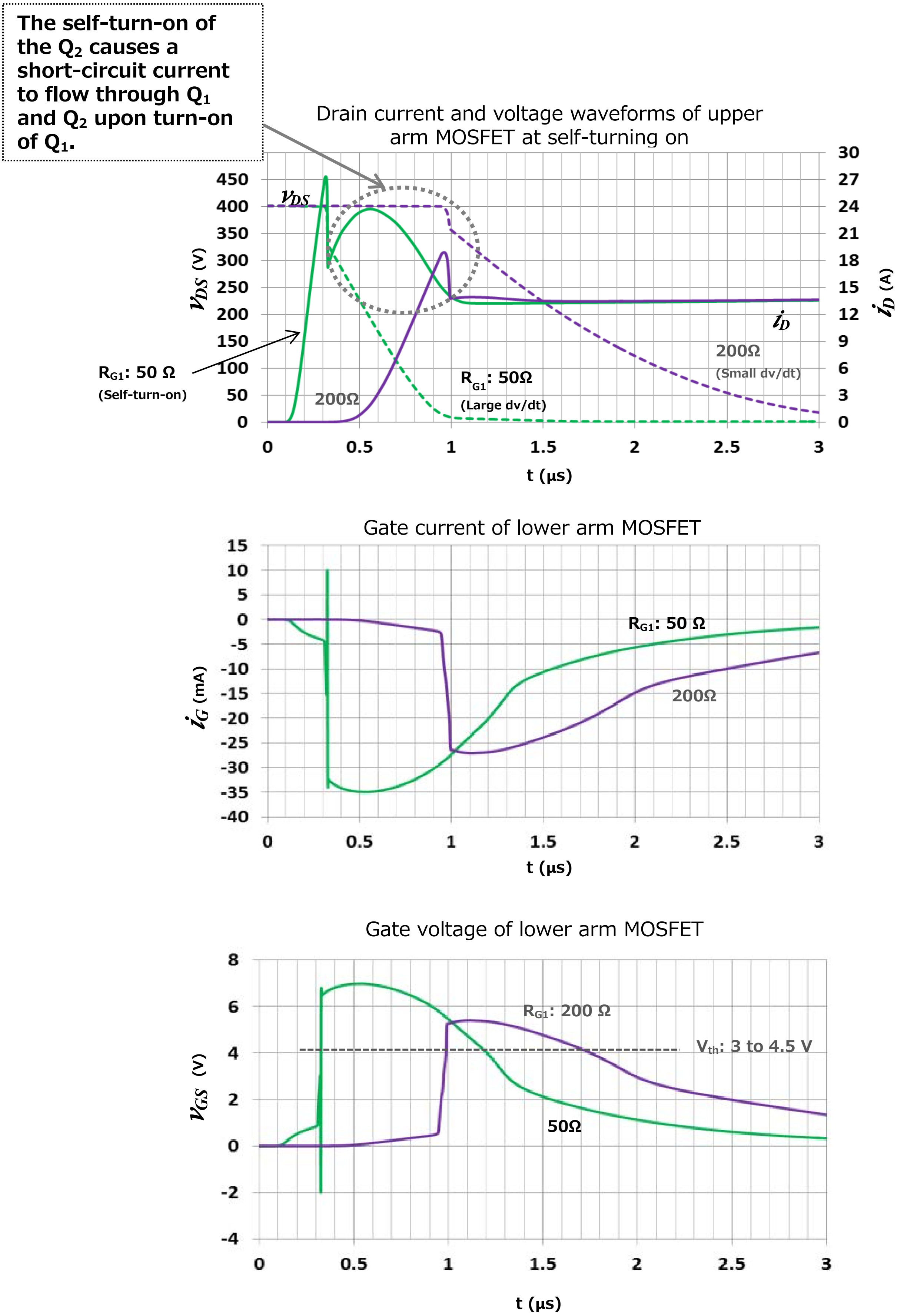


Figure 2.7b Turn-on curves

3. Preventing self-turn-on

3.1. Preventing MOSFET self-turn-on in a non-isolated DC-DC converter

When a voltage is applied to a MOSFET, a current generally flows via its gate-drain capacitance C_{gd}. This current is expressed as $i = C_{gd}\frac{dv}{dt}$.
As a result, a voltage is induced across the gate and source terminals:

$$v_{GS} = R_G C_{gd}\frac{dv}{dt}\left\{1 - \exp\left(\frac{-t}{(C_{gs} + C_{gd})R_G}\right)\right\}$$

(Here, the assumption is that MOSFET capacitances, C_{gs} and C_{gd}, do not change with the voltage.)
In an ultra-high-frequency (300- to 500-kHz) non-isolated DC/DC converter, the MOSFETs in it also switch at a very high frequency. In this case, a self-turn-on phenomenon occurs when the gate-source voltage v_{GS} of the MOSFET exceeds its V_{th}. v_{GS} is expressed as follows:

When the dv/dt transient is shorter than (C_{gs}+ C_{gd})·R_G

(i.e., when $t \ll (C_{gs}+C_{gd})\cdot R_G$)

$$v_{GS} \approx \frac{C_{gd}}{(C_{gs} + C_{gd})} v(t)$$

(where, v(t) can be considered to be equal to the supply voltage V when t is short.)

Preventing self-turn-on

Selecting MOSFETs with **a high V_{th} and a low C_{gd}/C_{gs} ratio** is of primary importance. In addition, a DC/DC converter circuit can be designed with:

· **a capacitor between the gate and source terminals of the MOSFET in order to further reduce the C_{gd}/C_{gs} ratio. (Figure 3.1)**

Care should be exercised, however, because adding a capacitor between the gate and source terminals of a MOSFET affects its switching speed.

It might be possible to reduce the dv/dt rate by slowing the turn-on of only the high-side device. However, this does not often serve as an effective solution because switching losses increase, considering many DC/DC converters are designed to operate at a high frequency.

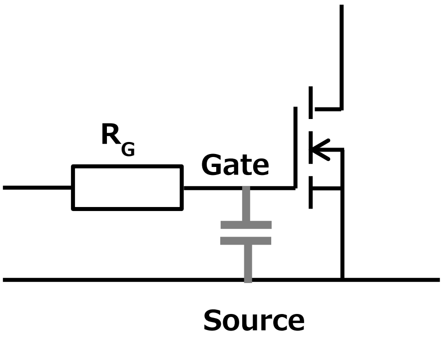


Figure 3.1 Adding a capacitor across the gate and source terminals

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3.2. Preventing MOSFET self-turn-on in an inverter configured as a bridge

When a voltage is applied to a MOSFET, a current generally flows via its gate-drain capacitance (C_{gd}). This current is expressed as $\boldsymbol{i = C_{gd}\frac{dv}{dt}}$.

As a result, a voltage is induced across the gate and source terminals:

$$\boldsymbol{v_{GS} = R_G C_{gd}\frac{dv}{dt}\left\{1 - \exp\left(\frac{-t}{(C_{gs} + C_{gd})R_G}\right)\right\}}$$

(Here, the assumption is that MOSFET capacitances, C_{gs} and C_{gd}, do not change with the voltage.)

Inverter circuits are typically used at a switching frequency of around 20 kHz. So, the MOSFETs in an inverter circuit are not required to switch as fast as those in a non-isolated DC/DC converter. v_{GS} fluctuates early during the dv/dt period according to the ratio between the gate-drain and gate-source capacitances, but a self-turn-on phenomenon is affected most significantly by the result of the following equation. When v_{GS}, which is calculated as follows, exceeds the V_{th} of a MOSFET, it experiences self-turn-on.

When the dv/dt transient is longer than (C_{gs}+ C_{gd})・R_G (i.e., t»(C_{gs}+ C_{gd})・R_G)

$$\boldsymbol{v_{GS} \approx R_G C_{gd}\frac{dv}{dt}}$$

Preventing self-turn-on

Selecting MOSFETs with **a high V_{th} and a low C_{gd}** is of primary importance. In addition, an inverter circuit can be designed as follows to prevent self-turn-on:

- Reduce the dv/dt rate during turn-on. (Increase the turn-on resistance.) (Figure 3.2)
- Reduce R_G during turn-off. (Reduce the turn-off resistance.) (Figure 3.2)
- Use a negative gate voltage. (Figure 3.3)
- Use a shunt circuit at the gate. (Figure 3.4)

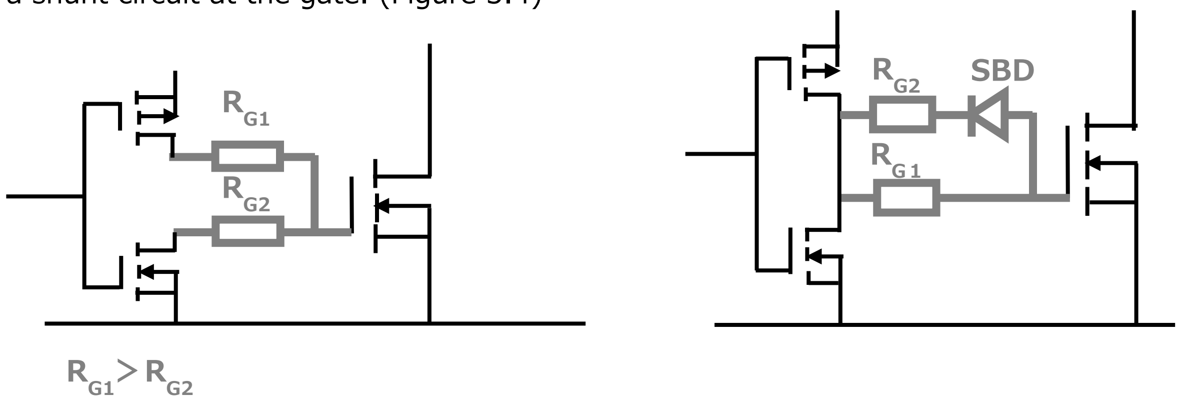

Figure 3.2 Using separate gate resistors for turn-on and turn-off

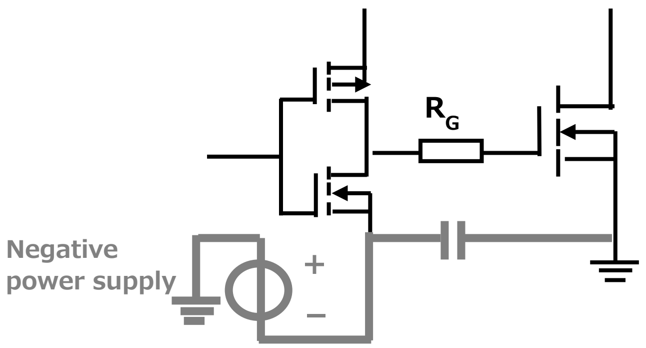

Figure 3.3 Using a negative gate power supply

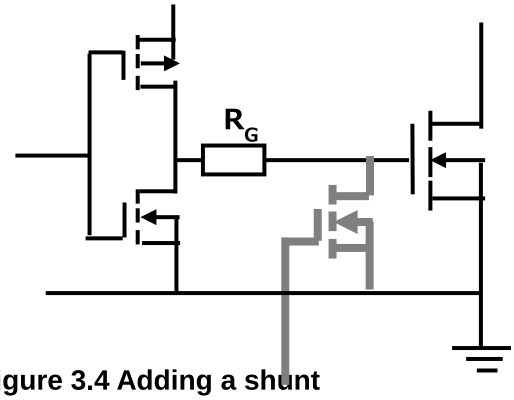

Figure 3.4 Adding a shunt circuit

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