32-bit RISC Microcontroller

TMPM3H Group(2)

Reference Manual
Memory Map
(MMAP-M3H(2))

Revision 2.0

2018-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Content

List of Figures

List of Tables

Preface

Related document

Document name
Arm documentation set Cortex-M3

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of two or more same kind of units and channels in same register name in the Register List.

  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0]→[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

The Flash memory uses the Super Flash® technology under license from Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

APB	Advanced Peripheral Bus
ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
AO	Constant energization region (8bit Bus)
A-PMD	Advanced Programmable Motor Control Circuit
CG	Clock Control and Operation Mode
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
FLASHIF	Flash Interface
I^2C	Inter-Integrated Circuit
I2CS	I^2C wake-up circuit from Stand-by mode
IA(INT-I/F)	Interrupt control register A
IB(INT-I/F)	Interrupt control register B
IMN	Interrupt Monitor
IO	IO Bus(32bit Peripheral Bus)
LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
PAMP	RAM Parity Circuit
RLM	Low speed oscillation / power supply control / reset
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Memory Map

The memory maps for TMPM3H group (2) are based on the Arm® Cortex®-M3 processor core memory map.
The internal ROM, internal RAM and special function registers (SFR) of TMPM3H group (2) are mapped to the Code, SRAM and peripheral regions of the Cortex-M3 respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register area is the processor core's internal register region.

For more information on each region, see the "Arm documentation set Cortex-M3".

Note that access to regions indicated as "Fault" causes a memory fault if memory faults are enabled, or causes a hard fault if memory faults are disabled. Also, do not access the vendor-specific region.

1.1. TMPM3HxFD

Code Flash : 512KB
RAM : 64KB
Data Flash : 32KB
Target product : TMPM3HQFDFG, TMPM3HPFDFG, TMPM3HNFDFG, TMPM3HNFDDFG, TMPM3HMFDFG, TMPM3HLFDUG

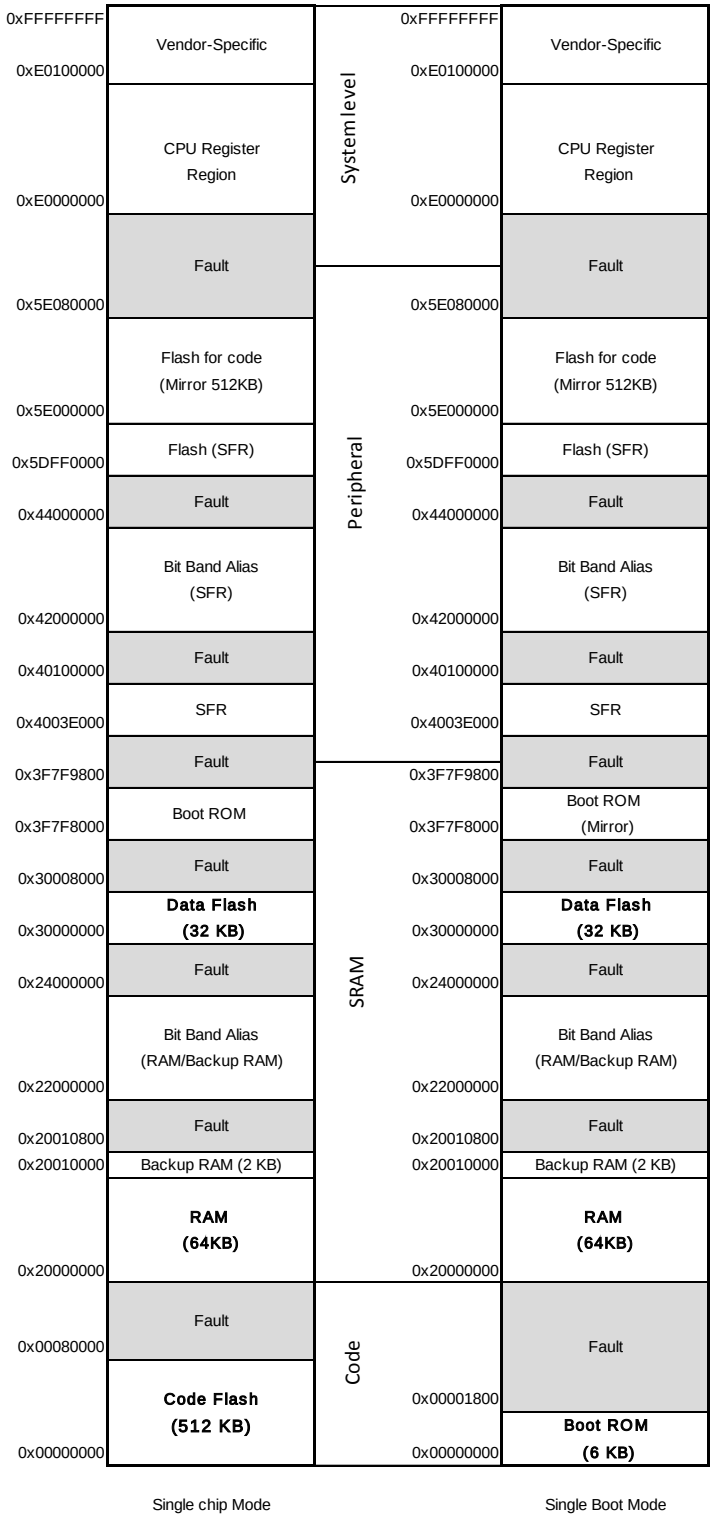

Figure 1.1 TMPM3HxFD

1.2. TMPM3HxFZ

Code Flash : 384KB
RAM : 64KB
Data Flash : 32KB
Target product : TMPM3HQFZFG, TMPM3HPFZFG, TMPM3HNFZFG, TMPM3HNFZDFG, TMPM3HMFZFG, TMPM3HLFZUG

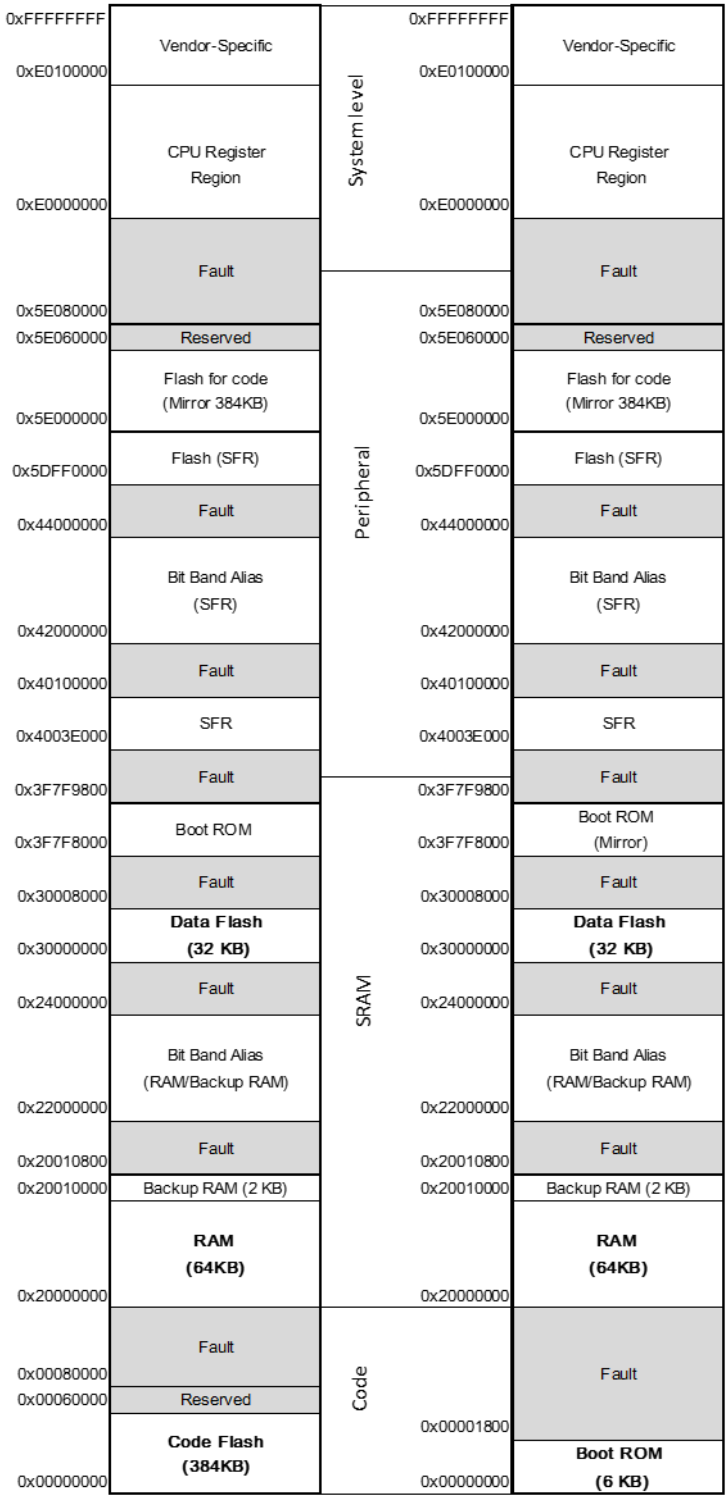

Figure 1.2 TMPM3HxFZ

1.3. TMPM3HxFY

Code Flash : 256KB
RAM : 64KB
Data Flash : 32KB
Target product : TMPM3HQFYFG, TMPM3HPFYFG, TMPM3HNFYFG, TMPM3HNFYDFG, TMPM3HMFYFG, TMPM3HLFYUG

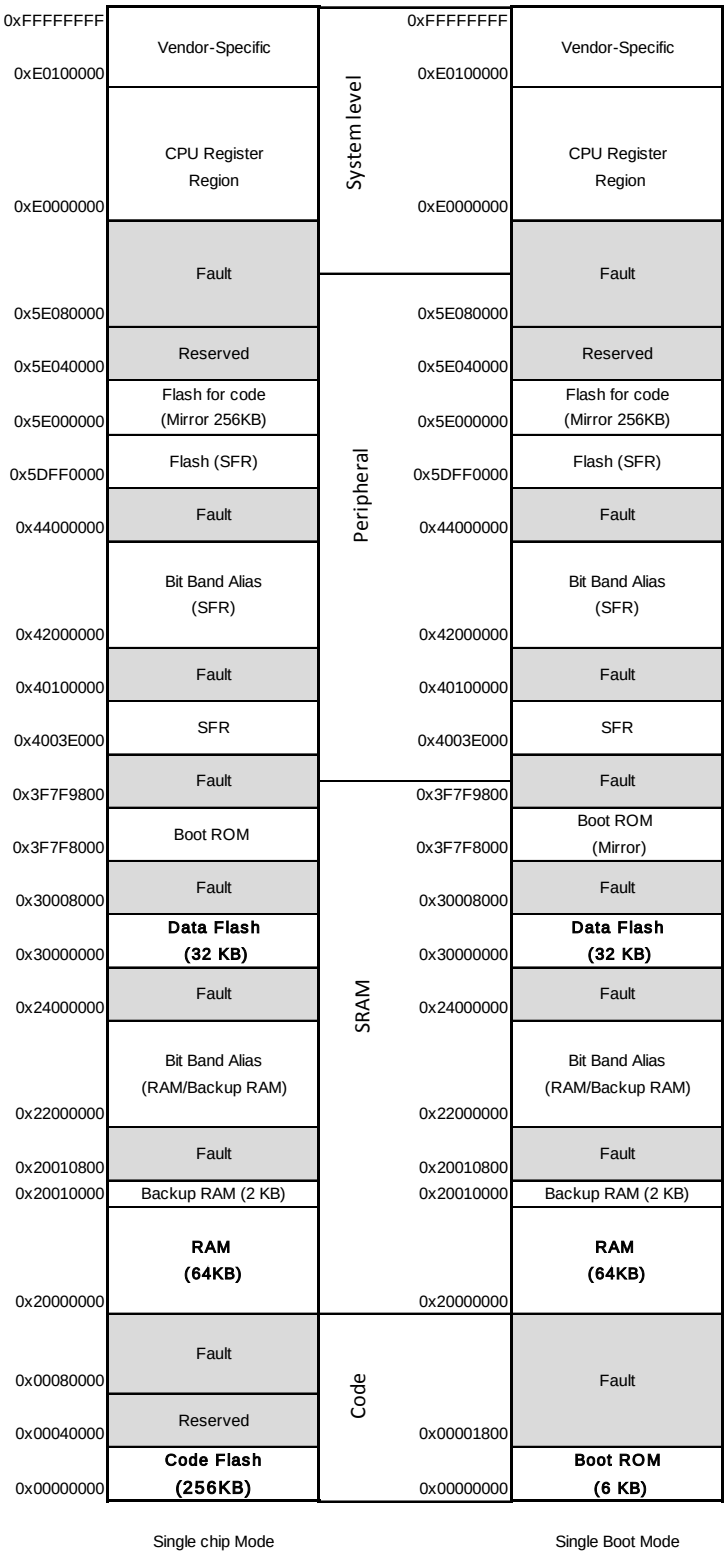

Figure 1.3 TMPM3HxFY

2. Bus Matrix

This MCU contains two bus masters such as a CPU core and DMA controllers.

Bus masters connect to slave ports (S0 to S4) of Bus Matrix. In the bus matrix, master ports (M0 to M14) connect to peripheral functions via connections described as (o) or (●) in the following figure. (●) shows a connection to a mirror area.

While multiple slaves are connected on the same bus master line in the Bus Matrix, if multiple slave accesses are generated at the same time, a priority is given to access from a master with the smallest slave number.

2.1. Structure

2.1.1. Single chip mode

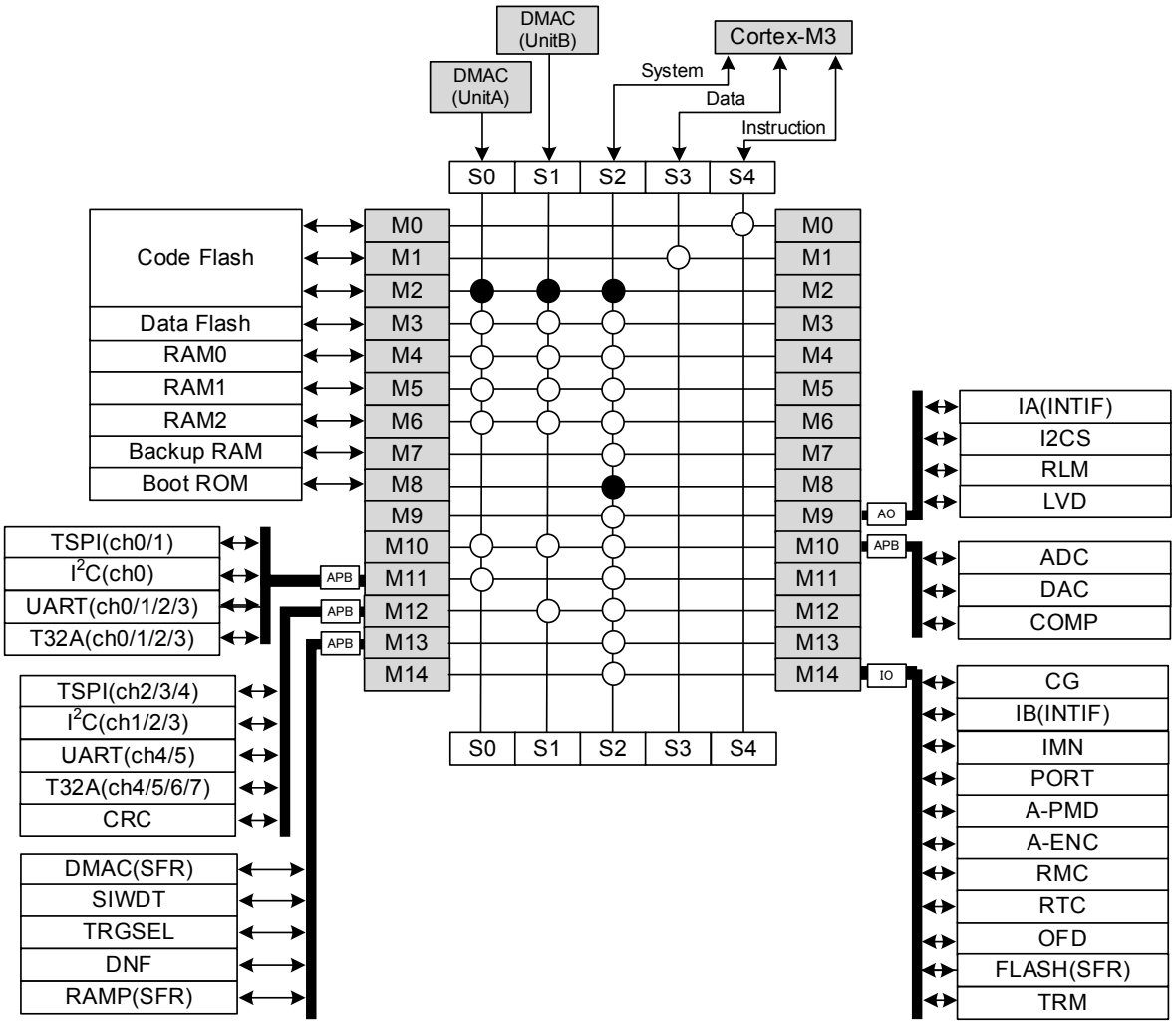

Figure 2.1 Single chip mode

2.1.2. Single boot mode

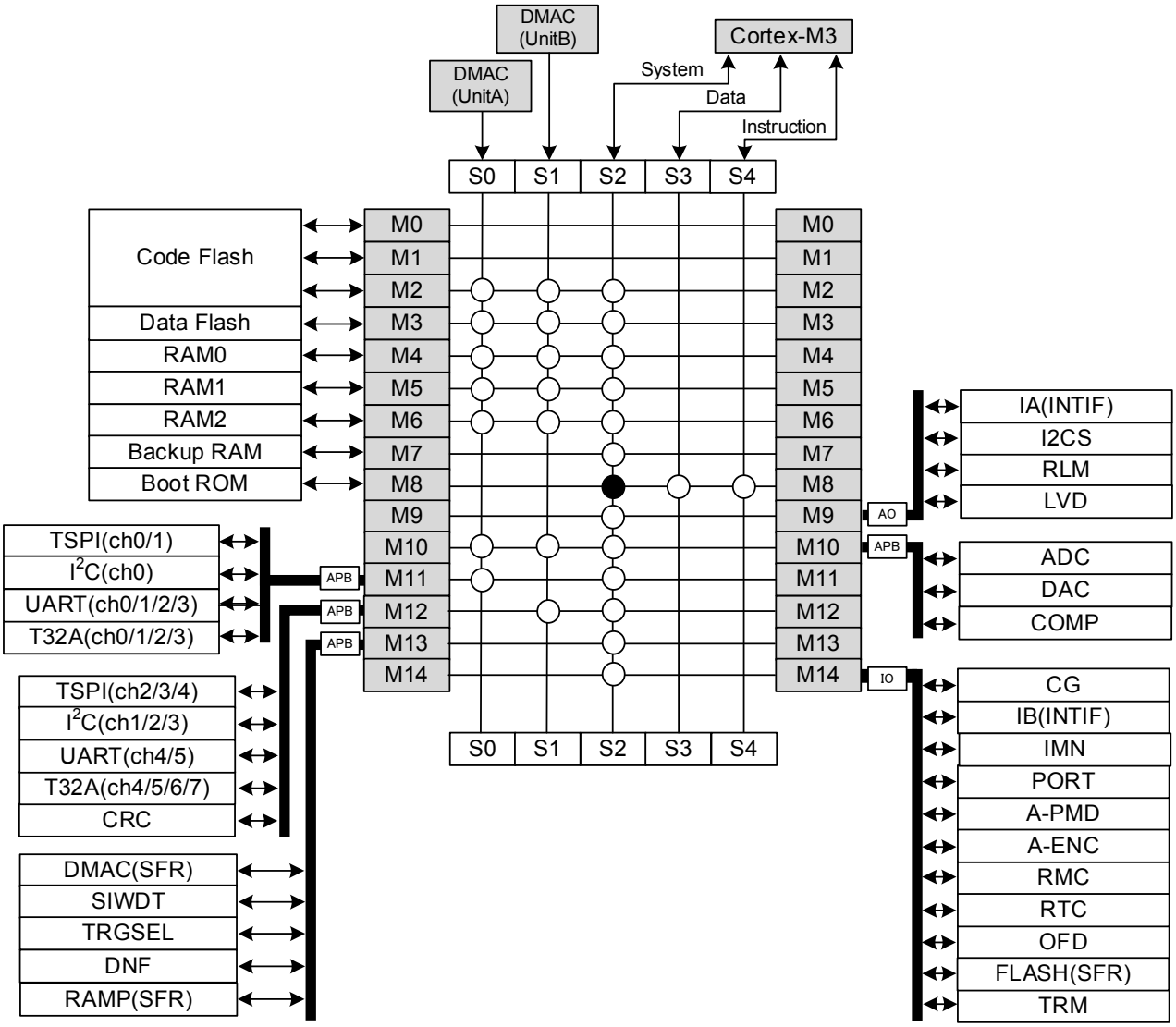

Figure 2.2 Single boot mode

2.2. Connection table

2.2.1. Code area / SRAM area

(1) Single chip mode

Table 2.1 Single chip mode

Start Address	Slave		Master				
			DMAC (Unit A)	DMAC (Unit B)	Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2	S3	S4
0x00000000	Code Flash	M0	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	-	✓	Fault
0x00080000	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M4	✓	✓	✓	-	-
0x20004000	RAM1	M5	✓	✓	✓	-	-
0x20008000	RAM2	M6	✓	✓	✓	-	-
0x20010000	Backup RAM	M7	Fault	Fault	✓	-	-
0x20010800	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM	M8	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.3 Peripheral area".							
0x5E000000	Code Flash (Mirror)	M2	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(2) Single boot mode

Table 2.2 Single boot mode

Start Address	Slave		Master				
			DMAC (Unit A)	DMAC (Unit B)	Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2	S3	S4
0x00000000	Boot ROM	M8	Fault	Fault	-	✓	✓
0x00001800	Fault	-	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M4	✓	✓	✓	-	-
0x20004000	RAM1	M5	✓	✓	✓	-	-
0x20008000	RAM2	M6	✓	✓	✓	-	-
0x20010000	Backup RAM	M7	Fault	Fault	✓	-	-
0x20010800	Fault	-	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	✓	-	-
0x24000000	Fault	-	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M3	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	-	-
0x3F7F8000	Boot ROM (Mirror)	M8	Fault	Fault	✓	-	-
0x3F7F9800	Fault	-	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.3 Peripheral area".							
0x5E000000	Code Flash (Mirror)	M2	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.2. Peripheral area

Table 2.3 Peripheral area

Start Address	Slave		Master				
			DMAC (Unit A)	DMAC (Unit B)	Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2	S3	S4
0x40000000	Fault	-	Fault	Fault	Fault	-	-
0x4003E000	IA(INTIF)	M9	Fault	Fault	✓	-	-
0x4003E400	RLM		Fault	Fault	✓	-	-
0x4003E800	I2CS		Fault	Fault	✓	-	-
0x4003EC00	LVD		Fault	Fault	✓	-	-
0x4004C000	DMAC(SFR)	M13	Fault	Fault	✓	-	-
0x40054000	DAC(ch0/1)	M10	✓	✓	✓	-	-
0x40098000	TSPI(ch0/1)	M11	✓	Fault	✓	-	-
0x4009A000	TSPI(ch2/3/4)	M12	Fault	✓	✓	-	-
0x400A0000	I^2C(ch0)	M11	✓	Fault	✓	-	-
0x400A1000	I^2C(ch1/2/3)	M12	Fault	✓	✓	-	-
0x400B8800	ADC	M10	✓	✓	✓	-	-
0x400BA000	T32A(ch0/1/2/3)	M11	✓	Fault	✓	-	-
0x400BA400	T32A(ch4/5/6/7)	M12	Fault	✓	✓	-	-
0x400BB000	UART(ch0/1/2/3)	M11	✓	Fault	✓	-	-
0x400BB400	SIWDT	M13	Fault	Fault	✓	-	-
0x400BB600	DNF		Fault	Fault	✓	-	-
0x400BB800	TRGSEL		Fault	Fault	✓	-	-
0x400BBB00	RAMP(Parity)		Fault	Fault	✓	-	-
0x400BBC00	CRC	M12	Fault	✓	✓	-	-
0x400BBD00	UART(ch4/5)		Fault	✓	✓	-	-
0x400BC000	COMP	M10	✓	✓	✓	-	-
0x400C0000	PORT	M14	Fault	Fault	✓	-	-
0x400CC000	RTC		Fault	Fault	✓	-	-
0x400E7000	RMC		Fault	Fault	✓	-	-
0x400F1000	OFD		Fault	Fault	✓	-	-
0x400F3000	CG		Fault	Fault	✓	-	-
0x400F3200	TRM		Fault	Fault	✓	-	-
0x400F4E00	IB(INTIF)		Fault	Fault	✓	-	-
0x400F4F00	IMN		Fault	Fault	✓	-	-
0x400F6000	A-PMD		Fault	Fault	✓	-	-
0x400F7000	A-ENC		Fault	Fault	✓	-	-
0x40100000	Fault	-	Fault	Fault	Fault	-	-
0x42000000	Bit Band Alias	-	Fault	Fault	✓	-	-
0x44000000	Fault	-	Fault	Fault	Fault	-	-
0x5DFF0000	FLASH(SFR)	M14	Fault	Fault	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2017-10-05	First release
1.1	2018-06-25	- Terms and Abbreviations: The mistyping was corrected. - 1.1. TMPM3HxFD/ 1.2. TMPM3HxFZ/ 1.3. TMPM3HxFY Corrected "Flash for code" -> "Code Flash" in figures 1.1 to 1.3. Deleted "TMPM3HMFDDFG", "TMPM3HMFZDFG", and "TMPM3HMFYDFG" of target product. - 2.1.1. Single chip mode / 2.1.2. Single boot mode Deleted “APB: Advanced Peripheral Bus, AO: 8bit-Bus for the non-block domain, IO: 32bit-Bus for the block domain” in Figure 2.1 and Figure 2.2. - 2.2.1. Code area / SRAM area Corrected contents in Table 2.1 and Table 2.2. - 2.2.2. Peripheral area Corrected chapter name and table name (Table 2.3). Corrected contents in Table 2.3. (Addition of TSPI (ch 2/3/4), others.)
2.0	2018-07-31	- Revised the SST's registered trademark. - Terms and Abbreviations revised "CG" - 1.1 added "TMPM3HLFDUG" as Target product. - 1.2 added "TMPM3HLFZUG" as Target product. - 1.3 added "TMPM3HLFYUG" as Target product.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**