

32-bit RISC Microcontroller

TXZ Family

Reference Manual Comparator (COMP-B)

Revision 1.2

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

Related document

| Document name |
|---|
| Clock Control and Operation Mode |
| 8-bit Digital to Analog Converter |
| Advanced Programmable Motor Control Circuit |
| 12-bit Analog to Digital Converter |
| Product Information |

Conventions

- Numeric formats follow the rules as shown below:
 - Hexadecimal: 0xABC
 - Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
 - Binary: 0b111 – It is possible to omit the “0b” when the number of bit can be distinctly understood from a sentence.
- “_N” is added to the end of signal names to indicate low active signals.
- It is called “assert” that a signal moves to its active level, “deassert” to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [] defines the register.
Example: [ABCD]
- “n” substitutes suffix number of two or more same kind of registers, fields, and bit names.
Example: [XYZ1], [XYZ2], [XYZ3] → [XYZn]
- “x” substitutes suffix number or character of units and channels in the Register List.
 - In case of unit, “x” means A, B, and C . . .
 - Example: [ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]
 - In case of channel, “x” means 0, 1, and 2 . . .
 - Example: [T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]
- The bit range of a register is written like as [m: n].
Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
Example: [ABCD]<EFG> = 0x01 (hexadecimal), [XYZn]<VW> = 1 (binary)
- Word and Byte represent the following bit length.
 - Byte: 8 bits
 - Half word: 16 bits
 - Word: 32 bits
 - Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
 - R: Read only
 - W: Write only
 - R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of “-” is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is “-“, follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is “-“, follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

| | |
|-------|---|
| ADC | Analog to Digital Converter |
| A-PMD | Advanced Programmable Motor Control Circuit |
| COMP | Comparator |
| DAC | Digital to Analog Converter |
| EMG | Emergency |

1. Outline

A comparator (COMP) compares analog input voltage (AINA00 or AINA01) with reference voltage.

Table 1.1 Comparator Functions

| Function classification | Function | A Functional Description or the range |
|-------------------------|------------------------------|---------------------------------------|
| comparison | Selection of compare voltage | Select AINA00 or AINA01 |
| | Reference voltage | Use output of built-in DAC channel 0 |

2. Configuration

A comparator compares voltage input (VINC) from AINA00 or AINA01 with reference voltage (VREFC: channel 0 of built-in 8-bit digital to analog converter(DAC) output). A comparative result (COMP output) is outputted to the EMG input of Advanced Programmable Control Circuit(A-PMD).

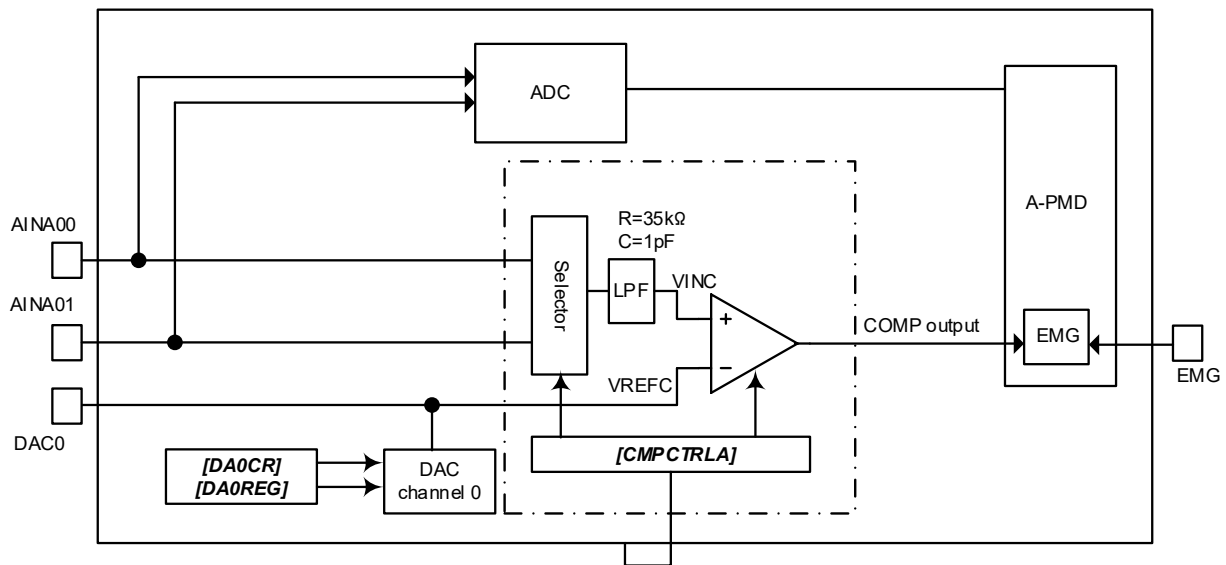


Figure 2.1 Configuration of Comparator and Outside circuits

Table 2.1 Signal List

| No | Symbol | Signal name | I/O | Related reference manual |
|----|--------|---------------------|--------|--|
| 1 | AINA00 | Analog input pin 00 | Input | Product Information, 12-bit Analog to Digital Converter |
| 2 | AINA01 | Analog input pin 01 | Input | Product Information, 12-bit Analog to Digital Converter |
| 3 | DAC0 | DAC channel0 output | Output | Product Information, 8-bit Digital to Analog Converter |

3. Operation description

3.1. Clock supply

When you use COMP, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (*[CGFSYSENA]*, *[CGFSYSMENA]*), fsys supply stop register B (*[CGFSYSENB]*, *[CGFSYSMENB]*), and fc supply stop registers (*[CGFCEN]*).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

3.2. Operation

1. Set up digital to analog converter used as reference voltage of COMP.

A conversion value is set to a *[DA0REG]* register, and *[DA0CR]<EN>* is set to "1". The voltage corresponding to a conversion value is outputted and it is inputted into a comparator as reference voltage. Please operate "2." after waiting for the stable time ($t_{sta}:4.5\mu s$) of DAC0 output.

Clear "0" to *[DA0CR]<EN>* then DAC channel 0 stops operation and the output of DAC0 becomes Hi-z. Please stop the comparator before stopping DAC channel 0.

Please refer to "8-bit Digital to Analog Converter" of the reference manual for detail.

2. Select voltage to compare and compare with reference voltage.

Select input voltage to compare by *[CMPCR]<CMPISEL>*. Next, set "1" to *[CMPCR]<CMPEN>*, then the comparator starts operation. Please operate "3." after waiting for comparator enabling time ($T_{sta}:5\mu s$).

When input voltage compare exceeds reference voltage, COMP output will be set to "1". Clear "0" to *[CMPCR]<CMPEN>*, a comparator stops operation and a COMP output is cleared to "0".

3. Set up A-PMD input.

Set "1" to *[PMDxEMGCR]<CPAIEN>*(enable input from comparator). Please refer to "Advanced Programmable Motor Control Circuit" of the reference manual for the details.

Note1: When use a comparator, DAC0 terminal must be open (Hi-z state).

When the output voltage of DAC is not stabilized, it recommends inserting a capacitor between DAC0 terminal and GND. Stable time for an output to go into less than 2 LSB after changing an DAC output setup is around 15 ms ($C=0.1\mu F$). Please adjust time according to stable condition.

Note2: Regardless to operation/stop of DAC channel 0, do not input voltage from DAC0 terminal.

Note3: VREFH is AVDD5 and VREFL is AVSS of 8-bit digital to analog converter.

3.3. Example for use

The table below shows an example of detection voltage setting when the input signal voltage is about 0V in normal condition and 1.5V when abnormality is detected.

Condition: DVDD5A=DVDD5B=AVDD5=5V, DVSSA=DVSSB=AVSS=0V
DAC: VREFH=5V, VREFL=0V, DAC accuracy ± 1 LSB

Table 3.1 Setting example (Calculation value)

| Reference voltage(V) | DAC channel 0 setting | | Detection voltage | |
|----------------------|-----------------------|------------|-------------------|--------|
| | <DAC[7:0]> | Voltage(V) | Min(V) | Max(V) |
| 0.5 | 00011010 | 0.508 | 0.466 | 0.533 |
| 0.8 | 00101001 | 0.801 | 0.759 | 0.826 |
| 1.0 | 00110100 | 1.016 | 0.974 | 1.040 |

Formula of detecting voltage:

$$V(\text{Max}) = (\text{DAC channel 0 setting voltage}) + 19.8\text{mV} + 5\text{mV}$$

$$V(\text{Min}) = (\text{DAC channel 0 setting voltage}) - 19.8\text{mV} - 22\text{mV}$$

4. Registers

4.1. Register List

The control register and address of a comparator is as follows.

| Function name | | Channel/Unit | Base address |
|---------------|------|--------------|--------------|
| Comparator | COMP | - | 0x400BC100 |

| Register name | | Address(Base+) |
|-----------------------------|-------------------|----------------|
| Comparator Control Register | <i>[CMPCTRLA]</i> | 0x0000 |

The control registers and address of DAC channel0 are as follows.

| Function name | | Channel/Unit | Base address |
|-----------------------------------|-----|--------------|--------------|
| 8-bit Digital to Analog Converter | DAC | ch0 | 0x40054000 |

| Register Name | | Address(Base+) |
|----------------------------------|-----------------|----------------|
| Control Register | <i>[DA0CR]</i> | 0x0000 |
| Converted Value Setting Register | <i>[DA0REG]</i> | 0x0004 |

4.2. Detail of Comparator Register

4.2.1. [CMPCTRLA] (Comparator Control Register)

| Bit | Bit Symbol | After reset | Type | Function |
|------|------------|-------------|------|---|
| 31:2 | - | 0 | R | Read as "0" |
| 1 | CMPISEL | 0 | R/W | Selection of analog input 0: AIN00 1: AIN01 |
| 0 | CMPEN | 0 | R/W | COMP operation 0: Stop 1: Operating |

4.3. Detail of Digital to Analog Converter Registers

4.3.1. [DA0CR] (Control Register)

| Bit | Bit Symbol | After Reset | Type | Function |
|------|------------|-------------|------|--|
| 31:1 | - | 0 | R | Read as "0" |
| 0 | EN | 0 | R/W | DAC operation 0: Stop 1: Operating |

4.3.2. [DA0REG] (Converted Value Setting Register)

| Bit | Bit Symbol | After Reset | Type | Function |
|------|------------|-------------|------|--|
| 31:8 | - | 0 | R | Read as "0" |
| 7:0 | DAC[7:0] | 0x00 | R/W | Converted value setting: Digital value corresponding to the analog output voltage value is set. The output voltage is calculated with the following formula. $DAC0 = \langle DAC \rangle \times (VREFH - VREFL) / 256$ |

5. Revision History

Table 5.1 Revision History

| Revision | Date | Description |
|----------|------------|---|
| 1.0 | 2017-10-11 | First release |
| 1.1 | 2018-03-02 | -1.Outline: Deleted “to EMG input on ... Circuit(A-PMD).” -2.Configuration: modified “A-PMD” to “Advanced ... Circuit(A-PMD)”, Corrected “[CMPCR]” to “[CMPCTRLA]” in Figure2.1, Modified “DAC0” to “DAC channel0” signal name in Table2.1. -3.3.Example for use: Deleted “value” in Table3.1 -4.1.Register List: Corrected “[CMPCR]” to “[CMPCTRLA]” in the Table, “register” to “registers”, Modified “DAC0” to “DAC channel0”. -4.2.1.: Corrected “[CMPCR]” to “[CMPCTRLA]” of Section title. |
| 1.2 | 2020-11-06 | -Modified footer design -Modified description of trademarks -3.2.Operation: Added description at Note1 -Updated “RESTRICTIONS ON PRODUCT USE” |

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