32-bit RISC Microcontroller

TMPM3H Group(2)

Reference Manual
Input/Output Ports
(PORT-M3H(2))

Revision 4.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 …
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n]
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

JTAG	Joint Test Action Group
SW	Serial Wire

1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

Function Classification	Function	Description
Port	-	Programmable pull-up /Programmable pull-down /Open-drain output are possible.
Peripheral Function pins	Clock Output	SCOUT pin
	External Interrupt	Interrupt pin has a noise filter(Filter width 30ns Typ.).
	32-bit Timer Event Counter	External trigger Input pin. Timer output pin.
	Real Time Clock	1Hz clock output pin
	Serial Peripheral Interface	Chip select input for slave operation 1 pin, Chip select 2 pins, Serial data of transmission pin, Serial data reception pin, Serial clock input/output pin
	Asynchronous Serial Communication Circuit	Data input pin, Data output 2 pins, Request to send signal pin, Clear to send signal pin.
	I^2C Interface	SCL signal pin, SDA signal pin
	Remote Control Signal preprocessor	Remote control data entry pin
	Analog to Digital Convertor	Analog input pin
	Digital to Analog Convertor	DAC output pin
	Advanced Programmable Motor Control Circuit	X/Y/Z phase output pins, U/V/W phase output pins, EMG detection input pin, OVV detection input pin
	Advanced Encoder Input Circuit	Encoder input pins
	Trigger Input	External trigger input pins
Debug pins	JTAG	JTAG Test Mode Selection pin, JTAG Serial clock input pin, JTAG Serial data output pin, JTAG Serial data input pin, JTAG Test reset input pin
	SW	Serial wire data input/output pin, Serial wire clock input pin, Serial wire viewer output pin
	Trace	Trace clock output pin, Trace data output 4pins
Control pins	High speed clock	High speed resonator connection pin, External clock input
	Low speed clock	Low speed resonator connection pin
	BOOT mode control	BOOT mode control pin

2. Function

2.1. Clock supply

When PORT is used, the corresponding clock enable bits should be set to “1” (Clock supply) in fsys supply stop register A (***[CGFSYSENA]***), fsys supply stop register B (***[CGFSYSENB]***), and fc supply stop register (***[CGFCEN]***). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to “Clock Control and Operation Mode” in Reference manual.

3. Signal connection list

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal connection list (1/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Asynchronous Serial Communication Circuit	UT0TXDA	PA1	27	23	17	19	16	14
		PA2	26	22	16	18	15	13
		PM1	35	31	24	26	19	-
		PM2	34	30	23	25	18	-
	UT0TXDB	PA0	28	24	18	20	17	15
		PM0	36	32	25	27	20	16
	UT0RXD	PA2	26	22	16	18	15	13
		PA1	27	23	17	19	16	14
		PM2	34	30	23	25	18	-
		PM1	35	31	24	26	19	-
	UT0CTS_N	PM3	33	29	22	24	-	-
		PM4	32	28	21	23	-	-
	UT0RTS_N	PM4	32	28	21	23	-	-
		PM3	33	29	22	24	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Asynchronous Serial Communication Circuit	UT1TXDA	PJ1	105	92	72	74	57	45
		PJ2	106	93	73	75	58	46
		PK1	111	98	78	80	63	51
		PK2	112	99	79	81	64	52
	UT1TXDB	PJ0	104	91	71	73	56	44
		PK0	110	97	77	79	62	50
	UT1RXD	PJ2	106	93	73	75	58	46
		PJ1	105	92	72	74	57	45
		PK2	112	99	79	81	64	52
		PK1	111	98	78	80	63	51
	UT1CTS_N	PJ3	107	94	74	76	59	47
		PJ4	108	95	75	77	60	48
		PK3	113	100	80	82	65	53
		PK4	114	101	81	83	66	54
	UT1RTS_N	PJ4	108	95	75	77	60	48
		PJ3	107	94	74	76	59	47
		PK4	114	101	81	83	66	54
		PK3	113	100	80	82	65	53

Table 3.2 Signal connection list (2/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Asynchronous Serial Communication Circuit	UT2TXDA	PB2	39	35	28	30	23	19
		PB3	40	36	29	31	24	20
		PL0	47	41	34	36	26	21
		PL1	48	42	35	37	27	22
	UT2RXD	PB3	40	36	29	31	24	20
		PB2	39	35	28	30	23	19
		PL1	48	42	35	37	27	22
		PL0	47	41	34	36	26	21
	UT2CTS_N	PB4	41	37	30	32	25	-
		PB5	42	38	31	33	-	-
		PL2	49	43	36	38	28	23
		PL3	50	44	37	39	29	24
	UT2RTS_N	PB5	42	38	31	33	-	-
		PB4	41	37	30	32	25	-
		PL3	50	44	37	39	29	24
		PL2	49	43	36	38	28	23
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Asynchronous Serial Communication Circuit	UT3TXDA	PA7	21	17	11	13	10	10
		PA6	22	18	12	14	11	11
		PG3	16	12	-	-	-	-
		PG2	15	11	-	-	-	-
	UT3TXDB	PG4	17	13	-	-	-	-
	UT3RXD	PA6	22	18	12	14	11	11
		PA7	21	17	11	13	10	10
		PG2	15	11	-	-	-	-
		PG3	16	12	-	-	-	-

Table 3.3 Signal connection list (3/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Asynchronous Serial Communication Circuit	UT4TXDA	PC3	86	73	57	59	47	38
		PC4	87	74	58	60	48	39
		PV6	81	-	-	-	-	-
		PV7	82	-	-	-	-	-
	UT4TXDB	PC2	85	72	56	58	46	-
		PV5	80	-	-	-	-	-
	UT4RXD	PC4	87	74	58	60	48	39
		PC3	86	73	57	59	47	38
		PV7	82	-	-	-	-	-
		PV6	81	-	-	-	-	-
	UT4CTS_N	PC5	88	75	59	61	49	-
		PC6	89	76	60	62	50	-
	UT4RTS_N	PC6	89	76	60	62	50	-
		PC5	88	75	59	61	49	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Asynchronous Serial Communication Circuit	UT5TXDA	PN3	100	87	67	69	52	41
		PN2	101	88	68	70	53	42
	UT5TXDB	PN4	99	86	66	68	51	40
	UT5RXD	PN2	101	88	68	70	53	42
		PN3	100	87	67	69	52	41
	UT5CTS_N	PN1	102	89	69	71	54	43
		PN0	103	90	70	72	55	-
	UT5RTS_N	PN0	103	90	70	72	55	-
		PN1	102	89	69	71	54	43
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
I^2C Interface	I2C0SCL	PC0	83	70	54	56	44	36
	I2C0SDA	PC1	84	71	55	57	45	37
	I2C1SCL	PA4	24	20	14	16	13	-
	I2C1SDA	PA5	23	19	13	15	12	-
	I2C2SCL	PL0	47	41	34	36	26	21
	I2C2SDA	PL1	48	42	35	37	27	22
	I2C3SCL	PT1	61	51	-	-	-	-
	I2C3SDA	PT0	62	52	-	-	-	-

Table 3.4 Signal connection list (4/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Serial Peripheral Interface	TSPI0SCK	PM0	36	32	25	27	20	16
		PA0	28	24	18	20	17	15
	TSPI0TXD	PM1	35	31	24	26	19	-
		PA1	27	23	17	19	16	14
	TSPI0RXD	PM2	34	30	23	25	18	-
		PA2	26	22	16	18	15	13
	TSPI0CS0	PM3	33	29	22	24	-	-
		PA3	25	21	15	17	14	12
	TSPI0CS1	PM4	32	28	21	23	-	-
		PA4	24	20	14	16	13	-
	TSPI0CSIN	PM3	33	29	22	24	-	-
		PA3	25	21	15	17	14	12
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Serial Peripheral Interface	TSPI1SCK	PB2	39	35	28	30	23	-
	TSPI1TXD	PB3	40	36	29	31	24	-
	TSPI1RXD	PB4	41	37	30	32	25	-
	TSPI1CS0	PB5	42	38	31	33	-	-
	TSPI1CS1	PB6	43	39	32	34	-	-
	TSPI1CSIN	PB5	42	38	31	33	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Serial Peripheral Interface	TSPI2SCK	PP0	63	53	41	43	31	-
		PT2	60	50	-	-	-	-
	TSPI2TXD	PP1	64	54	42	44	32	-
		PT3	59	49	-	-	-	-
	TSPI2RXD	PP2	65	55	43	45	33	-
		PT4	58	-	-	-	-	-
	TSPI2CS0	PT1	61	51	-	-	-	-
	TSPI2CS1	PT0	62	52	-	-	-	-
	TSPI2CSIN	PT1	61	51	-	-	-	-

Table 3.5 Signal connection list (5/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Serial Peripheral Interface	TSPI3SCK	PP5	120	107	87	89	72	-
	TSPI3TXD	PP4	119	106	86	88	71	-
	TSPI3RXD	PP3	118	105	85	87	70	-
	TSPI3CS0	PP6	121	108	88	90	73	-
	TSPI3CS1	PP7	122	109	89	91	-	-
	TSPI3CSIN	PP6	121	108	88	90	73	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Serial Peripheral Interface	TSPI4SCK	PH4	76	66	-	-	-	-
	TSPI4TXD	PH5	77	67	-	-	-	-
	TSPI4RXD	PH6	78	68	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
32-bit Timer Event Counter	T32A00OUTA	PA0	28	24	18	20	17	15
		PM0	36	32	25	27	20	16
	T32A00OUTB	PA3	25	21	15	17	14	12
		PM3	33	29	22	24	-	-
	T32A00OUTC	PA0	28	24	18	20	17	15
		PM0	36	32	25	27	20	16
	T32A00INA0	PA1	27	23	17	19	16	14
		PM1	35	31	24	26	19	-
	T32A00INA1	PA2	26	22	16	18	15	13
		PM2	34	30	23	25	18	-
	T32A00INB0	PA4	24	20	14	16	13	-
		PM4	32	28	21	23	-	-
	T32A00INB1	PA5	23	19	13	15	12	-
		PM5	31	27	20	22	-	-
	T32A00INC0	PA1	27	23	17	19	16	14
		PM1	35	31	24	26	19	-
	T32A00INC1	PA2	26	22	16	18	15	13
		PM2	34	30	23	25	18	-

Table 3.6 Signal connection list (6/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
32-bit Timer Event Counter	T32A01OUTA	PB0	37	33	26	28	21	17
		PP0	63	53	41	43	31	-
	T32A01OUTB	PB3	40	36	29	31	24	20
	T32A01OUTC	PB0	37	33	26	28	21	17
		PP0	63	53	41	43	31	-
	T32A01INA0	PB1	38	34	27	29	22	18
		PP1	64	54	42	44	32	-
	T32A01INA1	PB2	39	35	28	30	23	19
		PP2	65	55	43	45	33	-
	T32A01INB0	PB4	41	37	30	32	25	-
	T32A01INB1	PB5	42	38	31	33	-	-
	T32A01INC0	PB1	38	34	27	29	22	18
		PP1	64	54	42	44	32	-
	T32A01INC1	PB2	39	35	28	30	23	19
		PP2	65	55	43	45	33	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
32-bit Timer Event Counter	T32A02OUTA	PC0	83	70	54	56	44	36
		PR0	90	77	61	63	-	-
	T32A02OUTB	PC3	86	73	57	59	47	38
	T32A02OUTC	PC0	83	70	54	56	44	36
		PR0	90	77	61	63	-	-
	T32A02INA0	PC1	84	71	55	57	45	37
		PR1	91	78	62	64	-	-
	T32A02INA1	PC2	85	72	56	58	46	-
		PR2	92	79	63	65	-	-
	T32A02INB0	PC4	87	74	58	60	48	39
	T32A02INB1	PC5	88	75	59	61	49	-
	T32A02INC0	PC1	84	71	55	57	45	37
		PR1	91	78	62	64	-	-
	T32A02INC1	PC2	85	72	56	58	46	-
		PR2	92	79	63	65	-	-

Table 3.7 Signal connection list (7/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
32-bit Timer Event Counter	T32A03OUTB	PJ3	107	94	74	76	59	47
	T32A03OUTA	PJ0	104	91	71	73	56	44
	T32A03OUTC	PJ0	104	91	71	73	56	44
	T32A03INA0	PJ1	105	92	72	74	57	45
	T32A03INA1	PJ2	106	93	73	75	58	46
	T32A03INB0	PJ4	108	95	75	77	60	48
	T32A03INB1	PJ5	109	96	76	78	61	49
	T32A03INC0	PJ1	105	92	72	74	57	45
	T32A03INC1	PJ2	106	93	73	75	58	46
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
32-bit Timer Event Counter	T32A04OUTA	PK2	112	99	79	81	64	52
	T32A04INA0	PK3	113	100	80	82	65	53
	T32A04INA1	PK4	114	101	81	83	66	54
	T32A04OUTB	PK5	115	102	82	84	67	55
	T32A04INB0	PK6	116	103	83	85	68	56
	T32A04INB1	PK7	117	104	84	86	69	-
	T32A04OUTC	PK2	112	99	79	81	64	52
	T32A04INC0	PK3	113	100	80	82	65	53
	T32A04INC1	PK4	114	101	81	83	66	54
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
32-bit Timer Event Counter	T32A05OUTA	PN0	103	90	70	72	55	-
	T32A05INA0	PN1	102	89	69	71	54	43
	T32A05INA1	PN2	101	88	68	70	53	42
	T32A05OUTB	PN3	100	87	67	69	52	41
	T32A05INB0	PN4	99	86	66	68	51	40
	T32A05INB1	PN5	98	85	65	67	-	-
	T32A05OUTC	PN0	103	90	70	72	55	-
	T32A05INC0	PN1	102	89	69	71	54	43
	T32A05INC1	PN2	101	88	68	70	53	42

Table 3.8 Signal connection list (8/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
32-bit Timer Event Counter	T32A06OUTA	PL5	52	46	39	41	-	-
		PT5	57	-	-	-	-	-
	T32A06INA0	PL6	53	47	40	42	-	-
		PT6	56	-	-	-	-	-
	T32A06INA1	PL7	54	48	-	-	-	-
		PT7	55	-	-	-	-	-
	T32A06OUTB	PL2	49	43	36	38	28	23
		PT2	60	50	-	-	-	-
	T32A06INB0	PL3	50	44	37	39	29	24
		PT3	59	49	-	-	-	-
	T32A06INB1	PL4	51	45	38	40	30	25
		PT4	58	-	-	-	-	-
	T32A06OUTC	PL5	52	46	39	41	-	-
		PT5	57	-	-	-	-	-
	T32A06INC0	PL6	53	47	40	42	-	-
		PT6	56	-	-	-	-	-
	T32A06INC1	PL7	54	48	-	-	-	-
		PT7	55	-	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
32-bit Timer Event Counter	T32A07OUTA	PG2	15	11	-	-	-	-
	T32A07INA0	PG3	16	12	-	-	-	-
	T32A07INA1	PG4	17	13	-	-	-	-
	T32A07OUTB	PG5	18	14	-	-	-	-
	T32A07INB0	PG6	19	15	-	-	-	-
	T32A07INB1	PG7	20	16	-	-	-	-
	T32A07OUTC	PG2	15	11	-	-	-	-
	T32A07INC0	PG3	16	12	-	-	-	-
	T32A07INC1	PG4	17	13	-	-	-	-

Table 3.9 Signal connection list (9/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
12-bit Analog to Digital Convertor	AINA00	PD0	6	6	6	8	5	5
	AINA01	PD1	5	5	5	7	4	4
	AINA02	PD2	4	4	4	6	3	3
	AINA03	PD3	3	3	3	5	-	-
	AINA04	PE0	2	2	2	4	2	2
	AINA05	PE1	1	1	1	3	1	1
	AINA06	PE2	144	128	100	2	80	64
	AINA07	PE3	143	127	99	1	79	63
	AINA08	PE4	142	126	98	100	78	62
	AINA09	PE5	141	125	97	99	77	61
	AINA10	PE6	140	124	96	98	76	60
	AINA11	PF0	139	123	95	97	-	-
	AINA12	PF1	138	122	94	96	-	-
	AINA13	PF2	137	121	-	-	-	-
	AINA14	PF3	136	120	-	-	-	-
	AINA15	PF4	135	119	-	-	-	-
	AINA16	PF5	134	118	-	-	-	-
	AINA17	PF6	133	117	-	-	-	-
	AINA18	PF7	132	116	-	-	-	-
	AINA19	PD4	131	-	-	-	-	-
	AINA20	PD5	130	-	-	-	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
8-bit Digital to Analog Convertor	DAC0	PG0	9	9	9	11	8	8
	DAC1	PG1	10	10	10	12	9	9

Table 3.10 Signal connection list (10/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Exception	INT00	PC0	83	70	54	56	44	36
	INT01	PC1	84	71	55	57	45	37
	INT02	PC2	85	72	56	58	46	-
	INT03	PB1	38	34	27	29	22	18
	INT04	PJ4	108	95	75	77	60	48
	INT05	PK1	111	98	78	80	63	51
	INT06	PH3	74	64	52	54	42	34
	INT07	PA6	22	18	12	14	11	11
	INT08	PL3	50	44	37	39	29	24
	INT09	PM2	34	30	23	25	18	-
	INT10	PN3	100	87	67	69	52	41
	INT11	PA7	21	17	11	13	10	10
	INT12	PL4	51	45	38	40	30	25
	INT13	PK7	117	104	84	86	69	-
	INT14	PP3	118	105	85	87	70	57
	INT15	PM6	30	26	19	21	-	-
	INT16	PB7	44	40	33	35	-	-
	INT17	PV2	125	112	92	94	-	-
	INT18	PV3	126	113	93	95	-	-
	INT19	PH4	76	66	-	-	-	-
	INT20	PH5	77	67	-	-	-	-
	INT21	PH6	78	68	-	-	-	-
	INT22	PH7	79	69	-	-	-	-
	INT23	PT0	62	52	-	-	-	-
	INT24	PT1	61	51	-	-	-	-
	INT25	PT2	60	50	-	-	-	-
	INT26	PT3	59	49	-	-	-	-
	INT27	PG2	15	11	-	-	-	-
	INT28	PG3	16	12	-	-	-	-
	INT29	PT7	55	-	-	-	-	-
	INT30	PU0	45	-	-	-	-	-
	INT31	PU1	46	-	-	-	-	-

Table 3.11 Signal connection list (11/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Advanced Programmable Motor Control Circuit	UO0	PJ0	104	91	71	73	56	44
	XO0	PJ1	105	92	72	74	57	45
	VO0	PJ2	106	93	73	75	58	46
	YO0	PJ3	107	94	74	76	59	47
	WO0	PJ4	108	95	75	77	60	48
	ZO0	PJ5	109	96	76	78	61	49
	EMG0	PK0	110	97	77	79	62	50
	OVV0	PK1	111	98	78	80	63	51
	PMD0DBG	PP6	121	108	88	90	73	-
Advanced Encoder Input Circuit	ENC0A	PA0	28	24	18	20	17	15
	ENC0B	PA1	27	23	17	19	16	14
	ENC0Z	PA2	26	22	16	18	15	13
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Product Information (Trigger Selector)	TRGIN0	PB1	38	34	27	29	22	18
	TRGIN1	PA3	25	21	15	17	14	12
	TRGIN2	PN3	100	87	67	69	52	41
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Remote Control Signal preprocessor	RXIN0	PB1	38	34	27	29	22	18
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Real Time Clock	RTCOUT	PC2	85	72	56	58	46	-

Table 3.12 Signal connection list (12/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Debug Interface	TMS	PL4	51	45	38	40	30	25
	TCK	PL3	50	44	37	39	29	24
	TDO	PL2	49	43	36	38	28	23
	TDI	PL1	48	42	35	37	27	22
	TRST_N	PL0	47	41	34	36	26	21
	SWDIO	PL4	51	45	38	40	30	25
	SWCLK	PL3	50	44	37	39	29	24
	SWV	PL2	49	43	36	38	28	23
	TRACECLK	PM0	36	32	25	27	20	-
	TRACEDATA0	PM1	35	31	24	26	19	-
	TRACEDATA1	PM2	34	30	23	25	18	-
	TRACEDATA2	PM3	33	29	22	24	-	-
	TRACEDATA3	PM4	32	28	21	23	-	-
Related Reference Manual	**Function pin name**	**Port name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
Clock Control and Operation Mode	SCOUT	PB0	37	33	26	28	21	17
	X1	PH0	70	60	48	50	38	30
	X2	PH1	71	61	49	51	39	31
	XT1	PH2	73	63	51	53	41	33
	XT2	PH3	74	64	52	54	42	34
	EHCLKIN	PH0	70	60	48	50	38	30
Flash Memory	BOOT_N	PB0	37	33	26	28	21	17

Table 3.13 Signal connection list (13/13)

Related Reference Manual	Function pin name	Port name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
Input Output Port	N/A	PM7	29	25	-	-	-	-
		PR3	93	80	64	66	-	-
		PR4	94	81	-	-	-	-
		PR5	95	82	-	-	-	-
		PR6	96	83	-	-	-	-
		PR7	97	84	-	-	-	-
		PU2	14	-	-	-	-	-
		PU3	13	-	-	-	-	-
		PU4	12	-	-	-	-	-
		PU5	11	-	-	-	-	-
		PV0	123	110	90	92	74	58
		PV1	124	111	91	93	75	54
		PV4	127	-	-	-	-	-

4. Registers

The following registers should be set appropriately to use the ports.

Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

”x” and ”n” in the following table show a port name and a function number, respectively.

Register Name		Type	Setting Value	Description
[PxDATA]	Data Register	R/W	0 or 1	Read from and write to a port.
[PxCR]	Output Control Register	R/W	0: Output disabled 1: Output enabled	Output control.
[PxFRn]	Function Register n	R/W	0: PORT 1: Function	Function setting. When 1 is set, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled.
[PxOD]	Open-Drain Control Register	R/W	0: CMOS 1: Open-drain	Programmable open drain control. The programmable open-drain is a pseudo open-drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** = 1.
[PxPUP]	Pull-up Control Register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up control.
[PxPDN]	Pull-down Control Register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down control.
[PxIE]	Input Control Register	R/W	0: Input disabled 1: Input enabled	Input control. It takes 100ns(Max) that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled.

4.1. List of Register

When the bit which is assigned to no functions is read, 0 is returned. The write to the bit is ignored.

Table 4.1 Ports base address

Peripheral function		Channel/Unit	Base address
Input/output ports	PA	-	0x400C0000
	PB	-	0x400C0100
	PC	-	0x400C0200
	PD	-	0x400C0300
	PE	-	0x400C0400
	PF	-	0x400C0500
	PG	-	0x400C0600
	PH	-	0x400C0700
	PJ	-	0x400C0800
	PK	-	0x400C0900
	PL	-	0x400C0A00
	PM	-	0x400C0B00
	PN	-	0x400C0C00
	PP	-	0x400C0D00
	PR	-	0x400C0E00
	PT	-	0x400C0F00
	PU	-	0x400C1000
	PV	-	0x400C1100

Table 4.2 Register List (1/4)

Register Name	Address (Base+)	Port A	Port B	Port C	Port D	Port E
Data Register	0x0000	*[PADATA]*	*[PBDATA]*	*[PCDATA]*	*[PDDATA]*	*[PEDATA]*
Output Control Register	0x0004	*[PACR]*	*[PBCR]*	*[PCCR]*	*[PDCR]*	*[PECR]*
Function Register 1	0x0008	*[PAFR1]*	*[PBFR1]*	*[PCFR1]*	-	-
Function Register 2	0x000C	*[PAFR2]*	*[PBFR2]*	*[PCFR2]*	-	-
Function Register 3	0x0010	*[PAFR3]*	*[PBFR3]*	*[PCFR3]*	-	-
Function Register 4	0x0014	*[PAFR4]*	*[PBFR4]*	*[PCFR4]*	-	-
Function Register 5	0x0018	*[PAFR5]*	*[PBFR5]*	*[PCFR5]*	-	-
Function Register 6	0x001C	*[PAFR6]*	*[PBFR6]*	-	-	-
Open-Drain Control Register	0x0028	*[PAOD]*	*[PBOD]*	*[PCOD]*	*[PDOD]*	*[PEOD]*
Pull-up Control Register	0x002C	*[PAPUP]*	*[PBPUP]*	*[PCPUP]*	*[PDPUP]*	*[PEPUP]*
Pull-down Control Register	0x0030	*[PAPDN]*	*[PBPDN]*	*[PCPDN]*	*[PDPDN]*	*[PEPDN]*
Input Control Register	0x0038	*[PAIE]*	*[PBIE]*	*[PCIE]*	*[PDIE]*	*[PEIE]*

Note: Do not access the addresses described as "-"

Table 4.3 Register List (2/4)

Register Name	Address (Base+)	Port F	Port G	Port H	Port J	Port K
Data Register	0x0000	*[PFDATA]*	*[PGDATA]*	*[PHDATA]*	*[PJDATA]*	*[PKDATA]*
Output Control Register	0x0004	*[PFCR]*	*[PGCR]*	*[PHCR]*	*[PJCR]*	*[PKCR]*
Function Register 1	0x0008	-	*[PGFR1]*	*[PHFR1]*	*[PJFR1]*	*[PKFR1]*
Function Register 2	0x000C	-	*[PGFR2]*	-	*[PJFR2]*	*[PKFR2]*
Function Register 3	0x0010	-	*[PGFR3]*	-	*[PJFR3]*	*[PKFR3]*
Function Register 4	0x0014	-	*[PGFR4]*	-	*[PJFR4]*	*[PKFR4]*
Function Register 5	0x0018	-	-	-	*[PJFR5]*	*[PKFR5]*
Function Register 6	0x001C	-	-	-	-	-
Open-Drain Control Register	0x0028	*[PFOD]*	*[PGOD]*	*[PHOD]*	*[PJOD]*	*[PKOD]*
Pull-up Control Register	0x002C	*[PFPUP]*	*[PGPUP]*	*[PHPUP]*	*[PJPUP]*	*[PKPUP]*
Pull-down Control Register	0x0030	*[PFPDN]*	*[PGPDN]*	*[PHPDN]*	*[PJPDN]*	*[PKPDN]*
Input Control Register	0x0038	*[PFIE]*	*[PGIE]*	*[PHIE]*	*[PJIE]*	*[PKIE]*

Note: Do not access the addresses described as "-"

Table 4.4 Register List (3/4)

Register Name	Address (Base+)	Port L	Port M	Port N	Port P	Port R
Data Register	0x0000	*[PLDATA]*	*[PMDATA]*	*[PNDATA]*	*[PPDATA]*	*[PRDATA]*
Output Control Register	0x0004	*[PLCR]*	*[PMCR]*	*[PNCR]*	*[PPCR]*	*[PRCR]*
Function Register 1	0x0008	*[PLFR1]*	*[PMFR1]*	*[PNFR1]*	*[PPFR1]*	-
Function Register 2	0x000C	*[PLFR2]*	*[PMFR2]*	*[PNFR2]*	*[PPFR2]*	-
Function Register 3	0x0010	*[PLFR3]*	*[PMFR3]*	*[PNFR3]*	*[PPFR3]*	*[PRFR3]*
Function Register 4	0x0014	*[PLFR4]*	*[PMFR4]*	*[PNFR4]*	*[PPFR4]*	*[PRFR4]*
Function Register 5	0x0018	*[PLFR5]*	*[PMFR5]*	*[PNFR5]*	-	-
Function Register 6	0x001C	-	*[PMFR6]*	-	-	-
Open-Drain Control Register	0x0028	*[PLOD]*	*[PMOD]*	*[PNOD]*	*[PPOD]*	*[PROD]*
Pull-up Control Register	0x002C	*[PLPUP]*	*[PMPUP]*	*[PNPUP]*	*[PPPUP]*	*[PRPUP]*
Pull-down Control Register	0x0030	*[PLPDN]*	*[PMPDN]*	*[PNPDN]*	*[PPPDN]*	*[PRPDN]*
Input Control Register	0x0038	*[PLIE]*	*[PMIE]*	*[PNIE]*	*[PPIE]*	*[PRIE]*

Note: Do not access the addresses described as "-"

Table 4.5 Register List (4/4)

Register Name	Address (Base+)	Port T	Port U	Port V
Data Register	0x0000	*[PTDATA]*	*[PUDATA]*	*[PVDATA]*
Output Control Register	0x0004	*[PTCR]*	*[PUCR]*	*[PVCR]*
Function Register 1	0x0008	*[PTFR1]*	-	*[PVFR1]*
Function Register 2	0x000C	*[PTFR2]*	-	*[PVFR2]*
Function Register 3	0x0010	*[PTFR3]*	-	-
Function Register 4	0x0014	*[PTFR4]*	-	-
Function Register 5	0x0018	-	-	-
Function Register 6	0x001C	-	-	-
Open-Drain Control Register	0x0028	*[PTOD]*	*[PUOD]*	*[PVOD]*
Pull-up Control Register	0x002C	*[PTPUP]*	*[PUPUP]*	*[PVPUP]*
Pull-down Control Register	0x0030	*[PTPDN]*	*[PUPDN]*	*[PVPDN]*
Input Control Register	0x0038	*[PTIE]*	*[PUIE]*	*[PVIE]*

Note: Do not access the addresses described as "-"

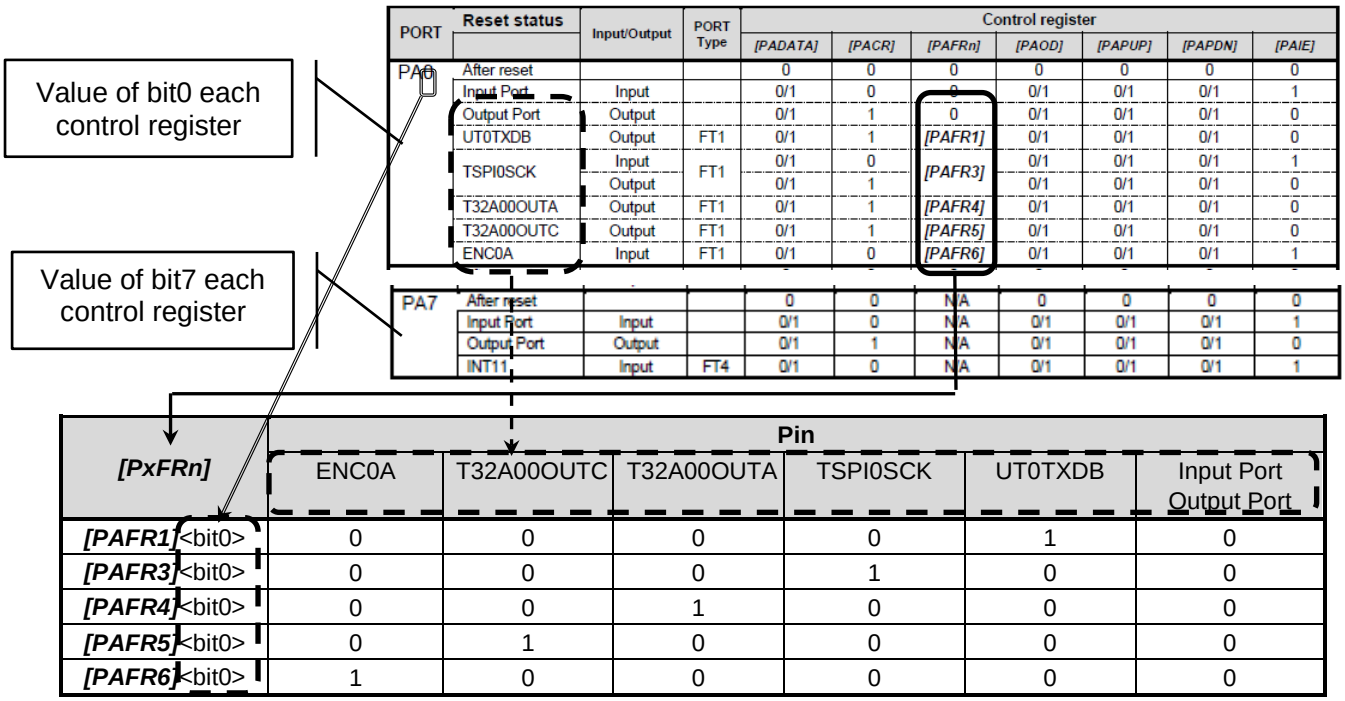
4.2. List of Port Functions and Settings

It is explained about viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the N/A in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.



PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	[PACR]	[PAFRn]	[PAOD]	[PAPUP]	[PAPDN]	[PAIE]
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDB	Output	FT1	0/1	1	[PAFR1]	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1	0/1	0	[PAFR3]	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	[PAFR4]	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	[PAFR5]	0/1	0/1	0/1	0
	ENC0A	Input	FT1	0/1	0	[PAFR6]	0/1	0/1	0/1	1
PA7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT11	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1

[PxFRn]	Pin					
	ENC0A	T32A00OUTC	T32A00OUTA	TSPI0SCK	UT0TXDB	Input Port Output Port
[PAFR1]<bit0>	0	0	0	0	1	0
[PAFR3]<bit0>	0	0	0	1	0	0
[PAFR4]<bit0>	0	0	1	0	0	0
[PAFR5]<bit0>	0	1	0	0	0	0
[PAFR6]<bit0>	1	0	0	0	0	0

4.2.1. Setting of using the alternated pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and enable output control register (***[PxCR]***<bit m>=1), then set the peripheral functions. If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), then set the peripheral functions.

To use peripheral functions such as I2C, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), then set the peripheral function.

- When multiple functions are assigned same pin, please choose only one function for usage.
- When same function are assigned multiple pins, please the function use exclusively.

4.2.2. PORT A

Table 4.6 Port A registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDB	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
	ENC0A	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FT2	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A00INA0	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	ENC0B	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A00INA1	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A00INC1	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	ENC0Z	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI0CS0	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A00OUTB	Output	FT1	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	TRGIN1	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C1SCL	I/O	FT1	0/1	1	***[PAFR1]***	1	0/1	0/1	1
	TSPI0CS1	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A00INB0	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C1SDA	I/O	FT1	0/1	1	***[PAFR1]***	1	0/1	0/1	1
	T32A00INB1	Input	FT1	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
PA6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT3RXD	Input	FT1	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FT1	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
PA7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT11	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT3TXDA	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1

4.2.3. PORT B

Table 4.7 Port B registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBPUP]*	*[PBPDN]*	*[PBIE]*
PB0	During reset (BOOT_N)	Input	FT6	0	0	0	0	1 (Note)	0	N/A (Note)
	After reset			0	0	0	0	0	0	N/A
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	N/A
	T32A01OUTA	Output	FT1	0/1	1	***[PBFR4]***	0/1	0/1	0/1	N/A
	T32A01OUTC	Output	FT1	0/1	1	***[PBFR5]***	0/1	0/1	0/1	N/A
	SCOUT	Output	FT1	0/1	1	***[PBFR6]***	0/1	0/1	0/1	N/A
PB1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	RXIN0	Input	FT1	0/1	0	***[PBFR1]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
	TRGIN0	Input	FT1	0/1	0	***[PBFR6]***	0/1	0/1	0/1	1
PB2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	TSPI1SCK	Input	FT1	0/1	0	***[PBFR3]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A01INA1	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
PB3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PBFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1	0/1	1	***[PBFR2]***	0/1	0/1	0/1	0
	TSPI1TXD	Output	FT2	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	T32A01OUTB	Output	FT1	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
PB4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PBFR1]***	0/1	0/1	0/1	1
	UT2RTS_N	Output	FT1	0/1	1	***[PBFR2]***	0/1	0/1	0/1	0
	TSPI1RXD	Input	FT1	0/1	0	***[PBFR3]***	0/1	0/1	0/1	1
	T32A01INB0	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
PB5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2RTS_N	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	TSPI1CS0	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	T32A01INB1	Input	FT1	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	TSPI1CSIN	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
PB6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS1	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
PB7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT16	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1

Note: ***[PBPUP]*** is enable during reset by the reset pin(RESET_N). ***[PBIE]*** is assigned as "N/A", but BOOT_N signal can be input.

4.2.4. PORT C

Table 4.8 Port C registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	I2C0SCL	I/O	FT1	0/1	1	***[PCFR1]***	1	0/1	0/1	1
	T32A02OUTA	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1	0/1	1	***[PCFR4]***	0/1	0/1	0/1	0
PC1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	I2C0SDA	I/O	FT1	0/1	1	***[PCFR1]***	1	0/1	0/1	1
	T32A02INA0	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FT1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
PC2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT4TXDB	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	T32A02INA1	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FT1	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
	RTCOUT	Output	FT1	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
PC3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT4TXDA	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT4RXD	Input	FT1	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	T32A02OUTB	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
PC4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT4RXD	Input	FT1	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT4TXDA	Output	FT1	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	T32A02INB0	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
PC5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT4CTS_N	Input	FT1	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT4RTS_N	Output	FT1	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	T32A02INB1	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
PC6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT4RTS_N	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT4CTS_N	Input	FT1	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1

4.2.5. PORT D

Table 4.9 Port D registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA00 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA01 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA02 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA03 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA19 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PD5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA20 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINx), ***[PDCR]*** should be output disable “0”,***[PDIE]*** should be input disable “0” , ***[PDPUP]*** should be pull-up disable”0” and ***[PDPDN]*** should be pull-down disable “0”.

4.2.6. PORT E

Table 4.10 Port E registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA04 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA05 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA06 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA07 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA08 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA09 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PE6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA10 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINx), ***[PECR]*** should be output disable “0”,***[PEIE]*** should be input disable “0”, ***[PEPUP]*** should be pull-up disable”0” and ***[PEPDN]*** should be pull-down disable “0”.

4.2.7. PORT F

Table 4.11 Port F registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA11 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA12 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA13 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA14 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA15 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA16 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA17 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PF7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA18 (Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINx), ***[PFCR]*** should be output disable “0”,***[PFIE]*** should be input disable “0” , ***[PFPUP]*** should be pull-up disable”0” and ***[PFPDN]*** should be pull-down disable “0”.

4.2.8. PORT G

Table 4.12 Port G registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	DAC0 (Note)	Output	FT13	0/1	0	N/A	0/1	0	0	0
PG1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	DAC1 (Note)	Output	FT13	0/1	0	N/A	0/1	0	0	0
PG2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT27	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT3RXD	Input	FT1	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FT1	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	T32A07OUTA	Output	FT1	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
	T32A07OUTC	Output	FT1	0/1	1	***[PGFR4]***	0/1	0/1	0/1	0
PG3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT28	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT3TXDA	Output	FT1	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FT1	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
	T32A07INA0	Input	FT1	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	T32A07INC0	Input	FT1	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
PG4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT3TXDB	Output	FT1	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	T32A07INA1	Input	FT1	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	T32A07INC1	Input	FT1	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
PG5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A07OUTB	Output	FT1	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
PG6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A07INB0	Input	FT1	0/1	0	***[PGFR3]***	0	0/1	0/1	1
PG7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A07INB1	Input	FT1	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1

Note: When using analog output(AINx), ***[PGCR]*** should be output disable “0”,***[PGIE]*** should be input disable “0” , ***[PGPUP]*** should be pull-up disable”0” and ***[PGPDN]*** should be pull-down disable “0”.

4.2.9. PORT H

Table 4.13 Port H registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PHDATA]	*[PHCR]*	*[PHFRn]*	*[PHOD]*	*[PHPUP]*	*[PHPDN]*	*[PHIE]*
PH0	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X1	Input	FT11	0/1	N/A	N/A	N/A	N/A	0	0
	EHCLKIN	Input	FT11	0/1	N/A	N/A	N/A	N/A	0	1
PH1	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X2	Output	FT11	0/1	N/A	N/A	N/A	N/A	0	0
PH2	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	XT1	Input	FT11	0/1	N/A	N/A	N/A	N/A	0	0
PH3	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	XT2	Output	FT11	0/1	N/A	N/A	N/A	N/A	0	0
	INT06	Input	FT11	0/1	N/A	N/A	N/A	N/A	0/1	1
PH4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT19	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	TSPI4SCK	Input	FT1	0/1	0	***[PHFR1]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
PH5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT20	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	TSPI4TXD	Output	FT2	0/1	1	***[PHFR1]***	0/1	0/1	0/1	0
PH6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT21	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	TSPI4RXD	Input	FT1	0/1	0	***[PHFR1]***	0/1	0/1	0/1	1
PH7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT22	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1

4.2.10. PORT J

Table 4.14 Port J registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PJDATA]	*[PJCR]*	*[PJFRn]*	*[PJOD]*	*[PJPUP]*	*[PJPDN]*	*[PJIE]*
PJ0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1TXDB	Output	FT1	0/1	1	***[PJFR1]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FT1	0/1	1	***[PJFR3]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FT1	0/1	1	***[PJFR4]***	0/1	0/1	0/1	0
	UO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1TXDA	Output	FT1	0/1	1	***[PJFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PJFR2]***	0/1	0/1	0/1	1
	T32A03INA0	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FT1	0/1	0	***[PJFR4]***	0/1	0/1	0/1	1
	XO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PJFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PJFR2]***	0/1	0/1	0/1	0
	T32A03INA1	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FT1	0/1	0	***[PJFR4]***	0/1	0/1	0/1	1
	VO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PJFR1]***	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PJFR2]***	0/1	0/1	0/1	0
	T32A03OUTB	Output	FT1	0/1	1	***[PJFR3]***	0/1	0/1	0/1	0
	YO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT04	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PJFR1]***	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PJFR2]***	0/1	0/1	0/1	1
	T32A03INB0	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	WO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ5	After reset	Input		0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03INB1	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	ZO0	Output	FT2	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0

4.2.11. PORT K

Table 4.15 Port K registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PKDATA]	*[PKCR]*	*[PKFRn]*	*[PKOD]*	*[PKPUP]*	*[PKPDN]*	*[PKIE]*
PK0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1TXDB	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	EMG0	Input	FT1	0/1	0	***[PKFR5]***	0/1	0/1	0/1	1
PK1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	OVV0	Input	FT1	0/1	0	***[PKFR5]***	0/1	0/1	0/1	1
PK2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	T32A04OUTA	Output	FT1	0/1	1	***[PKFR3]***	0/1	0/1	0/1	0
	T32A04OUTC	Output	FT1	0/1	1	***[PKFR4]***	0/1	0/1	0/1	0
PK3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	T32A04INA0	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	T32A04INC0	Input	FT1	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
PK4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1RTS_N	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A04INA1	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	T32A04INC1	Input	FT1	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
PK5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04OUTB	Output	FT1	0/1	1	***[PKFR3]***	0/1	0/1	0/1	0
PK6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04INB0	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
PK7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT13	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A04INB1	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1

4.2.12. PORT L

Table 4.16 Port L registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PLDATA]	*[PLCR]*	*[PLFRn]*	*[PLOD]*	*[PLPUP]*	*[PLPDN]*	*[PLIE]*
PL0	After reset (TRST_N)	Input	FT3	0	0	***[PLFR5]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2TXDA	Output	FT1	0/1	1	***[PLFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PLFR2]***	0/1	0/1	0/1	1
	I2C2SCL	I/O	FT1	0/1	1	***[PLFR3]***	1	0/1	0/1	1
PL1	After reset (TDI)	Input	FT1	0	0	***[PLFR5]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PLFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0
	I2C2SDA	I/O	FT1	0/1	1	***[PLFR3]***	1	0/1	0/1	1
PL2	After reset (TDO/SWV)	Output	FT2	0	1(Note)	***[PLFR5]***	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PLFR1]***	0/1	0/1	0/1	1
	UT2RTS_N	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0
	T32A06OUTB	Output	FT1	0/1	1	***[PLFR3]***	0/1	0/1	0/1	0
PL3	After reset (TCK/SWCLK)	Input	FT1	0	0	***[PLFR5]***	0	0	1	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT08	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT2RTS_N	Output	FT1	0/1	1	***[PLFR1]***	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PLFR2]***	0/1	0/1	0/1	1
	T32A06INB0	Input	FT1	0/1	0	***[PLFR3]***	0/1	0/1	0/1	1
PL4	After reset (TMS/SWDIO)	I/O	FT2	0	1(Note)	***[PLFR5]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT12	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A06INB1	Input	FT1	0/1	0	***[PLFR3]***	0/1	0/1	0/1	1
PL5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A06OUTA	Output	FT1	0/1	1	***[PLFR3]***	0/1	0/1	0/1	0
	T32A06OUTC	Output	FT1	0/1	1	***[PLFR4]***	0/1	0/1	0/1	0
PL6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A06INA0	Input	FT1	0/1	0	***[PLFR3]***	0/1	0/1	0/1	1
	T32A06INC0	Input	FT1	0/1	0	***[PLFR4]***	0/1	0/1	0/1	1
PL7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A06INA1	Input	FT1	0/1	0	***[PLFR3]***	0/1	0/1	0/1	1
	T32A06INC1	Input	FT1	0/1	0	***[PLFR4]***	0/1	0/1	0/1	1

Note: When receive the command from TOOL, it becomes output

4.2.13. PORT M

Table 4.17 Port M registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PMDATA]	*[PMCR]*	*[PMFRn]*	*[PMOD]*	*[PMPUP]*	*[PMPDN]*	*[PMIE]*
PM0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDB	Output	FT1	0/1	1	***[PMFR1]***	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1	0/1	0	***[PMFR3]***	0/1	0/1	0/1	1
		Output	FT1	0/1	1		0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	***[PMFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	***[PMFR5]***	0/1	0/1	0/1	0
	TRACECLK	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FT1	0/1	1	***[PMFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PMFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FT2	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	T32A00INA0	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TRACEDATA0	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT09	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FT1	0/1	0	***[PMFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FT1	0/1	0	***[PMFR3]***	0/1	0/1	0/1	1
	T32A00INA1	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	T32A00INC1	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TRACEDATA1	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1	0/1	0	***[PMFR1]***	0/1	0/1	0/1	1
	UT0RTS_N	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	TSPI0CS0	Output	FT1	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	T32A00OUTB	Output	FT1	0/1	1	***[PMFR4]***	0/1	0/1	0/1	0
	TSPI0CSIN	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TRACEDATA2	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RTS_N	Output	FT1	0/1	1	***[PMFR1]***	0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1	0/1	0	***[PMFR2]***	0/1	0/1	0/1	1
	TSPI0CS1	Output	FT1	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	T32A00INB0	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	TRACEDATA3	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
PM5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A00INB1	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
PM6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT15	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1
PM7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0

4.2.14. PORT N

Table 4.18 Port N registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PNDATA]	*[PNCR]*	*[PNFRn]*	*[PNOD]*	*[PNPUP]*	*[PNPDN]*	*[PNIE]*
PN0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5RTS_N	Output	FT1	0/1	1	***[PNFR1]***	0/1	0/1	0/1	0
	UT5CTS_N	Input	FT1	0/1	0	***[PNFR2]***	0/1	0/1	0/1	1
	T32A05OUTA	Output	FT1	0/1	1	***[PNFR3]***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FT1	0/1	1	***[PNFR4]***	0/1	0/1	0/1	0
PN1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5CTS_N	Input	FT1	0/1	0	***[PNFR1]***	0/1	0/1	0/1	1
	UT5RTS_N	Output	FT1	0/1	1	***[PNFR2]***	0/1	0/1	0/1	0
	T32A05INA0	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1
	T32A05INC0	Input	FT1	0/1	0	***[PNFR4]***	0/1	0/1	0/1	1
PN2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5RXD	Input	FT1	0/1	0	***[PNFR1]***	0/1	0/1	0/1	1
	UT5TXDA	Output	FT1	0/1	1	***[PNFR2]***	0/1	0/1	0/1	0
	T32A05INA1	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1
	T32A05INC1	Input	FT1	0/1	0	***[PNFR4]***	0/1	0/1	0/1	1
PN3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT10	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	UT5TXDA	Output	FT1	0/1	1	***[PNFR1]***	0/1	0/1	0/1	0
	UT5RXD	Input	FT1	0/1	0	***[PNFR2]***	0/1	0/1	0/1	1
	T32A05OUTB	Output	FT1	0/1	1	***[PNFR3]***	0/1	0/1	0/1	0
	TRGIN2	Input	FT1	0/1	0	***[PNFR5]***	0/1	0/1	0/1	1
PN4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5TXDB	Output	FT1	0/1	1	***[PNFR1]***	0/1	0/1	0/1	0
	T32A05INB0	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1
PN5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05INB1	Input	FT1	0/1	0	***[PNFR3]***	0/1	0/1	0/1	1

4.2.15. PORT P

Table 4.19 Port P registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PPDATA]	*[PPCR]*	*[PPFRn]*	*[PPOD]*	*[PPPUP]*	*[PPPDN]*	*[PPIE]*
PP0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI2SCK	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A01OUTA	Output	FT1	0/1	1	***[PPFR3]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FT1	0/1	1	***[PPFR4]***	0/1	0/1	0/1	0
PP1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI2TXD	Output	FT2	0/1	1	***[PPFR2]***	0/1	0/1	0/1	0
	T32A01INA0	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FT1	0/1	0	***[PPFR4]***	0/1	0/1	0/1	1
PP2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI2RXD	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A01INA1	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1	0/1	0	***[PPFR4]***	0/1	0/1	0/1	1
PP3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT14	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	TSPI3RXD	Input	FT1	0/1	0	***[PPFR1]***	0/1	0/1	0/1	1
PP4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI3TXD	Output	FT2	0/1	1	***[PPFR1]***	0/1	0/1	0/1	0
PP5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI3SCK	Input	FT1	0/1	0	***[PPFR1]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
PP6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI3CS0	Output	FT1	0/1	1	***[PPFR1]***	0/1	0/1	0/1	0
	TSPI3CSIN	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	PMD0DBG	Output	FT1	0/1	1	***[PPFR3]***	0/1	0/1	0/1	0
PP7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI3CS1	Output	FT1	0/1	1	***[PPFR1]***	0/1	0/1	0/1	0

4.2.16. PORT R

Table 4.20 Port R registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PRDATA]	*[PRCR]*	*[PRFRn]*	*[PROD]*	*[PRPUP]*	*[PRPDN]*	*[PRIE]*
PR0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02OUTA	Output	FT1	0/1	1	***[PRFR3]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1	0/1	1	***[PRFR4]***	0/1	0/1	0/1	0
PR1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02INA0	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FT1	0/1	0	***[PRFR4]***	0/1	0/1	0/1	1
PR2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02INA1	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FT1	0/1	0	***[PRFR4]***	0/1	0/1	0/1	1
PR3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PR4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PR5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PR6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PR7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0

4.2.17. PORT T

Table 4.21 Port T registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PTDATA]	*[PTCR]*	*[PTFRn]*	*[PTOD]*	*[PTPUP]*	*[PTPDN]*	*[PTIE]*
PT0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT23	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	I2C3SDA	I/O	FT1	0/1	1	***[PTFR1]***	1	0/1	0/1	1
	TSPI2CS1	Output	FT1	0/1	1	***[PTFR2]***	0/1	0/1	0/1	0
PT1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT24	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	I2C3SCL	I/O	FT1	0/1	1	***[PTFR1]***	1	0/1	0/1	1
	TSPI2CS0	Output	FT1	0/1	1	***[PTFR2]***	0/1	0/1	0/1	0
	TSPI2CSIN	Input	FT1	0/1	0	***[PTFR3]***	0/1	0/1	0/1	1
PT2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT25	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	TSPI2SCK	Input	FT1	0/1	0	***[PTFR1]***	0/1	0/1	0/1	1
		Output		0/1	1		0/1	0/1	0/1	0
	T32A06OUTB	Output	FT1	0/1	1	***[PTFR3]***	0/1	0/1	0/1	0
PT3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT26	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	TSPI2TXD	Output	FT2	0/1	1	***[PTFR1]***	0/1	0/1	0/1	0
	T32A06INB0	Input	FT1	0/1	0	***[PTFR3]***	0/1	0/1	0/1	1
PT4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI2RXD	Input	FT1	0/1	0	***[PTFR1]***	0/1	0/1	0/1	1
	T32A06INB1	Input	FT1	0/1	0	***[PTFR3]***	0/1	0/1	0/1	1
PT5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A06OUTA	Output	FT1	0/1	1	***[PTFR3]***	0/1	0/1	0/1	0
	T32A06OUTC	Output	FT1	0/1	1	***[PTFR4]***	0/1	0/1	0/1	0
PT6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A06INA0	Input	FT1	0/1	0	***[PTFR3]***	0/1	0/1	0/1	1
	T32A06INC0	Input	FT1	0/1	0	***[PTFR4]***	0/1	0/1	0/1	1
PT7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT29	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A06INA1	Input	FT1	0/1	0	***[PTFR3]***	0/1	0/1	0/1	1
	T32A06INC1	Input	FT1	0/1	0	***[PTFR4]***	0/1	0/1	0/1	1

4.2.18. PORT U

Table 4.22 Port U registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PUDATA]	*[PUCR]*	*[PUFRn]*	*[PUOD]*	*[PUPUP]*	*[PUPDN]*	*[PUIE]*
PU0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT30	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1
PU1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT31	Input	FT4	0/1	0	N/A	0/1	0/1	0/1	1
PU2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
PU3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
PU4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
PU5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0

4.2.19. PORT V

Table 4.23 Port V registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PVDATA]	*[PVCR]*	*[PVFRn]*	*[PVOD]*	*[PVPUP]*	*[PVPDN]*	*[PVIE]*
PV0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PV1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PV2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT17	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
PV3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT18	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
PV4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
PV5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT4TXDB	Output	FT1	0/1	1	***[PVFR1]***	0/1	0/1	0/1	0
PV6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT4TXDA	Output	FT1	0/1	1	***[PVFR1]***	0/1	0/1	0/1	0
	UT4RXD	Input	FT1	0/1	0	***[PVFR2]***	0/1	0/1	0/1	1
PV7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT4RXD	Input	FT1	0/1	0	***[PVFR1]***	0/1	0/1	0/1	1
	UT4TXDA	Output	FT1	0/1	1	***[PVFR2]***	0/1	0/1	0/1	0

5. Block Diagrams of Ports

The port has nine types of circuits, FT1 to FT6, FT11, FT13. Each circuit diagram is shown in the following page and after. The dot line block shows an equivalent circuit which is described in “Datasheet.”

The “I/O Reset” shown in the circuit diagram is described the power on reset(POR) or the reset pin(RESET_N). Although, “I/O Reset” of debug pins(TMS/SWDIO,TDI,TDO/SWV,TCK/SWCLK,TRST_N) is the power on reset(POR) only.

5.1. Type FT1

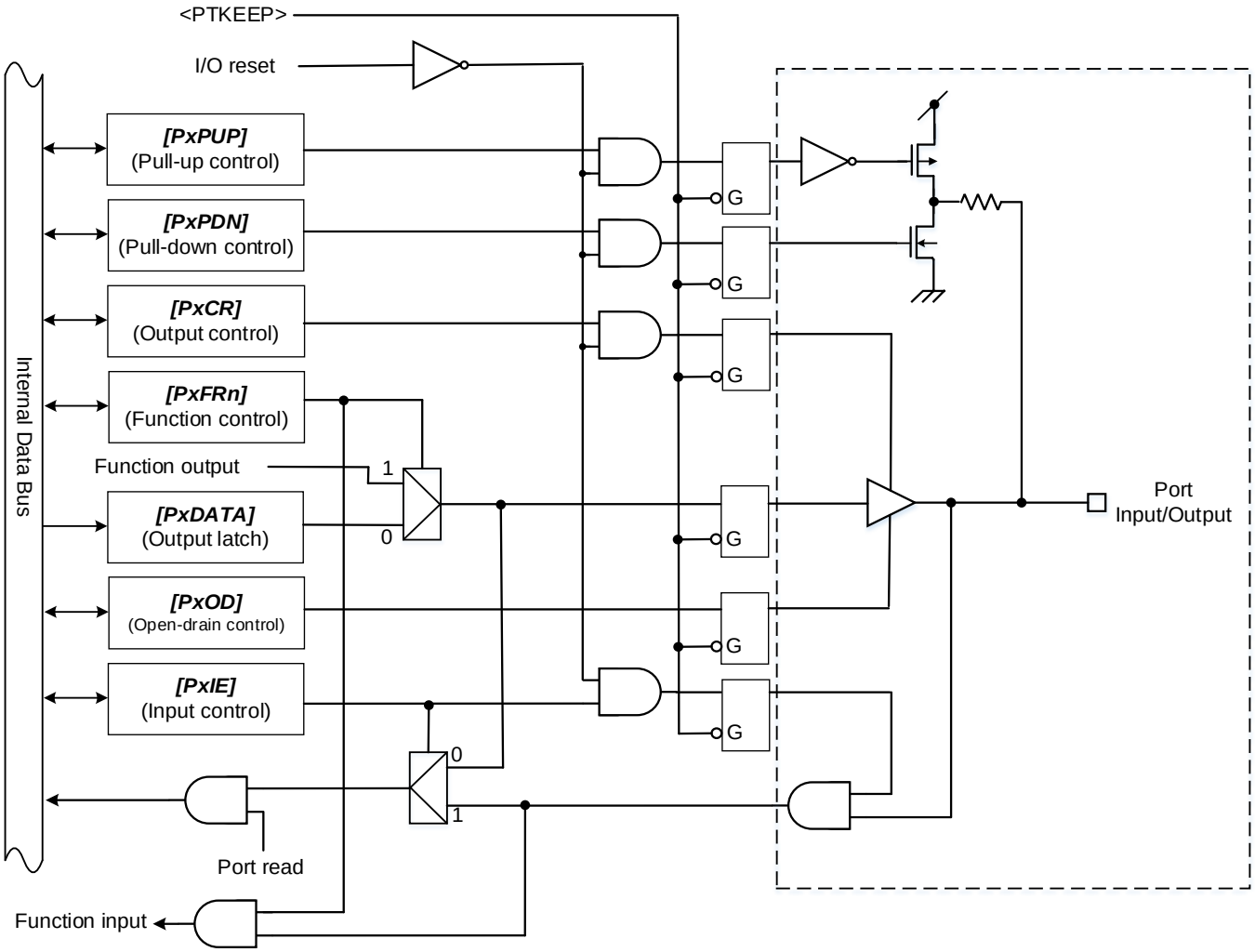


Figure 5.1 Port Type FT1

Note: ***[PxIE]*** is not available PB0 pin.

5.2. Type FT2

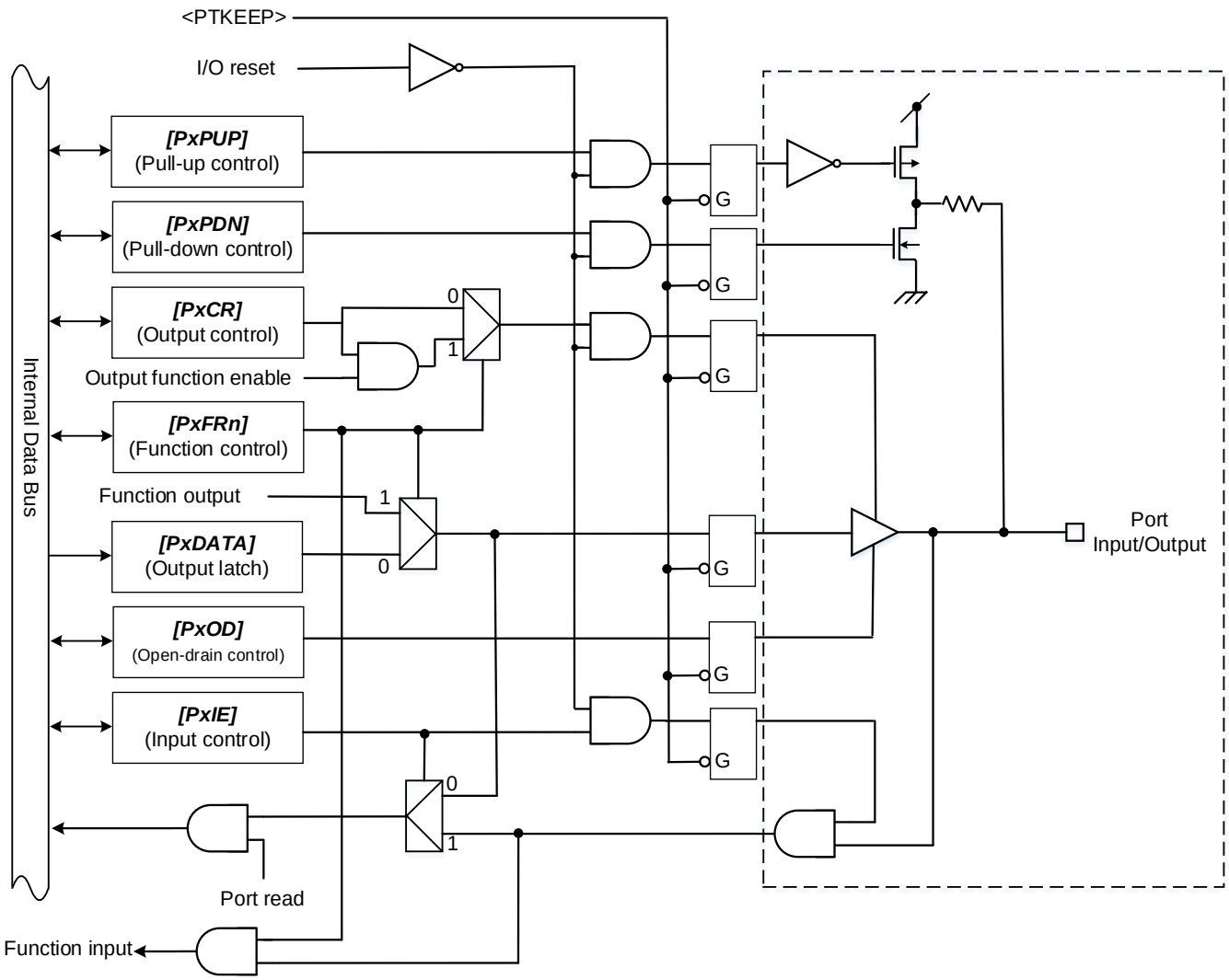


Figure 5.2 Port Type FT2

5.3. Type FT3

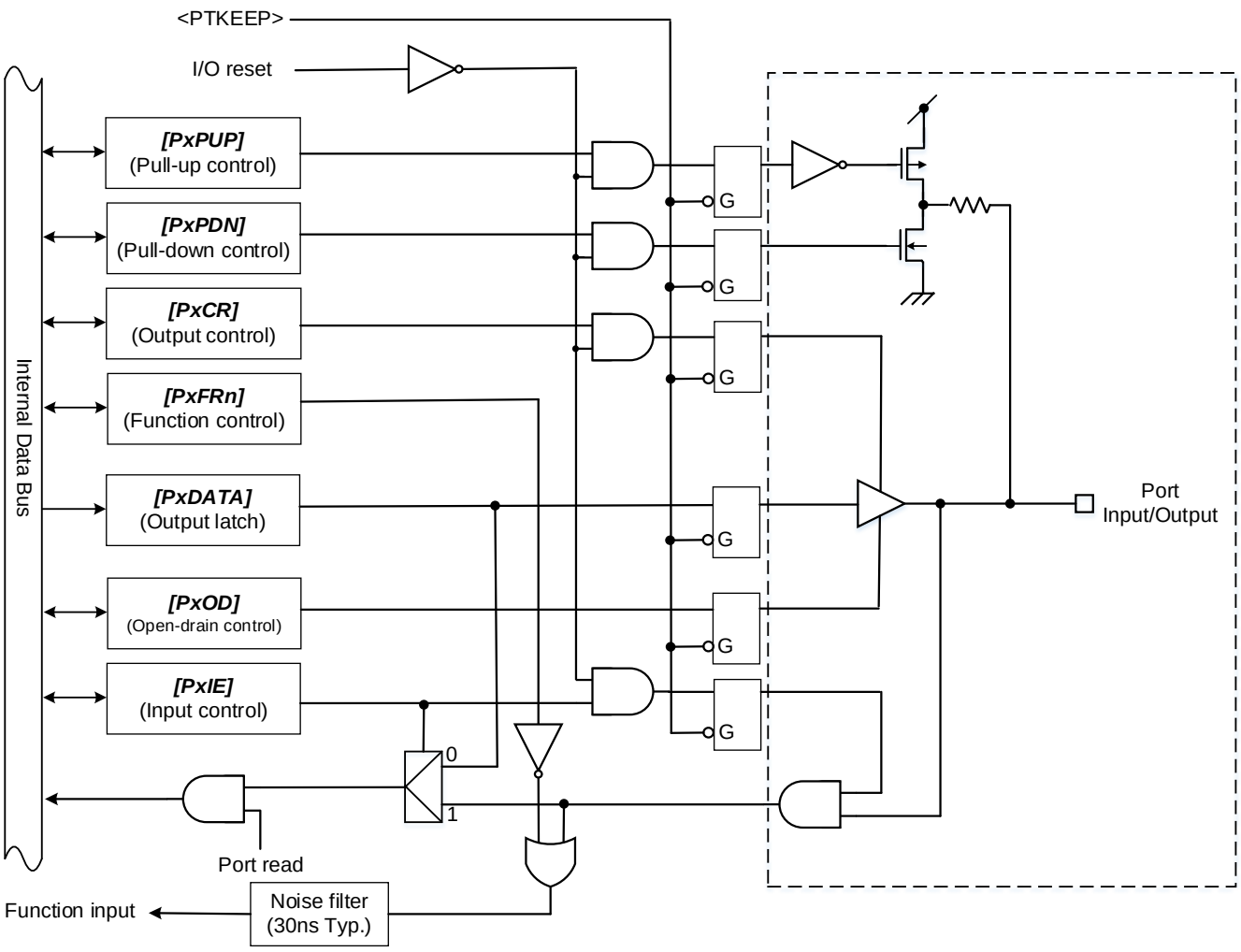


Figure 5.3 Port Type FT3

5.4. Type FT4

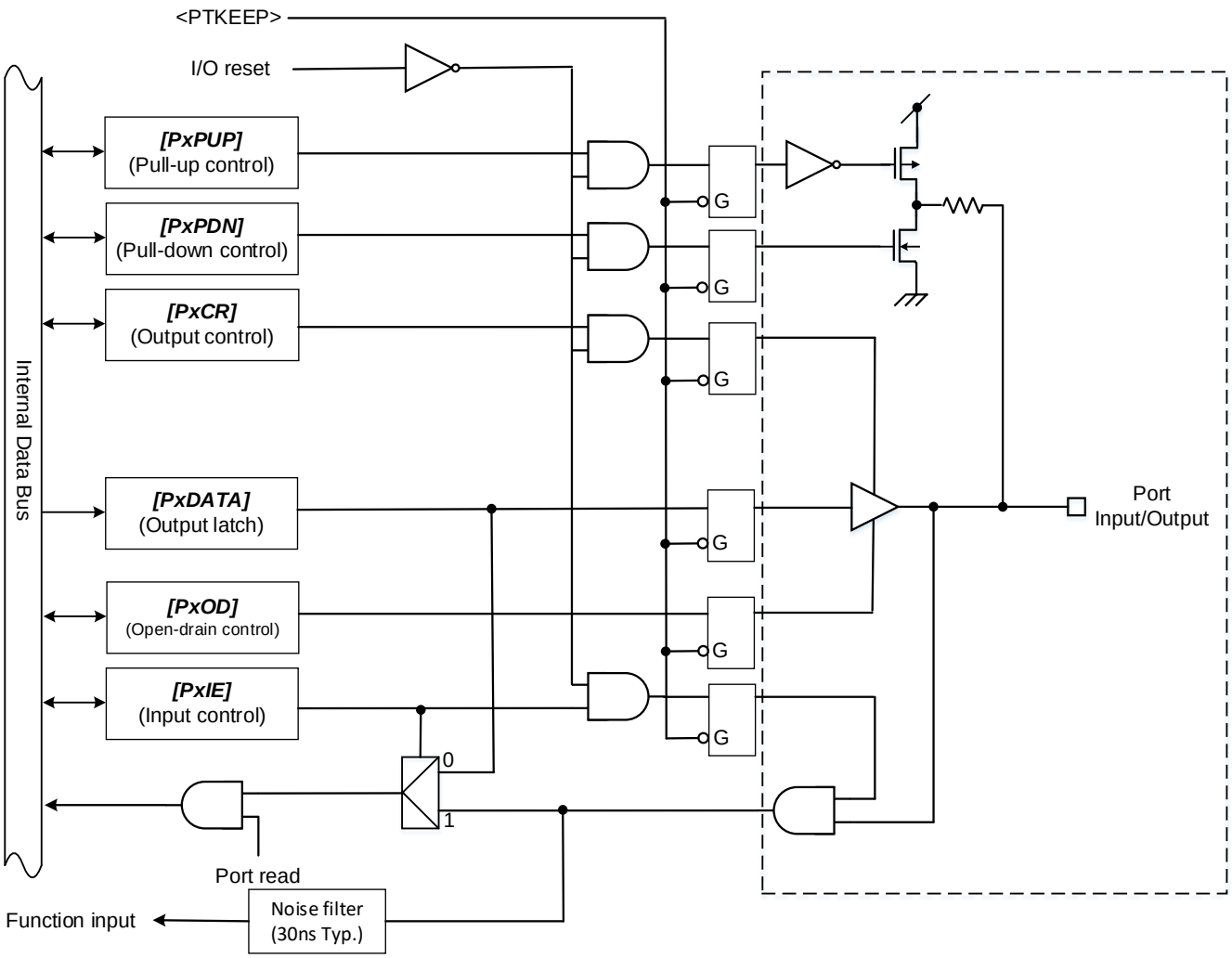


Figure 5.4 Port Type FT4

5.5. Type FT5

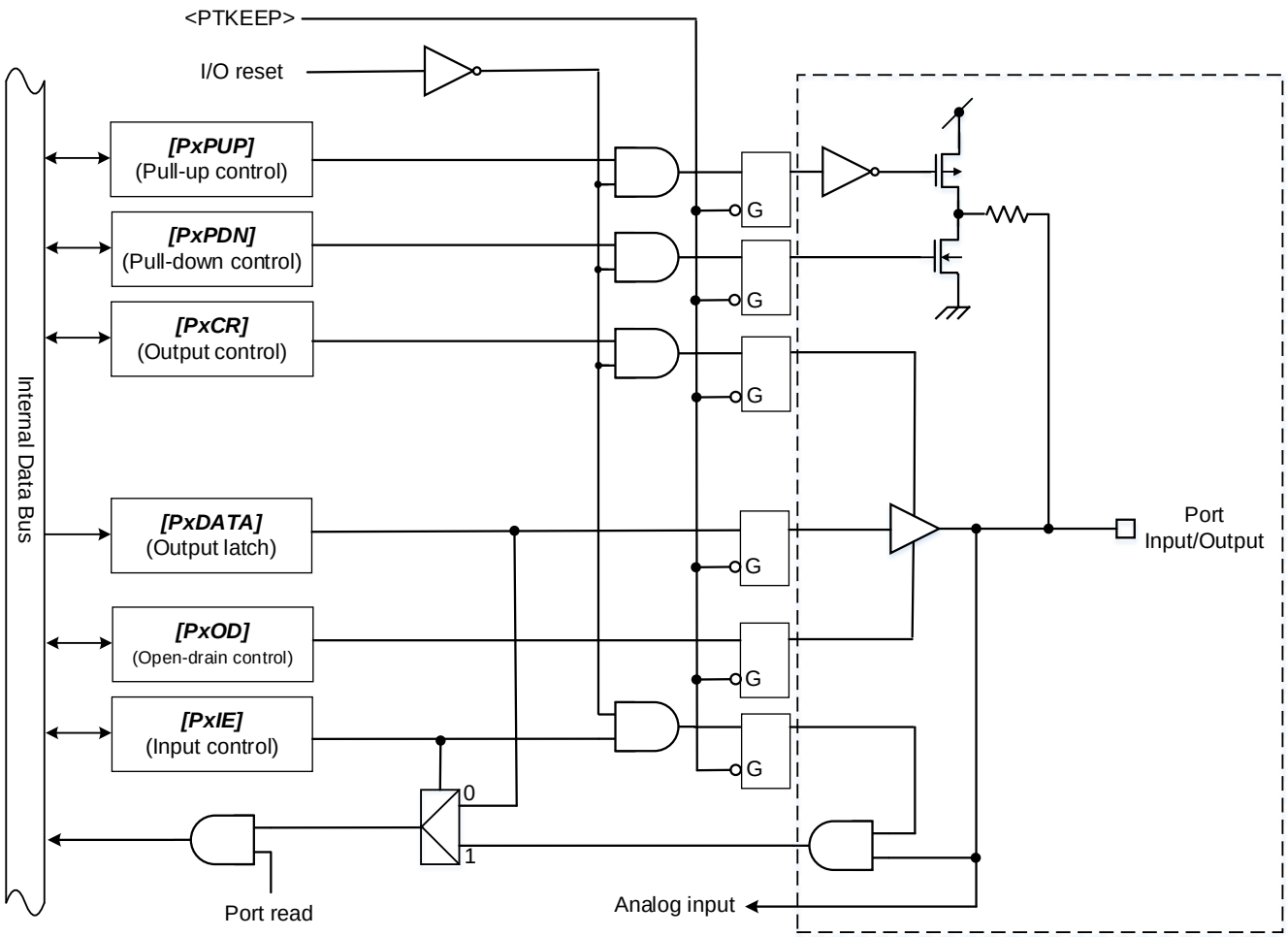


Figure 5.5 Port Type FT5

5.6. Type FT6

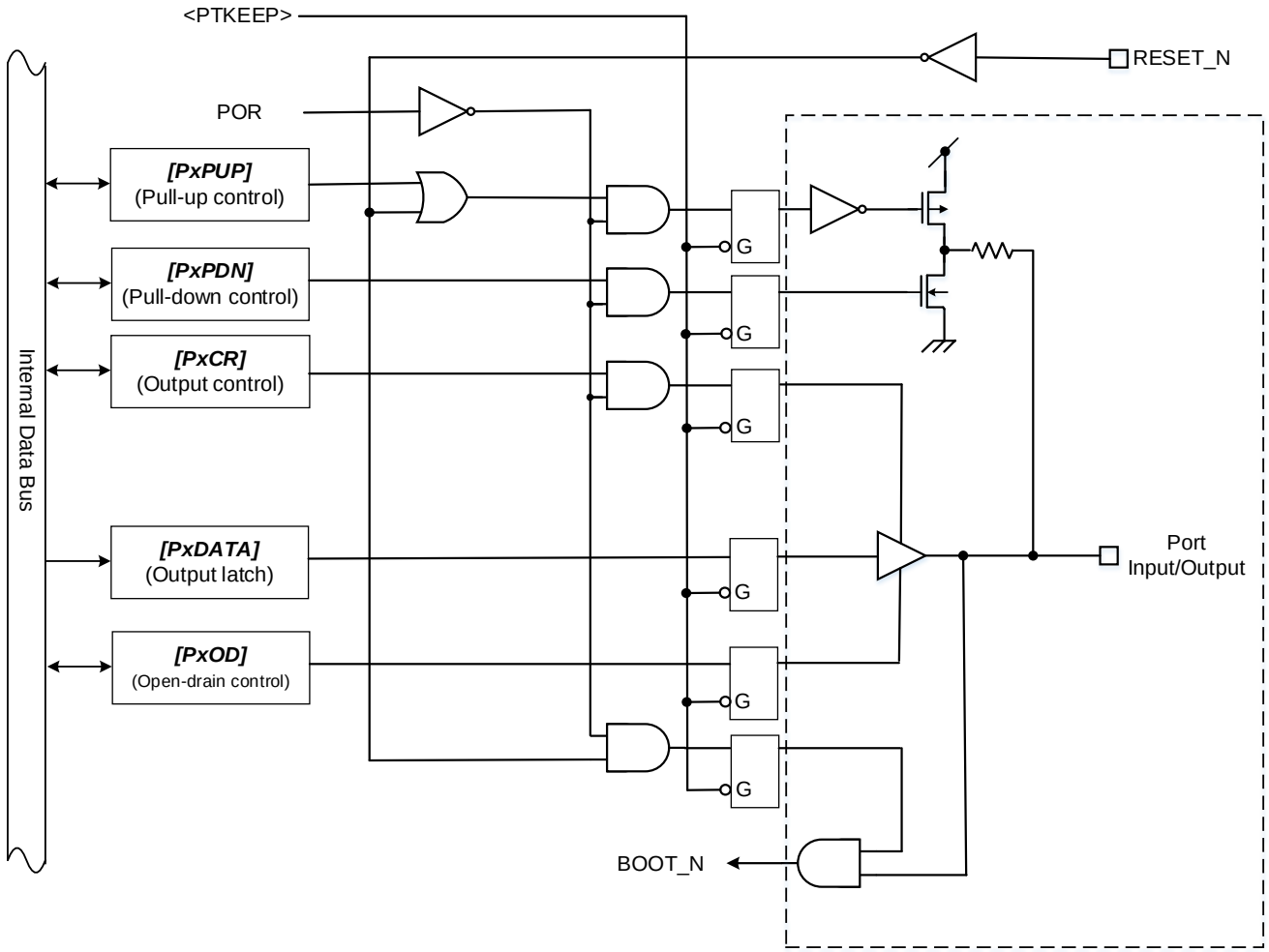


Figure 5.6 Port Type FT6

5.7. Type FT11

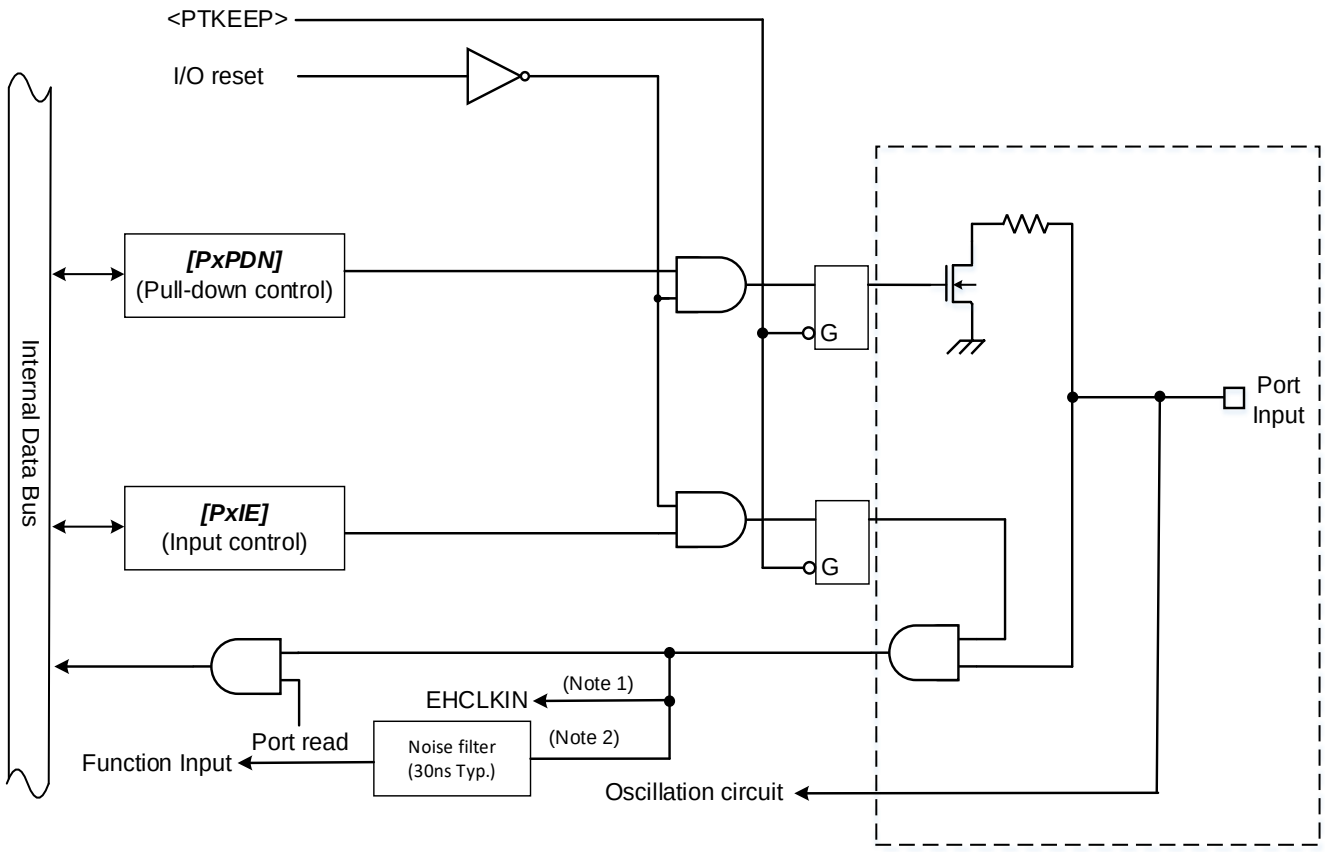


Figure 5.7 Port Type FT11

Note 1: PH0/X1/EHCLKIN pin
Note 2: PH3/XT2/INT06 pin

5.8. Type FT13

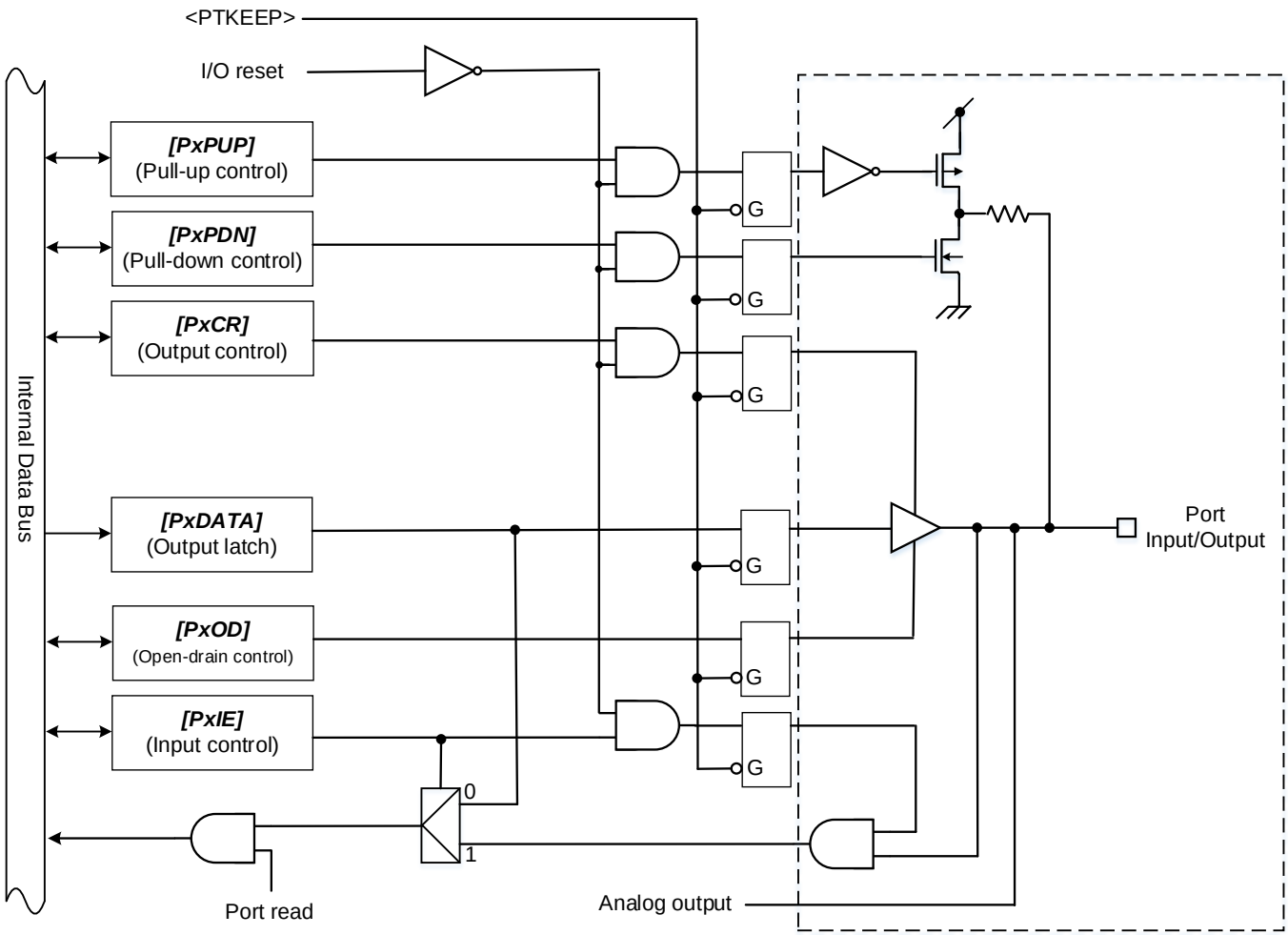


Figure 5.8 Port Type FT13

6. Precaution

6.1. pin status during a reset period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins(PL0 to PL4) are debug pin status.
- PB0(BOOT_N) works as a BOOT function. It is enabled to be input and pulled-up during pin reset period. At the rising edge of the reset signal, if PB0 is “High”, the device enters single chip mode and boots from the on chip flash memory. If PB0 is “Low”, the device enters single BOOT mode and boots from the internal BOOT ROM program.

6.2. Unused pins

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important points of using debug interface pins used as general-purpose ports

After releasing reset, If the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer reference manual of “Flash memory”.

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2018-07-31	First release
2.0	2017-11-15	-1.Outlines: Modified “Interrupt control” to “External Interrupt”, “32bit” to “32-bit”, “High speed resonator” to “High speed clock”,”Low speed resonator” to “Low speed clock”, Added “External high speed clock input” in Table1.1 -2.1.Clock supply: Deleted “***[CGFSYSMENA]***”,” ***[CGFSYSMENB]***” in description. -4.Registers: Added “Type(R/W)” and Modified “1.Open-drain” to “1.Open drain” of Setting Value, “some time” to “100ns(Max)” of description of ***[PxIE]*** in the table. -4.2.1. Setting of using the alternated pin: Modified title and description. -4.2.9. Corrected ECLKIN setting of ***[PHIE]*** “0” to “1”. -5.7. Type FT11: Corrected connection point of “EHCLKIN” in Figure5.7.
3.0	2018-06-19	-1. Outline Deleted Table title -4.2.1 Setting of using the alternated pin Modified ***[PxFR***] to ***[PxFRn]***. -4.2.2 PORT A Modified PORT Type of I2C1SCL/I2C1SDA, FT12 to FT1 -4.2.11 PORT K Modified function register of T32A04INB1, ***[PKFR2]*** to ***[PKFR3]***. -4.2.12 PORT L Modified PORT Type of I2C2SCL/I2C2SDA, FT12 to FT1 -4.2.17 PORT T Modified PORT Type of I2C3SCL/I2C3SDA, FT12 to FT1 -5.8 Type FT12 Moved noise filter location
4.0	2018-07-31	-Preface revised SST's Registered trademark -3. added the M3HL to Table 3.1. - Revised "RESTRICTIONS ON PRODUCT USE".
4.1	2019-08-01	1. Outlines Modified Function Classification: Debug pin to Debug pins, Control pin to Control pins. Corrected pin name according to the reference manual 4. Registers Modified Open Drain to Open-drain 4.2.4 PORT C Modified PORT Type of I2C0SCL/I2C0SDA, FT12 to FT1 4.2.5 PORD D Modified Note “When using analog input” to “When using analog input(AINx)” 4.2.6 PORD E Modified Note “When using analog input” to “When using analog input(AINx)” 4.2.7 PORD F Modified Note “When using analog input” to “When using analog input(AINx)” 4.2.8 PORD G Modified Note “When using analog input” to “When using analog input(AINx)” 4.2.12 PORT L Corrected Port Type of TDI,TCK/SWCLK: FT2 to FT1 5. Port Circuit Diagram Added description

		5.1 Type FT1 Added Note 5.7 Type FT11 Corrected connection of Function Input Deleted the chapter “Type FT12” 6.1 pin status during a reset period Corrected 2nd paragraph : “during reset period” to “during pin reset period”

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