32-Bit RISC Microcontroller

TMPM3H Group(2)

Reference Manual
Product Information
(PINFO-M3H(2))

Revision 3.3

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviation

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
A-PMD	Advanced Programmable Motor Control Circuit
COMP	Comparator
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DNF	Digital Noise Filter
DMAC	Direct Memory Access Controller
EHOSC	External High Speed Oscillator
ELOSC	External Low Speed Oscillator
IHOSC	Internal High Speed Oscillator
INT	Interrupt
I^2C	Inter-Integrated Circuit
I2CS	I^2C wake up circuit from Stand-by mode
LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
RAMP	RAM Parity
RMC	Remote control signal preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event counter
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

This chapter describes peripheral function related channels or number of units, information of pins and product specific functions information. Use this chapter in conjunction with Reference Manual for Peripheral Function.

2. Information of Peripheral Function

2.1. Register Base Address

The type of the register base address used by each peripheral function is shown in the following table.

Table 2.1 Register Base Address Type

Product	Register Base Address Type
TMPM3H group (2)	TYPE1

Please develop each peripheral function with reference to the above mentioned base address type.

If there is no description of “TYPE1/TYPE2/TYPE3” in the register base address of the reference manual, please use it as TYPE1.

2.2. Trigger Selector (TRGSEL)

The trigger selector is the circuit which selects the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger selected from eight triggers by ***[TSELxCRn]*** <INSELm> is outputted to the peripheral function of a connection destination.

"Figure 2.1 Example of trigger Selector Connection" is the example of the trigger signal which are port terminals (PB1, PA3, PN3) and timer register match trigger (A1, B1, C1) output from the 32-bit timer event counter (channel 6) are connected to TSPI (channel 0) via the trigger selector. The setup of input trigger selection (<INSEL39[2:0]>), edge detection condition selection (<UPDN39>), trigger output selection (<OUTSEL39>), and trigger output control (<EN39>) is performed by ***[TSEL0CR9]***.

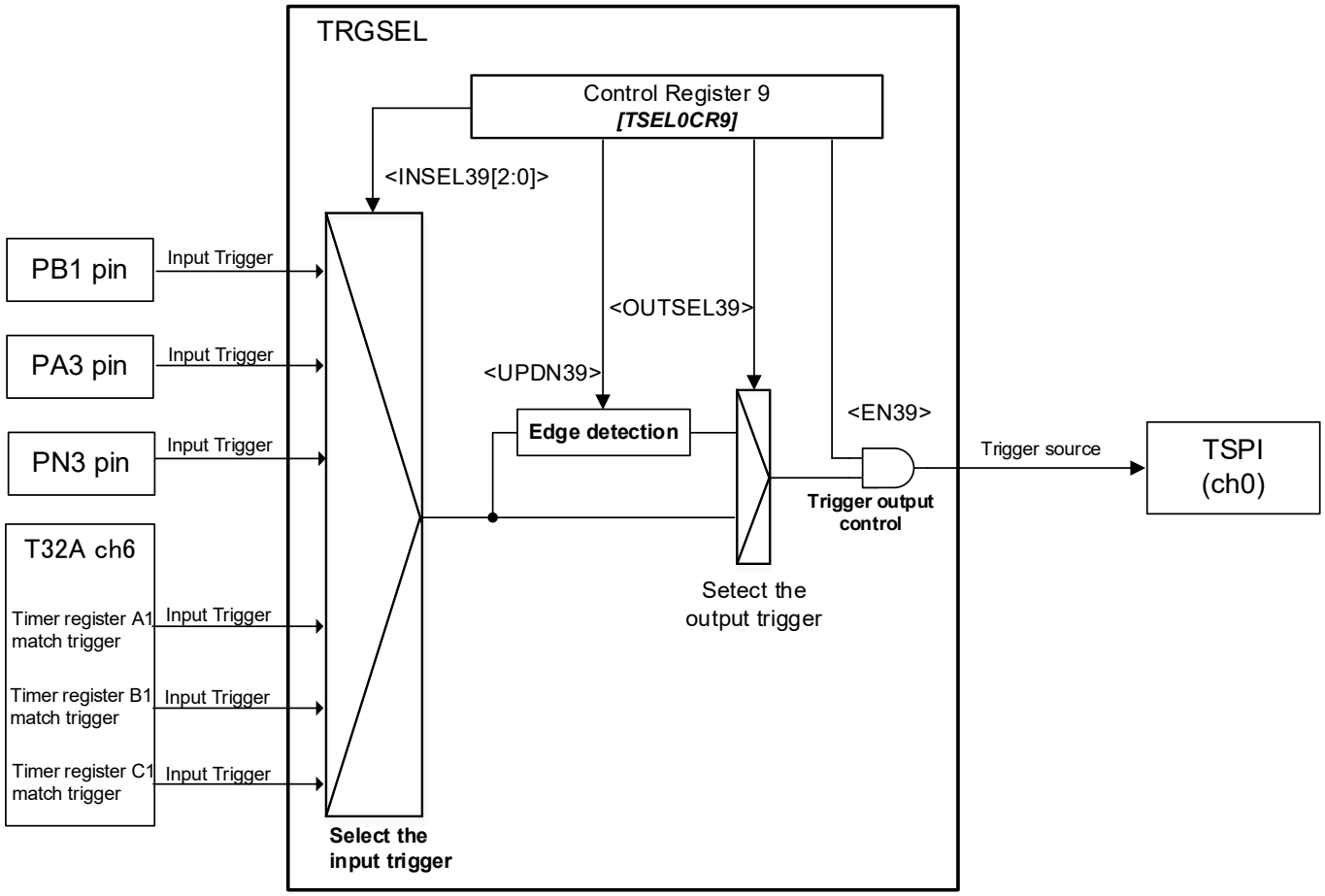

Figure 2.1 Example of trigger Selector Connection

2.2.1. Trigger selector and product table

The trigger selector of TMPM3H group (2) consists of 19 control registers (***[TSEL0CR0]*** to ***[TSEL0CR15]***, ***[TSEL1CR0]*** to ***[TSEL1CR2]***), and can control 74 triggers.

The control register, the connection destination, and correspondence products are shown in the following table.

Table 2.2 Trigger selector and product table (1/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR0]	INSEL0[2:0]	DMAC A ch15	- T32A ch0 DMA request at match A1 register - T32A ch0 DMA request at match C1 register - T32A ch1 DMA request at match A1 register - T32A ch1 DMA request at match C1 register	✓	✓	✓	✓	✓
	INSEL1[2:0]	DMAC A ch16	- T32A ch2 DMA request at match A1 register - T32A ch2 DMA request at match C1 register - T32A ch3 DMA request at match A1 register - T32A ch3 DMA request at match C1 register	✓	✓	✓	✓	✓
	INSEL2[2:0]	DMAC A ch17	- T32A ch0 DMA request at match B1 register - T32A ch1 DMA request at match B1 register	✓	✓	✓	✓	✓
	INSEL3[2:0]	DMAC A ch18	- T32A ch2 DMA request at match B1 register - T32A ch3 DMA request at match B1 register	✓	✓	✓	✓	✓
[TSEL0CR1]	INSEL4[2:0]	DMAC A ch19	- T32A ch0 DMA request at capture A0 register - T32A ch0 DMA request at capture A1 register - T32A ch1 DMA request at capture A0 register - T32A ch1 DMA request at capture A1 register - T32A ch0 DMA request at capture C0 register - T32A ch0 DMA request at capture C1 register - T32A ch1 DMA request at capture C0 register - T32A ch1 DMA request at capture C1 register	✓	✓	✓	✓	✓
	INSEL5[2:0]	DMAC A ch20	- T32A ch2 DMA request at capture A0 register - T32A ch2 DMA request at capture A1 register - T32A ch3 DMA request at capture A0 register - T32A ch3 DMA request at capture A1 register - T32A ch2 DMA request at capture C0 register - T32A ch2 DMA request at capture C1 register - T32A ch3 DMA request at capture C0 register - T32A ch3 DMA request at capture C1 register	✓	✓	✓	✓	✓
	INSEL6[2:0]	DMAC A ch21	- T32A ch0 DMA request at capture B0 register - T32A ch0 DMA request at capture B1 register - T32A ch1 DMA request at capture B0 register - T32A ch1 DMA request at capture B1 register	✓	✓	✓	✓	✓
	INSEL7[2:0]	DMAC A ch22	- T32A ch2 DMA request at capture B0 register - T32A ch2 DMA request at capture B1 register - T32A ch3 DMA request at capture B0 register - T32A ch3 DMA request at capture B1 register	✓	✓	✓	✓	✓

Table 2.3 Trigger selector and product table (2/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR2]	INSEL8[2:0]	DMAC A ch23	- DMAC A ch0 transmission end interrupt - DMAC A ch1 transmission end interrupt - DMAC A ch6 transmission end interrupt - DMAC A ch7 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL9[2:0]	DMAC A ch24	- DMAC A ch2 transmission end interrupt - DMAC A ch3 transmission end interrupt - DMAC A ch8 transmission end interrupt - DMAC A ch9 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL10[2:0]	DMAC A ch25	- DMAC A ch4 transmission end interrupt - DMAC A ch5 transmission end interrupt - DMAC A ch10 transmission end interrupt - DMAC A ch11 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL11[2:0]	DMAC A ch26	- DMAC A ch12 transmission end interrupt - DMAC A ch13 transmission end interrupt - DMAC A ch14 transmission end interrupt	✓	✓	✓	✓	✓
[TSEL0CR3]	INSEL12[2:0]	DMAC A ch27	- DMAC A ch15 transmission end interrupt - DMAC A ch19 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL13[2:0]	DMAC A ch28	- DMAC A ch16 transmission end interrupt - DMAC A ch20 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL14[2:0]	DMAC A ch29	- DMAC A ch17 transmission end interrupt - DMAC A ch21 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL15[2:0]	DMAC A ch30	- DMAC A ch18 transmission end interrupt - DMAC A ch22 transmission end interrupt	✓	✓	✓	✓	✓
[TSEL0CR4]	INSEL16[2:0]	DMAC A ch31	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2)	✓	✓	✓	✓	✓
	INSEL17[2:0]	DMAC B ch0	- TSPI ch2 Receive DMA request	✓	✓	✓	✓	-
			- I^2C ch3 Receiving DMA request	✓	✓	-	-	-
	INSEL18[2:0]	DMAC B ch1	- TSPI ch2 Transmit DMA request	✓	✓	✓	✓	-
			- I^2C ch3 Transmitting DMA request	✓	✓	-	-	-
	INSEL19[2:0]	DMAC B ch14	- ADC Unit A General purpose trigger DMA request - ADC Unit A Single conversion DMA request - ADC Unit A Continuous conversion DMA request	✓	✓	✓	✓	✓
[TSEL0CR5]	INSEL20[2:0]	DMAC B ch15	- T32A ch4 DMA request at match A1 register - T32A ch4 DMA request at match C1 register - T32A ch5 DMA request at match A1 register - T32A ch5 DMA request at match C1 register	✓	✓	✓	✓	✓
	INSEL21[2:0]	DMAC B ch16	- T32A ch6 DMA request at match A1 register - T32A ch6 DMA request at match C1 register - T32A ch7 DMA request at match A1 register - T32A ch7 DMA request at match C1 register	✓	✓	✓	✓	✓
	INSEL22[2:0]	DMAC B ch17	- T32A ch4 DMA request at match B1 register - T32A ch5 DMA request at match B1 register	✓	✓	✓	✓	✓
	INSEL23[2:0]	DMAC B ch18	- T32A ch6 DMA request at match B1 register - T32A ch7 DMA request at match B1 register	✓	✓	✓	✓	✓

Table 2.4 Trigger selector and product table (3/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR6]	INSEL24[2:0]	DMAC B ch19	- T32A ch4 DMA request at capture A0 register - T32A ch4 DMA request at capture A1 register - T32A ch5 DMA request at capture A0 register - T32A ch5 DMA request at capture A1 register - T32A ch4 DMA request at capture C0 register - T32A ch4 DMA request at capture C1 register - T32A ch5 DMA request at capture C0 register - T32A ch5 DMA request at capture C1 register	✓	✓	✓	✓	✓
	INSEL25[2:0]	DMAC B ch20	- T32A ch6 DMA request at capture A0 register - T32A ch6 DMA request at capture A1 register - T32A ch7 DMA request at capture A0 register - T32A ch7 DMA request at capture A1 register - T32A ch6 DMA request at capture C0 register - T32A ch6 DMA request at capture C1 register - T32A ch7 DMA request at capture C0 register - T32A ch7 DMA request at capture C1 register	✓	✓	✓	✓	✓
	INSEL26[2:0]	DMAC B ch21	- T32A ch4 DMA request at capture B0 register - T32A ch4 DMA request at capture B1 register - T32A ch5 DMA request at capture B0 register - T32A ch5 DMA request at capture B1 register	✓	✓	✓	✓	✓
	INSEL27[2:0]	DMAC B ch22	- T32A ch6 DMA request at capture B0 register - T32A ch6 DMA request at capture B1 register - T32A ch7 DMA request at capture B0 register - T32A ch7 DMA request at capture B1 register	✓	✓	✓	✓	✓
[TSEL0CR7]	INSEL28[2:0]	DMAC B ch23	- DMAC B ch0 transmission end interrupt - DMAC B ch1 transmission end interrupt - DMAC B ch6 transmission end interrupt - DMAC B ch7 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL29[2:0]	DMAC B ch24	- DMAC B ch2 transmission end interrupt - DMAC B ch3 transmission end interrupt - DMAC B ch8 transmission end interrupt - DMAC B ch9 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL30[2:0]	DMAC B ch25	- DMAC B ch4 transmission end interrupt - DMAC B ch5 transmission end interrupt - DMAC B ch10 transmission end interrupt - DMAC B ch11 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL31[2:0]	DMAC B ch26	- DMAC B ch12 transmission end interrupt - DMAC B ch13 transmission end interrupt - DMAC B ch14 transmission end interrupt	✓	✓	✓	✓	✓

Table 2.5 Trigger selector and product table (4/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR8]	INSEL32[2:0]	DMAC B ch27	- DMAC B ch15 transmission end interrupt - DMAC B ch19 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL33[2:0]	DMAC B ch28	- DMAC B ch16 transmission end interrupt - DMAC B ch20 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL34[2:0]	DMAC B ch29	- DMAC B ch17 transmission end interrupt - DMAC B ch21 transmission end interrupt	✓	✓	✓	✓	✓
	INSEL35[2:0]	DMAC B ch30	- DMAC B ch18 transmission end interrupt - DMAC B ch22 transmission end interrupt	✓	✓	✓	✓	✓
[TSEL0CR9]	INSEL36[2:0]	DMAC B ch31	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2)	✓	✓	✓	✓	✓
	INSEL37[2:0]	ADC (PMDTRG6)	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch7 Timer register A1 match trigger - T32A ch7 Timer register B1 match trigger - T32A ch7 Timer register C1 match trigger	✓	✓	✓	✓	✓
	INSEL38[2:0]	ADC (ADATRGIN) (General purpose trigger)	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch7 Timer register A1 match trigger - T32A ch7 Timer register B1 match trigger - T32A ch7 Timer register C1 match trigger	✓	✓	✓	✓	✓
	INSEL39[2:0]	TSPI ch0	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	✓

Table 2.6 Trigger selector and product table (5/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR10]	INSEL40[2:0]	TSPI ch1	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	-
	INSEL41[2:0]	TSPI ch2	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	-
	INSEL42[2:0]	TSPI ch3	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	-
	INSEL43[2:0]	TSPI ch4	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	-

Table 2.7 Trigger selector and product table (6/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR11]	INSEL44[2:0]	UART ch0	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	✓
	INSEL45[2:0]	UART ch1	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	✓
	INSEL46[2:0]	UART ch2	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	✓
	INSEL47[2:0]	UART ch3	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	✓

Table 2.8 Trigger selector and product table (7/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR12]	INSEL48[2:0]	UART ch4	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	✓
	INSEL49[2:0]	UART ch5	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer register B1 match trigger - T32A ch6 Timer register C1 match trigger	✓	✓	✓	✓	✓
	INSEL50[2:0]	T32A ch0 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch0 Transmission completion trigger - UART ch0 Reception completion trigger	✓	✓	✓	✓	✓
	INSEL51[2:0]	T32A ch0 Timer B	- T32A ch0 Timer register A0 match trigger - T32A ch0 Timer register A1 match trigger - T32A ch0 Timer A overflow trigger - T32A ch0 Timer A underflow trigger	✓	✓	✓	✓	✓

Table 2.9 Trigger selector and product table (8/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR13]	INSEL52[2:0]	T32A ch0 Timer C	- T32A ch7 Timer register C0 match trigger - T32A ch7 Timer register C1 match trigger - T32A ch7 Timer C overflow trigger - T32A ch7 Timer C underflow trigger	✓	✓	✓	✓	✓
	INSEL53[2:0]	T32A ch1 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch1 Transmission completion trigger - UART ch1 Reception completion trigger - I^2C ch0 interruption	✓	✓	✓	✓	✓
	INSEL54[2:0]	T32A ch1 Timer B	- T32A ch1 Timer register A0 match trigger - T32A ch1 Timer register A1 match trigger - T32A ch1 Timer A overflow trigger - T32A ch1 Timer A underflow trigger	✓	✓	✓	✓	✓
	INSEL55[2:0]	T32A ch1 Timer C	- T32A ch0 Timer register C0 match trigger - T32A ch0 Timer register C1 match trigger - T32A ch0 Timer C overflow trigger - T32A ch0 Timer C underflow trigger	✓	✓	✓	✓	✓

Table 2.10 Trigger selector and product table (9/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR14]	INSEL56[2:0]	T32A ch2 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch2 Transmission completion trigger - UART ch2 Reception completion trigger - TSPI ch0 Transmit completion signal - TSPI ch0 Receive completion signal	✓	✓	✓	✓	✓
			- I^2C ch1 interruption	✓	✓	✓	✓	–
	INSEL57[2:0]	T32A ch2 Timer B	- T32A ch2 Timer register A0 match trigger - T32A ch2 Timer register A1 match trigger - T32A ch2 Timer A overflow trigger - T32A ch2 Timer A underflow trigger	✓	✓	✓	✓	✓
	INSEL58[2:0]	T32A ch2 Timer C	- T32A ch1 Timer register C0 match trigger - T32A ch1 Timer register C1 match trigger - T32A ch1 Timer C overflow trigger - T32A ch1 Timer C underflow trigger	✓	✓	✓	✓	✓
	INSEL59[2:0]	T32A ch3 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch3 Transmission completion trigger - UART ch3 Reception completion trigger - I^2C ch2 interruption	✓	✓	✓	✓	✓
			- TSPI ch1 Transmit completion signal - TSPI ch1 Receive completion signal	✓	✓	✓	✓	–

Table 2.11 Trigger selector and product table (10/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL0CR15]	INSEL60[2:0]	T32A ch3 Timer B	- T32A ch3 Timer register A0 match trigger - T32A ch3 Timer register A1 match trigger - T32A ch3 Timer A overflow trigger - T32A ch3 Timer A underflow trigger	✓	✓	✓	✓	✓
	INSEL61[2:0]	T32A ch3 Timer C	- T32A ch2 Timer register C0 match trigger - T32A ch2 Timer register C1 match trigger - T32A ch2 Timer C overflow trigger - T32A ch2 Timer C underflow trigger	✓	✓	✓	✓	✓
	INSEL62[2:0]	T32A ch4 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch4 Transmission completion trigger - UART ch4 Reception completion trigger	✓	✓	✓	✓	✓
			- TSPI ch2 Transmit completion signal - TSPI ch2 Receive completion signal	✓	✓	✓	✓	–
			- I^2C ch3 interruption	✓	✓	–	–	–
	INSEL63[2:0]	T32A ch4 Timer B	- T32A ch4 Timer register A0 match trigger - T32A ch4 Timer register A1 match trigger - T32A ch4 Timer A overflow trigger - T32A ch4 Timer A underflow trigger	✓	✓	✓	✓	✓

Table 2.12 Trigger selector and product table (11/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL1CR0]	INSEL0[2:0]	T32A ch4 Timer C	- T32A ch3 Timer register C0 match trigger - T32A ch3 Timer register C1 match trigger - T32A ch3 Timer C overflow trigger - T32A ch3 Timer C underflow trigger	✓	✓	✓	✓	✓
	INSEL1[2:0]	T32A ch5 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - UART ch5 Transmission completion trigger - UART ch5 Reception completion trigger - A-ENC ch0 Dividing pulse signal	✓	✓	✓	✓	✓
			- TSPI ch3 Transmit completion signal - TSPI ch3 Receive completion signal	✓	✓	✓	✓	–
	INSEL2[2:0]	T32A ch5 Timer B	- T32A ch5 Timer register A0 match trigger - T32A ch5 Timer register A1 match trigger - T32A ch5 Timer A overflow trigger - T32A ch5 Timer A underflow trigger	✓	✓	✓	✓	✓
	INSEL3[2:0]	T32A ch5 Timer C	- T32A ch4 Timer register C0 match trigger - T32A ch4 Timer register C1 match trigger - T32A ch4 Timer C overflow trigger - T32A ch4 Timer C underflow trigger	✓	✓	✓	✓	✓

Table 2.13 Trigger selector and product table (12/12)

Register	Bit Symbol	Trigger Source	Input Trigger	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
[TSEL1CR1]	INSEL4[2:0]	T32A ch6 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2)	✓	✓	✓	✓	✓
			- TSPI ch4 Transmit completion signal - TSPI ch4 Receive completion signal	✓	✓	–	–	–
			- ELOSC Low speed clock	✓	✓	✓	✓	✓
	INSEL5[2:0]	T32A ch6 Timer B	- T32A ch6 Timer register A0 match trigger - T32A ch6 Timer register A1 match trigger - T32A ch6 Timer A overflow trigger - T32A ch6 Timer A underflow trigger	✓	✓	✓	✓	✓
	INSEL6[2:0]	T32A ch6 Timer C	- T32A ch5 Timer register C0 match trigger - T32A ch5 Timer register C1 match trigger - T32A ch5 Timer C overflow trigger - T32A ch5 Timer C underflow trigger	✓	✓	✓	✓	✓
	INSEL7[2:0]	T32A ch7 Timer A	- PB1 pin (TRGIN0) - PA3 pin (TRGIN1) - PN3 pin (TRGIN2) - ADC unit A General purpose trigger interrupt - ADC unit A Single conversion interrupt - ADC unit A Continuous conversion interrupt - ADC unit A Monitor function interrupt 0 - ADC unit A Monitor function interrupt 1	✓	✓	✓	✓	✓
[TSEL1CR2]	INSEL8[2:0]	T32A ch7 Timer B	- T32A ch7 Timer register A0 match trigger - T32A ch7 Timer register A1 match trigger - T32A ch7 Timer A overflow trigger - T32A ch7 Timer A underflow trigger	✓	✓	✓	✓	✓
	INSEL9[2:0]	T32A ch7 Timer C	- T32A ch6 Timer register C0 match trigger - T32A ch6 Timer register C1 match trigger - T32A ch6 Timer C overflow trigger - T32A ch6 Timer C underflow trigger	✓	✓	✓	✓	✓

2.2.2. Directions for use and setup

When you use TRGSEL, please set as "1"(clock supply) the clock enabling bit (***[CGFSYSENA]***, ***[CGFSYSENB]***, and ***[CGFCEN]*** registers) to which CG corresponds. Please refer to "Clock Control and Operational Mode" of the reference manual for details.

Please perform a setup of a trigger selector in following order.

(1) Selection of an input trigger (***[TSELxCRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger subdevice bit (***[TSELxCRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSELxCRn]*** <UPDNm>)

For the input trigger signal which needs edge detection, selection of rising edge or falling edge detection is performed.

Please set up selection of edge detection conditions in the selection bit ***([TSELxCRn]***<UPDNm>) of a control register.

The following shows the trigger signal which needs edge detection. For other trigger signals, do not set to enable edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)
- ELOSC Low speed clock (fs)

(3) Selection of a trigger output (***[TSELxCRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSELxCRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSELxCRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is selected.

Please set up selection of output (enable/disable) in the setting bit (***[TSELxCRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSELxCRn]***<ENm> is set to "1".

2.2.3. List of Registers

The table below shows control registers and their addresses.

Peripheral function		Channel/Unit	Base address
Trigger selector	TRGSEL	ch0	0x400BB800
		ch1	0x400BB900

Register name		Address(Base+)
Control Register0	***[TSELxCR0]***	0x0000
Control Register1	***[TSELxCR1]***	0x0004
Control Register2	***[TSELxCR2]***	0x0008
Control Register3	***[TSELxCR3]***	0x000C
Control Register4	***[TSELxCR4]***	0x0010
Control Register5	***[TSELxCR5]***	0x0014
Control Register6	***[TSELxCR6]***	0x0018
Control Register7	***[TSELxCR7]***	0x001C
Control Register8	***[TSELxCR8]***	0x0020
Control Register9	***[TSELxCR9]***	0x0024
Control Register10	***[TSELxCR10]***	0x0028
Control Register11	***[TSELxCR11]***	0x002C
Control Register12	***[TSELxCR12]***	0x0030
Control Register13	***[TSELxCR13]***	0x0034
Control Register14	***[TSELxCR14]***	0x0038
Control Register15	***[TSELxCR15]***	0x003C

2.2.4. Detail of Registers

The following chapters show the details of a register.

The sign in the functional column parenthesis of each table expresses each function signal name.

2.2.4.1. *[TSEL0CR0]* (Control Register 0)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL3[2:0]	000	R/W	Selection of an input trigger (DMAC A ch18) 000: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 001: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN3	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL3	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN3	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL2[2:0]	000	R/W	Selection of an input trigger (DMAC A ch17) 000: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 001: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN2	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL2	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
16	EN2	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
15	-	0	R	Read as “0”

Bit	Bit Symbol	After Reset	Type	Function
14:12	INSEL1[2:0]	000	R/W	Selection of an input trigger (DMAC A ch16) 000: T32A ch2 DMA request at match A1 register (T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register (T32A02DMAREQCMPC1) 010: T32A ch3 DMA request at match A1 register (T32A03DMAREQCMPA1) 011: T32A ch3 DMA request at match C1 register (T32A03DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN1	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL1	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN1	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL0[2:0]	000	R/W	Selection of an input trigger (DMAC A ch15) 000: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 001: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 010: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 011: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN0	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL0	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN0	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.2. *[TSEL0CR1]* (Control Register 1)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL7[2:0]	000	R/W	Selection of an input trigger (DMAC A ch22) 000: T32A ch2 DMA request at capture B0 register (T32A02DMAREQCAPB0) 001: T32A ch2 DMA request at capture B1 register (T32A02DMAREQCAPB1) 010: T32A ch3 DMA request at capture B0 register (T32A03DMAREQCAPB0) 011: T32A ch3 DMA request at capture B1 register (T32A03DMAREQCAPB1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN7	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL7	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN7	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL6[2:0]	000	R/W	Selection of an input trigger (DMAC A ch21) 000: T32A ch0 DMA request at capture B0 register (T32A00DMAREQCAPB0) 001: T32A ch0 DMA request at capture B1 register (T32A00DMAREQCAPB1) 010: T32A ch1 DMA request at capture B0 register (T32A01DMAREQCAPB0) 011: T32A ch1 DMA request at capture B1 register (T32A01DMAREQCAPB1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN6	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL6	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN6	0	R/W	Setup of trigger output control 0: Disable 1: Enable
15	-	0	R	Read as “0”

Bit	Bit Symbol	After Reset	Type	Function
14:12	INSEL5[2:0]	000	R/W	Selection of an input trigger (DMAC A ch20) 000: T32A ch2 DMA request at capture A0 register (T32A02DMAREQCAPA0) 001: T32A ch2 DMA request at capture A1 register (T32A02DMAREQCAPA1) 010: T32A ch3 DMA request at capture A0 register (T32A03DMAREQCAPA0) 011: T32A ch3 DMA request at capture A1 register (T32A03DMAREQCAPA1) 100: T32A ch2 DMA request at capture C0 register (T32A02DMAREQCAPC0) 101: T32A ch2 DMA request at capture C1 register (T32A02DMAREQCAPC1) 110: T32A ch3 DMA request at capture C0 register (T32A03DMAREQCAPC0) 111: T32A ch3 DMA request at capture C1 register (T32A03DMAREQCAPC1)
11	-	0	R	Read as “0”
10	UPDN5	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL5	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN5	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL4[2:0]	000	R/W	Selection of an input trigger (DMAC A ch19) 000: T32A ch0 DMA request at capture A0 register (T32A00DMAREQCAPA0) 001: T32A ch0 DMA request at capture A1 register (T32A00DMAREQCAPA1) 010: T32A ch1 DMA request at capture A0 register (T32A01DMAREQCAPA0) 011: T32A ch1 DMA request at capture A1 register (T32A01DMAREQCAPA1) 100: T32A ch0 DMA request at capture C0 register (T32A00DMAREQCAPC0) 101: T32A ch0 DMA request at capture C1 register (T32A00DMAREQCAPC1) 110: T32A ch1 DMA request at capture C0 register (T32A01DMAREQCAPC0) 111: T32A ch1 DMA request at capture C1 register (T32A01DMAREQCAPC1)
3	-	0	R	Read as “0”
2	UPDN4	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL4	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN4	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.3. *[TSEL0CR2]* (Control Register 2)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL11[2:0]	000	R/W	Selection of an input trigger (DMAC A ch26) 000: DMAC A ch12 transmission end interrupt (INTDMAATC12) 001: DMAC A ch13 transmission end interrupt (INTDMAATC13) 010: DMAC A ch14 transmission end interrupt (INTDMAATC14) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN11	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL11	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN11	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL10[2:0]	000	R/W	Selection of an input trigger (DMAC A ch25) 000: DMAC A ch4 transmission end interrupt (INTDMAATC4) 001: DMAC A ch5 transmission end interrupt (INTDMAATC5) 010: DMAC A ch10 transmission end interrupt (INTDMAATC10) 011: DMAC A ch11 transmission end interrupt (INTDMAATC11) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN10	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL10	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN10	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL9[2:0]	000	R/W	Selection of an input trigger (DMAC A ch24) 000: DMAC A ch2 transmission end interrupt (INTDMAATC2) 001: DMAC A ch3 transmission end interrupt (INTDMAATC3) 010: DMAC A ch8 transmission end interrupt (INTDMAATC8) 011: DMAC A ch9 transmission end interrupt (INTDMAATC9) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN9	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL9	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN9	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL8[2:0]	000	R/W	Selection of an input trigger (DMAC A ch23) 000: DMAC A ch0 transmission end interrupt (INTDMAATC0) 001: DMAC A ch1 transmission end interrupt (INTDMAATC1) 010: DMAC A ch6 transmission end interrupt (INTDMAATC6) 011: DMAC A ch7 transmission end interrupt (INTDMAATC7) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN8	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL8	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN8	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.4. *[TSEL0CR3]* (Control Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL15[2:0]	000	R/W	Selection of an input trigger (DMAC A ch30) 000: DMAC A ch18 transmission end interrupt (INTDMAATC18) 001: DMAC A ch22 transmission end interrupt (INTDMAATC22) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN15	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL15	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN15	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL14[2:0]	000	R/W	Selection of an input trigger (DMAC A ch29) 000: DMAC A ch17 transmission end interrupt (INTDMAATC17) 001: DMAC A ch21 transmission end interrupt (INTDMAATC21) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN14	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL14	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN14	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL13[2:0]	000	R/W	Selection of an input trigger (DMAC A ch28) 000: DMAC A ch16 transmission end interrupt (INTDMAATC16) 001: DMAC A ch20 transmission end interrupt (INTDMAATC20) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN13	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL13	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN13	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL12[2:0]	000	R/W	Selection of an input trigger (DMAC A ch27) 000: DMAC A ch15 transmission end interrupt (INTDMAATC15) 001: DMAC A ch19 transmission end interrupt (INTDMAATC19) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN12	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL12	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN12	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.5. *[TSEL0CR4]* (Control Register 4)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL19[2:0]	000	R/W	Selection of an input trigger (DMAC B ch14) 000: ADC unit A General purpose trigger DMA request (ADATRG_DMAREQ) 001: ADC unit A Single conversion DMA request (ADASGL_DMAREQ) 010: ADC unit A Continuous conversion DMA request (ADACNT_DMAREQ) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN19	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL19	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN19	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL18[2:0]	000	R/W	Selection of an input trigger (DMAC B ch1) 000: TSPI ch2 Transmit DMA request (TSPI2TX_DMA) 001: I^2C ch3 Transmitting DMA request (I2C3TXDMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN18	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL18	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN18	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL17[2:0]	000	R/W	Selection of an input trigger (DMAC B ch0) 000: TSPI ch2 Receive DMA request (TSPI2RX_DMA) 001: I^2C ch3 Receiving DMA request (I2C3RXDMAREQ) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN17	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL17	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN17	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL16[2:0]	000	R/W	Selection of an input trigger (DMAC A ch31) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved When <INSEL16[2:0]> is set to “000”(PB1 pin), “001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL16> to “1”.
3	-	0	R	Read as “0”
2	UPDN16	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL16	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN16	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.6. *[TSEL0CR5]* (Control Register 5)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL23[2:0]	000	R/W	Selection of an input trigger (DMAC B ch18) 000: T32A ch6 DMA request at match B1 register (T32A06DMAREQCMPB1) 001: T32A ch7 DMA request at match B1 register (T32A07DMAREQCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN23	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL23	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN23	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL22[2:0]	000	R/W	Selection of an input trigger (DMAC B ch17) 000: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 001: T32A ch5 DMA request at match B1 register (T32A05DMAREQCMPB1) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN22	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL22	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN22	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL21[2:0]	000	R/W	Selection of an input trigger (DMAC B ch16) 000: T32A ch6 DMA request at match A1 register (T32A06DMAREQCMPA1) 001: T32A ch6 DMA request at match C1 register (T32A06DMAREQCMPC1) 010: T32A ch7 DMA request at match A1 register (T32A07DMAREQCMPA1) 011: T32A ch7 DMA request at match C1 register (T32A07DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN21	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL21	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN21	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL20[2:0]	000	R/W	Selection of an input trigger (DMAC B ch15) 000: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 001: T32A ch4 DMA request at match C1 register (T32A04DMAREQCMPC1) 010: T32A ch5 DMA request at match A1 register (T32A05DMAREQCMPA1) 011: T32A ch5 DMA request at match C1 register (T32A05DMAREQCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN20	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL20	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN20	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.7. *[TSEL0CR6]* (Control Register 6)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL27[2:0]	000	R/W	Selection of an input trigger (DMAC B ch22) 000: T32A ch6 DMA request at capture B0 register (T32A06DMAREQCAPB0) 001: T32A ch6 DMA request at capture B1 register (T32A06DMAREQCAPB1) 010: T32A ch7 DMA request at capture B0 register (T32A07DMAREQCAPB0) 011: T32A ch7 DMA request at capture B1 register (T32A07DMAREQCAPB1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN27	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL27	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN27	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL26[2:0]	000	R/W	Selection of an input trigger (DMAC B ch21) 000: T32A ch4 DMA request at capture B0 register (T32A04DMAREQCAPB0) 001: T32A ch4 DMA request at capture B1 register (T32A04DMAREQCAPB1) 010: T32A ch5 DMA request at capture B0 register (T32A05DMAREQCAPB0) 011: T32A ch5 DMA request at capture B1 register (T32A05DMAREQCAPB1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN26	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL26	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN26	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL25[2:0]	000	R/W	Selection of an input trigger (DMAC B ch20) 000: T32A ch6 DMA request at capture A0 register (T32A06DMAREQCAPA0) 001: T32A ch6 DMA request at capture A1 register (T32A06DMAREQCAPA1) 010: T32A ch7 DMA request at capture A0 register (T32A07DMAREQCAPA0) 011: T32A ch7 DMA request at capture A1 register (T32A07DMAREQCAPA1) 100: T32A ch6 DMA request at capture C0 register (T32A06DMAREQCAPC0) 101: T32A ch6 DMA request at capture C1 register (T32A06DMAREQCAPC1) 110: T32A ch7 DMA request at capture C0 register (T32A07DMAREQCAPC0) 111: T32A ch7 DMA request at capture C1 register (T32A07DMAREQCAPC1)
11	-	0	R	Read as “0”
10	UPDN25	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL25	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN25	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL24[2:0]	000	R/W	Selection of an input trigger (DMAC B ch19) 000: T32A ch4 DMA request at capture A0 register (T32A04DMAREQCAPA0) 001: T32A ch4 DMA request at capture A1 register (T32A04DMAREQCAPA1) 010: T32A ch5 DMA request at capture A0 register (T32A05DMAREQCAPA0) 011: T32A ch5 DMA request at capture A1 register (T32A05DMAREQCAPA1) 100: T32A ch4 DMA request at capture C0 register (T32A04DMAREQCAPC0) 101: T32A ch4 DMA request at capture C1 register (T32A04DMAREQCAPC1) 110: T32A ch5 DMA request at capture C0 register (T32A05DMAREQCAPC0) 111: T32A ch5 DMA request at capture C1 register (T32A05DMAREQCAPC1)
3	-	0	R	Read as “0”
2	UPDN24	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL24	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN24	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.8. *[TSEL0CR7]* (Control Register 7)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL31[2:0]	000	R/W	Selection of an input trigger (DMAC B ch26) 000: DMAC B ch12 transmission end interrupt (INTDMABTC12) 001: DMAC B ch13 transmission end interrupt (INTDMABTC13) 010: DMAC B ch14 transmission end interrupt (INTDMABTC14) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN31	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL31	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN31	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL30[2:0]	000	R/W	Selection of an input trigger (DMAC B ch25) 000: DMAC B ch4 transmission end interrupt (INTDMABTC4) 001: DMAC B ch5 transmission end interrupt (INTDMABTC5) 010: DMAC B ch10 transmission end interrupt (INTDMABTC10) 011: DMAC B ch11 transmission end interrupt (INTDMABTC11) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN30	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL30	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN30	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL29[2:0]	000	R/W	Selection of an input trigger (DMAC B ch24) 000: DMAC B ch2 transmission end interrupt (INTDMABTC2) 001: DMAC B ch3 transmission end interrupt (INTDMABTC3) 010: DMAC B ch8 transmission end interrupt (INTDMABTC8) 011: DMAC B ch9 transmission end interrupt (INTDMABTC9) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN29	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL29	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN29	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL28[2:0]	000	R/W	Selection of an input trigger (DMAC B ch23) 000: DMAC B ch0 transmission end interrupt (INTDMABTC0) 001: DMAC B ch1 transmission end interrupt (INTDMABTC1) 010: DMAC B ch6 transmission end interrupt (INTDMABTC6) 011: DMAC B ch7 transmission end interrupt (INTDMABTC7) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN28	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL28	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN28	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.9. *[TSEL0CR8]* (Control Register 8)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL35[2:0]	000	R/W	Selection of an input trigger (DMAC B ch30) 000: DMAC B ch18 transmission end interrupt (INTDMABTC18) 001: DMAC B ch22 transmission end interrupt (INTDMABTC22) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN35	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL35	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN35	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL34[2:0]	000	R/W	Selection of an input trigger (DMAC B ch29) 000: DMAC B ch17 transmission end interrupt (INTDMABTC17) 001: DMAC B ch21 transmission end interrupt (INTDMABTC21) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN34	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL34	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN34	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL33[2:0]	000	R/W	Selection of an input trigger (DMAC B ch28) 000: DMAC B ch16 transmission end interrupt (INTDMABTC16) 001: DMAC B ch20 transmission end interrupt (INTDMABTC20) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN33	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL33	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN33	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL32[2:0]	000	R/W	Selection of an input trigger (DMAC B ch27) 000: DMAC B ch15 transmission end interrupt (INTDMABTC15) 001: DMAC B ch19 transmission end interrupt (INTDMABTC19) 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN32	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL32	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN32	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.10. *[TSEL0CR9]* (Control Register 9)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL39[2:0]	000	R/W	Selection of an input trigger (TSPI ch0) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL39[2:0]> is set to “000”(PB1 pin), “001“(PA3 pin) or “010”(PN3 pin), set <OUTSEL39> to “1”.
27	-	0	R	Read as “0”
26	UPDN39	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL39	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN39	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL38[2:0]	000	R/W	Selection of an input trigger (ADC general purpose trigger) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch7 Timer register A1 match trigger (T32A07TRGOUTCMPA1) 100: T32A ch7 Timer register B1 match trigger (T32A07TRGOUTCMPB1) 101: T32A ch7 Timer register C1 match trigger (T32A07TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL38[2:0]> is set to “000”(PB1 pin), “001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL38> to “1”.
19	-	0	R	Read as “0”
18	UPDN38	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL38	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN38	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL37[2:0]	000	R/W	Selection of an input trigger (PMDTRG6 of ADC) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch7 Timer register A1 match trigger (T32A07TRGOUTCMPA1) 100: T32A ch7 Timer register B1 match trigger (T32A07TRGOUTCMPB1) 101: T32A ch7 Timer register C1 match trigger (T32A07TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL37[2:0]> is set to “000”(PB1 pin), “001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL37> to “1”.
11	-	0	R	Read as “0”
10	UPDN37	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL37	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN37	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL36[2:0]	000	R/W	Selection of an input trigger (DMAC B ch31) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved When <INSEL36[2:0]> is set to “000”(PB1 pin), “001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL36> to “1”.
3	-	0	R	Read as “0”
2	UPDN36	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL36	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN36	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.11. *[TSEL0CR10]* (Control Register 10)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL43[2:0]	000	R/W	Selection of an input trigger (TSPI ch4) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL43[2:0]> is set to “000”(PB1 pin), “001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL43> to “1”.
27	-	0	R	Read as “0”
26	UPDN43	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL43	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN43	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL42[2:0]	000	R/W	Selection of an input trigger (TSPI ch3) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL42[2:0]> is set to” 000”(PB1 pin), “001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL42> to “1”.
19	-	0	R	Read as “0”
18	UPDN42	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL42	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN42	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL41[2:0]	000	R/W	Selection of an input trigger (TSPI ch2) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL41[2:0]> is set to “000”(PB1 pin),” 001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL41> to “1”.
11	-	0	R	Read as “0”
10	UPDN41	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL41	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN41	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL40[2:0]	000	R/W	Selection of an input trigger (TSPI ch1) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL40[2:0]> is set to “000”(PB1 pin),” 001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL40> to “1”.
3	-	0	R	Read as “0”
2	UPDN40	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL40	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN40	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.12. *[TSEL0CR11]* (Control Register 11)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL47[2:0]	000	R/W	Selection of an input trigger (UART ch3) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL47[2:0]> is set to “000”(PB1 pin),” 001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL47> to “1”.
27	-	0	R	Read as “0”
26	UPDN47	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL47	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN47	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL46[2:0]	000	R/W	Selection of an input trigger (UART ch2) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL46[2:0]> is set to “000”(PB1 pin),” 001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL46> to "1".
19	-	0	R	Read as “0”
18	UPDN46	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL46	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN46	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL45[2:0]	000	R/W	Selection of an input trigger (UART ch1) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL45[2:0]> is set to “000”(PB1 pin), “001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL45> to “1".
11	-	0	R	Read as “0”
10	UPDN45	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL45	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN45	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL44[2:0]	000	R/W	Selection of an input trigger (UART ch0) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL44[2:0]> is set to “000”(PB1 pin),” 001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL44> to “1".
3	-	0	R	Read as “0”
2	UPDN44	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL44	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN44	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.13. *[TSEL0CR12]* (Control Register 12)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL51[2:0]	000	R/W	Selection of an input trigger (T32A ch0 Timer B) 000: T32A ch0 Timer register A0 match trigger (T32A00TRGOUTCMPA0) 001: T32A ch0 Timer register A1 match trigger (T32A00TRGOUTCMPA1) 010: T32A ch0 Timer A overflow trigger (T32A00TRGOUTOFA) 011: T32A ch0 Timer A underflow trigger (T32A00TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN51	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL51	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN51	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL50[2:0]	000	R/W	Selection of an input trigger (T32A ch0 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: UART ch0 Transmission completion trigger (UART0TXTRG) 100: UART ch0 Reception completion trigger (UART0RXTRG) 101: Reserved 110: Reserved 111: Reserved When <INSEL50[2:0]> is set to “000”(PB1 pin) ,” 001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL50> to “1".
19	-	0	R	Read as “0”
18	UPDN50	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL50	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN50	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL49[2:0]	000	R/W	Selection of an input trigger (UART ch5) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL49[2:0]> is set to “000”(PB1 pin),”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL49> to “1".
11	-	0	R	Read as “0”
10	UPDN49	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL49	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN49	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL48[2:0]	000	R/W	Selection of an input trigger (UART ch4) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 100: T32A ch6 Timer register B1 match trigger (T32A06TRGOUTCMPB1) 101: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 110: Reserved 111: Reserved When <INSEL48[2:0]> is set to “000”(PB1 pin),”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL48> to “1".
3	-	0	R	Read as “0”
2	UPDN48	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL48	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN48	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.14. *[TSEL0CR13]* (Control Register 13)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL55[2:0]	000	R/W	Selection of an input trigger (T32A ch1 Timer C) 000: T32A ch0 Timer register C0 match trigger (T32A00TRGOUTCMPC0) 001: T32A ch0 Timer register C1 match trigger (T32A00TRGOUTCMPC1) 010: T32A ch0 Timer C overflow trigger (T32A00TRGOUTOFC) 011: T32A ch0 Timer C underflow trigger (T32A00TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN55	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL55	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN55	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL54[2:0]	000	R/W	Selection of an input trigger (T32A ch1 Timer B) 000: T32A ch1 Timer register A0 match trigger (T32A01TRGOUTCMPA0) 001: T32A ch1 Timer register A1 match trigger (T32A01TRGOUTCMPA1) 010: T32A ch1 Timer A overflow trigger (T32A01TRGOUTOFA) 011: T32A ch1 Timer A underflow trigger (T32A01TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN54	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL54	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN504	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL53[2:0]	000	R/W	Selection of an input trigger (T32A ch1 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: UART ch1 Transmission completion trigger (UART1TXTRG) 100: UART ch1 Reception completion trigger (UART1RXTRG) 101: I^2C ch0 interrupt (INTI2C0) 110: Reserved 111: Reserved When <INSEL53[2:0]> is set to “000”(PB1 pin),”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL53> to “1".
11	-	0	R	Read as “0”
10	UPDN53	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL53	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN53	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL52[2:0]	000	R/W	Selection of an input trigger (T32A ch0 Timer C) 000: T32A ch7 Timer register C0 match trigger (T32A07TRGOUTCMPC0) 001: T32A ch7 Timer register C1 match trigger (T32A07TRGOUTCMPC1) 010: T32A ch7 Timer C overflow trigger (T32A07TRGOUTOFC) 011: T32A ch7 Timer C underflow trigger (T32A07TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN52	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL52	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN52	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.15. *[TSEL0CR14]* (Control Register 14)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL59[2:0]	000	R/W	Selection of an input trigger (T32A ch3 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: UART ch3 Transmission completion trigger (UART3TXTRG) 100: UART ch3 Reception completion trigger (UART3RXTRG) 101: TSPI ch1 transmission completion signal (TSPI1TXEND) 110: TSPI ch1 reception completion signal (TSPI1RXEND) 111: I^2C ch2 interrupt (INTI2C2) When <INSEL59[2:0]> is set to “000”(PB1 pin),”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL59> to “1“.
27	-	0	R	Read as “0”
26	UPDN59	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL59	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN59	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL58[2:0]	000	R/W	Selection of an input trigger (T32A ch2 Timer C) 000: T32A ch1 Timer register C0 match trigger (T32A01TRGOUTCMPC0) 001: T32A ch1 Timer register C1 match trigger (T32A01TRGOUTCMPC1) 010: T32A ch1 Timer C overflow trigger (T32A01TRGOUTOFC) 011: T32A ch1 Timer C underflow trigger (T32A01TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN58	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL58	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN58	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL57[2:0]	000	R/W	Selection of an input trigger (T32A ch2 Timer B) 000: T32A ch2 Timer register A0 match trigger (T32A02TRGOUTCMPA0) 001: T32A ch2 Timer register A1 match trigger (T32A02TRGOUTCMPA1) 010: T32A ch2 Timer A overflow trigger (T32A02TRGOUTOFA) 011: T32A ch2 Timer A underflow trigger (T32A02TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN57	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL57	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN57	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL56[2:0]	000	R/W	Selection of an input trigger (T32A ch2 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: UART ch2 Transmission completion trigger (UART2TXTRG) 100: UART ch2 Reception completion trigger (UART2RXTRG) 101: TSPI ch0 transmission completion signal (TSPI0TXEND) 110: TSPI ch0 reception completion signal (TSPI0RXEND) 111: I^2C ch1 interrupt (INTI2C1)(Note) When <INSEL56[2:0]> is set to “000”(PB1 pin),”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL56> to “1".
3	-	0	R	Read as “0”
2	UPDN56	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL56	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN56	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Note: There is no I^2C channel 1 in M3HL

2.2.4.16. *[TSEL0CR15]* (Control Register 15)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL63[2:0]	000	R/W	Selection of an input trigger (T32A ch4 Timer B) 000: T32A ch4 Timer register A0 match trigger (T32A04TRGOUTCMPA0) 001: T32A ch4 Timer register A1 match trigger (T32A04TRGOUTCMPA1) 010: T32A ch4 Timer A overflow trigger (T32A04TRGOUTOFA) 011: T32A ch4 Timer A underflow trigger (T32A04TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN63	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL63	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN63	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL62[2:0]	000	R/W	Selection of an input trigger (T32A ch4 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: UART ch4 Transmission completion trigger (UART4TXTRG) 100: UART ch4 Reception completion trigger (UART4RXTRG) 101: TSPI ch2 transmission completion signal (TSPI2TXEND) 110: TSPI ch2 reception completion signal (TSPI2RXEND) 111: I^2C ch3 interrupt (INTI2C3)(Note) When <INSEL62[2:0]> is set to “000”(PB1 pin),”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL62> to “1".
19	-	0	R	Read as “0”
18	UPDN62	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL62	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN62	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Note: There is no I^2C channel 3 in M3HN / M3HM / M3HL.

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL61[2:0]	000	R/W	Selection of an input trigger (T32A ch3 Timer C) 000: T32A ch2 Timer register C0 match trigger (T32A02TRGOUTCMPC0) 001: T32A ch2 Timer register C1 match trigger (T32A02TRGOUTCMPC1) 010: T32A ch2 Timer C overflow trigger (T32A02TRGOUTOFC) 011: T32A ch2 Timer C underflow trigger (T32A02TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN61	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL61	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN61	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL60[2:0]	000	R/W	Selection of an input trigger (T32A ch3 Timer B) 000: T32A ch3 Timer register A0 match trigger (T32A03TRGOUTCMPA0) 001: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 010: T32A ch3 Timer A overflow trigger (T32A03TRGOUTOFA) 011: T32A ch3 Timer A underflow trigger (T32A03TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN60	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL60	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN60	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.17. *[TSEL1CR0]* (Control Register 0)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL3[2:0]	000	R/W	Selection of an input trigger (T32A ch5 Timer C) 000: T32A ch4 Timer register C0 match trigger (T32A04TRGOUTCMPC0) 001: T32A ch4 Timer register C1 match trigger (T32A04TRGOUTCMPC1) 010: T32A ch4 Timer C overflow trigger (T32A04TRGOUTOFC) 011: T32A ch4 Timer C underflow trigger (T32A04TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	-	0	R	Read as “0”
26	UPDN3	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL3	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN3	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL2[2:0]	000	R/W	Selection of an input trigger (T32A ch5 Timer B) 000: T32A ch5 Timer register A0 match trigger (T32A05TRGOUTCMPA0) 001: T32A ch5 Timer register A1 match trigger (T32A05TRGOUTCMPA1) 010: T32A ch5 Timer A overflow trigger (T32A05TRGOUTOFA) 011: T32A ch5 Timer A underflow trigger (T32A05TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN2	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL2	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN2	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL1[2:0]	000	R/W	Selection of an input trigger (T32A ch5 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: UART ch5 Transmission completion trigger (UART5TXTRG) 100: UART ch5 Reception completion trigger (UART5RXTRG) 101: TSPI ch3 transmission completion signal (TSPI3TXEND) 110: TSPI ch3 reception completion signal (TSPI3RXEND) 111: A-ENC ch0 Dividing pulse signal (ENC0TIMPLS) When <INSEL1[2:0]> is set to “000”(PB1 pin),”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL1> to “1".
11	-	0	R	Read as “0”
10	UPDN1	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL1	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN1	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL0[2:0]	000	R/W	Selection of an input trigger (T32A ch4 Timer C) 000: T32A ch3 Timer register C0 match trigger (T32A03TRGOUTCMPC0) 001: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 010: T32A ch3 Timer C overflow trigger (T32A03TRGOUTOFC) 011: T32A ch3 Timer C underflow trigger (T32A03TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN0	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL0	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN0	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.2.4.18. *[TSEL1CR1]* (Control Register 1)

Bit	Bit Symbol	After Reset	Type	Function
31	-	0	R	Read as “0”
30:28	INSEL7[2:0] (INSEL71[2:0])	000	R/W	Selection of an input trigger (T32A ch7 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: ADC unit A General purpose trigger interrupt (INTADATRG) 100: ADC unit A Single conversion interrupt (INTADASG) 101: ADC unit A Continuous conversion interrupt (INTADACNT) 110: ADC unit A Monitor function interrupt 0 (INTADACP0) 111: ADC unit A Monitor function interrupt 1 (INTADACP1) When <INSEL7[2:0]> is set to “000”(PB1 pin), ”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL7> to “1".
27	-	0	R	Read as “0”
26	UPDN7	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
25	OUTSEL7	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
24	EN7	0	R/W	Setup of trigger output control 0: Disable 1: Enable
23	-	0	R	Read as “0”
22:20	INSEL6[2:0] (INSEL70[2:0])	000	R/W	Selection of an input trigger (T32A ch6 Timer C) 000: T32A ch5 Timer register C0 match trigger (T32A05TRGOUTCMPC0) 001: T32A ch5 Timer register C1 match trigger (T32A05TRGOUTCMPC1) 010: T32A ch5 Timer C overflow trigger (T32A05TRGOUTOFC) 011: T32A ch5 Timer C underflow trigger (T32A05TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	-	0	R	Read as “0”
18	UPDN6	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
17	OUTSEL6	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
16	EN6	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Bit	Bit Symbol	After Reset	Type	Function
15	-	0	R	Read as “0”
14:12	INSEL5 [2:0] (INSEL69[2:0])	000	R/W	Selection of an input trigger (T32A ch6 Timer B) 000: T32A ch6 Timer register A0 match trigger (T32A06TRGOUTCMPA0) 001: T32A ch6 Timer register A1 match trigger (T32A06TRGOUTCMPA1) 010: T32A ch6 Timer A overflow trigger (T32A06TRGOUTOFA) 011: T32A ch6 Timer A underflow trigger (T32A06TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN5	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL5	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN5	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL4[2:0] (INSEL68[2:0])	000	R/W	Selection of an input trigger (T32A ch6 Timer A) 000: PB1 pin (TRGIN0) 001: PA3 pin (TRGIN1) 010: PN3 pin (TRGIN2) 011: TSPI ch4 Transmission completion signal (TSPI4TXEND) (Note) 100: TSPI ch4 Reception completion signal (TSPT4RXEND) (Note) 101: ELOSC Low speed clock (fs) 110: Reserved 111: Reserved When <INSEL4[2:0]> is set to “000”(PB1 pin), ”001”(PA3 pin) or “010”(PN3 pin), set <OUTSEL4> to “1".
3	-	0	R	Read as “0”
2	UPDN4	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL4	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN4	0	R/W	Setup of trigger output control 0: Disable 1: Enable

Note: There is no TSPI channel 4 in M3HN / M3HM / M3HL.

2.2.4.19. *[TSEL1CR2]* (Control Register 2)

Bit	Bit Symbol	After Reset	Type	Function
31:15	-	0	R	Read as “0”
14:12	INSEL9[2:0] (INSEL73[2:0])	000	R/W	Selection of an input trigger (T32A ch7 Timer C) 000: T32A ch6 Timer register C0 match trigger (T32A06TRGOUTCMPC0) 001: T32A ch6 Timer register C1 match trigger (T32A06TRGOUTCMPC1) 010: T32A ch6 Timer C overflow trigger (T32A06TRGOUTOFC) 011: T32A ch6 Timer C underflow trigger (T32A06TRGOUTUFC) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	-	0	R	Read as “0”
10	UPDN9	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
9	OUTSEL9	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
8	EN9	0	R/W	Setup of trigger output control 0: Disable 1: Enable
7	-	0	R	Read as “0”
6:4	INSEL8[2:0] (INSEL72[2:0])	000	R/W	Selection of an input trigger (T32A ch7 Timer B) 000: T32A ch7 Timer register A0 match trigger (T32A07TRGOUTCMPA0) 001: T32A ch7 Timer register A1 match trigger (T32A07TRGOUTCMPA1) 010: T32A ch7 Timer A overflow trigger (T32A07TRGOUTOFA) 011: T32A ch7 Timer A underflow trigger (T32A07TRGOUTUFA) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	-	0	R	Read as “0”
2	UPDN8	0	R/W	Selection of edge detection conditions 0: Rising edge detection 1: falling edge detection
1	OUTSEL8	0	R/W	Selection of a trigger output 0: Edge detection is disable 1: Edge detection is enable
0	EN8	0	R/W	Setup of trigger output control 0: Disable 1: Enable

2.3. Clock Selective Watchdog Timer (SIWDT)

2.3.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.14 SIWDT Built-in channel

Product	SIWDT Built-in channel (✓: Available, -: N/A)
	ch0
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.3.2. Count clock

The clock selective watchdog timer can select the clock to count. The clock which can be selected as the following table is shown.

Table 2.15 SIWDT Count clock

Clock	Signal name	Selection
System clock	fsys	It selects by the ***[SIWD0MOD]***<WDCLS> register.
Internal High Speed Oscillator1 Clock	f_{IHOSC1}	
Internal High Speed Oscillator2 Clock	f_{IHOSC2}	

2.3.3. Control Output

When the Internal High Speed Oscillator2 (f_{IHOSC2}) is selected, it is possible to forbid rewriting of the Internal High Speed Oscillator 2.

Table 2.16 SIWDT Control Output

Control Output	Signal name	Remarks
The protection signal of an Internal High Speed Oscillator2 oscillation control bit (***[CGOSCCR]***<IHOSC2EN>).	OSCPRO	It sets up by the ***[SIWD0OSCCR]***<OSCPRO> register.

2.4. Oscillation Frequency Detector (OFD)

2.4.1. Built-in List

The following table shows the built-in list for each product.

Table 2.17 OFD Built-in List

Product	Built-in OFD (✓: Available, -: N/A)
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.4.2. Reference clock

The frequency detection circuit operates with the clock in the following table as the reference clock.

Table 2.18 OFD Reference clock

Reference clock	Signal name	divide value
Internal High Speed Oscillator 2	f_{IHOSC2}	256

2.4.3. Detection object clock

An Oscillation Frequency Detector selects clock to monitor from the detection object clock of the following table.

Table 2.19 OFD Detection object clock

Detection object clock		Signal name
Input Signal	External High Speed Oscillator Clock	f_{EHOSC}
	It is the clock selected by ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> of CG (Clock control part).	fc

2.5. Debug interface

2.5.1. Debugging interface terminal list of each product.

This has the JTAG(TMS,TCK,TDI,TRST_N) and Serial Wire(SWDIO,SWCLK,SWV).

Table 2.20 Debugging interface terminal list

Debugging pin (Signal name)	Port	Product table (✓: Available, -: N/A)				
		M3HQ	M3HP	M3HN	M3HM	M3HL
SWDIO	PL4	✓	✓	✓	✓	✓
TMS						
SWCLK	PL3	✓	✓	✓	✓	✓
TCK						
SWV	PL2	✓	✓	✓	✓	✓
TDO						
TDI	PL1	✓	✓	✓	✓	✓
TRST_N	PL0	✓	✓	✓	✓	✓
TRACECLK	PM0	✓	✓	✓	✓	-
TRACEDATA0	PM1	✓	✓	✓	✓	-
TRACEDATA1	PM2	✓	✓	✓	✓	-
TRACEDATA2	PM3	✓	✓	✓	-	-
TRACEDATA3	PM4	✓	✓	✓	-	-

2.6. Flash Memory

2.6.1. Clock for Programming/Erasing

As for flash memory, the clock of the following table is used for programming/erasing of the code flash or the data flash.

Table 2.21 Clock for Programming/Erasing

Clock for Programming/Erasing
f_{IHOSC1}

2.6.2. The code flash block configuration of each product.

The code flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.22 The code flash of each product

AREA	Block name		TMPM3HQFDFG TMPM3HPFDFG TMPM3HNFDFG TMPM3HNFDDFG TMPM3HMFDFG TMPM3HLFDUG	TMPM3HQFZFG TMPM3HPFZFG TMPM3HNFZFG TMPM3HNFZDFG TMPM3HMFZFG TMPM3HLFZUG	TMPM3HQFYFG TMPM3HPFYFG TMPM3HNFYFG TMPM3HNFYDFG TMPM3HMFYFG TMPM3HLFYUG	Block Size (KB)
0	Block0	PG0	✓	✓	✓	4
		PG1	✓	✓	✓	4
		PG2	✓	✓	✓	4
		PG3	✓	✓	✓	4
		PG4	✓	✓	✓	4
		PG5	✓	✓	✓	4
		PG6	✓	✓	✓	4
		PG7	✓	✓	✓	4
	Block1		✓	✓	✓	32
	Block2		✓	✓	✓	32
	Block3		✓	✓	✓	32
	Block4		✓	✓	✓	32
	Block5		✓	✓	✓	32
	Block6		✓	✓	✓	32
	Block7		✓	✓	✓	32
	Block8		✓	✓	-	32
	Block9		✓	✓	-	32
	Block10		✓	✓	-	32
	Block11		✓	✓	-	32
	Block12		✓	-	-	32
	Block13		✓	-	-	32
	Block14		✓	-	-	32
	Block15		✓	-	-	32

Note: ✓: Available, -: N/A

2.6.3. The data flash block configuration of each product.

Block configuration of data flash memory is shown in the following table.

Table 2.23 The data flash of each product

AREA	Block name	TMPM3HQFDFG TMPM3HPFDFG TMPM3HNFDFG TMPM3HMFDFG TMPM3HLFDUG TMPM3HQFZFG TMPM3HPFZFG TMPM3HNFZFG TMPM3HMFZFG TMPM3HLFZUG TMPM3HQFYFG TMPM3HPFYFG TMPM3HNFYFG TMPM3HMFYFG TMPM3HLFYUG	Block Size (KB)
4	Block0	✓	4
	Block1	✓	4
	Block2	✓	4
	Block3	✓	4
	Block4	✓	4
	Block5	✓	4
	Block6	✓	4
	Block7	✓	4

Note: ✓: Available, -: N/A

2.6.4. Single boot use resource

The peripheral function of the following table is used in single boot.

Table 2.24 Single boot use resource

Peripheral function	Channel	Pin name
BOOT	-	PB0 (BOOT_N)
UART	ch0	PA1/PA2 (UT0TXDA/UT0RXD) or, PM1/PM2 (UT0TXDA/UT0RXD) (Note)
T32A	ch0	-

Note: At the time of single boot start, the selection of PA1/PA2 or PM1/PM2 is distinguished automatically by the state of the terminal. During the automatic distinction, internal pull-up of PA2/UT0RXD and PM2/UT0RXD enabled, and the "High" level is outputted. Please keep the "High" level (open or "High" level input) of UT0RXD which is not used at this time. As for UT0RXD which is not used after automatic distinction finishes, "Hi-z" is outputted.

The range of the RAM address transmitted by the RAM loader command should use the following table.

Table 2.25 The end address in which RAM transmission is possible

Product name	The end address in which RAM transmission is possible
TMPM3HQFDFG TMPM3HPFDFG TMPM3HNFDFG TMPM3HMFDFG TMPM3HLFDUG TMPM3HQFZFG TMPM3HPFZFG TMPM3HNFZFG TMPM3HMFZFG TMPM3HLFZUG TMPM3HQFYFG TMPM3HPFYFG TMPM3HNFYFG TMPM3HMFYFG TMPM3HLFYUG	0x20000400 to 0x2000FFFF

2.7. DMA Controller (DMAC)

2.7.1. Built-in unit

The built-in unit for each product is shown in the following table.

Table 2.26 DMAC Built-in unit

Product	DMAC Built-in unit (✓: Available, -: N/A)	
	unit A	unit B
M3HQ	✓	✓
M3HP	✓	✓
M3HN	✓	✓
M3HM	✓	✓
M3HL	✓	✓

2.7.2. DMA request list

A DMA request list is shown in the following table.

The channel which has a register name in the trigger selector column of a table should select the request used by a trigger selector. "-" in a table does not have an applicable function.

Table 2.27 DMA unit A Request list (1/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
0	TSPI ch0 Receive DMA request	TSPI0RX_DMA	-	TSPI ch0 Receive DMA request	TSPI0RX_DMA
1	TSPI ch0 Transmit DMA request	TSPI0TX_DMA	-	TSPI ch0 Transmit DMA request	TSPI0TX_DMA
2	TSPI ch1 Receive DMA request (Note1)	TSPI1RX_DMA	-	TSPI ch1 Receive DMA request (Note1)	TSPI1RX_DMA
3	TSPI ch1 Transmit DMA request (Note1)	TSPI1TX_DMA	-	TSPI ch1 Transmit DMA request (Note1)	TSPI1TX_DMA
4	-	-	-	I^2C ch0 Receiving DMA request	I2C0RXDMAREQ
5	-	-	-	I^2C ch0 Transmitting DMA request	I2C0TXDMAREQ
6	UART ch0 Reception DMA request	UART0RX_DMAREQ	-	UART ch0 Reception DMA request	UART0RX_DMAREQ
7	UART ch0 Transmission DMA request	UART0TX_DMAREQ	-	UART ch0 Transmission DMA request	UART0TX_DMAREQ
8	UART ch1 Reception DMA request	UART1RX_DMAREQ	-	UART ch1 Reception DMA request	UART1RX_DMAREQ
9	UART ch1 Transmission DMA request	UART1TX_DMAREQ	-	UART ch1 Transmission DMA request	UART1TX_DMAREQ
10	UART ch2 Reception DMA request	UART2RX_DMAREQ	-	UART ch2 Reception DMA request	UART2RX_DMAREQ
11	UART ch2 Transmission DMA request	UART2TX_DMAREQ	-	UART ch2 Transmission DMA request	UART2TX_DMAREQ
12	UART ch3 Reception DMA request	UART3RX_DMAREQ	-	UART ch3 Reception DMA request	UART3RX_DMAREQ
13	UART ch3 Transmission DMA request	UART3TX_DMAREQ	-	UART ch3 Transmission DMA request	UART3TX_DMAREQ

Note1: There is no TSPI channel1 in M3HL.

Table 2.28 DMA unit A Request list (2/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
14	-	-	-	A-PMD ch0 PWM interrupt	INTPMD0
15	-	-	***[TSEL0CR0]*** <INSEL0[2:0]> (Note)	T32A ch0 DMA request at match A1 register	T32A00DMAREQCMPA1
				T32A ch0 DMA request at match C1 register	T32A00DMAREQCMPC1
				T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1
				T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1
16	-	-	***[TSEL0CR0]*** <INSEL1[2:0]> (Note)	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1
				T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1
				T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1
				T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1
17	-	-	***[TSEL0CR0]*** <INSEL2[2:0]> (Note)	T32A ch0 DMA request at match B1 register	T32A00DMAREQCMPB1
				T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1
18	-	-	***[TSEL0CR0]*** <INSEL3[2:0]> (Note)	T32A ch2 DMA request at match B1 register	T32A02DMAREQCMPB1
				T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1
19	-	-	***[TSEL0CR1]*** <INSEL4[2:0]> (Note)	T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0
				T32A ch0 DMA request at capture A1 register	T32A00DMAREQCAPA1
				T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0
				T32A ch1 DMA request at capture A1 register	T32A01DMAREQCAPA1
				T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0
				T32A ch0 DMA request at capture C1 register	T32A00DMAREQCAPC1
				T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0
				T32A ch1 DMA request at capture C1 register	T32A01DMAREQCAPC1

Note: ch15 to ch31 select the trigger source of a DMA request by a trigger selector. Please refer to " 2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.29 DMA unit A Request list (3/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
20	-	-	***[TSEL0CR1]*** <INSEL5[2:0]> (Note)	T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0
				T32A ch2 DMA request at capture A1 register	T32A02DMAREQCAPA1
				T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0
				T32A ch3 DMA request at capture A1 register	T32A03DMAREQCAPA1
				T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0
				T32A ch2 DMA request at capture C1 register	T32A02DMAREQCAPC1
				T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0
				T32A ch3 DMA request at capture C1 register	T32A03DMAREQCAPC1
21	-	-	***[TSEL0CR1]*** <INSEL6[2:0]> (Note)	T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0
				T32A ch0 DMA request at capture B1 register	T32A00DMAREQCAPB1
				T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0
				T32A ch1 DMA request at capture B1 register	T32A01DMAREQCAPB1
22	-	-	***[TSEL0CR1]*** <INSEL7[2:0]> (Note)	T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0
				T32A ch2 DMA request at capture B1 register	T32A02DMAREQCAPB1
				T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0
				T32A ch3 DMA request at capture B1 register	T32A03DMAREQCAPB1
23	-	-	***[TSEL0CR2]*** <INSEL8[2:0]> (Note)	DMAC A ch0 transmission end interrupt	INTDMAATC0
				DMAC A ch1 transmission end interrupt	INTDMAATC1
				DMAC A ch6 transmission end interrupt	INTDMAATC6
				DMAC A ch7 transmission end interrupt	INTDMAATC7
24	-	-	***[TSEL0CR2]*** <INSEL9[2:0]> (Note)	DMAC A ch2 transmission end interrupt	INTDMAATC2
				DMAC A ch3 transmission end interrupt	INTDMAATC3
				DMAC A ch8 transmission end interrupt	INTDMAATC8
				DMAC A ch9 transmission end interrupt	INTDMAATC9

Note: ch15 to ch31 select the trigger source of a DMA request by a trigger selector. Please refer to " 2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.30 DMA unit A Request list (4/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
25	-	-	***[TSEL0CR2]*** <INSEL10[2:0]> (Note)	DMAC A ch4 transmission end interrupt	INTDMAATC4
				DMAC A ch5 transmission end interrupt	INTDMAATC5
				DMAC A ch10 transmission end interrupt	INTDMAATC10
				DMAC A ch11 transmission end interrupt	INTDMAATC11
26	-	-	***[TSEL0CR2]*** <INSEL11[2:0]> (Note)	DMAC A ch12 transmission end interrupt	INTDMAATC12
				DMAC A ch13 transmission end interrupt	INTDMAATC13
				DMAC A ch14 transmission end interrupt	INTDMAATC14
27	-	-	***[TSEL0CR3]*** <INSEL12[2:0]> (Note)	DMAC A ch15 transmission end interrupt	INTDMAATC15
				DMAC A ch19 transmission end interrupt	INTDMAATC19
28	-	-	***[TSEL0CR3]*** <INSEL13[2:0]> (Note)	DMAC A ch16 transmission end interrupt	INTDMAATC16
				DMAC A ch20 transmission end interrupt	INTDMAATC20
29	-	-	***[TSEL0CR3]*** <INSEL14[2:0]> (Note)	DMAC A ch17 transmission end interrupt	INTDMAATC17
				DMAC A ch21 transmission end interrupt	INTDMAATC21
30	-	-	***[TSEL0CR3]*** <INSEL15[2:0]> (Note)	DMAC A ch18 transmission end interrupt	INTDMAATC18
				DMAC A ch22 transmission end interrupt	INTDMAATC22
31	-	-	***[TSEL0CR4]*** <INSEL16[2:0]> (Note)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2

Note: ch15 to ch31 select the trigger source of a DMA request by a trigger selector. Please refer to " 2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.31 DMA unit B Request list (1/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
0	TSPI ch2 Receive DMA request(Note2)	TSPI2RX_DMA	***[TSEL0CR4]*** <INSEL17[2:0]> (Note1)	TSPI ch2 Receive DMA request(Note2)	TSPI2RX_DMA
				I^2C ch3 Receiving DMA request (Note3)	I2C3RXDMAREQ
1	TSPI ch2 Transmit DMA request(Note2)	TSPI2TX_DMA	***[TSEL0CR4]*** <INSEL18[2:0]> (Note1)	TSPI ch2 Transmit DMA request(Note2)	TSPI2TX_DMA
				I^2C ch3 Transmitting DMA request (Note3)	I2C3TXDMAREQ
2	TSPI ch3 Receive DMA request(Note2)	TSPI3RX_DMA	-	TSPI ch3 Receive DMA request (Note2)	TSPI3RX_DMA
3	TSPI ch3 Transmit DMA request(Note2)	TSPI3TX_DMA	-	TSPI ch3 Transmit DMA request (Note2)	TSPI3TX_DMA
4	TSPI ch4 Receive DMA Request(Note4)	TSPI4RX_DMA	-	TSPI ch4 Receive DMA request (Note4)	TSPI4RX_DMA
5	TSPI ch4 Transmit DMA request (Note4)	TSPI4TX_DMA	-	TSPI ch4 Transmit DMA request (Note4)	TSPI4TX_DMA
6	-	-	-	I^2C ch1 Receiving DMA request (Note2)	I2C1RXDMAREQ
7	-	-	-	I^2C ch1 Transmitting DMA request (Note2)	I2C1TXDMAREQ
8	-	-	-	I^2C ch2 Receiving DMA request	I2C2RXDMAREQ
9	-	-	-	I^2C ch2 Transmitting DMA request	I2C2TXDMAREQ
10	UART ch4 Reception DMA request	UART4RX_DMAREQ	-	UART ch4 Reception DMA request	UART4RX_DMAREQ
11	UART ch4 Transmission DMA request	UART4TX_DMAREQ	-	UART ch4 Transmission DMA request	UART4TX_DMAREQ
12	UART ch5 Reception DMA request	UART5RX_DMAREQ	-	UART ch5 Reception DMA request	UART5RX_DMAREQ
13	UART ch5 Transmission DMA request	UART5TX_DMAREQ	-	UART ch5 Transmission DMA request	UART5TX_DMAREQ
14	-	-	***[TSEL0CR4]*** <INSEL19[2:0]> (Note1)	ADC unit A General purpose trigger DMA request	ADATRG_DMAREQ
				ADC unit A Single conversion DMA request	ADASGL_DMAREQ
				ADC unit A Continuous conversion DMA request	ADACNT_DMAREQ
15	-	-	***[TSEL0CR5]*** <INSEL20[2:0]> (Note1)	T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1
				T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1
				T32A ch5 DMA request at match A1 register	T32A05DMAREQCMPA1
				T32A ch5 DMA request at match C1 register	T32A05DMAREQCMPC1
16	-	-	***[TSEL0CR5]*** <INSEL21[2:0]> (Note1)	T32A ch6 DMA request at match A1 register	T32A06DMAREQCMPA1
				T32A ch6 DMA request at match C1 register	T32A06DMAREQCMPC1
				T32A ch7 DMA request at match A1 register	T32A07DMAREQCMPA1
				T32A ch7 DMA request at match C1 register	T32A07DMAREQCMPC1

Note1: ch0,ch1 and ch14 to ch31 select the trigger source of a DMA request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: There is no TSPI ch 2, ch 3 and I²C ch 1 in M3HL.
Note3: There is no I²C ch 3 in M3HN / M3HM / M3HL.
Note4: There is no TSPI ch 4 in M3HN / M3HM / M3HL.

Table 2.32 DMA unit B Request list (2/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
17	-	-	***[TSEL0CR5]*** <INSEL22[2:0]> (Note)	T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1
				T32A ch5 DMA request at match B1 register	T32A05DMAREQCMPB1
18	-	-	***[TSEL0CR5]*** <INSEL23[2:0]> (Note)	T32A ch6 DMA request at match B1 register	T32A06DMAREQCMPB1
				T32A ch7 DMA request at match B1 register	T32A07DMAREQCMPB1
19	-	-	***[TSEL0CR6]*** <INSEL24[2:0]> (Note)	T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0
				T32A ch4 DMA request at capture A1 register	T32A04DMAREQCAPA1
				T32A ch5 DMA request at capture A0 register	T32A05DMAREQCAPA0
				T32A ch5 DMA request at capture A1 register	T32A05DMAREQCAPA1
				T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0
				T32A ch4 DMA request at capture C1 register	T32A04DMAREQCAPC1
				T32A ch5 DMA request at capture C0 register	T32A05DMAREQCAPC0
				T32A ch5 DMA request at capture C1 register	T32A05DMAREQCAPC1
20	-	-	***[TSEL0CR6]*** <INSEL25[2:0]> (Note)	T32A ch6 DMA request at capture A0 register	T32A06DMAREQCAPA0
				T32A ch6 DMA request at capture A1 register	T32A06DMAREQCAPA1
				T32A ch7 DMA request at capture A0 register	T32A07DMAREQCAPA0
				T32A ch7 DMA request at capture A1 register	T32A07DMAREQCAPA1
				T32A ch6 DMA request at capture C0 register	T32A06DMAREQCAPC0
				T32A ch6 DMA request at capture C1 register	T32A06DMAREQCAPC1
				T32A ch7 DMA request at capture C0 register	T32A07DMAREQCAPC0
				T32A ch7 DMA request at capture C1 register	T32A07DMAREQCAPC1
21	-	-	***[TSEL0CR6]*** <INSEL26[2:0]> (Note)	T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0
				T32A ch4 DMA request at capture B1 register	T32A04DMAREQCAPB1
				T32A ch5 DMA request at capture B0 register	T32A05DMAREQCAPB0
				T32A ch5 DMA request at capture B1 register	T32A05DMAREQCAPB1

Note: ch0, ch1 and ch14 to ch31 select the trigger source of a DMA request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.33 DMA unit B Request list (3/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
22	-	-	***[TSEL0CR6]*** <INSEL27[2:0]> (Note)	T32A ch6 DMA request at capture B0 register	T32A06DMAREQCAPB0
				T32A ch6 DMA request at capture B1 register	T32A06DMAREQCAPB1
				T32A ch7 DMA request at capture B0 register	T32A07DMAREQCAPB0
				T32A ch7 DMA request at capture B1 register	T32A07DMAREQCAPB1
23	-	-	***[TSEL0CR7]*** <INSEL28[2:0]> (Note)	DMAC B ch0 transmission end interrupt	INTDMABTC0
				DMAC B ch1 transmission end interrupt	INTDMABTC1
				DMAC B ch6 transmission end interrupt	INTDMABTC6
				DMAC B ch7 transmission end interrupt	INTDMABTC7
24	-	-	***[TSEL0CR7]*** <INSEL29[2:0]> (Note)	DMAC B ch2 transmission end interrupt	INTDMABTC2
				DMAC B ch3 transmission end interrupt	INTDMABTC3
				DMAC B ch8 transmission end interrupt	INTDMABTC8
				DMAC B ch9 transmission end interrupt	INTDMABTC9
25	-	-	***[TSEL0CR7]*** <INSEL30[2:0]> (Note)	DMAC B ch4 transmission end interrupt	INTDMABTC4
				DMAC B ch5 transmission end interrupt	INTDMABTC5
				DMAC B ch10 transmission end interrupt	INTDMABTC10
				DMAC B ch11 transmission end interrupt	INTDMABTC11
26	-	-	***[TSEL0CR7]*** <INSEL31[2:0]> (Note)	DMAC B ch12 transmission end interrupt	INTDMABTC12
				DMAC B ch13 transmission end interrupt	INTDMABTC13
				DMAC B ch14 transmission end interrupt	INTDMABTC14
27	-	-	***[TSEL0CR8]*** <INSEL32[2:0]> (Note)	DMAC B ch15 transmission end interrupt	INTDMABTC15
				DMAC B ch19 transmission end interrupt	INTDMABTC19
28	-	-	***[TSEL0CR8]*** <INSEL33[2:0]> (Note)	DMAC B ch16 transmission end interrupt	INTDMABTC16
				DMAC B ch20 transmission end interrupt	INTDMABTC20

Note: ch0, ch1 and ch14 to ch31 select the trigger source of a DMA request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.34 DMA unit B Request list (4/4)

ch	Single transmission		Burst transmission		
		Signal name	Trigger selector		Signal name
29	-	-	***[TSEL0CR8]*** <INSEL34[2:0]> (Note)	DMAC B ch17 transmission end interrupt	INTDMABTC17
				DMAC B ch21transmission end interrupt	INTDMABTC21
30	-	-	***[TSEL0CR8]*** <INSEL35[2:0]> (Note)	DMAC B ch18 transmission end interrupt	INTDMABTC18
				DMAC B ch22 transmission end interrupt	INTDMABTC22
31	-	-	***[TSEL0CR9]*** <INSEL36[2:0]> (Note)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2

Note: ch0, ch1 and ch14 to ch31 select the trigger source of a DMA request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

2.8. Advanced Programmable Motor Control Circuit (A-PMD)

2.8.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.35 A-PMD Built-in channel

Product	A-PMD Built-in channel (✓: Available, -: N/A)
	ch0
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.8.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.36 A-PMD Functional pin

Channel	Functional pin		Signal name	Port	Product table (✓: Available, -: N/A)				
					M3HQ	M3HP	M3HN	M3HM	M3HL
A-PMD ch0	XO0	Output	XO0	PJ1	✓	✓	✓	✓	✓
	YO0	Output	YO0	PJ3	✓	✓	✓	✓	✓
	ZO0	Output	ZO0	PJ5	✓	✓	✓	✓	✓
	UO0	Output	UO0	PJ0	✓	✓	✓	✓	✓
	VO0	Output	VO0	PJ2	✓	✓	✓	✓	✓
	WO0	Output	WO0	PJ4	✓	✓	✓	✓	✓
	PMD0DBG	Output	PMD0DBG	PP6	✓	✓	✓	✓	-
	EMG0	Input	EMG0	PK0	✓	✓	✓	✓	✓
	OVV0	Input	OVV0	PK1	✓	✓	✓	✓	✓

2.8.3. DMA request

The advanced programmable motor control circuit has the DMA request shown in the following table.

Table 2.37 A-PMD DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel			
					Unit	Single Transmission	Burst Transmission
ch0	A-PMD ch0 PWM interrupt	INTPMD0	-	14	A	-	✓

Note: ✓: Available, -: N/A

2.8.4. Other connections

The advanced programmable motor control circuit is connected with the peripheral function inside, as shown in the following table.

Table 2.38 A-PMD ch0 Internal signal connection specification: Input

channel	Input/ output	Functional input	Signal name	Input Signal		
				Peripheral function		Signal name
ch0	Input	OVV state signal (AD monitoring function 0)	ADACMP0L_N	ADC unit A	Monitor function output0 for PMD protect function	ADACP0L_N
		OVV state signal (AD monitoring function 1)	ADACMP1L_N		Monitor function output1 for PMD protect function	ADACP1L_N
		ADC conversion complete interrupt A(PMD0DBG)	INTADAPDA		ADC conversion complete interrupt A	INTADAPDA
		ADC conversion complete interrupt B(PMD0DBG)	INTADAPDB		ADC conversion complete interrupt B	INTADAPDB
		Commutation trigger (ENC position detection sync)	INTENC00	A-ENC ch0	Encoder input interruption 0	INTENC00
		Commutation trigger (ENC MCMP completion sync)	ENC0CTRGO		The commutation trigger	ENC0CTRGO
		Commutation trigger (General purpose timer sync)	PMD0TMR	T32A ch3	Timer register A0 match trigger	T32A03TRGOUTCMPA0

Table 2.39 A-PMD ch0 Internal signal connection specification: Output

channel	Input/ output	Functional Output			Destination	
			Signal name	Peripheral function		Signal name
ch0	Output	ADC synchronous sampling Output 0	PMD0TRG0	ADC unit A	PMD trigger 0	PMDTRG0
		ADC synchronous sampling Output 1	PMD0TRG1		PMD trigger 1	PMDTRG1
		ADC synchronous sampling Output 2	PMD0TRG2		PMD trigger 2	PMDTRG2
		ADC synchronous sampling Output 3	PMD0TRG3		PMD trigger 3	PMDTRG3
		ADC synchronous sampling Output 4	PMD0TRG4		PMD trigger 4	PMDTRG4
		ADC synchronous sampling Output 5	PMD0TRG5		PMD trigger 5	PMDTRG5
		PWM signal for the encoder input	PMD0PWMON	A-ENC ch0	The PWM signal for a sampling	ENC0PWMON

2.8.5. Additional setting of using PMD0DBG

Debug output can be set in ***[PMDxDBGOUTCR]***. To set the ADC conversion timing monitor (<DBGMD[1: 0]> = 00) in the debug mode selection, set the following register at the same time.

Table 2.40 Setting value of ADC mode setting register3

Register Name	Value	address(Base+)
[ADxMOD3]<MOD3[31:0]>	0x00000001	0x001C

2.9. Advanced Encoder Input Circuit (A-ENC)

2.9.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.41 A-ENC Built-in channel

Product	A-ENC Built-in channel (✓: Available, -: N/A)
	ch0
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.9.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.42 A-ENC Functional pin and port

Channel	Functional pin		Signal name	Port	Product table (✓: Available, -: N/A)				
					M3HQ	M3HP	M3HN	M3HM	M3HL
A-ENC ch0	ENC0A	Input	ENC0A	PA0	✓	✓	✓	✓	✓
	ENC0B	Input	ENC0B	PA1	✓	✓	✓	✓	✓
	ENC0Z	Input	ENC0Z	PA2	✓	✓	✓	✓	✓

2.9.3. Internal signal connection specification

2.9.3.1. T32A / A-PMD connection

The advanced encoder input circuit is connected with the peripheral function inside, as shown in the following table. "-" in a table does not have an applicable function.

Table 2.43 A-ENC Internal signal connection specification: Input

Input/ output	Functional input	Signal name	Peripheral function	Input Signal	Signal name
Input	Timer output signal in general	ENC0PSGI	T32A ch5	T32A ch5 Timer A output	T32A05OUTA
	The PWM signal for a sampling	ENC0PWMON	A-PMD ch0	PWM signal for the encoder input	PMD0PWMON

Table 2.44 A-ENC Internal signal connection specification: Output

Input /output	Functional Output		Trigger selector		Destination	
		Signal name		Peripheral function		Signal name
Output	Divided pulse signal	ENC0TIMPLS	***[TSEL1CR0]*** <INSEL1[2:0]> (Note)	T32A ch5	T32A ch5 Timer A internal trigger input	T32A05TRGINAPHCK
	The commutation trigger	ENC0CTRGO	-	A-PMD ch0	Commutation trigger (ENC MCMP completion sync)	ENC0CTRGO
	Encoder input interruption 0	INTENC00	-		Commutation trigger (ENC position detection sync)	INTENC00

Note: ***[TSEL1CR0]***<INSEL9[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

2.10. 12-bit Analog to Digital Converter (ADC)

2.10.1. Built-in unit

The built-in unit for each product is shown in the following table.

Table 2.45 ADC Built-in unit

Product	ADC Built-in unit (✓: Available, -: N/A)
	unit A
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.10.2. Functional pin and port

The functional pin is assigned to the port of the following table.

There is also a channel which does not have a functional pin by a product.

Table 2.46 ADC Functional pin and a port

Input channel	Functional pin (Signal name)	Port	Product table (✓: Available, -: N/A)				
			M3HQ	M3HP	M3HN	M3HM	M3HL
ch0	AINA00	PD0	✓	✓	✓	✓	✓
ch1	AINA01	PD1	✓	✓	✓	✓	✓
ch2	AINA02	PD2	✓	✓	✓	✓	✓
ch3	AINA03	PD3	✓	✓	✓	-	-
ch4	AINA04	PE0	✓	✓	✓	✓	✓
ch5	AINA05	PE1	✓	✓	✓	✓	✓
ch6	AINA06	PE2	✓	✓	✓	✓	✓
ch7	AINA07	PE3	✓	✓	✓	✓	✓
ch8	AINA08	PE4	✓	✓	✓	✓	✓
ch9	AINA09	PE5	✓	✓	✓	✓	✓
ch10	AINA10	PE6	✓	✓	✓	✓	✓
ch11	AINA11	PF0	✓	✓	✓	-	-
ch12	AINA12	PF1	✓	✓	✓	-	-
ch13	AINA13	PF2	✓	✓	-	-	-
ch14	AINA14	PF3	✓	✓	-	-	-
ch15	AINA15	PF4	✓	✓	-	-	-
ch16	AINA16	PF5	✓	✓	-	-	-
ch17	AINA17	PF6	✓	✓	-	-	-
ch18	AINA18	PF7	✓	✓	-	-	-
ch19	AINA19	PD4	✓	-	-	-	-
ch20	AINA20	PD5	✓	-	-	-	-
ch21	AINA21	DAC0	✓	✓	✓	✓	✓

Note: When using ch21,the DAC0 pin must be open.

2.10.3. Clock for the ADC conversion

The clock which shows the 12-bit Analog to Digital Converter in the following table at the conversion clock is used.

Table 2.47 ADC Clock for the conversion

Clock for the conversion
ADCLK

2.10.4. Set of mode setting register 2

Please be sure to set up the value of the following table about the setting value of the mode setting register 2 (***[ADxMOD2]***).

Table 2.48 ADC Set of mode setting register 2

Register name	Value
[ADxMOD2]<MOD2[31:0]>	0x00000300

2.10.5. DMA request

A 12-bit Analog to Digital Converter has the DMA request shown in the following table.

Table 2.49 ADC DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel			
					Unit	Single Transmission	Burst Transmission
ADC Unit A	General purpose trigger DMA request	ADATRG_DMAREQ	***[TSEL0CR4]*** <INSEL19[2:0]> (Note1)	14	B	-	✓
	Single conversion DMA request	ADASGL_DMAREQ				-	✓
	Continuous conversion DMA request	ADACNT_DMAREQ				-	✓

Note1: ***[TSEL0CR4]***<INSEL19[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2: ✓: Available, -: N/A

2.10.6. Internal signal connection specification

2.10.6.1. Start-trigger connection specification

The 12-bit Analog to Digital Converter has the AD translation function by the trigger signal.

The input trigger signal which has a register name in the trigger selector column of the following table should select the input trigger used by a trigger selector. "-" in a table does not have an applicable function.

Table 2.50 ADC Start trigger connection specification

Connection destination (Signal name)	Starting trigger		
	Trigger selector	Input trigger signal	Signal name
PMDTRG0	-	PMD trigger 0	PMD0TRG0
PMDTRG1	-	PMD trigger 1	PMD0TRG1
PMDTRG2	-	PMD trigger 2	PMD0TRG2
PMDTRG3	-	PMD trigger 3	PMD0TRG3
PMDTRG4	-	PMD trigger 4	PMD0TRG4
PMDTRG5	-	PMD trigger 5	PMD0TRG5
PMDTRG6	***[TSEL0CR9]*** <INSEL37[2:0]> (Note)	PB1 pin	TRGIN0
		PA3 pin	TRGIN1
		PN3 pin	TRGIN2
		T32A ch7 Timer register A1 match trigger	T32A07TRGOUTCMPA1
		T32A ch7 Timer register B1 match trigger	T32A07TRGOUTCMPB1
		T32A ch7 Timer register C1 match trigger	T32A07TRGOUTCMPC1
PMDTRG7	-	-	-
PMDTRG8	-	-	-
PMDTRG9	-	-	-
PMDTRG10	-	-	-
PMDTRG11	-	-	-
ADATRGIN	***[TSEL0CR9]*** <INSEL38[2:0]> (Note)	PB1 pin	TRGIN0
		PA3 pin	TRGIN1
		PN3 pin	TRGIN2
		T32A ch7 Timer register A1 match trigger	T32A07TRGOUTCMPA1
		T32A ch7 Timer register B1 match trigger	T32A07TRGOUTCMPB1
		T32A ch7 Timer register C1 match trigger	T32A07TRGOUTCMPC1

Note: ***[TSEL0CR9]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

2.10.6.2. T32A / A-PMD connection

In addition to this, the 12-bit Analog to Digital Converter is connected with the peripheral function inside, as shown in the following table. "-" in a table does not have an applicable function.

Table 2.51 ADC Internal signal connection specification: Output

Input /output	Functional Output				Destination	
		Signal name	Trigger selector	Peripheral function		Signal name
Output	ADC A General purpose trigger interrupt	INTADATRG	***[TSEL1CR1]*** <INSEL7[2:0]> (Note)	T32A	Timer A ch7	T32A07TRGINAPCK
	ADC A Single conversion interrupt	INTADASGL				
	ADC A Continuous conversion interrupt	INTADACNT				
	ADC A Monitor function 0 interrupt	INTADACP0				
	ADC A Monitor function 1 interrupt	INTADACP1				
	ADC A Monitor function 0 output for PMD protect function	ADACP0L_N	-	A-PMD ch0	OVV state signal (AD monitor function 0)	ADACMP0L_N
	ADC A Monitor function 1 output for PMD protect function	ADACP1L_N	-		OVV state signal (AD monitor function 1)	ADACMP1L_N

Note: ***[TSEL1CR1]***<INSEL7[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

2.11. 8-bit Digital to Analog Converter (DAC)

2.11.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.52 DAC Built-in channel

Product	DAC Built-in channel (✓: Available, -: N/A)	
	ch0	ch1
M3HQ	✓	✓
M3HP	✓	✓
M3HN	✓	✓
M3HM	✓	✓
M3HL	✓	✓

2.11.2. Functional pin and a port

The functional terminal is assigned to the following ports.

Table 2.53 DAC Functional pin and a port

Channel	Functional pin (Signal name)	Port	Product table (✓: Available, -: N/A)				
			M3HQ	M3HP	M3HN	M3HM	M3HL
DAC ch0	DAC0	PG0	✓	✓	✓	✓	✓
DAC ch1	DAC1	PG1	✓	✓	✓	✓	✓

VREFH is connected to AVDD5 and VREFL is connected to AVSS.

2.12. Comparator (COMP)

2.12.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.54 Comparator Built-in channel

Product	COMP Built-in channel (✓: Available, -: N/A)
	ch0
M3HM	✓
M3HN	✓
M3HP	✓
M3HQ	✓
M3HL	✓

Table 2.55 COMP Functional pin

Functional pin		Signal name	Product table (✓: Available, -: N/A)				
			M3HQ	M3HP	M3HN	M3HM	M3HL
AINA00	Input	AINA00(ADC)	✓	✓	✓	✓	✓
AINA01	Input	AINA01(ADC)	✓	✓	✓	✓	✓
DAC0(VREFC)	Input	DAC ch0	✓	✓	✓	✓	✓
COMP output	Output	CMPA(A-PMD)	✓	✓	✓	✓	✓

2.13. Voltage Detection Circuit (LVD)

2.13.1. Built-in List

The following table shows the built-in list for each product.

Table 2.56 LVD Built-in List

Product	Built-in LVD (✓: Available, -: N/A)
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.13.2. LVD Detection power supply

A voltage detecting circuit monitors the power supply of the following table.

Table 2.57 LVD Detection power supply

LVD Detection power supply	Power supply name
Digital power source terminal	DVDD5A, DVDD5B

2.14. 32-bit Timer Event Counter (T32A)

2.14.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.58 T32A Built-in channel

Product	T32A Built-in channel (✓: Available, -: N/A)							
	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7
M3HQ	✓	✓	✓	✓	✓	✓	✓	✓
M3HP	✓	✓	✓	✓	✓	✓	✓	✓
M3HN	✓	✓	✓	✓	✓	✓	✓	✓
M3HM	✓	✓	✓	✓	✓	✓	✓	✓
M3HL	✓	✓	✓	✓	✓	✓	✓	✓

2.14.2. Functional pin and port

The functional pin is assigned to the port of the following tables.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.59 T32A Functional pin and a port (1/3)

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
T32A ch0	T32A00OUTA	Output	PA0 / PM0	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
	T32A00OUTB	Output	PA3 / PM3	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	T32A00OUTC	Output	PA0 / PM0	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
	T32A00INA0	Input	PA1 / PM1	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	T32A00INA1	Input	PA2 / PM2	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	T32A00INB0	Input	PA4 / PM4	✓/✓	✓/✓	✓/✓	✓/-	-/-
	T32A00INB1	Input	PA5 / PM5	✓/✓	✓/✓	✓/✓	✓/-	-/-
	T32A00INC0	Input	PA1 / PM1	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	T32A00INC1	Input	PA2 / PM2	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
T32A ch1	T32A01OUTA	Output	PB0 / PP0	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	T32A01OUTB	Output	PB3	✓	✓	✓	✓	✓
	T32A01OUTC	Output	PB0 / PP0	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	T32A01INA0	Input	PB1 / PP1	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	T32A01INA1	Input	PB2 / PP2	✓/✓	✓/✓	✓/✓	✓/✓	-/-
	T32A01INB0	Input	PB4	✓	✓	✓	✓	-
	T32A01INB1	Input	PB5	✓	✓	✓	-	-
	T32A01INC0	Input	PB1 / PP1	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	T32A01INC1	Input	PB2 / PP2	✓/✓	✓/✓	✓/✓	✓/✓	✓/-

Table 2.60 T32A Functional signal and a port (2/3)

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
T32A ch2	T32A02OUTA	Output	PC0 / PR0	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	T32A02OUTB	Output	PC3	✓	✓	✓	✓	✓
	T32A02OUTC	Output	PC0 / PR0	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	T32A02INA0	Input	PC1 / PR1	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	T32A02INA1	Input	PC2 / PR2	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	T32A02INB0	Input	PC4	✓	✓	✓	✓	✓
	T32A02INB1	Input	PC5	✓	✓	✓	✓	-
	T32A02INC0	Input	PC1 / PR1	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	T32A02INC1	Input	PC2 / PR2	✓/✓	✓/✓	✓/✓	✓/-	-/-
T32A ch3	T32A03OUTA	Output	PJ0	✓	✓	✓	✓	✓
	T32A03OUTB	Output	PJ3	✓	✓	✓	✓	✓
	T32A03OUTC	Output	PJ0	✓	✓	✓	✓	✓
	T32A03INA0	Input	PJ1	✓	✓	✓	✓	✓
	T32A03INA1	Input	PJ2	✓	✓	✓	✓	✓
	T32A03INB0	Input	PJ4	✓	✓	✓	✓	✓
	T32A03INB1	Input	PJ5	✓	✓	✓	✓	✓
	T32A03INC0	Input	PJ1	✓	✓	✓	✓	✓
	T32A03INC1	Input	PJ2	✓	✓	✓	✓	✓
T32A ch4	T32A04OUTA	Output	PK2	✓	✓	✓	✓	✓
	T32A04OUTB	Output	PK5	✓	✓	✓	✓	✓
	T32A04OUTC	Output	PK2	✓	✓	✓	✓	✓
	T32A04INA0	Input	PK3	✓	✓	✓	✓	✓
	T32A04INA1	Input	PK4	✓	✓	✓	✓	✓
	T32A04INB0	Input	PK6	✓	✓	✓	✓	✓
	T32A04INB1	Input	PK7	✓	✓	✓	✓	-
	T32A04INC0	Input	PK3	✓	✓	✓	✓	✓
	T32A04INC1	Input	PK4	✓	✓	✓	✓	✓
T32A ch5	T32A05OUTA	Output	PN0	✓	✓	✓	✓	-
	T32A05OUTB	Output	PN3	✓	✓	✓	✓	✓
	T32A05OUTC	Output	PN0	✓	✓	✓	✓	✓
	T32A05INA0	Input	PN1	✓	✓	✓	✓	✓
	T32A05INA1	Input	PN2	✓	✓	✓	✓	✓
	T32A05INB0	Input	PN4	✓	✓	✓	✓	-
	T32A05INB1	Input	PN5	✓	✓	✓	-	-
	T32A05INC0	Input	PN1	✓	✓	✓	✓	✓
	T32A05INC1	Input	PN2	✓	✓	✓	✓	✓

Table 2.61 T32A Functional pin and a port (3/3)

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
T32A ch6	T32A06OUTA	Output	PL5/PT5	✓/✓	✓/-	✓/-	- /-	- /-
	T32A06OUTB	Output	PL2/PT2	✓/✓	✓/✓	✓/-	✓/-	✓/-
	T32A06OUTC	Output	PL5/PT5	✓/✓	✓/-	✓/-	- /-	- /-
	T32A06INA0	Input	PL6/PT6	✓/✓	✓/-	✓/-	- /-	- /-
	T32A06INA1	Input	PL7/PT7	✓/✓	✓/-	- /-	- /-	- /-
	T32A06INB0	Input	PL3/PT3	✓/✓	✓/✓	✓/-	✓/-	✓/-
	T32A06INB1	Input	PL4/PT4	✓/✓	✓/-	✓/-	✓/-	✓/-
	T32A06INC0	Input	PL6/PT6	✓/✓	✓/-	✓/-	- /-	- /-
	T32A06INC1	Input	PL7/PT7	✓/✓	✓/-	- /-	- /-	- /-
T32A ch7	T32A07OUTA	Output	PG2	✓	✓	-	-	-
	T32A07OUTB	Output	PG5	✓	✓	-	-	-
	T32A07OUTC	Output	PG2	✓	✓	-	-	-
	T32A07INA0	Input	PG3	✓	✓	-	-	-
	T32A07INA1	Input	PG4	✓	✓	-	-	-
	T32A07INB0	Input	PG6	✓	✓	-	-	-
	T32A07INB1	Input	PG7	✓	✓	-	-	-
	T32A07INC0	Input	PG3	✓	✓	-	-	-
	T32A07INC1	Input	PG4	✓	✓	-	-	-

2.14.3. Clock for prescaler

The clock which a 32-bit Timer Event Counter shows in the following table for prescaler is used.

Table 2.62 T32A Clock for prescaler

Clock for prescaler
ΦT0

2.14.4. Internal signal connection specification

The capture trigger signal which shows 32-bit Timer Event Counter in the following tables is connected.

The input trigger signal which has a register name in the trigger selector column of the following table should select the input trigger used by a trigger selector.

2.14.4.1. Capture trigger signal connection specification

Table 2.63 T32A Capture trigger signal connection specification (1/4)

Channel	Timer	Capture trigger input Signal name	Trigger source: Trigger selector	Trigger source: Input trigger signal	Trigger source: Signal name
T32A ch0	A	T32A00TRGINAPHCK (Other timer outputs)	-	-	-
		T32A00TRGINAPCK (Internal trigger input)	***[TSEL0CR12]*** <INSEL50[2:0]> (Note)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				UART ch0 Transmission completion trigger	UART0TXTRG
				UART ch0 Reception completion trigger	UART0RXTRG
	B	T32A00TRGINBPHCK (Other timer outputs)	T32A ch0 Timer A Output		T32A00OUTA
		T32A00TRGINBPCK (Other timer inputs)	***[TSEL0CR12]*** <INSEL51[2:0]> (Note)	T32A ch0 Timer register A0 match trigger	T32A00TRGOUTCMPA0
				T32A ch0 Timer register A1 match trigger	T32A00TRGOUTCMPA1
				T32A ch0 Timer A overflow trigger	T32A00TRGOUTOFA
				T32A ch0 Timer A underflow trigger	T32A00TRGOUTUFA
	C	T32A00TRGINCPHCK (Other timer outputs)	-	-	-
		T32A00TRGINCPCK (Internal trigger input)	***[TSEL0CR13]*** <INSEL52[2:0]> (Note)	T32A ch7 Timer register C0 match trigger	T32A07TRGOUTCMPC0
				T32A ch7 Timer register C1 match trigger	T32A07TRGOUTCMPC1
				T32A ch7 Timer C overflow trigger	T32A07TRGOUTOFC
				T32A ch7 Timer C underflow trigger	T32A07TRGOUTUFC
T32A ch1	A	T32A01TRGINAPHCK (Other timer outputs)	-	-	-
		T32A01TRGINAPCK (Internal trigger input)	***[TSEL0CR13]*** <INSEL53[2:0]> (Note)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				UART ch1 Transmission completion trigger	UART1TXTRG
				UART ch1 Reception completion trigger	UART1RXTRG
				I^2C ch0 interrupt	INTI2C0
	B	T32A01TRGINBPHCK (Other timer outputs)	T32A ch1 Timer A Output		T32A01OUTA
		T32A01TRGINBPCK (Internal trigger input)	***[TSEL0CR13]*** <INSEL54[2:0]> (Note)	T32A ch1 Timer register A0 match trigger	T32A01TRGOUTCMPA0
				T32A ch1 Timer register A1 match trigger	T32A01TRGOUTCMPA1
				T32A ch1 Timer A overflow trigger	T32A01TRGOUTOFA
				T32A ch1 Timer A underflow trigger	T32A01TRGOUTUFA
	C	T32A01TRGINCPHCK (Other timer outputs)	T32A ch0 Timer C Output		T32A00OUTC
		T32A01TRGINCPCK (Internal trigger input)	***[TSEL0CR13]*** <INSEL55[2:0]> (Note)	T32A ch0 Timer register C0 match trigger	T32A00TRGOUTCMPC0
				T32A ch0 Timer register C1 match trigger	T32A00TRGOUTCMPC1
				T32A ch0 Timer C overflow trigger	T32A00TRGOUTOFC
				T32A ch0 Timer C underflow trigger	T32A00TRGOUTUFC

Note: ***[TSEL0CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Table 2.64 T32A Capture trigger signal connection specification (2/4)

Channel			Trigger source		
	Timer	capture trigger input□Signal name	Trigger selector	Input trigger signal	Signal name
T32A ch2	A	T32A02TRGINAPHCK (Other timer outputs)	-	-	-
		T32A02TRGINAPCK (Internal trigger input)	***[TSEL0CR14]*** <INSEL56[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				UART ch2 Transmission completion trigger	UART2TXTRG
				UART ch2 Reception completion trigger	UART2RXTRG
				TSPI ch0 transmission completion trigger	TSPI0TXEND
				TSPI ch0 reception completion trigger	TSPI0RXEND
				I^2C ch1 I^2C interruption	INTI2C1
	B	T32A02TRGINBPHCK (Other timer outputs)	T32A ch2 Timer A Output		T32A02OUTA
		T32A02TRGINBPCK (Internal trigger input)	***[TSEL0CR14]*** <INSEL57[2:0]> (Note1)	T32A ch2 Timer register A0 match trigger	T32A02TRGOUTCMPA0
				T32A ch2 Timer register A1 match trigger	T32A02TRGOUTCMPA1
				T32A ch2 Timer A overflow trigger	T32A02TRGOUTOFA
				T32A ch2 Timer A underflow trigger	T32A02TRGOUTUFA
	C	T32A02TRGINCPHCK (Other timer outputs)	-	-	-
		T32A02TRGINCPCK (Internal trigger input)	***[TSEL0CR14]*** <INSEL58[2:0]> (Note1)	T32A ch1 Timer register C0 match trigger	T32A01TRGOUTCMPC0
				T32A ch1 Timer register C1 match trigger	T32A01TRGOUTCMPC1
				T32A ch1 Timer C overflow trigger	T32A01TRGOUTOFC
				T32A ch1 Timer C underflow trigger	T32A01TRGOUTUFC
T32A ch3	A	T32A03TRGINAPHCK (Other timer outputs)	-	-	-
		T32A03TRGINAPCK (Internal trigger input)	***[TSEL0CR14]*** <INSEL59[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				UART ch3 Transmission completion trigger	UART3TXTRG
				UART ch3 Reception completion trigger	UART3RXTRG
				TSPI ch1 Transmit completion (Note2)	TSPI1TXEND
				TSPI ch1 Receive completion (Note2)	TSPI1RXEND
				I^2C ch2 interruption	INTI2C2
	B	T32A03TRGINBPHCK (Other timer outputs)	T32A ch3 Timer A Output		T32A03OUTA
		T32A03TRGINBPCK (Internal trigger input)	***[TSEL0CR15]*** <INSEL60 [2:0]> (Note1)	T32A ch3 Timer register A0 match trigger	T32A03TRGOUTCMPA0
				T32A ch3 Timer register A1 match trigger	T32A03TRGOUTCMPA1
				T32A ch3 Timer A overflow trigger	T32A03TRGOUTOFA
				T32A ch3 Timer A underflow trigger	T32A03TRGOUTUFA
	C	T32A03TRGINCPHCK (Other timer outputs)	T32A ch2 Timer C Output		T32A02OUTC
		T32A03TRGINCPCK (Internal trigger input)	***[TSEL0CR15]*** <INSEL61 [2:0]> (Note1)	T32A ch2 Timer register C0 match trigger	T32A02TRGOUTCMPC0
				T32A ch2 Timer register C1 match trigger	T32A02TRGOUTCMPC1
				T32A ch2 Timer C overflow trigger	T32A02TRGOUTOFC
				T32A ch2 Timer C underflow trigger	T32A02TRGOUTUFC

Note1: ***[TSEL0CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2: There is no TSPI ch1 in M3HL.

Table 2.65 T32A Capture trigger signal connection specification (3/4)

Channel			Trigger source		
	Timer	capture trigger input□Signal name	Trigger selector	Input trigger signal	Signal name
T32A ch4	A	T32A04TRGINAPHCK (Other timer outputs)	-	-	-
		T32A04TRGINAPCK (Internal trigger input)	***[TSEL0CR15]*** <INSEL62[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				UART ch4 Transmission completion trigger	UART4TXTRG
				UART ch4 Reception completion trigger	UART4RXTRG
				TSPI ch2 transmission completion signal (Note2)	TSPI2TXEND
				TSPI ch2 reception completion signal(Note2)	TSPI2RXEND
				I^2C ch3 I^2C interruption (Note3)	INTI2C3
	B	T32A04TRGINBPHCK (Other timer outputs)	T32A ch4 Timer A Output		T32A04OUTA
		T32A04TRGINBPCK (Internal trigger input)	***[TSEL0CR15]*** <INSEL63[2:0]> (Note1)	T32A ch4 Timer register A0 match trigger	T32A04TRGOUTCMPA0
				T32A ch4 Timer register A1 match trigger	T32A04TRGOUTCMPA1
				T32A ch4 Timer A overflow trigger	T32A04TRGOUTOFA
				T32A ch4 Timer A underflow trigger	T32A04TRGOUTUFA
	C	T32A04TRGINCPHCK (Other timer outputs)	-	-	-
		T32A04TRGINCPCK (Internal trigger input)	***[TSEL1CR0]*** <INSEL0[2:0]> (Note1)	T32A ch3 Timer register C0 match trigger	T32A03TRGOUTCMPC0
				T32A ch3 Timer register C1 match trigger	T32A03TRGOUTCMPC1
				T32A ch3 Timer C overflow trigger	T32A03TRGOUTOFC
				T32A ch3 Timer C underflow trigger	T32A03TRGOUTUFC
T32A ch5	A	T32A05TRGINAPHCK (Other timer outputs)	-	-	-
		T32A05TRGINAPCK (Internal trigger input)	***[TSEL1CR0]*** <INSEL1[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				UART ch5 Transmission completion trigger	UART5TXTRG
				UART ch5 Reception completion trigger	UART5RXTRG
				TSPI ch3Transmit completion signal (Note2)	TSPI3TXEND
				TSPI ch3 Receive completion signal (Note2)	TSPI3RXEND
				A-ENC ch0 Dividing pulse signal	ENC0TIMPLS
	B	T32A05TRGINBPHCK (Other timer outputs)	T32A ch5 Timer A Output		T32A05OUTA
		T32A05TRGINBPCK (Internal trigger input)	***[TSEL1CR0]*** <INSEL2[2:0]> (Note1)	T32A ch5 Timer register A0 match trigger	T32A05TRGOUTCMPA0
				T32A ch5 Timer register A1 match trigger	T32A05TRGOUTCMPA1
				T32A ch5 Timer A overflow trigger	T32A05TRGOUTOFA
				T32A ch5 Timer A underflow trigger	T32A05TRGOUTUFA
	C	T32A05TRGINCPHCK (Other timer outputs)	T32A ch4 Timer C Output		T32A04OUTC
		T32A05TRGINCPCK (Internal trigger input)	***[TSEL1CR0]*** <INSEL3[2:0]> (Note1)	T32A ch4 Timer register C0 match trigger	T32A04TRGOUTCMPC0
				T32A ch4 Timer register C1 match trigger	T32A04TRGOUTCMPC1
				T32A ch4 Timer C overflow trigger	T32A04TRGOUTOFC
				T32A ch4 Timer C underflow trigger	T32A04TRGOUTUFC

Note1: ***[TSELxCRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2: There is no TSPI ch2,ch3 in M3HL.

Note3: There is no I^2C ch3 in M3HN / M3HM/ M3HL.

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Table 2.66 T32A Capture trigger signal connection specification (4/4)

Channel			Trigger source		
	Timer	capture trigger input□Signal name	Trigger selector	Input trigger signal	Signal name
T32A ch6	A	T32A06TRGINAPHCK (Other timer outputs)	-	-	-
		T32A06TRGINAPCK (Internal trigger input)	***[TSEL1CR1]*** <INSEL4[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				TSPI ch4 Transmit completion signal (Note2)	TSPI4TXEND
				TSPI ch4 Receive completion signal(Note2)	TSPI4RXEND
				ELOSC Low speed clock	fs
	B	T32A06TRGINBPHCK (Other timer outputs)	T32A ch6 Timer A Output		T32A06OUTA
		T32A06TRGINBPCK (Internal trigger input)	***[TSEL1CR1]*** <INSEL5[2:0]> (Note1)	T32A ch6 Timer register A0 match trigger	T32A06TRGOUTCMPA0
				T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
				T32A ch6 Timer A overflow trigger	T32A06TRGOUTOFA
				T32A ch6 Timer A underflow trigger	T32A06TRGOUTUFA
	C	T32A06TRGINCPHCK (Other timer outputs)	-	-	-
		T32A06TRGINCPCK (Internal trigger input)	***[TSEL1CR1]*** <INSEL6[2:0]> (Note1***)***	T32A ch5 Timer register C0 match trigger	T32A05TRGOUTCMPC0
				T32A ch5 Timer register C1 match trigger	T32A05TRGOUTCMPC1
				T32A ch5 Timer C overflow trigger	T32A05TRGOUTOFC
				T32A ch5 Timer C underflow trigger	T32A05TRGOUTUFC
T32A ch7	A	T32A07TRGINAPHCK (Other timer outputs)	-	-	-
		T32A07TRGINAPCK (Internal trigger input)	***[TSEL1CR1]*** <INSEL7[2:0]> (Note1)	PB1 pin	TRGIN0
				PA3 pin	TRGIN1
				PN3 pin	TRGIN2
				ADC unit A General purpose trigger interrupt	INTADATRG
				ADC unit A Single conversion interrupt	INTADASGL
				ADC unit A Continuous conversion interrupt	INTADACNT
				ADC unit A Monitor function interrupt 0	INTADACP0
				ADC unit A Monitor function interrupt 1	INTADACP1
	B	T32A07TRGINBPHCK (Other timer outputs)	T32A ch7 Timer A Output		T32A07OUTA
		T32A07TRGINBPCK (Internal trigger input)	***[TSEL1CR2]*** <INSEL8[2:0]> (Note1)	T32A ch7 Timer register A0 match trigger	T32A07TRGOUTCMPA0
				T32A ch7 Timer register A1 match trigger	T32A07TRGOUTCMPA1
				T32A ch7 Timer A overflow trigger	T32A07TRGOUTOFA
				T32A ch7 Timer A underflow trigger	T32A07TRGOUTUFA
	C	T32A07TRGINCPHCK (Other timer outputs)	T32A ch6 Timer C Output		T32A06OUTC
		T32A07TRGINCPCK (Internal trigger input)	***[TSEL1CR2]*** <INSEL9[2:0]> (Note1)	T32A ch6 Timer register C0 match trigger	T32A06TRGOUTCMPC0
				T32A ch6 Timer register C1 match trigger	T32A06TRGOUTCMPC1
				T32A ch6 Timer C overflow trigger	T32A06TRGOUTOFC
				T32A ch6 Timer C underflow trigger	T32A06TRGOUTUFC

Note1: ***[TSEL1CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2: There is no TSPI channel 4 in M3HN / M3HM /M3HL.

2.14.4.2. Synchronous control connection specification

The timer synchronous connection specification of a 32-bit Timer Event Counter is shown in the following tables.

Table 2.67 T32A Synchronous control connection specification (1/2)

Master				Slave			
channel	Timer	Function (Output)	Signal name	channel	Timer	Function (input)	Signal name
ch0	A	Trigger output for synchronous start A	T32A00SYNCSTARTOUTA	ch0	B	Synchronous start at trigger input B	T32A00SYNCSTARTB
				ch1	A	Synchronous start at trigger input A	T32A01SYNCSTARTA
					B	Synchronous start at trigger input B	T32A01SYNCSTARTB
		Trigger output for synchronous stop A	T32A00SYNCSTOPOUTA	ch0	B	Synchronous stop at trigger input B	T32A00SYNCSTOPB
				ch1	A	Synchronous stop at trigger input A	T32A01SYNCSTOPA
					B	Synchronous stop at trigger input B	T32A01SYNCSTOPB
		Trigger output for synchronous reload A	T32A00SYNCRELOADOUTA	ch0	B	Synchronous reload at trigger input B	T32A00SYNCRELOADB
				ch1	A	Synchronous reload at trigger input A	T32A01SYNCRELOADA
					B	Synchronous reload at trigger input B	T32A01SYNCRELOADB
	C	Trigger output for synchronous start C	T32A00SYNCSTARTOUTC	ch1	C	Synchronous start at trigger input C	T32A01SYNCSTARTC
		Trigger output for synchronous stop C	T32A00SYNCSTOPOUTC			Synchronous stop at trigger input C	T32A01SYNCSTOPC
		Trigger output for synchronous reload C	T32A00SYNCRELOADOUTC			Synchronous reload at trigger input C	T32A01SYNCRELOADC
ch2	A	Trigger output for synchronous start A	T32A02SYNCSTARTOUTA	ch2	B	Synchronous start at trigger input B	T32A02SYNCSTARTB
				ch3	A	Synchronous start at trigger input A	T32A03SYNCSTARTA
					B	Synchronous start at trigger input B	T32A03SYNCSTARTB
		Trigger output for synchronous stop A	T32A02SYNCSTOPOUTA	ch2	B	Synchronous stop at trigger input B	T32A02SYNCSTOPB
				ch3	A	Synchronous stop at trigger input A	T32A03SYNCSTOPA
					B	Synchronous stop at trigger input B	T32A03SYNCSTOPB
		Trigger output for synchronous reload A	T32A02SYNCRELOADOUTA	ch2	B	Synchronous reload at trigger input B	T32A02SYNCRELOADB
				ch3	A	Synchronous reload at trigger input A	T32A03SYNCRELOADA
					B	Synchronous reload at trigger input B	T32A03SYNCRELOADB
	C	Trigger output for synchronous start C	T32A02SYNCSTARTOUTC	ch3	C	Synchronous start at trigger input C	T32A03SYNCSTARTC
		Trigger output for synchronous stop C	T32A02SYNCSTOPOUTC			Synchronous stop at trigger input C	T32A03SYNCSTOPC
		Trigger output for synchronous reload C	T32A02SYNCRELOADOUTC			Synchronous reload at trigger input C	T32A03SYNCRELOADC

Table 2.68 T32A Synchronous control connection specification (2/2)

Master				Slave			
channel	Timer	Function (Output)	Signal name	channel	Timer	Function (input)	Signal name
ch4	A	Trigger output for synchronous start A	T32A04SYNCSTARTOUTA	ch4	B	Synchronous start at trigger input B	T32A04SYNCSTARTB
				ch5	A	Synchronous start at trigger input A	T32A05SYNCSTARTA
					B	Synchronous start at trigger input B	T32A05SYNCSTARTB
		Trigger output for synchronous stop A	T32A04SYNCSTOPOUTA	ch4	B	Synchronous stop at trigger input B	T32A04SYNCSTOPB
				ch5	A	Synchronous stop at trigger input A	T32A05SYNCSTOPA
					B	Synchronous stop at trigger input B	T32A05SYNCSTOPB
		Trigger output for synchronous reload A	T32A04SYNCRELOADOUTA	ch4	B	Synchronous reload at trigger input B	T32A04SYNCRELOADB
				ch5	A	Synchronous reload at trigger input A	T32A05SYNCRELOADA
					B	Synchronous reload at trigger input B	T32A05SYNCRELOADB
	C	Trigger output for synchronous start C	T32A04SYNCSTARTOUTC	ch5	C	Synchronous start at trigger input C	T32A05SYNCSTARTC
		Trigger output for synchronous stop C	T32A04SYNCSTOPOUTC			Synchronous stop at trigger input C	T32A05SYNCSTOPC
		Trigger output for synchronous reload C	T32A04SYNCRELOADOUTC			Synchronous reload at trigger input C	T32A05SYNCRELOADC
ch6	A	Trigger output for synchronous start A	T32A06SYNCSTARTOUTA	ch6	B	Synchronous start at trigger input B	T32A06SYNCSTARTB
				ch7	A	Synchronous start at trigger input A	T32A07SYNCSTARTA
					B	Synchronous start at trigger input B	T32A07SYNCSTARTB
		Trigger output for synchronous stop A	T32A06SYNCSTOPOUTA	ch6	B	Synchronous stop at trigger input B	T32A06SYNCSTOPB
				ch7	A	Synchronous stop at trigger input A	T32A07SYNCSTOPA
					B	Synchronous stop at trigger input B	T32A07SYNCSTOPB
		Trigger output for synchronous reload A	T32A06SYNCRELOADOUTA	ch6	B	Synchronous reload at trigger input B	T32A06SYNCRELOADB
				ch7	A	Synchronous reload at trigger input A	T32A07SYNCRELOADA
					B	Synchronous reload at trigger input B	T32A07SYNCRELOADB
	C	Trigger output for synchronous start C	T32A06SYNCSTARTOUTC	ch7	C	Synchronous start at trigger input C	T32A07SYNCSTARTC
		Trigger output for synchronous stop C	T32A06SYNCSTOPOUTC			Synchronous stop at trigger input C	T32A07SYNCSTOPC
		Trigger output for synchronous reload C	T32A06SYNCRELOADOUTC			Synchronous reload at trigger input C	T32A07SYNCRELOADC

2.14.5. Pulse count correspondence classified by product List

As the pulse count specification of a 32-bit Timer Event Counter is shown in the following table, correspondence changes with products.

Table 2.69 T32A Pulse count support list

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
T32A ch0	2-phase pulse count 1-phase pulse count				
T32A ch1	2-phase pulse count 1-phase pulse count				
T32A ch2	2-phase pulse count 1-phase pulse count				1-phase pulse count (T32A02INC0 only)
T32A ch3	2-phase pulse count 1-phase pulse count				
T32A ch4	2-phase pulse count 1-phase pulse count				
T32A ch5	2-phase pulse count 1-phase pulse count				
T32A ch6	2-phase pulse count 1-phase pulse count		1-phase pulse count (T32A06INC0 only)	-	-
T32A ch7	2-phase pulse count 1-phase pulse count		-	-	-

2.14.6. DMA request

The 32-bit Timer Event Counter has the DMA request shown in the following tables.

When there is mention of the register name in the trigger selector column of the table, please select a request to use with a trigger selector.

Table 2.70 T32A DMA request (1/3)

Channel	Request	Signal name	Trigger selector (Note2)	DMA request channel			
					Unit	Single Transmission	Burst Transmission
T32A ch0	T32A ch0 DMA request at match A1 register	T32A00DMAREQCMPA1	***[TSEL0CR0]*** <INSEL0[2:0]>	15	A	-	✓
	T32A ch0 DMA request at match C1 register	T32A00DMAREQCMPC1					
	T32A ch0 DMA request at match B1 register	T32A00DMAREQCMPB1	***[TSEL0CR0]*** <INSEL2[2:0]>	17	A	-	✓
	T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0	***[TSEL0CR1]*** <INSEL4[2:0]>	19	A	-	✓
	T32A ch0 DMA request at capture A1 register	T32A00DMAREQCAPA1					
	T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0					
	T32A ch0 DMA request at capture C1 register	T32A00DMAREQCAPC1					
	T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0	***[TSEL0CR1]*** <INSEL6[2:0]>	21	A	-	✓
	T32A ch0 DMA request at capture B1 register	T32A00DMAREQCAPB1					
T32A ch1	T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR0]*** <INSEL0[2:0]>	15	A	-	✓
	T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1					
	T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1	***[TSEL0CR0]*** <INSEL2[2:0]>	17	A	-	✓
	T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0	***[TSEL0CR1]*** <INSEL4[2:0]>	19	A	-	✓
	T32A ch1 DMA request at capture A1 register	T32A01DMAREQCAPA1					
	T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0					
	T32A ch1 DMA request at capture C1 register	T32A01DMAREQCAPC1					
	T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0	***[TSEL0CR1]*** <INSEL6[2:0]>	21	A	-	✓
	T32A ch1 DMA request at capture B1 register	T32A01DMAREQCAPB1					

Note1: ✓: Available, -: N/A

Note2: ***[TSEL0CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Table 2.71 T32A DMA request (2/2)

Channel	Request	Signal name	Trigger selector (Note2)	DMA request channel			
					Unit	Single Transmission	Burst Transmission
T32A ch2	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1	***[TSEL0CR0]*** <INSEL1[2:0]>	16	A	-	✓
	T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1					
	T32A ch2 DMA request at match B1 register	T32A02DMAREQCMPB1	***[TSEL0CR0]*** <INSEL3[2:0]> (Note)	18	A	-	✓
	T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0	***[TSEL0CR1]*** <INSEL5[2:0]>	20	A	-	✓
	T32A ch2 DMA request at capture A1 register	T32A02DMAREQCAPA1					
	T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0					
	T32A ch2 DMA request at capture C1 register	T32A02DMAREQCAPC1					
	T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0	***[TSEL0CR1]*** <INSEL7[2:0]>	22	A	-	✓
	T32A ch2 DMA request at capture B1 register	T32A02DMAREQCAPB1					
T32A ch3	T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1	***[TSEL0CR0]*** <INSEL1[2:0]>	16	A	-	✓
	T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1					
	T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1	***[TSEL0CR0]*** <INSEL3[2:0]>	18	A	-	✓
	T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0	***[TSEL0CR1]*** <INSEL5[2:0]>	20	A	-	✓
	T32A ch3 DMA request at capture A1 register	T32A03DMAREQCAPA1					
	T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0					
	T32A ch3 DMA request at capture C1 register	T32A03DMAREQCAPC1					
	T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0	***[TSEL0CR1]*** <INSEL7[2:0]>	22	A	-	✓
	T32A ch3 DMA request at capture B1 register	T32A03DMAREQCAPB1					
T32A ch4	T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1	***[TSEL0CR5]*** <INSEL20[2:0]>	15	B	-	✓
	T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1					
	T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1	***[TSEL0CR5]*** <INSEL22[2:0]>	17	B	-	✓
	T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0	***[TSEL0CR6]*** <INSEL24[2:0]>	19	B	-	✓
	T32A ch4 DMA request at capture A1 register	T32A04DMAREQCAPA1					
	T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0					
	T32A ch4 DMA request at capture C1 register	T32A04DMAREQCAPC1					
	T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0	***[TSEL0CR6]*** <INSEL26[2:0]>	21	B	-	✓
	T32A ch4 DMA request at capture B1 register	T32A04DMAREQCAPB1					

Note1: ✓: Available, -: N/A

Note2: ***[TSEL0CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Table 2.72 T32A DMA request (3/3)

Channel	Request	Signal name	Trigger selector (Note2)	DMA request channel			
					Unit	Single Transmission	Burst Transmission
T32A ch5	T32A ch5 DMA request at match A1 register	T32A05DMAREQCMPA1	***[TSEL0CR5]*** <INSEL20[2:0]>	15	B	-	✓
	T32A ch5 DMA request at match C1 register	T32A05DMAREQCMPC1					
	T32A ch5 DMA request at match B1 register	T32A05DMAREQCMPB1	***[TSEL0CR5]*** <INSEL22[2:0]>	17	B	-	✓
	T32A ch5 DMA request at capture A0 register	T32A05DMAREQCAPA0	***[TSEL0CR6]*** <INSEL24[2:0]>	19	B	-	✓
	T32A ch5 DMA request at capture A1 register	T32A05DMAREQCAPA1					
	T32A ch5 DMA request at capture C0 register	T32A05DMAREQCAPC0					
	T32A ch5 DMA request at capture C1 register	T32A05DMAREQCAPC1					
	T32A ch5 DMA request at capture B0 register	T32A05DMAREQCAPB0	***[TSEL0CR6]*** <INSEL26[2:0]>	21	B	-	✓
	T32A ch5 DMA request at capture B1 register	T32A05DMAREQCAPB1					
T32A ch6	T32A ch6 DMA request at match A1 register	T32A06DMAREQCMPA1	***[TSEL0CR5]*** <INSEL21[2:0]>	16	B	-	✓
	T32A ch6 DMA request at match C1 register	T32A06DMAREQCMPC1					
	T32A ch6 DMA request at match B1 register	T32A06DMAREQCMPB1	***[TSEL0CR5]*** <INSEL23[2:0]>	18	B	-	✓
	T32A ch6 DMA request at capture A0 register	T32A06DMAREQCAPA0	***[TSEL0CR6]*** <INSEL25[2:0]>	20	B	-	✓
	T32A ch6 DMA request at capture A1 register	T32A06DMAREQCAPA1					
	T32A ch6 DMA request at capture C0 register	T32A06DMAREQCAPC0					
	T32A ch6 DMA request at capture C1 register	T32A06DMAREQCAPC1					
	T32A ch6 DMA request at capture B0 register	T32A06DMAREQCAPB0	***[TSEL0CR6]*** <INSEL27[2:0]>	22	B	-	✓
	T32A ch6 DMA request at capture B1 register	T32A06DMAREQCAPB1					
T32A ch7	T32A ch7 DMA request at match A1 register	T32A07DMAREQCMPA1	***[TSEL0CR5]*** <INSEL21[2:0]>	16	B	-	✓
	T32A ch7 DMA request at match C1 register	T32A07DMAREQCMPC1					
	T32A ch7 DMA request at match B1 register	T32A07DMAREQCMPB1	***[TSEL0CR5]*** <INSEL23[2:0]>	18	B	-	✓
	T32A ch7 DMA request at capture A0 register	T32A07DMAREQCAPA0	***[TSEL0CR6]*** <INSEL25[2:0]>	20	B	-	✓
	T32A ch7 DMA request at capture A1 register	T32A07DMAREQCAPA1					
	T32A ch7 DMA request at capture C0 register	T32A07DMAREQCAPC0					
	T32A ch7 DMA request at capture C1 register	T32A07DMAREQCAPC1					
	T32A ch7 DMA request at capture B0 register	T32A07DMAREQCAPB0	***[TSEL0CR6]*** <INSEL27[2:0]>	22	B	-	✓
	T32A ch7 DMA request at capture B1 register	T32A07DMAREQCAPB1					

Note1: ✓: Available, -: N/A

Note2: ***[TSEL0CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

2.14.7. Non corresponding interruption

Every count interrupt (INTT32AxEVRYC) does not correspond in the TMPM3H group (2).

2.15. Real Time Clock (RTC)

2.15.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.73 RTC Built-in List

Product	Built-in RTC (✓: Available, -: N/A)
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.15.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.74 RTC Functional pin and a port

Functional pin (Signal name)		Port	Product table (✓: Available, -: N/A)				
			M3HQ	M3HP	M3HN	M3HM	M3HL
RTCOUT	Output	PC2	✓	✓	✓	✓	–

Note: TMPM3H group (2) does not have an ALARM_N pin.

2.15.3. RTC count clock

The clock which shows the clock count clock of a Real Time Clock in the following table is used.

Table 2.75 RTC Count clock

Count clock
fs

2.16. Asynchronous Serial Communication Circuit (UART)

2.16.1. Built-in channel

The built-in channel for every product is shown in the following table.

The maximum UART communication speed for M3H Group (2) products is 2.5Mbps.

Table 2.76 UART Built-in channel

Product	UART Built-in channel (✓: Available, -: N/A)					
	ch0	ch1	ch2	ch3	ch4	ch5
M3HQ	✓	✓	✓	✓	✓	✓
M3HP	✓	✓	✓	✓	✓	✓
M3HN	✓	✓	✓	✓	✓	✓
M3HM	✓	✓	✓	✓	✓	✓
M3HL	✓	✓	✓	✓	✓	✓

2.16.2. Functional pin and port

The functional pin is assigned to the port of the following table.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.77 UART Functional pin signal and a port

Channel	Functional pin (Signal name)		Port	Product table(✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
UART ch0	UT0TXDA	Output	PA1 / PA2 / PM1 / PM2	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/-/-
	UT0TXDB	Output	PA0 / PM0	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
	UT0RXD	Input	PA2 / PA1 / PM2 / PM1	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/-/-
	UT0CTS_N	Input	PM3 / PM4	✓/✓	✓/✓	✓/✓	- /-	-/-
	UT0RTS_N	Output	PM4 / PM3	✓/✓	✓/✓	✓/✓	- /-	-/-
UART ch1	UT1TXDA	Output	PJ1 / PJ2 / PK1 / PK2	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓
	UT1TXDB	Output	PJ0 / PK0	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
	UT1RXD	Input	PJ2 / PJ1 / PK2 / PK1	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓
	UT1CTS_N	Input	PJ3 / PJ4 / PK3 / PK4	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓
	UT1RTS_N	Output	PJ4 / PJ3 / PK4 / PK3	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓
UART ch2	UT2TXDA	Output	PB2 / PB3 / PL0 / PL1	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓
	UT2TXDB	Output	-	-	-	-	-	-
	UT2RXD	Input	PB3 / PB2 / PL1 / PL0	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓
	UT2CTS_N	Input	PB4 / PB5 / PL2 / PL3	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/- /✓/✓	-/-/✓/✓
	UT2RTS_N	Output	PB5 / PB4 / PL3 / PL2	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/✓/✓	-/-/✓/✓
UART ch3	UT3TXDA	Output	PA7/ PA6 / PG3 / PG2	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/- /-	✓/✓/- /-	✓/✓/-/-
	UT3TXDB	Output	PG4	✓	✓	-	-	-
	UT3RXD	Input	PA6/ PA7 / PG2 / PG3	✓/✓/✓/✓	✓/✓/✓/✓	✓/✓/- /-	✓/✓/- /-	✓/✓/-/-
	UT3CTS_N	Input	-	-	-	-	-	-
	UT3RTS_N	Output	-	-	-	-	-	-
UART ch4	UT4TXDA	Output	PC3 / PC4 / PV6 / PV7	✓/✓/✓/✓	✓/✓/-/-	✓/✓/- /-	✓/✓/- /-	✓/✓/-/-
	UT4TXDB	Output	PC2 / PV5	✓/✓	✓/-	✓/-	✓/-	-/-
	UT4RXD	Input	PC4 / PC3 / PV7/ PV6	✓/✓/✓/✓	✓/✓/-/-	✓/✓/- /-	✓/✓/- /-	✓/✓/-/-
	UT4CTS_N	Input	PC5/ PC6	✓/✓	✓/✓	✓/✓	✓/✓	-/-
	UT4RTS_N	Output	PC6 / PC5	✓/✓	✓/✓	✓/✓	✓/✓	-/-
UART ch5	UT5TXDA	Output	PN3/PN2	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
	UT5TXDB	Output	PN4	✓	✓	✓	✓	✓
	UT5RXD	Input	PN2 / PN3	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
	UT5CTS_N	Input	PN1 / PN0	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	UT5RTS_N	Output	PN0 / PN1	✓/✓	✓/✓	✓/✓	✓/✓	-/✓

2.16.3. Half clock mode list for each product

The asynchronous serial communication circuit has no half clock mode depending on the product as shown in the table below.

Table 2.78 UART Half clock mode adaptive list

Channel	Product table (✓: Available, -: N/A)				
	M3HQ	M3HP	M3HN	M3HM	M3HL
UART ch0	✓	✓	✓	✓	✓
UART ch1	✓	✓	✓	✓	✓
UART ch2	-	-	-	-	-
UART ch3	✓	✓	-	-	-
UART ch4	✓	✓	✓	✓	-
UART ch5	✓	✓	✓	✓	✓

2.16.4. Clock for prescaler

The clock which an asynchronous serial communication circuit shows in the following table for prescaler is used.

Table 2.79 UART Clock for prescaler

Clock for prescaler
ΦT0

2.16.5. DMA request

An asynchronous serial communication circuit has the DMA request shown in the following table.

"-" in a table does not have an applicable function.

Table 2.80 UART DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel			
					Unit	Single Transmission	Burst Transmission
UART ch0	UART ch0 Reception DMA request	UART0RX_DMAREQ	-	6	A	✓	✓
	UART ch0 Transmission DMA request	UART0TX_DMAREQ		7	A	✓	✓
UART ch1	UART ch1 Reception DMA request	UART1RX_DMAREQ	-	8	A	✓	✓
	UART ch1 Transmission DMA request	UART1TX_DMAREQ		9	A	✓	✓
UART ch2	UART ch2 Reception DMA request	UART2RX_DMAREQ	-	10	A	✓	✓
	UART ch2 Transmission DMA request	UART2TX_DMAREQ		11	A	✓	✓
UART ch3	UART ch3 Reception DMA request	UART3RX_DMAREQ	-	12	A	✓	✓
	UART ch3 Transmission DMA request	UART3TX_DMAREQ		13	A	✓	✓
UART ch4	UART ch4 Reception DMA request	UART4RX_DMAREQ	-	10	B	✓	✓
	UART ch4Transmission DMA request	UART4TX_DMAREQ		11	B	✓	✓
UART ch5	UART ch5 Reception DMA request	UART5RX_DMAREQ	-	12	B	✓	✓
	UART ch5 Transmission DMA request	UART5TX_DMAREQ		13	B	✓	✓

Note: ✓: Available, -: N/A

2.16.6. Internal signal connection specification

2.16.6.1. Trigger transmission signal connection specification

An asynchronous serial communication circuit has a transmitting function by a trigger signal.

A trigger signal selects and uses the trigger source shown in the following table by a trigger selector.

Table 2.81 UART Trigger transmission signal connection specification

Channel		Trigger source		
	Signal name	Trigger selector (Note)	Trigger selector	Signal name
UART ch0	UART0TRGIN (Input)	***[TSEL0CR11]*** <INSEL44[2:0]>	PB1 pin	TRGIN0
			PA3 Pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register C1 match trigger	T32A06TRGOUTCMPC1
UART ch1	UART1TRGIN (Input)	***[TSEL0CR11]*** <INSEL45[2:0]>	PB1 pin	TRGIN0
			PA3 Pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register C1 match trigger	T32A06TRGOUTCMPC1
UART ch2	UART2TRGIN (Input)	***[TSEL0CR11]*** <INSEL46[2:0]>	PB1 pin	TRGIN0
			PA3 Pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register C1 match trigger	T32A06TRGOUTCMPC1
UART ch3	UART3TRGIN (Input)	***[TSEL0CR11]*** <INSEL47[2:0]>	PB1 pin	TRGIN0
			PA3 Pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register C1 match trigger	T32A06TRGOUTCMPC1
UART ch4	UART4TRGIN (Input)	***[TSEL0CR12]*** <INSEL48[2:0]>	PB1 pin	TRGIN0
			PA3 Pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register C1 match trigger	T32A06TRGOUTCMPC1
UART ch5	UART5TRGIN (Input)	***[TSEL0CR12]*** <INSEL49[2:0]>	PB1 pin	TRGIN0
			PA3 Pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register C1 match trigger	T32A06TRGOUTCMPC1

Note: ***[TSEL0CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

2.16.6.2. T32A connection

In addition to this, the asynchronous serial communication circuit is connected with the peripheral function inside, as shown in the following table.

Table 2.82 UART Internal connection specification: Output

Input/ output	Functional Output		Trigger selector (Note)	Destination		
		Signal name		Peripheral function		Signal name
Output	UART ch0 Transmission completion trigger	UART0TXTRG	***[TSEL0CR12]*** <INSEL50[2:0]>	T32A	Timer A ch0	T32A00TRGINAPCK
	UART ch0 Reception completion trigger	UART0RXTRG				
	UART ch1 Transmission completion trigger	UART1TXTRG	***[TSEL0CR13]*** <INSEL53[2:0]>	T32A	Timer A ch1	T32A01TRGINAPCK
	UART ch1 Reception completion trigger	UART1RXTRG				
	UART ch2 Transmission completion trigger	UART2TXTRG	***[TSEL0CR14]*** <INSEL56[2:0]>	T32A	Timer A ch2	T32A02TRGINAPCK
	UART ch2 Reception completion trigger	UART2RXTRG				
	UART ch3 Transmission completion trigger	UART3TXTRG	***[TSEL0CR14]*** <INSEL59[2:0]>	T32A	Timer A ch3	T32A03TRGINAPCK
	UART ch3 Reception completion trigger	UART3RXTRG				
	UART ch4 Transmission completion trigger	UART4TXTRG	***[TSEL0CR15]*** <INSEL62[2:0]>	T32A	Timer A ch4	T32A04TRGINAPCK
	UART ch4 Reception completion trigger	UART4RXTRG				
	UART ch5 Transmission completion trigger	UART5TXTRG	***[TSEL1CR0]*** <INSEL1[2:0]>	T32A	Timer A ch5	T32A05TRGINAPCK
	UART ch5 Reception completion trigger	UART5RXTRG				

Note: ***[TSELxCRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

2.17. I²C interface (I²C)

2.17.1. Built-in channel

The built-in channel for each product is shown in the following table.

The I²C interface in M3H Group (2) products supports standard mode and fast mode.

Table 2.83 I²C interface Built-in channel

Product	I²C Built-in channel (✓: Available, -: N/A)			
	ch0	ch1	ch2	ch3
M3HQ	✓	✓	✓	✓
M3HP	✓	✓	✓	✓
M3HN	✓	✓	✓	-
M3HM	✓	✓	✓	-
M3HL	✓	-	✓	-

2.17.2. Functional pin and port

The functional pin is assigned to the port of the following table.

Table 2.84 I²C Functional pin and port

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
I²C ch0	I2C0SCL	Input/output	PC0	✓	✓	✓	✓	✓
	I2C0SDA	Input/output	PC1	✓	✓	✓	✓	✓
I²C ch1	I2C1SCL	Input/output	PA4	✓	✓	✓	✓	-
	I2C1SDA	Input/output	PA5	✓	✓	✓	✓	-
I²C ch2	I2C2SCL	Input/output	PL0	✓	✓	✓	✓	✓
	I2C2SDA	Input/output	PL1	✓	✓	✓	✓	✓
I²C ch3	I2C3SCL	Input/output	PT1	✓	✓	-	-	-
	I2C3SDA	Input/output	PT0	✓	✓	-	-	-

2.17.3. Clock for prescaler

The clock which an I²C interface shows in the following table for prescaler is used.

Table 2.85 I²C Clock for prescaler

Clock for prescaler
fsys

2.17.4. Address match wakeup function support

The address match wakeup function differs depending on the product as shown in the table below.

Table 2.86 I²C Wakeup function adaptive list

Channel	Product table (✓: Available, -: N/A)				
	M3HQ	M3HP	M3HN	M3HM	M3HL
I²C ch0	✓	✓	✓	✓	✓
I²C ch1	-	-	-	-	-
I²C ch2	-	-	-	-	-
I²C ch3	-	-	-	-	-

2.17.5. Filter

Filter built-in is shown in the table below. Address match wakeup function(I2CS) of channel 0 use analog filter.

Table 2.87 I²C Interface Filter

Channel		Filter Type
I²C ch0		Digital
	I2CS	Analog
I²C ch1		Digital
I²C ch2		Digital
I²C ch3		Digital

2.17.6. DMA request

The I²C interface has the DMA request shown in the following table.

Table 2.88 I²C DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel			
					Unit	Single Transmission	Burst Transmission
I²C ch0	I²C ch0 Receiving DMA request	I2C0RXDMAREQ	-	4	A	-	✓
	I²C ch0 Transmitting DMA request	I2C0TXDMAREQ		5	A	-	✓
I²C ch1 (Note2)	I²C ch1 Receiving DMA request	I2C1RXDMAREQ	-	6	B	-	✓
	I²C ch1 Transmitting DMA request	I2C1TXDMAREQ		7	B	-	✓
I2C ch2	I²C ch2 Receiving DMA request	I2C2RXDMAREQ	-	8	B	-	✓
	I²C ch2 Transmitting DMA request	I2C2TXDMAREQ		9	B	-	✓
I²C ch3 (Note3)	I²C ch3 Receiving DMA request	I2C3RXDMAREQ	***[TSEL0CR4]*** <INSEL17[2:0]> (Note1)	0	B	-	✓
	I²C ch3 Transmitting DMA request	I2C3TXDMAREQ	***[TSEL0CR4]*** <INSEL18[2:0]> (Note1)	1	B	-	✓

Note1: ***[TSEL0CR4]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2: There is not I²C ch 1 in M3HL.

Note3: There is no I²C ch 3 in M3HN / M3HM / M3HL.

Note4: ✓: Available, -: N/A

2.18. Serial Peripheral Interface (TSPI)

2.18.1. Built-in channel

The built-in channel for each product is shown in the following table.

M3H group (2) Maximum transfer clock of TSPI is 20 MHz. The maximum value varies depending on the channel, refer to the electrical characteristics of the data sheet.

Table 2.89 TSPI Built-in channel

Product	TSPI Built-in channel (✓: Available, -: N/A)				
	ch0	ch1	ch2	ch3	ch4
M3HQ	✓	✓	✓	✓	✓
M3HP	✓	✓	✓	✓	✓
M3HN	✓	✓	✓	✓	-
M3HM	✓	✓	✓	✓	-
M3HL	✓	-	-	-	-

2.18.2. Functional pin and port

The functional pin is assigned to the port below.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.90 TSPI Functional pin and a port

Channel	Functional pin (signal name)		Port	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
TSPI ch0	TSPI0SCK	Input/output	PA0 / PM0	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
	TSPI0TXD	Output	PA1 / PM1	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	TSPI0RXD	Input	PA2 / PM2	✓/✓	✓/✓	✓/✓	✓/✓	✓/-
	TSPI0CSIN	Input	PA3 / PM3	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	TSPI0CS0	Output	PA3 / PM3	✓/✓	✓/✓	✓/✓	✓/-	✓/-
	TSPI0CS1	Output	PA4 / PM4	✓/✓	✓/✓	✓/✓	✓/-	-/-
TSPI ch1	TSPI1SCK	Input/output	PB2	✓	✓	✓	✓	-
	TSPI1TXD	Output	PB3	✓	✓	✓	✓	-
	TSPI1RXD	Input	PB4	✓	✓	✓	✓	-
	TSPI1CSIN	Input	PB5	✓	✓	✓	-	-
	TSPI1CS0	Output	PB5	✓	✓	✓	-	-
	TSPI1CS1	Output	PB6	✓	✓	✓	-	-
TSPI ch2	TSPI2SCK	Input/output	PP0 / PT2	✓/✓	✓/✓	✓/-	✓/-	-/-
	TSPI2TXD	Output	PP1 / PT3	✓/✓	✓/✓	✓/-	✓/-	-/-
	TSPI2RXD	Input	PP2 / PT4	✓/✓	✓/-	✓/-	✓/-	-/-
	TSPI2CSIN	Input	PT1	✓	✓	-	-	-
	TSPI2CS0	Output	PT1	✓	✓	-	-	-
	TSPI2CS1	Output	PT0	✓	✓	-	-	-
TSPI ch3	TSPI3SCK	Input/output	PP5	✓	✓	✓	✓	-
	TSPI3TXD	Output	PP4	✓	✓	✓	✓	-
	TSPI3RXD	Input	PP3	✓	✓	✓	✓	-
	TSPI3CSIN	Input	PT6	✓	✓	✓	✓	-
	TSPI3CS0	Output	PT6	✓	✓	✓	✓	-
	TSPI3CS1	Output	PT7	✓	✓	✓	-	-
TSPI ch4	TSPI4SCK	Input/output	PH4	✓	✓	-	-	-
	TSPI4TXD	Output	PH5	✓	✓	-	-	-
	TSPI4RXD	Input	PH6	✓	✓	-	-	-

2.18.3. Transfer mode list for each product

The serial peripheral interface has different transfer modes that can be used depending on the product as shown in the following table.

Table 2.91 TSPI Mode support list

Channel	Mode support				
	M3HQ	M3HP	M3HN	M3HM	M3HL
TSPI ch0	SPI mode SIO mode				
TSPI ch1	SPI mode SIO mode			SIO mode	-
TSPI ch2	SPI mode SIO mode		SIO mode		-
TSPI ch3	SPI mode SIO mode				-
TSPI ch4	SIO mode		-		

2.18.4. Clock

The clock which a serial peripheral interface shows in the following table for clock is used.

Table 2.92 TSPI Clock

Operation clock	Clock for prescaler
fsys	ΦT0

2.18.5. DMA request

A serial peripheral interface has the DMA request shown in the following table.

Table 2.93 TSPI DMA request

Channel	Request	Signal name	Trigger selector	DMA request channel			
					UNIT	Single Transmission	Burst Transmission
TSPI ch0	TSPI ch0 Receive DMA request	TSPI0RX_DMA	-	0	A	✓	✓
	TSPI ch0 Transmit DMA request	TSPI0TX_DMA		1	A	✓	✓
TSPI ch1 (Note2)	TSPI ch1 Receive DMA request	TSPI1RX_DMA	-	2	A	✓	✓
	TSPI ch1 Transmit DMA request	TSPI1TX_DMA		3	A	✓	✓
TSPI ch2 (Note2)	TSPI ch2 Receive DMA request	TSPI2RX_DMA	***[TSEL0CR4]*** <INSEL17[2:0]> (Note1)	0	B	✓	✓
	TSPI ch2 Transmit DMA request	TSPI2TX_DMA	***[TSEL0CR4]*** <INSEL18[2:0]> (Note1)	1	B	✓	✓
TSPI ch3 (Note2)	TSPI ch3 Receive DMA request	TSPI3RX_DMA	-	2	B	✓	✓
	TSPI ch3 Transmit DMA request	TSPI3TX_DMA		3	B	✓	✓
TSPI ch4 (Note3)	TSPI ch4 Receive DMA request	TSPI4RX_DMA	-	4	B	✓	✓
	TSPI ch4 Transmit DMA request	TSPI4TX_DMA		5	B	✓	✓

Note1: ***[TSEL0CR4]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2 There is no TSPI ch 1, ch 2, and ch 3 in M3HL

Note3 There is no TSPI ch 4 in M3HN / M3HM /M3HL

Note4 ✓: Available, -: N/A

2.18.6. Internal signal connection specification

A serial peripheral interface has a transmitting function by a trigger signal.

A trigger signal selects and uses the trigger source shown in the following table by a trigger selector.

2.18.6.1. Trigger transmitting signal connection specification

Table 2.94 TSPI Trigger transmission specification

Channel	Signal name	Trigger source		
		Trigger selector (Note1)	Input trigger signal	Signal name
TSPI ch0	TSPI0TRG (Input)	***[TSEL0CR9]*** <INSEL39[2:0]>	PB1 pin	TRGIN0
			PA3 pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPC1
TSPI ch1 (Note2)	TSPI1TRG (Input)	***[TSEL0CR10]*** <INSEL40[2:0]>	PB1 pin	TRGIN0
			PA3 pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPC1
TSPI ch2 (Note2)	TSPI2TRG (Input)	***[TSEL0CR10]*** <INSEL41[2:0]>	PB1 pin	TRGIN0
			PA3 pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPC1
TSPI ch3 (Note2)	TSPI3TRG (Input)	***[TSEL0CR10]*** <INSEL42[2:0]>	PB1 pin	TRGIN0
			PA3 pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPC1
TSPI ch4 (Note3)	TSPI4TRG (Input)	***[TSEL0CR10]*** <INSEL43[2:0]>	PB1 pin	TRGIN0
			PA3 pin	TRGIN1
			PN3 pin	TRGIN2
			T32A ch6 Timer register A1 match trigger	T32A06TRGOUTCMPA1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPB1
			T32A ch6 Timer register B1 match trigger	T32A06TRGOUTCMPC1

Note1: ***[TSEL0CRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2: There is no TSPI ch 1, ch 2, and ch 3 in M3HL.

Note3: There is no TSPI ch 4 in M3HN / M3HM / M3HL.

2.18.6.2. T32A connection

In addition to this, the serial peripheral interface is connected with the peripheral function inside, as shown in the following table.

Table 2.95 TSPI Internal connection specification (Output)

Input/ output	Functional Output	Signal name	Trigger selector (Note1)	Peripheral function	Destination	Signal name
Output	TSPI ch0 Transmit Completion	TSPI0TXEND	***[TSEL0CR14]*** <INSEL56[2:0]>	T32A ch2	Timer A internal trigger input	T32A02TRGINAPCK
	TSPI ch0 Receive completion	TSPI0RXEND				
	TSPI ch1 Transmit Completion (Note2)	TSPI1TXEND	***[TSEL0CR14]*** <INSEL59[2:0]>	T32A ch3	Timer A internal trigger input	T32A03TRGINAPCK
	TSPI ch1 Receive Completion (Note2)	TSPI1RXEND				
	TSPI ch2 Transmit Completion (Note2)	TSPI2TXEND	***[TSEL0CR15]*** <INSEL61[2:0]>	T32A ch4	Timer A internal trigger input	T32A04TRGINAPCK
	TSPI ch2 receive completion (Note2)	TSPI2RXEND				
	TSPI ch3 Transmit Completion (Note2)	TSPI3TXEND	***[TSEL1CR0]*** <INSEL1[2:0]>	T32A ch5	Timer A internal trigger input	T32A05TRGINAPCK
	TSPI ch3 Receive Completion (Note2)	TSPI3RXEND				
	TSPI ch4 Transmit Completion (Note3)	TSPI4TXEND	***[TSEL1CR1]*** <INSEL4[2:0]>	T32A ch6	Timer A internal trigger input	T32A06TRGINAPCK
	TSPI ch4 Receive completion (Note3)	TSPI4RXEND				

Note1: ***[TSELxCRn]***<INSELm[2:0]> selects the trigger source of the start trigger via the trigger selector. For details on the connection destination, refer to "2.2. Trigger Selector (TRGSEL)".

Note2: There is no TSPI ch 1, ch 2, and ch 3 in M3HL.

Note3: There is no TSPI ch 4 in M3HN / M3HM / M3HL.

2.19. Remote Control Signal Preprocessor (RMC)

2.19.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.96 RMC Built-in channel

Product	RMC Built-in channel (✓: Available, -: N/A)
	ch0
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.19.2. Functional pin and port

The functional terminal is assigned to the following ports.

Table 2.97 RMC Functional pin and a port

Functional pin (Signal name)		Port	Product table (✓: Available, -: N/A)				
			M3HQ	M3HP	M3HN	M3HM	M3HL
RXIN0	Input	PB1	✓	✓	✓	✓	✓

2.19.3. Sampling clock

The remote control receiving circuit can select the sampling clock shown in the following table.

Table 2.98 RMC Sampling clock

Clock		Clock source	
	Signal name		Signal name
Low speed clock	fs	External Low speed oscillator	fs
Timer trigger for clock source	TB0OUT	T32A ch7 Timer A output	T32A07OUTA

Note: Please select the sampling clock by ***[RMC0FSSEL]*** <RMCCLK>.

2.20. Digital Noise Filter Circuit (DNF)

2.20.1. Built-in unit

The built-in unit for each product is shown in the following table.

Table 2.99 DNF Built-in unit

Product	DNF Built-in unit (✓: Available, -: N/A)	
	unit A	unit B
M3HQ	✓	✓
M3HP	✓	✓
M3HN	✓	✓
M3HM	✓	-
M3HL	✓	-

2.20.2. External interrupt pin and DNF

Digital noise filter circuits correspond to the following external interruption pins.

Table 2.100 External interruption pin and DNF correspondence

External interruption Pin (signal name)	Port	Unit	Setup Register name	Product table (✓: Available, -: N/A)				
				M3HQ	M3HP	M3HN	M3HM	M3HL
INT00	PC0	A	***[DNFAENCR]***<NFEN0>	✓	✓	✓	✓	✓
INT01	PC1		***[DNFAENCR]***<NFEN1>	✓	✓	✓	✓	✓
INT02	PC2		***[DNFAENCR]***<NFEN2>	✓	✓	✓	✓	-
INT03	PB1		***[DNFAENCR]***<NFEN3>	✓	✓	✓	✓	✓
INT04	PJ4		***[DNFAENCR]***<NFEN4>	✓	✓	✓	✓	✓
INT05	PK1		***[DNFAENCR]***<NFEN5>	✓	✓	✓	✓	✓
INT06	PH3		***[DNFAENCR]***<NFEN6>	✓	✓	✓	✓	✓
INT07	PA6		***[DNFAENCR]***<NFEN7>	✓	✓	✓	✓	✓
INT08	PL3		***[DNFAENCR]***<NFEN8>	✓	✓	✓	✓	✓
INT09	PM2		***[DNFAENCR]***<NFEN9>	✓	✓	✓	✓	-
INT10	PN3		***[DNFAENCR]***<NFEN10>	✓	✓	✓	✓	✓
INT11	PA7		***[DNFAENCR]***<NFEN11>	✓	✓	✓	✓	✓
INT12	PL4		***[DNFAENCR]***<NFEN12>	✓	✓	✓	✓	✓
INT13	PK7		***[DNFAENCR]***<NFEN13>	✓	✓	✓	✓	-
INT14	PP3		***[DNFAENCR]***<NFEN14>	✓	✓	✓	✓	✓
INT15	PM6		***[DNFAENCR]***<NFEN15>	✓	✓	✓	-	-
INT16	PB7	B	***[DNFBENCR]***<NFEN0>	✓	✓	✓	-	-
INT17	PV2		***[DNFBENCR]***<NFEN1>	✓	✓	✓	-	-
INT18	PV3		***[DNFBENCR]***<NFEN2>	✓	✓	✓	-	-
INT19	PH4		***[DNFBENCR]***<NFEN3>	✓	✓	-	-	-
INT20	PH5		***[DNFBENCR]***<NFEN4>	✓	✓	-	-	-
INT21	PH6		***[DNFBENCR]***<NFEN5>	✓	✓	-	-	-
INT22	PH7		***[DNFBENCR]***<NFEN6>	✓	✓	-	-	-
INT23	PT0		***[DNFBENCR]***<NFEN7>	✓	✓	-	-	-
INT24	PT1		***[DNFBENCR]***<NFEN8>	✓	✓	-	-	-
INT25	PT2		***[DNFBENCR]***<NFEN9>	✓	✓	-	-	-
INT26	PT3		***[DNFBENCR]***<NFEN10>	✓	✓	-	-	-
INT27	PG2		***[DNFBENCR]***<NFEN11>	✓	✓	-	-	-
INT28	PG3		***[DNFBENCR]***<NFEN12>	✓	✓	-	-	-
INT29	PT7		***[DNFBENCR]***<NFEN13>	✓	-	-	-	-
INT30	PU0		***[DNFBENCR]***<NFEN14>	✓	-	-	-	-
INT31	PU1		***[DNFBENCR]***<NFEN15>	✓	-	-	-	-

2.20.3. Sampling source clock

The clock in which the digital noise filter circuit is shown as a sauce clock of the sampling at following table is used.

Table 2.101 DNF Sampling source clock

Sampling source clock
fc

2.21. CRC calculation Circuit (CRC)

2.21.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.102 CRC Built-in channel

Product	CRC Built-in channel (✓: Available, -: N/A))
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.22. RAM Parity (RAMP)

2.22.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.103 RAM Parity Built-in channel

Product	RAMP Built-in channel (✓: Available, -: N/A)
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.22.2. Error judgment Block Area

Table 2.104 RAM area and address of RAM Parity

Register name	RAM area address	Product table (✓: Available, -: N/A)				
		M3HQ	M3HP	M3HN	M3HM	M3HL
[RPARST]<RPARFG3>	0x20010000-0x200107FF	✓	✓	✓	✓	✓
[RPARST]<RPARFG2>	0x20008000-0x2000FFFF	✓	✓	✓	✓	✓
[RPARST]<RPARFG1>	0x20004000-0x20007FFF	✓	✓	✓	✓	✓
[RPARST]<RPARFG0>	0x20000000-0x20003FFF	✓	✓	✓	✓	✓

2.23. Trimming Circuit (TRM)

2.23.1. Built-in List

The following table shows the built-in list for each product.

Table 2.105 TRM Built-in List

Product	Built-in TRM (✓: Available, -: N/A)
M3HQ	✓
M3HP	✓
M3HN	✓
M3HM	✓
M3HL	✓

2.23.2. Object oscillator

The object oscillator of a trimming circuit is an oscillator shown in the following table.

Table 2.106 TRM Trimming oscillator

Object oscillator	Oscillator name
Internal High Speed Oscillator 1	IHOSC1

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2017-10-19	First release
2.0	2017-11-15	-2.10.6.2.: Modified ”Functional Output” of Table 2.49 (INTADACP0/1) -2.14.4.2.: Corrected “Signal name” of Table 2.64,Table 2.65
3.0	2018-08-09	-added M3HL product information into the table of each section. -Related document added IP symbol, modified Document name of Flash Memory. -Revised "SST registered trademarks". -Terms and Abbreviation contents modified of "A-PMD" and "IHOSC". -2.1 Revised the sentence (TYPE1/TYPE2 → TYPE1/TYPE2/TYPE3) -2.2.1 table 2.10 contents modified (row of INSEL56 & INSEL59) table 2.11 contents modified (row of INSEL62) table 2.12 contents modified (row of INSEL1) table 2.13 contents modified (row of INSEL4) -2.2.2 Sentence (3) deleted the reference section. -2.2.4.15 contents modified of row of bit 30:28 & row of bit 6:4. Note added. -2,2,4,16 contents modified of row of bit 22:20. Note added. -2.2.4.17 contents modified of row of bit 14:12. -2.2.4.18 contents modified of row of bit 30:28, row of bit 22:20, row of bit 14:12 and row of bit 6:4. Note added. -2.2.4.19 contents modified of row of bit 14:12 and row of bit 6:4. -2.3.1 Added M3HL in Table 2.14 -2.4.1 added new section -2.4.2 contents modified of table 2.18. -2.5.1 modified port name of SWCLK/TCK,SWV/TDO,TDI,TRST_N in Table 2.20, added M3HL in Table 2.20. -2.6.2 added M3HL in Table 2.22 -2.6.3 added M3HL in Table 2.23 -2.6.4 deleted M3HNxDx and added M3HL in the Product name of Table 2.25 -2.7.1 added M3HL in Table 2.26 -2.7.2 Note1 added in Table 2.27 , Note2,3,4 modified.in Table 2.31, -2.8.1 added M3HL in Table 2.35 -2.8.2 added M3HL in Table 2.36 -2.8.4 contents modified in Table 2.38. -2.8.5 added new section(Additional setting of using PMD0DBG). -2.9.1 added M3HL in Table 2.41 -2.9.2 added M3HL in Table 2.42 -2.10.1 added M3HL in Table 2.45 -2.10.2 added M3HL in Table 2.46, deleted Note2, modified Note1 to Note -2.10.6.2 modified Destinaion in Table 2.51 -2.11.1 added M3HL in Table 2.52 -2.11.2 added M3HL in Table 2.53 -2.12.1 added new section as Built-in-List. added M3HL in Table 2.54 added M3HL in Table 2.55 -2.13.1 added new section as Built-in-List. added M3HL in Table 2.56 -2.14.1 added M3HL in Table 2.58 -2.14.2 added M3HL in Table 2.59 to Table 2.61 -2.14.4.1 modified the section title and the title of Table 2.63,Table 2.64. added Note2 in Table 2.64, modified the title of Table 2.65 and added Note2. modified the title of Table 2.66 and Note2. -2.14.4.2 modified T32A02SYNCSTARTC to T32A01SYNCSTARTC, T32A02SYNCSTOPC to T32A01SYNCSTOPC, T32A02SYNCRELOADC to T32A01SYNCRELOADC in Table 2.67 modified T32A04SYNCSTARTOUTA to T32A04SYNCRELOADOUTA, T32A06SYNCSTARTOUTA to T32A06SYNCRELOADOUTA in Table 2.68. -2.14.5. contents modified of ch6 ,column M3HN and added M3HL in Table 2.69 -2.14.6. added Note2 in Table 2.70, Table 2.71 and Table 2.72. -2.15.1. added M3HL in Table 2.73 -2.15.2. added M3HL in Table 2.74

		-2.16.1. added M3HL in Table 2.76 -2.16.2. added M3HL in Table 2.77 -2.16.3. added M3HL in Table 2.78, M3HN/M3HM (ch3/4) modified ✓ to "–" in Table 2.78 -2.16.6.2 contents modified of Table 2.82. -2.17.1 added M3HL in Table 2.83 -2.17.2 added M3HL in Table 2.84 -2.17.4 added M3HL in Table 2.86 -2.17.5 modified the section title and sentence, modified the contents in Table 2.87. -2.17.6 modified the contents in table 2.88, added the Note2. -2.18.1 modified the sentence. added M3HL in Table2.89 -2.18.2 added M3HL in Table 2.90 -2.18.3 added M3HL in Table 2.91 -2.18.5 modified the contents in Table 2.93, added the Note2, Note3. -2.18.6.1 modified the contents in Table 2.94, added the Note2. Note3. -2.18.6.2 modified the contents in Table 2.95, added the Note2, Note3. -2.19.1 added M3HL in Table 2.96 -2.19.2 added M3HL in Table 2.97 -2.20.1 added M3HL in Table 2.99 -2.20.2 added M3HL in Table 2.100 -2.21.1 added new section. added M3HL in Table 2.102 -2.22. added new section as "2.22.1" and "2.22.2", and then modified the contents in Table 2.103 and Table 2.104. -2.23.1 added new section as "Built-in List" and added M3HL in Table 2.105 -Revised "Restrictions On Product Use".
3.1	2018-10-29	-Related document modified "Comaprator" to "Comparator". -2.4.1 Table 2.17 modified "OFD built-in" to "Built-in OFD" -2.4.2 Table 2.18 modified "divide vaule" to "divide value". -2.7.2 Table 2.31 added M3HL to "Note3". -2.14.5 Table 2.69 modified "1-pahse" to "1-phase". -2.13.1 Table 2.56 modified "LVD built-in" to "Built-in LVD" -2.17.5 Table 2.87 modified the title "Intetface " to "Interface" -2.23.1 Table 2.105 modified "TRM Built-in channel" to "Built-in TRM"
3.2	2019-02-28	-2.17.4 Modified title -2.17.5 Modified wakeup to Address match wakeup Table 2.87 Added I2CS of ch0 - 2.18.4 Modified title Table 2.92 Added item of operation clock
3.3	2021-01-21	- Modified of Footer layout & Date of Copyright. - 2.16.2 Table 2.77 modified(UT4TXDA&UT4RXD of UART ch4 in M3HP, product table for All package of UART ch5) - 2.18.2 Table2.90 modified (Product table of TSPI0TXD in M3HL)

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