

MOSFETs Silicon N-Channel MOS

# SSM6N67NU

## 1. Applications

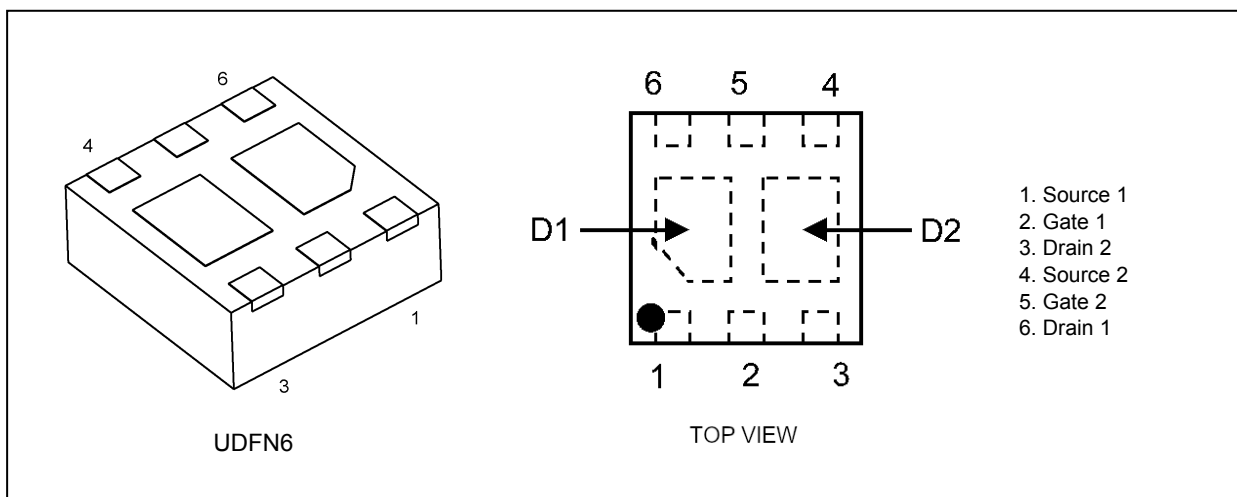
- Power Management Switches
- DC-DC Converters

## 2. Features

- (1) AEC-Q101 qualified (Note 1)
- (2) 1.8-V gate drive voltage.
- (3) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 39.1 \text{ m}\Omega$  (max) (@ $V_{GS} = 4.5 \text{ V}$ )
  - $R_{DS(ON)} = 53 \text{ m}\Omega$  (max) (@ $V_{GS} = 2.5 \text{ V}$ )
  - $R_{DS(ON)} = 82 \text{ m}\Omega$  (max) (@ $V_{GS} = 1.8 \text{ V}$ )

Note 1: For detail information, please contact our sales.

## 3. Packaging and Pin Assignment



Start of commercial production  
2018-03

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ ) (Q1,Q2 Common)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	30	V
Gate-source voltage	$V_{GSS}$	12/-8	
Drain current (DC) (Note 1)	$I_D$	4	A
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	10	
Power dissipation (Note 3)	$P_D$	1	W
Power dissipation ( $t \leq 10\text{ s}$ ) (Note 3)	$P_D$	2	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2: Pulse width (PW)  $\leq 10\text{ ms}$ , duty  $\leq 1\%$

Note 3: Device mounted on an FR-4 board.(total dissipation)  
( $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$  ,Cu pad:  $645\text{ mm}^2$ )

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-ambient thermal resistance (Note 1)	$R_{th(ch-a)}$	125	$^\circ\text{C/W}$

Note 1: Device mounted on an  $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$  FR4 glass epoxy board (Cu pad:  $645\text{ mm}^2$ )

### 6. Electrical Characteristics

#### 6.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )(Q1,Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DD} = 0\text{ V}, V_{GS} = 10/-8\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	—	—	1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = 1\text{ mA}, V_{GS} = -8\text{ V}$	18	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = 3\text{ V}, I_D = 1\text{ mA}$	0.40	—	1.00	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = 2.0\text{ A}, V_{GS} = 4.5\text{ V}$	—	30	39.1	$\text{m}\Omega$
		$I_D = 1.0\text{ A}, V_{GS} = 2.5\text{ V}$	—	37	53	
		$I_D = 0.5\text{ A}, V_{GS} = 1.8\text{ V}$	—	46	82	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 2.0\text{ A}$	6.0	12.0	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 6.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )(Q1,Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	310	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	20	—	
Output capacitance	$C_{oss}$		—	52	—	
Switching time (turn-on time) (Note 1)	$t_{on}$	$V_{DD} = 15\text{ V}, I_D = 1.0\text{ A},$	—	26	—	ns
Switching time (turn-off time) (Note 1)	$t_{off}$	$V_{GS} = 0\text{ to }2.5\text{ V}, R_{GS} = 4.7\text{ }\Omega$	—	17	—	

Note 1: See chapter 6.3

#### 6.3. Switching Time Test Circuit

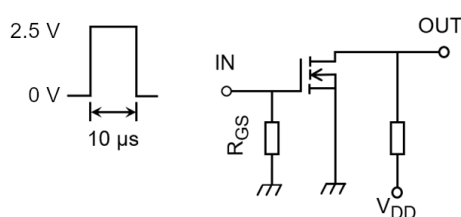


Fig. 6.3.1 Switching Time Test Circuit

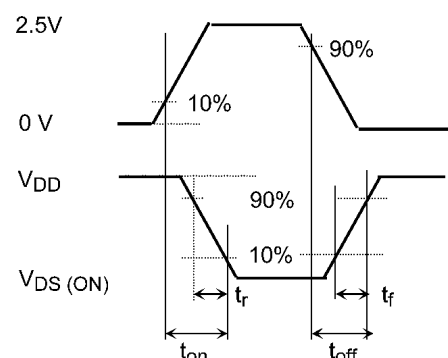


Fig. 6.3.2 Input Waveform/Output Waveform

### 6.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ ) (Q1,Q2 Common)

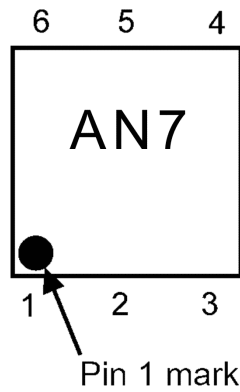
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = 15\text{ V}$ , $I_D = 4.0\text{ A}$ , $V_{GS} = 4.5\text{ V}$	—	3.2	—	nC
Gate-source charge 1	$Q_{gs1}$		—	0.5	—	
Gate-drain charge	$Q_{gd}$		—	0.7	—	

### 6.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ ) (Q1,Q2 Common)

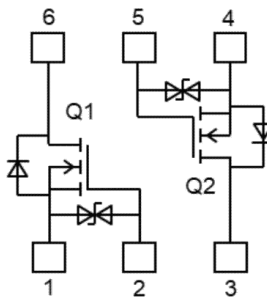
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_{DR} = 4.0\text{ A}$ , $V_{GS} = 0\text{ V}$	—	0.8	1.2	V

Note 1: Pulse measurement.

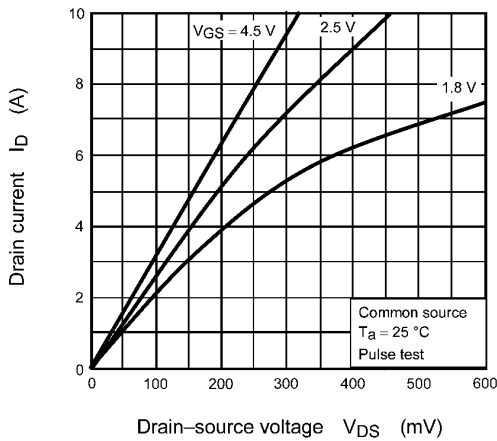
## 7. Marking



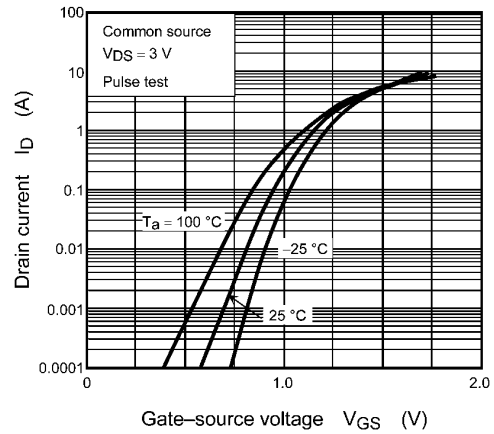
## 8. Internal Equivalent Circuit



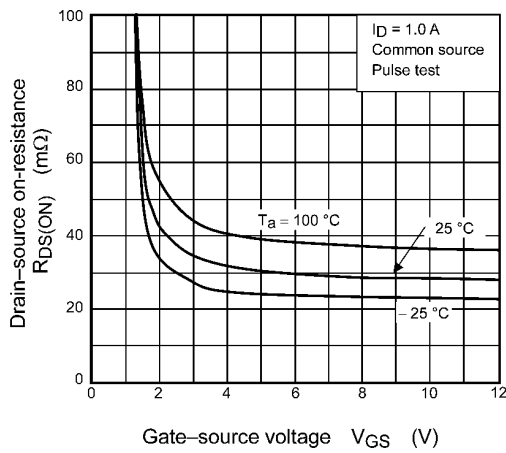
### 9. Characteristics Curves (Q1,Q2 Common) (Note)



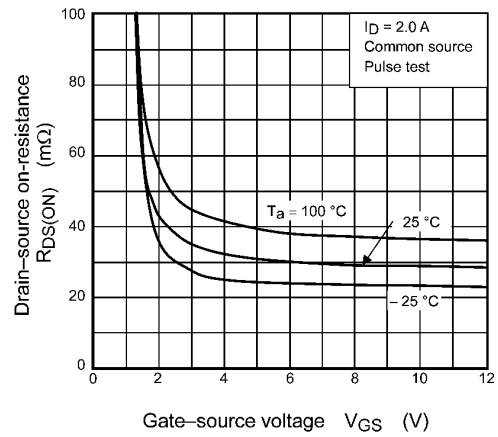
**Fig. 9.1**  $I_D - V_{DS}$



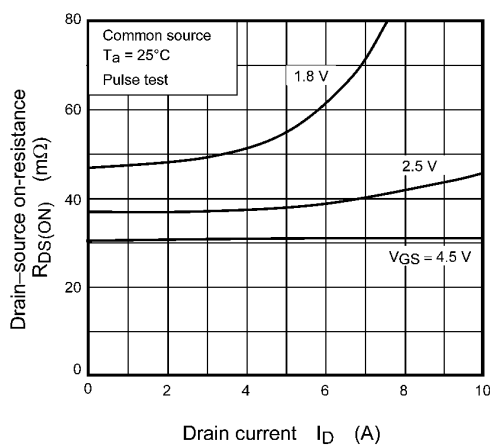
**Fig. 9.2**  $I_D - V_{GS}$



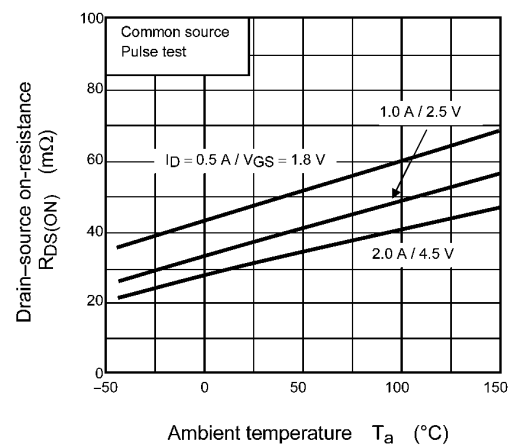
**Fig. 9.3**  $R_{DS(ON)} - V_{GS}$



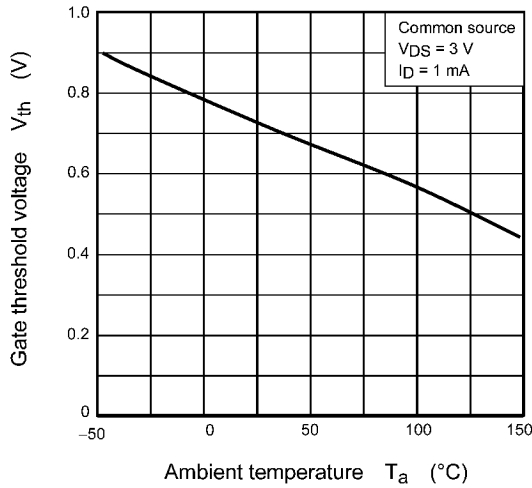
**Fig. 9.4**  $R_{DS(ON)} - V_{GS}$



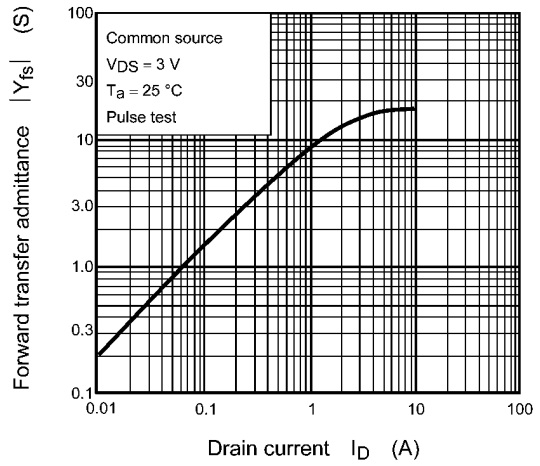
**Fig. 9.5**  $R_{DS(ON)} - I_D$



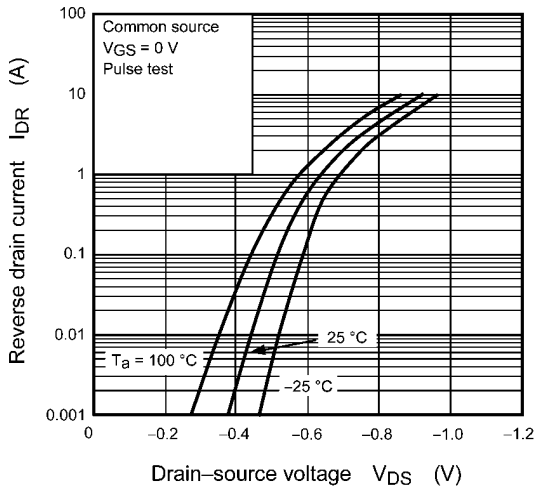
**Fig. 9.6**  $R_{DS(ON)} - T_a$



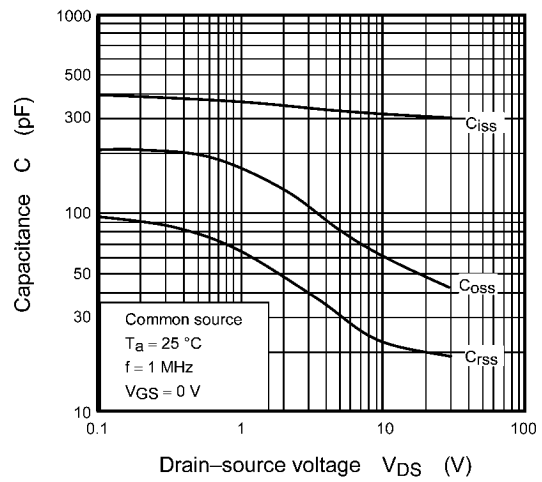
**Fig. 9.7  $V_{th} - T_a$**



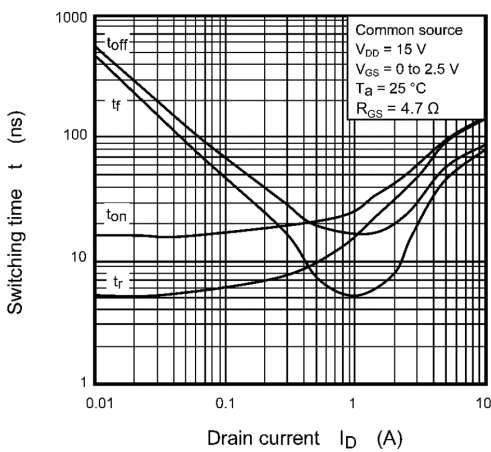
**Fig. 9.8  $|Y_{fs}| - I_D$**



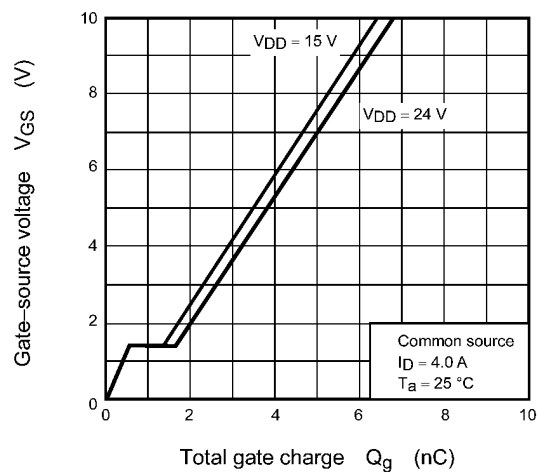
**Fig. 9.9  $I_{DR} - V_{DS}$**



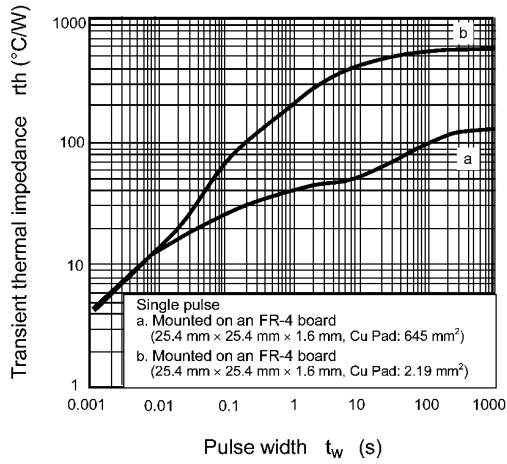
**Fig. 9.10  $C - V_{DS}$**



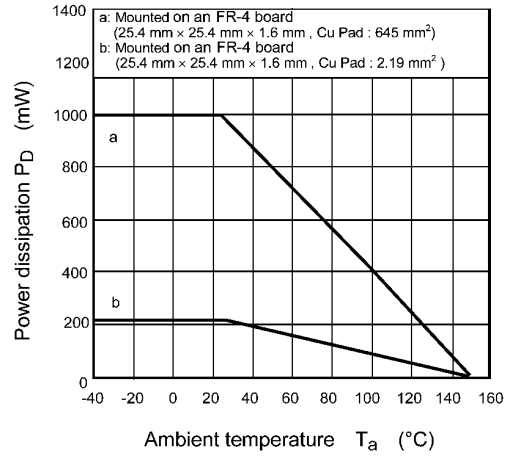
**Fig. 9.11  $t - I_D$**



**Fig. 9.12 Dynamic Input Characteristics**



**Fig. 9.13**  $r_{th} - t_w$

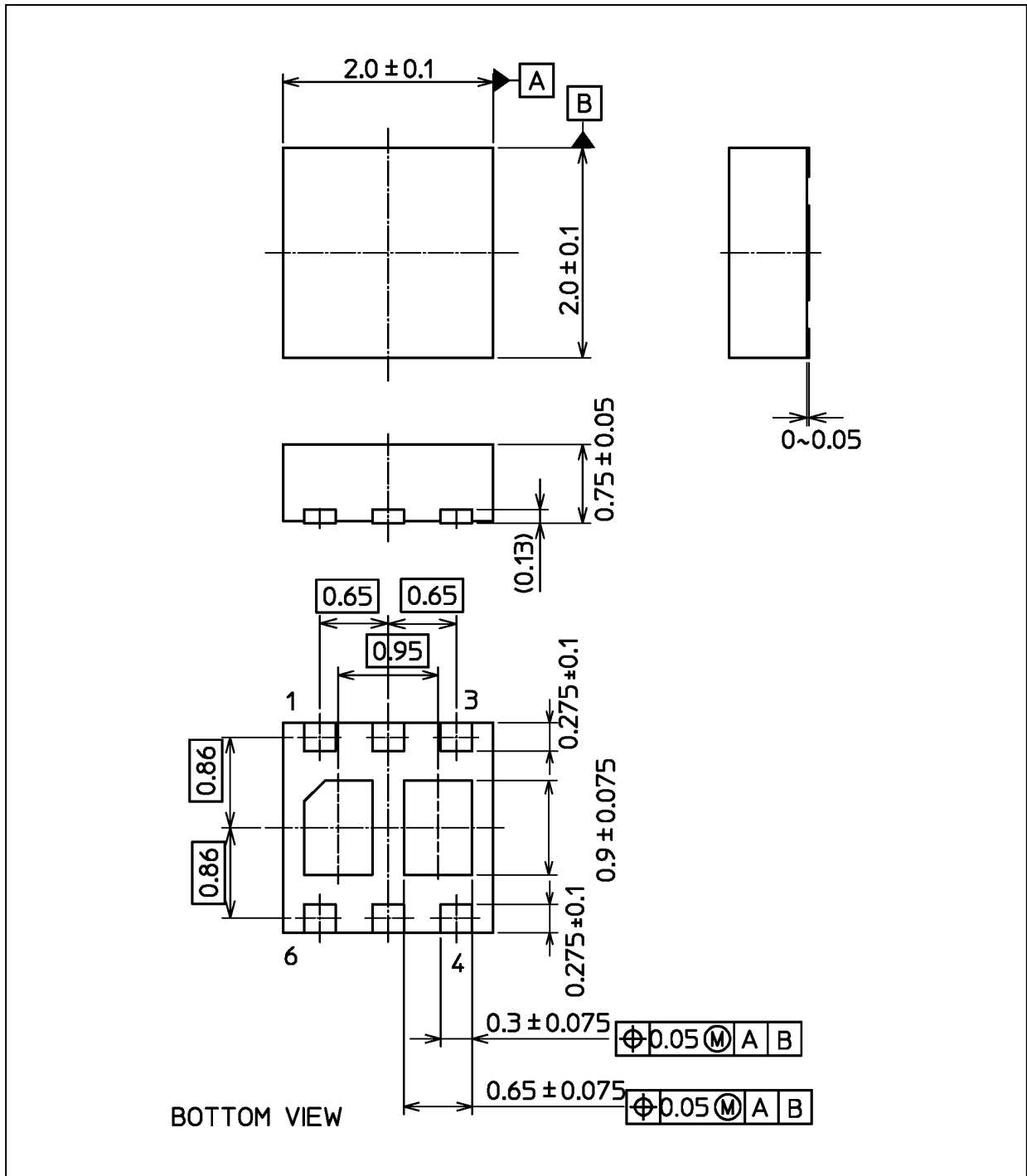


**Fig. 9.14**  $P_D - T_a$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm



Weight: 8.5 mg (typ.)

Package Name(s)
Nickname: UDFN6

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