

TOSHIBA CCD Linear Image Sensor CCD (Charge Coupled Device)

TCD2711DG

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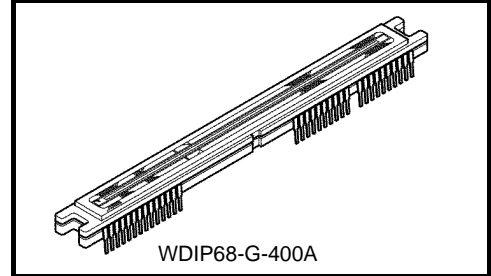
TCD2711DG

The TCD2711DG is a high sensitive and low dark current 7500 elements × 3 lines output CCD color linear image sensor.

The device contains a row of 7500 elements × 3 lines photodiodes which provide 24 lines/mm across a A3 size paper. The device is operated by 5.0 V pulse and 10 V power supply.

Features

- Number of Image Sensing Elements: 7500 elements × 3 lines
- Image Sensing Element Size: 9.325 μm by 9.325 μm on 9.325 μm center
- Photo Sensing Region: High sensitive PN photodiode
- Clock: 2-phase (5 V)
- Power Supply Voltage: 10 V (typ.)
- Distance between Photodiode Array: 18.65 μm (2 lines) R array – G array, G array – B array
- Internal Circuit: Clamp circuit
- Package: 68 pin CERDIP
- Color Filter: Red, Green, Blue

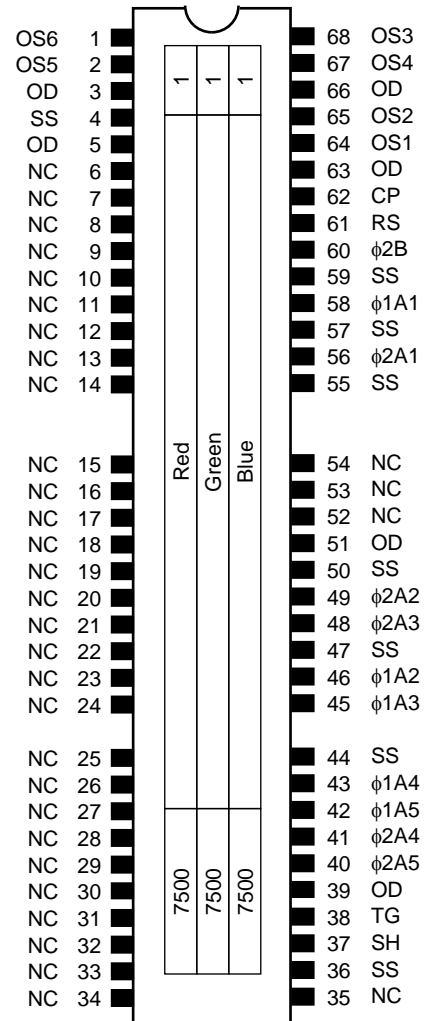


ABSOLUTE MAXIMUM RATINGS (Note 1)

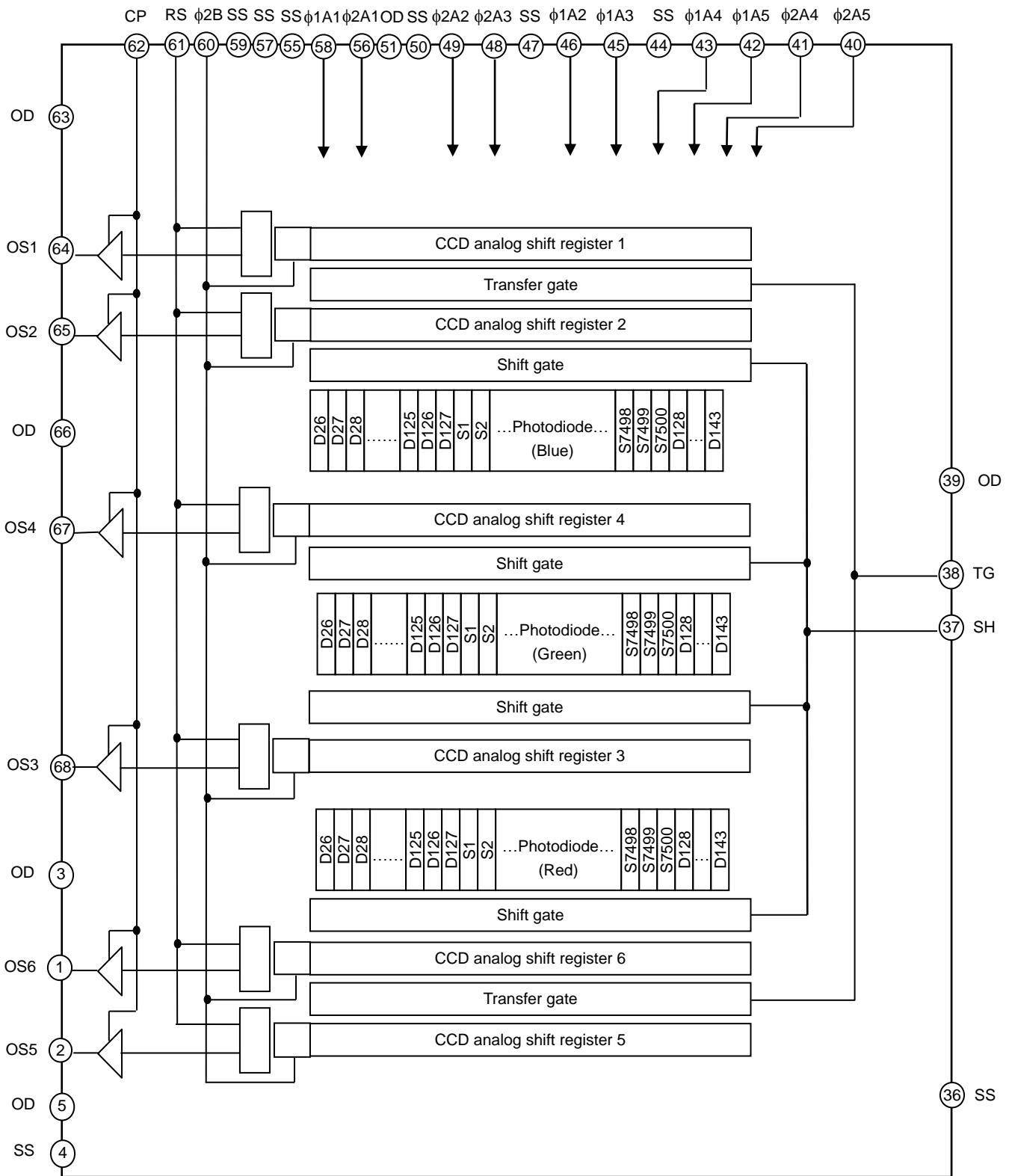
Characteristics	Symbol	Rating	Unit
Clock pulse voltage	$V_{\phi A}$	-0.3 to +8.0	V
Last stage clock pulse voltage	$V_{\phi B}$		
Shift pulse voltage	V_{SH}		
Reset pulse voltage	V_{RS}		
Clamp pulse voltage	V_{CP}		
Transfer pulse voltage	V_{TG}		
Power supply voltage	V_{OD}	-0.3 to +13.5	V
Operating temperature	T_{opr}	0 to 60	°C
Storage temperature	T_{stg}	-25 to +85	°C

Note 1: All voltages are with respect to SS terminals (ground).
 None of the ABSOLUTE MAXIMUM RATINGS must be exceeded, even instantaneously.
 If any one of the ABSOLUTE MAXIMUM RATINGS is exceeded, the electrical characteristics, reliability and life time of the device cannot be guaranteed. If the ABSOLUTE MAXIMUM RATINGS are exceeded, the device can be permanently damaged or degraded.
 Create a system design in such a manner that any of the ABSOLUTE MAXIMUM RATINGS will not be exceeded under any circumstances.

Pin Connections (top view)



Circuit Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	OS6	Output signal 6 (Red(Even))	68	OS3	Output signal 3 (Green(Odd))
2	OS5	Output signal 5 (Red(Odd))	67	OS4	Output signal 4 (Green(Even))
3	OD	Power supply	66	OD	Power supply
4	SS	Ground	65	OS2	Output signal 2 (Blue(Even))
5	OD	Power supply	64	OS1	Output signal 1 (Blue(Odd))
6	NC	Non connection	63	OD	Power supply
7	NC	Non connection	62	CP	Clamp gate
8	NC	Non connection	61	RS	Reset gate
9	NC	Non connection	60	ϕ 2B	Last stage transfer clock (phase 2)
10	NC	Non connection	59	SS	Ground
11	NC	Non connection	58	ϕ 1A1	Transfer clock 1 (phase 1)
12	NC	Non connection	57	SS	Ground
13	NC	Non connection	56	ϕ 2A1	Transfer clock 1 (phase 2)
14	NC	Non connection	55	SS	Ground
15	NC	Non connection	54	NC	Non connection
16	NC	Non connection	53	NC	Non connection
17	NC	Non connection	52	NC	Non connection
18	NC	Non connection	51	OD	Power supply
19	NC	Non connection	50	SS	Ground
20	NC	Non connection	49	ϕ 2A2	Transfer clock 2 (phase 2)
21	NC	Non connection	48	ϕ 2A3	Transfer clock 3 (phase 2)
22	NC	Non connection	47	SS	Ground
23	NC	Non connection	46	ϕ 1A2	Transfer clock 2 (phase 1)
24	NC	Non connection	45	ϕ 1A3	Transfer clock 3 (phase 1)
25	NC	Non connection	44	SS	Ground
26	NC	Non connection	43	ϕ 1A4	Transfer clock 4 (phase 1)
27	NC	Non connection	42	ϕ 1A5	Transfer clock 5 (phase 1)
28	NC	Non connection	41	ϕ 2A4	Transfer clock 4 (phase 2)
29	NC	Non connection	40	ϕ 2A5	Transfer clock 5 (phase 2)
30	NC	Non connection	39	OD	Power supply
31	NC	Non connection	38	TG	Transfer gate
32	NC	Non connection	37	SH	Shift gate
33	NC	Non connection	36	SS	Ground
34	NC	Non connection	35	NC	Non connection

Optical/Electrical Characteristics

Ta = 25°C, VOD = 10 V, Vφ = VSH = VRS = VCP = VTG = 5 V (pulse), fφ = 1.0 MHz,
 tINT (integration time) = 10 ms, light source = A light source + CM500S (t = 1.0 mm)

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	RR	13.2	18.9	24.6	V/lx·s	(Note 2)
	Green	RG	14.2	20.4	26.6		
	Blue	RB	9.3	13.4	17.5		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Saturation output voltage		VSAT	1.2	1.5	—	V	(Note 5)
Saturation exposure		SE	0.04	0.07	—	lx·s	(Note 6)
Dark signal voltage		VDRK	—	3	6	mV	(Note 7)
Dark signal non uniformity		DSNU	—	8	12	mV	(Note 8)
DC power dissipation		PD	—	590	900	mW	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		ZO	—	0.2	0.5	kΩ	—
DC output signal voltage		VOS	3.5	5.0	6.5	V	(Note 9)
Random noise		NDσ	—	0.9	—	mV	(Note 10)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature, and the incident light is 50 % of SE (typ.).

$$\text{PRNU (1)} = \frac{\Delta X}{\bar{X}} \times 100 (\%)$$

\bar{X} : Average of total signal outputs
 ΔX : The maximum deviation from \bar{X} .

Note 4: PRNU (3) is defined as the maximum voltage with next pixel, where measured approximately 50 mV of signal output.

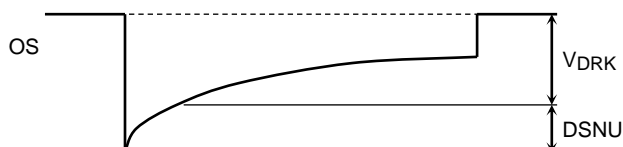
Note 5: VSAT is defined as the minimum saturation output voltage of all effective pixels.

Note 6: Definition of SE:

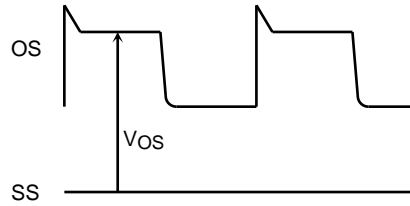
$$\text{SE} = \frac{V_{\text{SAT}}}{R_G}$$

Note 7: VDRK is defined as average dark signal voltage of all effective pixels.

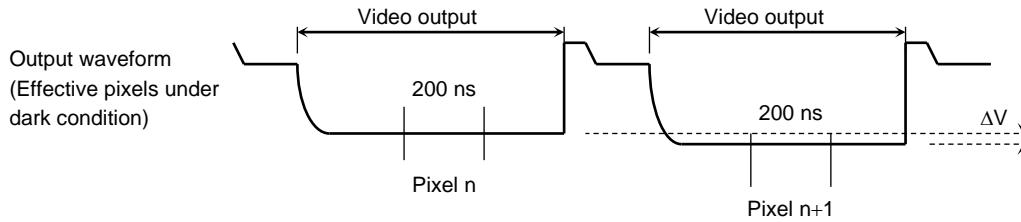
Note 8: DSNU is defined by the difference between average value (VDRK) and the maximum value of the dark voltage.



Note 9: DC output signal voltage is defined as follows.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



- 1) Two adjacent pixels (pixel n and n+1) in one reading are fixed as measurement points.
- 2) Each of the output levels at video output periods averaged over 200 ns period to get V(n) and V(n+1).
- 3) V(n+1) is subtracted from V(n) to get ΔV.

$$\Delta V = V(n) - V(n+1)$$
- 4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta V_i| \qquad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta V_i| - \overline{\Delta V})^2}$$

- 5) Procedure 2), 3) and 4) are repeated 10 times to get sigma value.
- 6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

- 7) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$ND_{\sigma} = \frac{1}{\sqrt{2}} \overline{\sigma}$$

Recommended Operating Conditions (Ta = 25°C)

For best performance, the device should be used within the Recommended Operating Conditions.

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	"H" level	$V_{\phi1A}$	4.75	5.0	5.5	V
	"L" level	$V_{\phi2A}$	0	0	0.25	
Last stage clock pulse voltage	"H" level	$V_{\phi2B}$	4.75	5.0	5.5	V
	"L" level		0	0	0.25	
Shift pulse voltage	"H" level	V_{SH}	4.75	5.0	5.5	V
	"L" level		0	0	0.25	
Reset pulse voltage	"H" level	V_{RS}	4.75	5.0	5.5	V
	"L" level		0	0	0.25	
Clamp pulse voltage	"H" level	V_{CP}	4.75	5.0	5.5	V
	"L" level		0	0	0.25	
Transfer pulse voltage	"H" level	V_{TG}	4.75	5.0	5.5	V
	"L" level		0	0	0.25	
Power supply voltage		V_{OD}	9.5	10.0	10.5	V

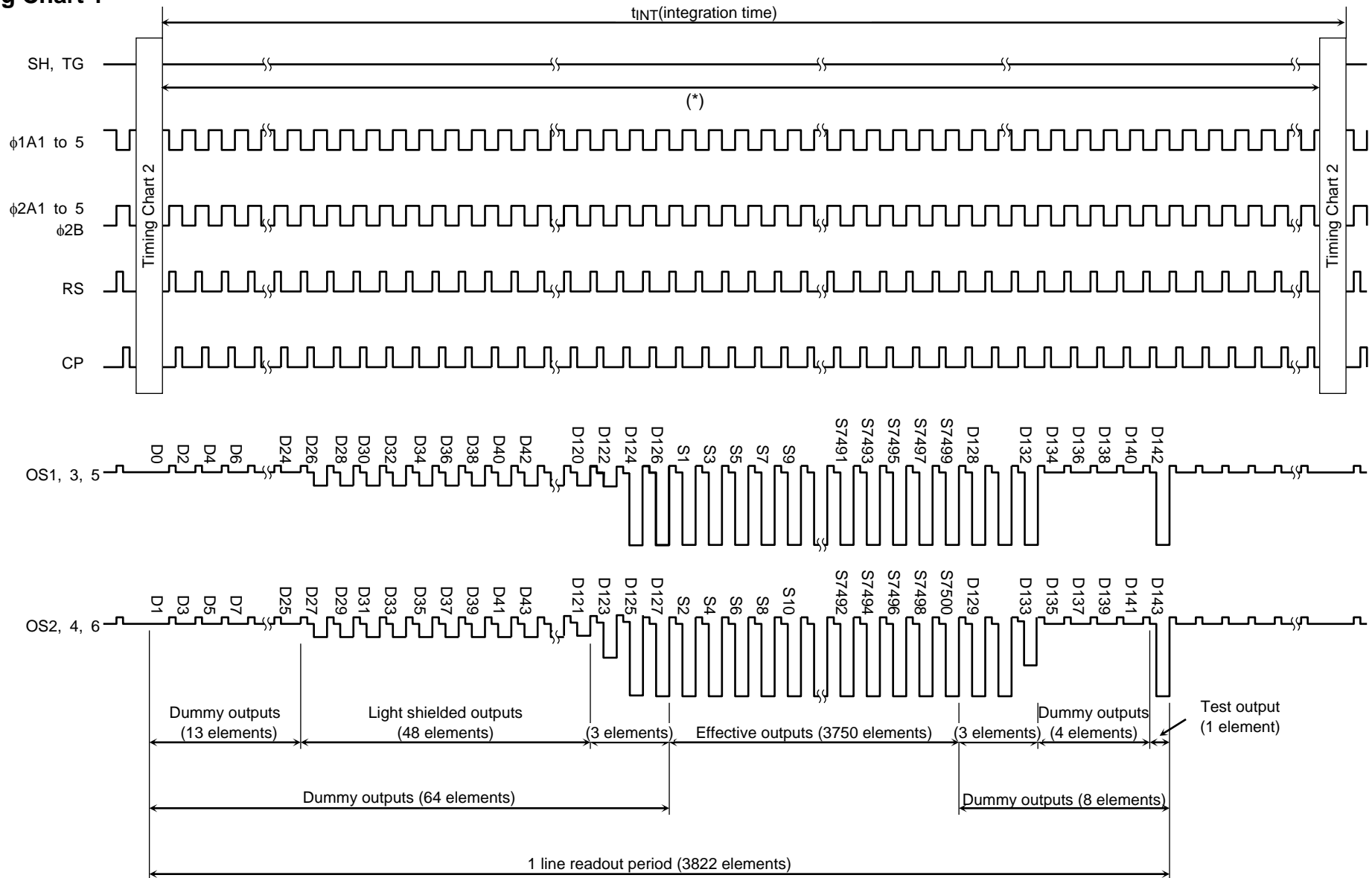
Clock Characteristics (Ta = 25°C)

For best performance, the device should be used within the Recommended Operating Conditions.

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse frequency		f_{ϕ}	0.2	1.0	35.0	MHz
Reset pulse frequency		f_{RS}	0.2	1.0	35.0	MHz
Clamp pulse frequency		f_{CP}	0.2	1.0	35.0	MHz
Clock capacitance (Note 12)	$C_{\phi1A}$	—	153	—	—	pF
	$C_{\phi2A}$	—	162	—	—	pF
Last stage clock capacitance		$C_{\phi B}$	—	3	—	pF
Shift gate capacitance		C_{SH}	—	32	—	pF
Reset gate capacitance		C_{RS}	—	5	—	pF
Clamp gate capacitance		C_{CP}	—	3	—	pF
Transfer gate capacitance		C_{TG}	—	5	—	pF

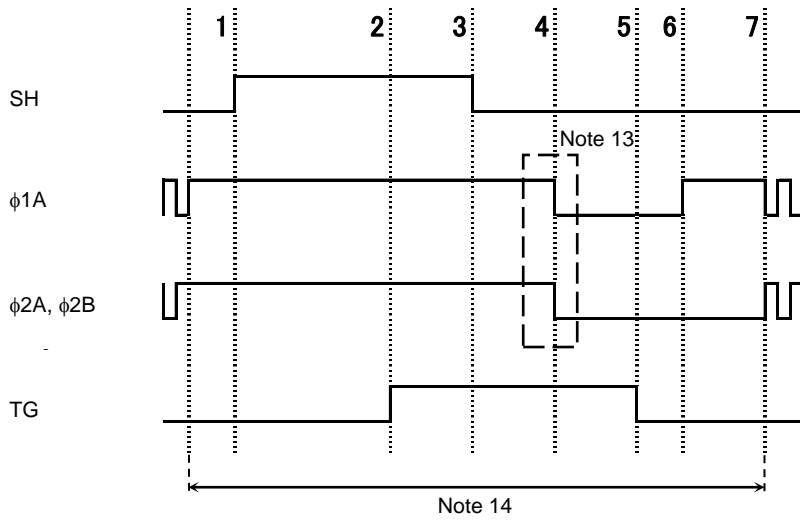
Note 12: $V_{OD} = 10$ V, Input capacitance per a pin.

Timing Chart 1

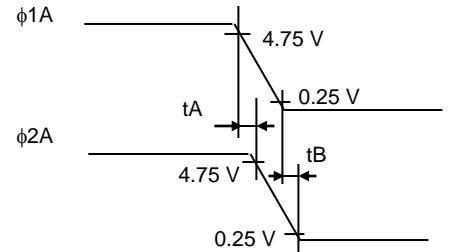


(*) : Keep the SH and TG pins "L" level.

Timing Chart 2 (Vertical Transfer Period)



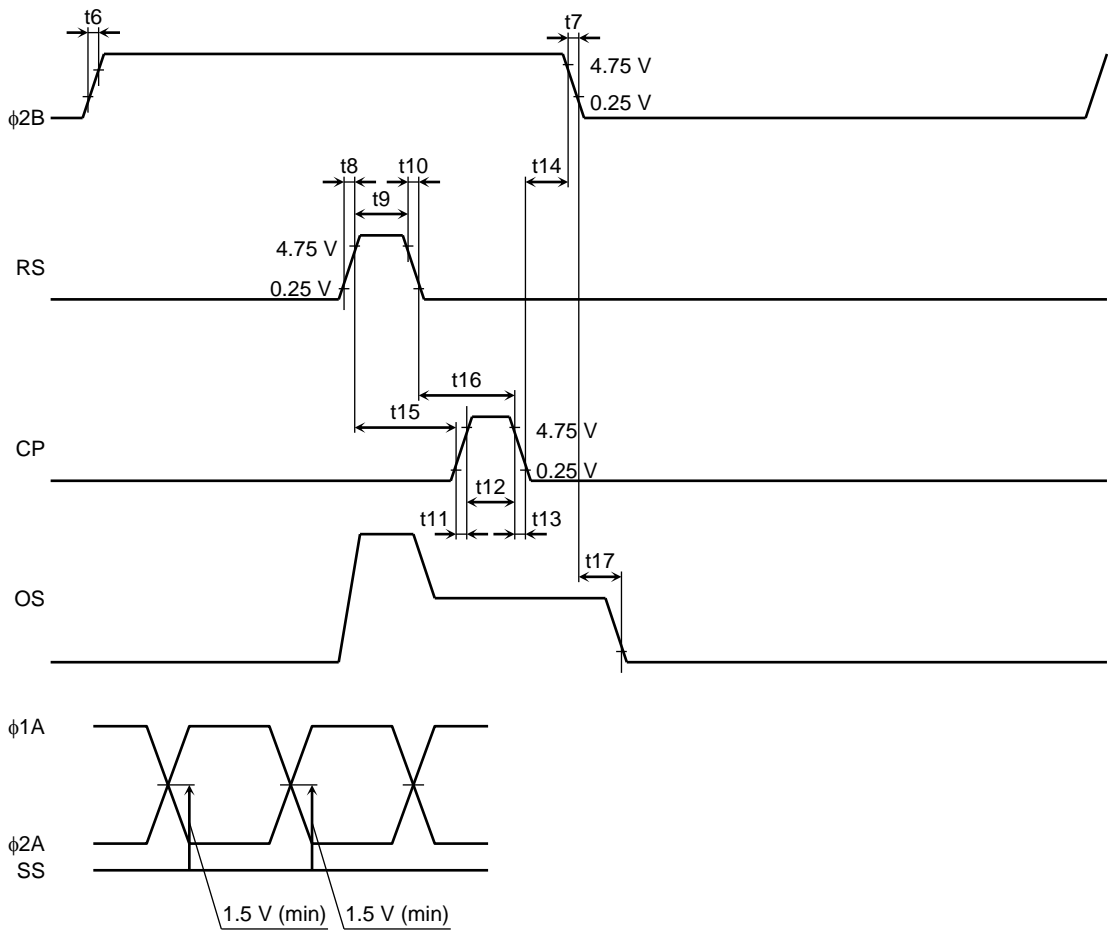
Note 13: For timing address 4



※ φ2B is no care.

Note 14: Keep the RS and CP pins "L" level.

Timing Requirements 1



Characteristics	Symbol	Min	Typ. (Note 15)	Max	Unit
ϕ 2B pulse rise time, fall time	t6, t7	0	50	—	ns
RS pulse rise time, fall time	t8, t10	0	20	—	ns
RS pulse width	t9	6	100	—	ns
CP pulse rise time, fall time	t11, t13	0	20	—	ns
CP pulse width	t12	6	200	—	ns
Pulse timing of ϕ 2B and CP	t14	0	40	—	ns
Pulse timing of RS and CP	t15	0	0	—	ns
	t16	6	100	—	ns
Video data delay time	t17	—	7	—	ns

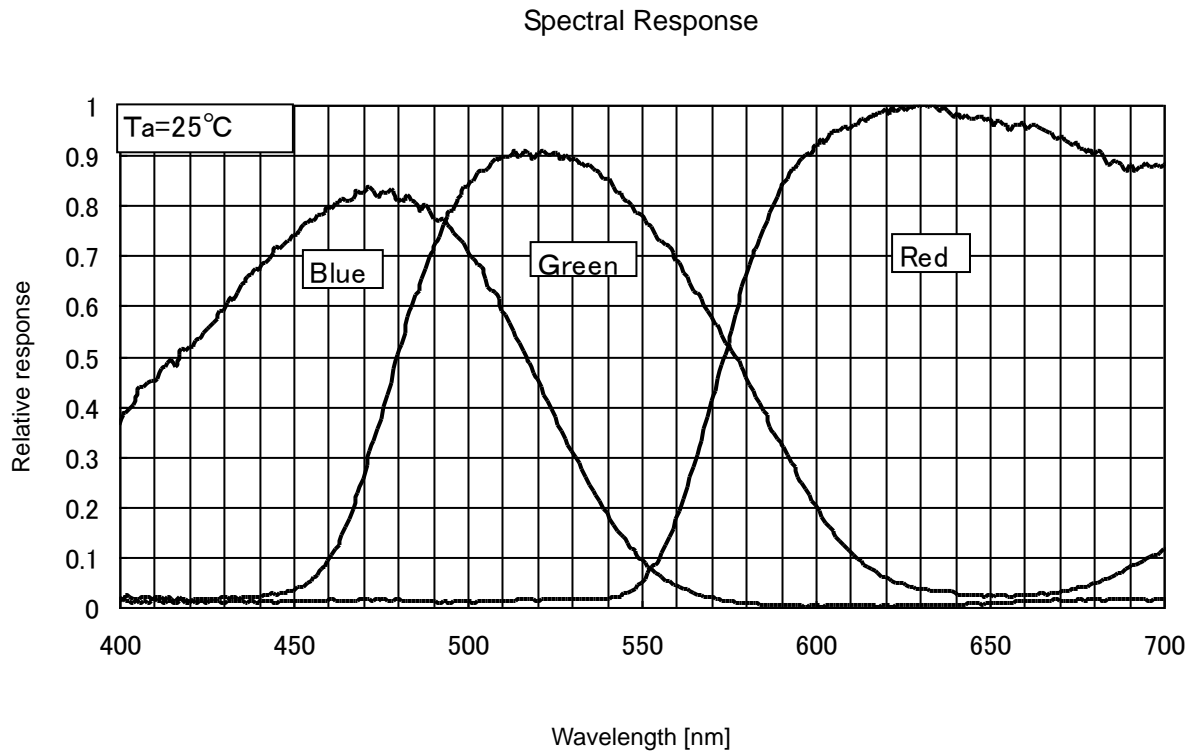
Note 15: Measured with $f_{RS} = 1$ MHz.

Timing Requirements 2 (Vertical Transfer Period)

Timing address	Min	Typ.	Max	Unit
1	250	500	—	ns
2	1000	2000	—	ns
3	500	1000	—	ns
4	500	1000	—	ns
5	500	1000	—	ns
6	250	500	—	ns
7	500	1000	—	ns
Vertical transfer time	3.5	7.0	—	μ s

Timing address 4		Min	Typ.	Max	Unit
ϕ 1A, ϕ 2A timing	tA	-0.5	0	+0.5	ns
	tB	-0.5	0	+0.5	ns

Typical Spectral Response



Cautions**1. Electrostatic Breakdown**

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting pliers or pincer.
- d. Ionized air is recommended for discharge when handling CCD image sensors.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Mounting on a PCB

This package is sensitive to mechanical stress.

TOSHIBA recommends using IC inserters for mounting, instead of using lead forming equipment.

Since this package is not strong against mechanical stress, you should not reform the lead frame.

We recommend to use an IC-inserter when you assemble to PCB.

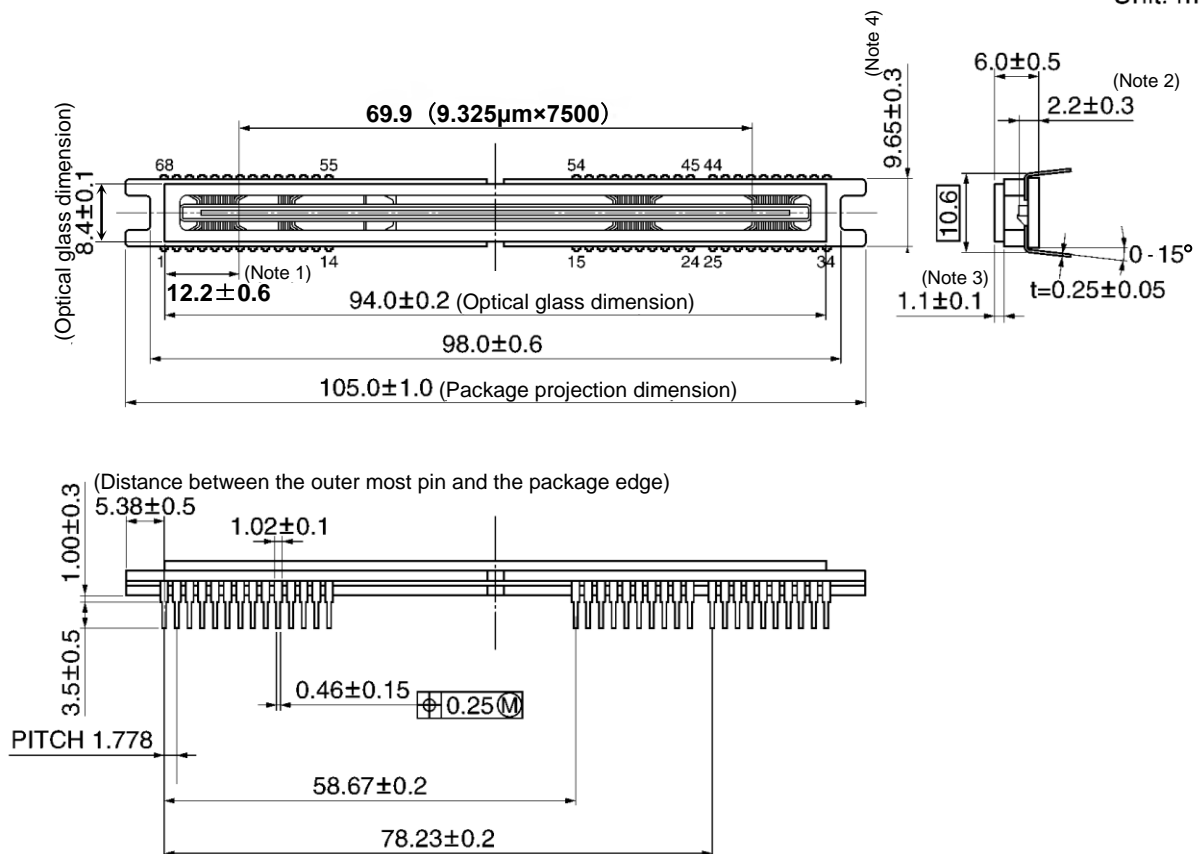
5. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.

Using a soldering iron, complete soldering within three seconds for lead temperatures of up to 350°C.

Package Dimensions WDIP68-G-400A

Unit: mm



Note 1: Distance between the center of the first pin and the first pixel (S1).

Note 2: Distance between the top of the chip and bottom of the package.

Note 3: Glass thickness ($n = 1.5$).

Note 4: Dimensional tolerance is ± 0.3 mm for the 10 mm range from each ceramic edge, ± 0.4 mm for the 10 mm to 27 mm range and ± 0.5 mm for the inner range.

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