32-bit RISC Microcontroller

TMPM4G Group(1)

Reference Manual
Input/Output Ports
(PORT-M4G(1))

Revision 2.3

2019-06

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-" , follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

JTAG	Joint Test Action Group
NBD	Non Break Debug
SW	Serial Wire

1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

Table 1.1 Features

Function Classification	Function	Description
Port	-	Programmable pull-up /Programmable pull-down /Open-drain output are possible.
Peripheral Function pins	Interrupt control	External Interrupt pin Interrupt pin has a noise filter(Filter width 30ns Typ.).
	32-bit Timer Event Counter	Input capture input pin. Timer output pin.
	Serial Peripheral Interface	Chip select input 1 pin, Chip select output 4 pins, Data input pin, Data output pin, Clock input/output pin
	Asynchronous Serial Communication Circuit	Data input pin, Data output pin, Handshake function pins.
	Full Universal Asynchronous Receiver Transmitter	Data input pin, Data output pin, Handshake function pins, IrDA1.0 data input/output pin
	I^2C Interface	Data input/output pin, Clock input/output pin
	Serial Memory Interface	Chip select input/output pin, Data input/output pin, Clock input/output pin
	Multi-Function DMA Controller	MDMA Request input pin
	High Speed DMA Controller	HDMA Request input pin
	Interval Sensor Detection	Data input pin, Data output pin
	Consumer Electronics Control	Data input/output pin,
	External Bus Interface	Address bus output pin, Data bus input/output pin, Read strobe output pin, Write strobe output pin, Chip Select output pin, Byte Enable output pin, Address Latch Enable output pin, Wait input pin, Clock output pin
	Advanced Programmable Motor Control Circuit	X/Y/Z phase output pins, U/V/W phase output pins, EMG detection input pin, Overvoltage detection input pin.
	Remote Control Signal preprocessor	Data input pin
	12-bit Analog to Digital Convertor	Analog input pin, AD Trigger input pin
	8-bit Digital to Analog Convertor	DAC output pin
	Real Time Clock	1Hz clock output pin, Alarm output pin
	Trigger Input(TRGSEL)	TRGINx pin
Debug pins	JTAG	Test select input pin, Serial clock input pin, Serial data output pin, Serial data input pin, Test reset pin
	SW	Serial wire data input/output pin, Serial wire clock input pin, Serial wire viewer output pin
	Trace	Trace clock output pin, Trace data output 4pins.
	NBDIF	NBD synchronous input pin, NBD clock input pin, NBD data output 4pins.
Control pins	High speed resonator	High speed resonator connection pin, External High speed clock input
	Low speed resonator	Low speed resonator connection pin, External Low Speed clock input
	BOOT mode control	BOOT mode control pin

2. Function

2.1. Clock supply

When PORT is used, the corresponding clock enable bits should be set to “1” (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB]***), and fc supply stop register (***[CGFCEN]***). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to “Clock Control and Operation Mode” in Reference manual.

3. Signal connection list

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal connection list (1/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
Asynchronous Serial Communication Circuit	UT0RXD	PE2	60	52	48	39	T5	P5
		PH4	89	73	65	51	R16	N14
		PH5	88	72	64	50	T15	P13
	UT0TXDA	PE3	61	53	49	40	T6	N6
		PH5	88	72	64	50	T15	P13
		PH4	89	73	65	51	R16	N14
	UT0CTS_N	PE1	59	51	47	38	R5	N5
		PH7	86	70	62	48	R14	N12
		PH6	87	71	63	49	R15	P12
	UT0RTS_N	PE0	58	50	46	37	R4	N4
		PH6	87	71	63	49	R15	P12
		PH7	86	70	62	48	R14	N12
	UT1RXD	PH0	93	77	69	55	N16	L11
		PH1	92	76	68	54	N15	M13
		PV4	81	65	61	-	R12	N10
	UT1TXDA	PH1	92	76	68	54	N15	M13
		PH0	93	77	69	55	N16	L11
		PV5	80	64	60	-	T12	P9
	UT1CTS_N	PH3	90	74	66	52	P15	N13
		PH2	91	75	67	53	P16	M14
		PV6	79	63	59	-	T11	N9
	UT1RTS_N	PH2	91	75	67	53	P16	M14
		PH3	90	74	66	52	P15	N13
		PV7	78	62	58	-	R11	L9

Table 3.2 Signal connection list (2/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
Asynchronous Serial Communication Circuit	UT2RXD	PG0	129	105	93	72	D15	D13
		PG1	130	106	94	73	C16	C14
	UT2TXDA	PG1	130	106	94	73	C16	C14
		PG0	129	105	93	72	D15	D13
	UT2CTS_N	PG3	132	108	96	75	B16	B14
		PG2	131	107	95	74	C15	C13
	UT2RTS_N	PG2	131	107	95	74	C15	C13
		PG3	132	108	96	75	B16	B14
	UT3RXD	PU6	40	-	-	-	L4	-
		PV0	115	97	89	-	F12	F10
		PV1	114	96	88	-	G13	F11
	UT3TXDA	PU7	41	-	-	-	M4	-
		PV1	114	96	88	-	G13	F11
		PV0	115	97	89	-	F12	F10
	UT3CTS_N	PU5	39	-	-	-	L5	-
		PV3	112	94	86	-	H13	G10
		PV2	113	95	87	-	G12	G11
	UT3RTS_N	PU4	38	-	-	-	K5	-
		PV2	113	95	87	-	G12	G11
		PV3	112	94	86	-	H13	G10
	UT4RXD	PM0	124	102	-	-	E16	D14
		PM1	123	101	-	-	F15	E13
		PU1	35	-	-	-	J4	-
	UT4TXDA	PM1	123	101	-	-	F15	E13
		PM0	124	102	-	-	E16	D14
		PU0	34	-	-	-	H4	-
	UT4CTS_N	PM3	121	99	-	-	E13	F13
		PM2	122	100	-	-	F16	E14
		PU2	36	-	-	-	J5	-
	UT4RTS_N	PM2	122	100	-	-	F16	E14
		PM3	121	99	-	-	E13	F13
		PU3	37	-	-	-	K4	-

Table 3.3 Signal connection list (3/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
Asynchronous Serial Communication Circuit	UT5RXD	PJ0	168	-	-	-	B5	-
		PJ1	167	-	-	-	B6	-
	UT5TXDA	PJ1	167	-	-	-	B6	-
		PJ0	168	-	-	-	B5	-
	UT5CTS_N	PJ3	165	-	-	-	D7	-
		PJ2	166	-	-	-	D6	-
	UT5RTS_N	PJ2	166	-	-	-	D6	-
		PJ3	165	-	-	-	D7	-
Full Asynchronous Serial Communication Circuit	FUT0RXD	PG5	96	80	72	58	M13	K11
		PJ5	68	-	-	-	R9	-
	FUT0TXD	PG4	97	81	73	59	L12	K13
		PJ4	69	-	-	-	T9	-
	FUT0CTS_N	PG7	94	78	70	56	M15	L13
	FUT0RTS_N	PG6	95	79	71	57	M16	L14
	FUT0IROUT	PG4	97	81	73	59	L12	K13
	FUT0IRIN	PG5	96	80	72	58	M13	K11
	FUT1RXD	PJ7	66	-	-	-	N9	-
		PM6	83	67	-	-	R13	N11
	FUT1TXD	PJ6	67	-	-	-	R8	-
		PM7	82	66	-	-	T13	P10
	FUT1CTS_N	PM4	85	69	-	-	N12	L10
	FUT1RTS_N	PM5	84	68	-	-	T14	P11
	FUT1IROUT	PM7	82	66	-	-	T13	P10
	FUT1IRIN	PM6	83	67	-	-	R13	N11
I^2C Interface	I2C0SDA	PG2	131	107	95	74	C15	C13
	I2C0SCL	PG3	132	108	96	75	B16	B14
	I2C1SDA	PF2	174	142	126	99	B4	B4
	I2C1SCL	PF3	175	143	127	100	A3	A3
	I2C2SDA	PG4	97	81	73	59	L12	K13
		PV5	80	64	60	-	T12	P9
	I2C2SCL	PG5	96	80	72	58	M13	K11
		PV4	81	65	61	-	R12	N10
	I2C3SDA	PJ6	67	-	-	-	R8	-
		PM0	124	102	-	-	E16	D14
	I2C3SCL	PJ7	66	-	-	-	N9	-
		PM1	123	101	-	-	F15	E13

Table 3.4 Signal connection list (4/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
I^2C Interface	I2C4SDA	PJ3	165	-	-	-	D7	-
		PM6	83	67	-	-	R13	N11
	I2C4SCL	PJ2	166	-	-	-	D6	-
		PM7	82	66	-	-	T13	P10
Interval Sensor Detection Circuit	ISDAIN0	PE4	62	54	50	41	R6	P6
	ISDAIN1	PE5	63	55	51	42	R7	P7
	ISDAIN2	PE6	64	56	52	43	T7	N7
	ISDAIN3	PE7	65	57	53	44	T8	N8
	ISDAOUT	PK0	111	93	85	71	H12	H10
	ISDBIN0	PV0	115	97	89	-	F12	F10
	ISDBIN1	PV1	114	96	88	-	G13	F11
	ISDBIN2	PV2	113	95	87	-	G12	G11
	ISDBIN3	PV3	112	94	86	-	H13	G10
	ISDBOUT	PK1	110	92	84	70	J12	H11
	ISDCIN0	PW4	120	-	-	-	G15	-
	ISDCIN1	PW5	119	-	-	-	G16	-
	ISDCIN2	PW6	118	-	-	-	H15	-
	ISDCIN3	PW7	117	-	-	-	H16	-
	ISDCOUT	PY4	30	30	26	21	M2	K2
Serial Peripheral Interface	TSPI0CSIN	PA0	29	29	25	20	L1	J4
	TSPI0CS0	PA0	29	29	25	20	L1	J4
	TSPI0CS1	PA4	25	25	21	16	J1	H2
	TSPI0CS2	PA5	24	24	20	15	J2	G1
	TSPI0CS3	PA6	23	23	19	14	H1	G2
	TSPI0RXD	PA2	27	27	23	18	K1	J2
	TSPI0TXD	PA3	26	26	22	17	K2	H1
	TSPI0SCK	PA1	28	28	24	19	L2	J1
	TSPI1CSIN	PL0	103	85	77	63	L13	J11
	TSPI1CS0	PL0	103	85	77	63	L13	J11
	TSPI1CS1	PK4	107	89	81	67	J15	G14
	TSPI1CS2	PK5	106	88	80	66	K15	H13
	TSPI1CS3	PK6	105	87	79	65	J16	H14
	TSPI1RXD	PL2	101	83	75	61	L15	J13
	TSPI1TXD	PL3	100	82	74	60	L16	K14
	TSPI1SCK	PL1	102	84	76	62	K16	J14

Table 3.5 Signal connection list (5/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
Serial Peripheral Interface	TSPI2CSIN	PA7	22	22	18	13	H2	J5
	TSPI2CS0	PA7	22	22	18	13	H2	J5
	TSPI2CS1	PA3	26	26	22	17	K2	H1
	TSPI2RXD	PA5	24	24	20	15	J2	G1
	TSPI2TXD	PA4	25	25	21	16	J1	H2
	TSPI2SCK	PA6	23	23	19	14	H1	G2
	TSPI3CSIN	PK7	104	86	78	64	K12	J10
	TSPI3CS0	PK7	104	86	78	64	K12	J10
	TSPI3CS1	PL3	100	82	74	60	L16	K14
	TSPI3RXD	PK5	106	88	80	66	K15	H13
	TSPI3TXD	PK4	107	89	81	67	J15	G14
	TSPI3SCK	PK6	105	87	79	65	J16	H14
	TSPI4CSIN	PD0	48	40	36	29	N5	L4
	TSPI4CS0	PD0	48	40	36	29	N5	L4
	TSPI4RXD	PD2	50	42	38	31	N6	K6
	TSPI4TXD	PD3	51	43	39	32	M7	L6
	TSPI4SCK	PD1	49	41	37	30	M6	L5
	TSPI5CSIN	PV7	78	62	58	-	R11	L9
	TSPI5CS0	PV7	78	62	58	-	R11	L9
	TSPI5RXD	PV4	81	65	61	-	R12	N10
	TSPI5TXD	PV5	80	64	60	-	T12	P9
	TSPI5SCK	PV6	79	63	59	-	T11	N9
	TSPI6CSIN	PM3	121	99	-	-	E13	F13
	TSPI6CS0	PM3	121	99	-	-	E13	F13
	TSPI6RXD	PM1	123	101	-	-	F15	E13
	TSPI6TXD	PM0	124	102	-	-	E16	D14
	TSPI6SCK	PM2	122	100	-	-	F16	E14
	TSPI7CSIN	PM4	85	69	-	-	N12	L10
	TSPI7CS0	PM4	85	69	-	-	N12	L10
	TSPI7RXD	PM6	83	67	-	-	R13	N11
	TSPI7TXD	PM7	82	66	-	-	T13	P10
	TSPI7SCK	PM5	84	68	-	-	T14	P11

Table 3.6 Signal connection list (6/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
Serial Peripheral Interface	TSPI8CSIN	PW0	77	-	-	-	M11	-
	TSPI8CS0	PW0	77	-	-	-	M11	-
	TSPI8RXD	PW2	75	-	-	-	M10	-
	TSPI8TXD	PW3	74	-	-	-	N10	-
	TSPI8SCK	PW1	76	-	-	-	N11	-
Serial Memory Interface	SMI0CS1_N	PK0	111	93	85	71	H12	H10
	SMI0D0	PK2	109	91	83	69	J13	F14
	SMI0D1	PK3	108	90	82	68	K13	G13
	SMI0D2	PK4	107	89	81	67	J15	G14
	SMI0D3	PK5	106	88	80	66	K15	H13
	SMI0CLK	PK6	105	87	79	65	J16	H14
	SMI0CS0_N	PK7	104	86	78	64	K12	J10
32-bit Timer Event Counter	T32A00INA0	PA0	29	29	25	20	L1	J4
		PK0	111	93	85	71	H12	H10
	T32A00INA1	PA3	26	26	22	17	K2	H1
	T32A00OUTA	PA1	28	28	24	19	L2	J1
		PW1	76	-	-	-	N11	-
	T32A00INB0	PA3	26	26	22	17	K2	H1
		PK1	110	92	84	70	J12	H11
	T32A00INB1	PA0	29	29	25	20	L1	J4
	T32A00OUTB	PA2	27	27	23	18	K1	J2
		PW0	77	-	-	-	M11	-
	T32A00INC0	PA0	29	29	25	20	L1	J4
		PK0	111	93	85	71	H12	H10
	T32A00INC1	PA3	26	26	22	17	K2	H1
		PK1	110	92	84	70	J12	H11
	T32A00OUTC	PA1	28	28	24	19	L2	J1
		PW1	76	-	-	-	N11	-

Table 3.7 Signal connection list (7/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
32-bit Timer Event Counter	T32A01INA0	PA4	25	25	21	16	J1	H2
		PK6	105	87	79	65	J16	H14
	T32A01INA1	PA7	22	22	18	13	H2	J5
	T32A01OUTA	PA5	24	24	20	15	J2	G1
		PW2	75	-	-	-	M10	-
	T32A01INB0	PA7	22	22	18	13	H2	J5
		PK7	104	86	78	64	K12	J10
	T32A01INB1	PA4	25	25	21	16	J1	H2
	T32A01OUTB	PA6	23	23	19	14	H1	G2
		PW3	74	-	-	-	N10	-
	T32A01INC0	PA4	25	25	21	16	J1	H2
		PK6	105	87	79	65	J16	H14
	T32A01INC1	PA7	22	22	18	13	H2	J5
		PK7	104	86	78	64	K12	J10
	T32A01OUTC	PA5	24	24	20	15	J2	G1
		PW2	75	-	-	-	M10	-
	T32A02INA0	PB0	21	21	17	12	G1	H4
		PL0	103	85	77	63	L13	J11
	T32A02INA1	PB1	20	20	16	11	G2	H5
	T32A02OUTA	PB2	19	19	15	10	F1	F1
		PG5	96	80	72	58	M13	K11
	T32A02INB0	PB1	20	20	16	11	G2	H5
		PL3	100	82	74	60	L16	K14
	T32A02INB1	PB0	21	21	17	12	G1	H4
	T32A02OUTB	PB3	18	18	14	9	F2	F2
		PG4	97	81	73	59	L12	K13
	T32A02INC0	PB0	21	21	17	12	G1	H4
		PL0	103	85	77	63	L13	J11
	T32A02INC1	PB1	20	20	16	11	G2	H5
		PL3	100	82	74	60	L16	K14
	T32A02OUTC	PB2	19	19	15	10	F1	F1
		PG5	96	80	72	58	M13	K11

Table 3.8 Signal connection list (8/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
32-bit Timer Event Counter	T32A03INA0	PB6	15	15	11	6	G4	G4
		PJ4	69	-	-	-	T9	-
	T32A03INA1	PB7	14	14	10	5	G5	G5
	T32A03OUTA	PB4	17	17	13	8	E1	E1
		PT3	31	31	27	22	H5	K4
	T32A03INB0	PB7	14	14	10	5	G5	G5
		PJ5	68	-	-	-	R9	-
	T32A03INB1	PB6	15	15	11	6	G4	G4
	T32A03OUTB	PB5	16	16	12	7	E2	E2
		PT5	73	61	57	-	R10	K9
	T32A03INC0	PB6	15	15	11	6	G4	G4
		PJ4	69	-	-	-	T9	-
	T32A03INC1	PB7	14	14	10	5	G5	G5
		PJ5	68	-	-	-	R9	-
	T32A03OUTC	PB4	17	17	13	8	E1	E1
		PT3	31	31	27	22	H5	K4
	T32A04INA0	PD0	48	40	36	29	N5	L4
		PP0	141	117	105	84	D12	D11
	T32A04INA1	PD1	49	41	37	30	M6	L5
		PP1	142	118	106	85	D11	D10
	T32A04OUTA	PD2	50	42	38	31	N6	K6
		PV5	80	64	60	-	T12	P9
	T32A04INB0	PD1	49	41	37	30	M6	L5
		PP1	142	118	106	85	D11	D10
	T32A04INB1	PD0	48	40	36	29	N5	L4
		PP0	141	117	105	84	D12	D11
	T32A04OUTB	PD3	51	43	39	32	M7	L6
		PV4	81	65	61	-	R12	N10
	T32A04INC0	PD0	48	40	36	29	N5	L4
		PP0	141	117	105	84	D12	D11
	T32A04INC1	PD1	49	41	37	30	M6	L5
		PP1	142	118	106	85	D11	D10
	T32A04OUTC	PD2	50	42	38	31	N6	K6
		PV5	80	64	60	-	T12	P9

Table 3.9 Signal connection list (9/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
32-bit Timer Event Counter	T32A05INA0	PD6	54	46	42	35	N8	K8
		PP2	143	119	107	86	B11	B9
	T32A05INA1	PD7	55	47	43	36	M9	L8
		PP3	144	120	108	87	A11	A9
	T32A05OUTA	PD4	52	44	40	33	N7	L7
		PV6	79	63	59	-	T11	N9
	T32A05INB0	PD7	55	47	43	36	M9	L8
		PP3	144	120	108	87	A11	A9
	T32A05INB1	PD6	54	46	42	35	N8	K8
		PP2	143	119	107	86	B11	B9
	T32A05OUTB	PD5	53	45	41	34	M8	K7
		PV7	78	62	58	-	R11	L9
	T32A05INC0	PD6	54	46	42	35	N8	K8
		PP2	143	119	107	86	B11	B9
	T32A05INC1	PD7	55	47	43	36	M9	L8
		PP3	144	120	108	87	A11	A9
	T32A05OUTC	PD4	52	44	40	33	N7	L7
		PV6	79	63	59	-	T11	N9
	T32A06INA0	PE2	60	52	48	39	T5	P5
		PP4	145	121	109	88	E11	D9
	T32A06INA1	PE0	58	50	46	37	R4	N4
		PP5	146	122	110	89	D10	E9
	T32A06OUTA	PE1	59	51	47	38	R5	N5
		PM5	84	68	-	-	T14	P11
	T32A06INB0	PE3	61	53	49	40	T6	N6
		PP5	146	122	110	89	D10	E9
	T32A06INB1	PE0	58	50	46	37	R4	N4
		PP4	145	121	109	88	E11	D9
	T32A06OUTB	PE0	58	50	46	37	R4	N4
		PM4	85	69	-	-	N12	L10
	T32A06INC0	PE2	60	52	48	39	T5	P5
		PP4	145	121	109	88	E11	D9
	T32A06INC1	PE3	61	53	49	40	T6	N6
		PP5	146	122	110	89	D10	E9
	T32A06OUTC	PE1	59	51	47	38	R5	N5
		PM5	84	68	-	-	T14	P11

Table 3.10 Signal connection list (10/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
32-bit Timer Event Counter	T32A07INA0	PE4	62	54	50	41	R6	P6
		PP6	147	123	111	90	B10	B8
	T32A07INA1	PE7	65	57	53	44	T8	N8
		PP7	148	124	112	91	A10	A8
	T32A07OUTA	PE6	64	56	52	43	T7	N7
		PM6	83	67	-	-	R13	N11
	T32A07INB0	PE5	63	55	51	42	R7	P7
		PP7	148	124	112	91	A10	A8
	T32A07INB1	PE7	65	57	53	44	T8	N8
		PP6	147	123	111	90	B10	B8
	T32A07OUTB	PE7	65	57	53	44	T8	N8
		PM7	82	66	-	-	T13	P10
	T32A07INC0	PE4	62	54	50	41	R6	P6
		PP6	147	123	111	90	B10	B8
	T32A07INC1	PE5	63	55	51	42	R7	P7
		PP7	148	124	112	91	A10	A8
	T32A07OUTC	PE6	64	56	52	43	T7	N7
		PM6	83	67	-	-	R13	N11
	T32A08INA0	PC0	11	11	7	-	F4	F4
		PR0	149	125	113	-	E10	D8
	T32A08OUTA	PC2	9	9	5	-	D1	D1
		PL4	126	-	-	-	D16	-
	T32A08INB0	PC1	10	10	6	-	F5	F5
		PR1	150	126	114	-	D9	E8
	T32A08OUTB	PC3	8	8	4	-	D2	D2
		PL5	125	-	-	-	E15	-
	T32A08INC0	PC0	11	11	7	-	F4	F4
		PR0	149	125	113	-	E10	D8
	T32A08INC1	PC1	10	10	6	-	F5	F5
		PR1	150	126	114	-	D9	E8
	T32A08OUTC	PC2	9	9	5	-	D1	D1
		PL4	126	-	-	-	D16	-

Table 3.11 Signal connection list (11/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
32-bit Timer Event Counter	T32A09INA0	PR2	151	127	115	-	B9	B7
		PV0	115	97	89	-	F12	F10
	T32A09OUTA	PL6	164	-	-	-	E7	-
		PV2	113	95	87	-	G12	G11
	T32A09INB0	PR3	152	128	116	-	A9	A7
		PV1	114	96	88	-	G13	F11
	T32A09OUTB	PL7	163	-	-	-	E8	-
		PV3	112	94	86	-	H13	G10
	T32A09INC0	PR2	151	127	115	-	B9	B7
		PV0	115	97	89	-	F12	F10
	T32A09INC1	PR3	152	128	116	-	A9	A7
		PV1	114	96	88	-	G13	F11
	T32A09OUTC	PL6	164	-	-	-	E7	-
		PV2	113	95	87	-	G12	G11
	T32A10INA0	PR4	153	129	-	-	A8	D7
		PW4	120	-	-	-	G15	-
	T32A10INA1	PW7	117	-	-	-	H16	-
	T32A10OUTA	PC4	7	7	-	-	C1	C1
		PW5	119	-	-	-	G16	-
	T32A10INB0	PR5	154	130	-	-	B8	E7
	T32A10OUTB	PC5	6	6	-	-	C2	C2
		PW4	120	-	-	-	G15	-
	T32A10INC0	PR4	153	129	-	-	A8	D7
	T32A10INC1	PR5	154	130	-	-	B8	E7
	T32A10OUTC	PC4	7	7	-	-	C1	C1
		PW5	119	-	-	-	G16	-

Table 3.12 Signal connection list (12/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
32-bit Timer Event Counter	T32A11INA0	PR6	155	131	-	-	E9	E6
		PW7	117	-	-	-	H16	-
	T32A11INA1	PW4	120	-	-	-	G15	-
	T32A11OUTA	PM2	122	100	-	-	F16	E14
		PW6	118	-	-	-	H15	-
	T32A11INB0	PR7	156	132	-	-	D8	D6
	T32A11OUTB	PM3	121	99	-	-	E13	F13
		PW7	117	-	-	-	H16	-
	T32A11INC0	PR6	155	131	-	-	E9	E6
	T32A11INC1	PR7	156	132	-	-	D8	D6
	T32A11OUTC	PM2	122	100	-	-	F16	E14
		PW6	118	-	-	-	H15	-
	T32A12INA0	PU2	36	-	-	-	J5	-
	T32A12OUTA	PU0	34	-	-	-	H4	-
	T32A12INB0	PU3	37	-	-	-	K4	-
	T32A12OUTB	PU1	35	-	-	-	J4	-
	T32A12INC0	PU2	36	-	-	-	J5	-
	T32A12INC1	PU3	37	-	-	-	K4	-
	T32A12OUTC	PU0	34	-	-	-	H4	-
	T32A13INA0	PU5	39	-	-	-	L5	-
	T32A13OUTA	PU6	40	-	-	-	L4	-
	T32A13INB0	PU4	38	-	-	-	K5	-
	T32A13OUTB	PU7	41	-	-	-	M4	-
	T32A13INC0	PU5	39	-	-	-	L5	-
	T32A13INC1	PU4	38	-	-	-	K5	-
	T32A13OUTC	PU6	40	-	-	-	L4	-

Table 3.13 Signal connection list (13/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
External Bus Interface	EA00	PA0	29	29	25	20	L1	J4
	EA01	PA1	28	28	24	19	L2	J1
	EA02	PA2	27	27	23	18	K1	J2
	EA03	PA3	26	26	22	17	K2	H1
	EA04	PA4	25	25	21	16	J1	H2
	EA05	PA5	24	24	20	15	J2	G1
	EA06	PA6	23	23	19	14	H1	G2
	EA07	PA7	22	22	18	13	H2	J5
	EA08	PB0	21	21	17	12	G1	H4
	EA09	PB1	20	20	16	11	G2	H5
	EA10	PB2	19	19	15	10	F1	F1
	EA11	PB3	18	18	14	9	F2	F2
	EA12	PB4	17	17	13	8	E1	E1
	EA13	PB5	16	16	12	7	E2	E2
	EA14	PB6	15	15	11	6	G4	G4
	EA15	PB7	14	14	10	5	G5	G5
	EA16	PC0	11	11	7	-	F4	F4
		PE7	65	57	53	44	T8	N8
	EA17	PC1	10	10	6	-	F5	F5
		PE6	64	56	52	43	T7	N7
	EA18	PC2	9	9	5	-	D1	D1
		PE5	63	55	51	42	R7	P7
	EA19	PC3	8	8	4	-	D2	D2
		PE4	62	54	50	41	R6	P6
	EA20	PC4	7	7	-	-	C1	C1
		PE3	61	53	49	40	T6	N6
	EA21	PC5	6	6	-	-	C2	C2
		PE2	60	52	48	39	T5	P5
	EA22	PC6	5	5	-	-	E4	E4
		PE1	59	51	47	38	R5	N5
	EA23	PC7	4	4	-	-	D4	D4
		PE0	58	50	46	37	R4	N4

Table 3.14 Signal connection list (14/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
External Bus Interface	ED00/EAD00	PD0	48	40	36	29	N5	L4
	ED01/EAD01	PD1	49	41	37	30	M6	L5
	ED02/EAD02	PD2	50	42	38	31	N6	K6
	ED03/EAD03	PD3	51	43	39	32	M7	L6
	ED04/EAD04	PD4	52	44	40	33	N7	L7
	ED05/EAD05	PD5	53	45	41	34	M8	K7
	ED06/EAD06	PD6	54	46	42	35	N8	K8
	ED07/EAD07	PD7	55	47	43	36	M9	L8
	ED08/EAD08	PE0	58	50	46	37	R4	N4
	ED09/EAD09	PE1	59	51	47	38	R5	N5
	ED10/EAD10	PE2	60	52	48	39	T5	P5
	ED11/EAD11	PE3	61	53	49	40	T6	N6
	ED12/EAD12	PE4	62	54	50	41	R6	P6
	ED13/EAD13	PE5	63	55	51	42	R7	P7
	ED14/EAD14	PE6	64	56	52	43	T7	N7
	ED15/EAD15	PE7	65	57	53	44	T8	N8
	ERD_N	PF0	172	140	124	97	D5	D5
	EWR_N	PF1	173	141	125	98	A4	B5
	ECS0_N	PK2	109	91	83	69	J13	F14
	ECS1_N	PK3	108	90	82	68	K13	G13
	ECS2_N	PF4	176	144	128	-	A2	A2
	ECS3_N	PF5	1	1	1	-	B3	B3
	EBELL_N	PF6	2	2	2	1	B2	B2
	EBELH_N	PF7	3	3	3	2	B1	B1
	EALE	PG0	129	105	93	72	D15	D13
	EWAIT_N	PG1	130	106	94	73	C16	C14
	EEXBCLK	PY4	30	30	26	21	M2	K2

Table 3.15 Signal connection list (15/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
12-bit Analog to Digital Converter Product Information	AINA00	PN0	133	109	97	76	B15	B13
	AINA01	PN1	134	110	98	77	A15	A13
	AINA02	PN2	135	111	99	78	B14	B12
	AINA03	PN3	136	112	100	79	A14	A12
	AINA04	PN4	137	113	101	80	B13	B11
	AINA05	PN5	138	114	102	81	A13	A11
	AINA06	PN6	139	115	103	82	B12	B10
	AINA07	PN7	140	116	104	83	A12	A10
	AINA08	PP0	141	117	105	84	D12	D11
	AINA09	PP1	142	118	106	85	D11	D10
	AINA10	PP2	143	119	107	86	B11	B9
	AINA11	PP3	144	120	108	87	A11	A9
	AINA12	PP4	145	121	109	88	E11	D9
	AINA13	PP5	146	122	110	89	D10	E9
	AINA14	PP6	147	123	111	90	B10	B8
	AINA15	PP7	148	124	112	91	A10	A8
	AINA16	PR0	149	125	113	-	E10	D8
	AINA17	PR1	150	126	114	-	D9	E8
	AINA18	PR2	151	127	115	-	B9	B7
	AINA19	PR3	152	128	116	-	A9	A7
	AINA20	PR4	153	129	-	-	A8	D7
	AINA21	PR5	154	130	-	-	B8	E7
	AINA22	PR6	155	131	-	-	E9	E6
	AINA23	PR7	156	132	-	-	D8	D6
	TRGIN0	PG3	132	108	96	75	B16	B14
	TRGIN1	PL7	163	-	-	-	E8	-
8-bit Digital to Analog Converter	DAC0	PT0	159	135	119	94	A6	A5
	DAC1	PT1	160	136	120	95	A5	A4

Table 3.16 Signal connection list (16/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
EXCEPTION	INT00a	PK7	104	86	78	64	K12	J10
	INT00b	PT3	31	31	27	22	H5	K4
	INT01a	PL0	103	85	77	63	L13	J11
	INT01b	PT4	116	98	90	-	F13	E11
	INT02a	PA0	29	29	25	20	L1	J4
	INT02b	PT5	73	61	57	-	R10	K9
	INT03a	PA7	22	22	18	13	H2	J5
	INT03b	PL6	164	-	-	-	E7	-
	INT04a	PB0	21	21	17	12	G1	H4
	INT04b	PF0	172	140	124	97	D5	D5
	INT05a	PB1	20	20	16	11	G2	H5
	INT05b	PF7	3	3	3	2	B1	B1
	INT06a	PB6	15	15	11	6	G4	G4
	INT06b	PU2	36	-	-	-	J5	-
	INT07a	PB7	14	14	10	5	G5	G5
	INT07b	PU3	37	-	-	-	K4	-
	INT08a	PG0	129	105	93	72	D15	D13
	INT08b	PU4	38	-	-	-	K5	-
	INT09a	PG1	130	106	94	73	C16	C14
	INT09b	PU5	39	-	-	-	L5	-
	INT10a	PK0	111	93	85	71	H12	H10
	INT10b	PP6	147	123	111	90	B10	B8
	INT11a	PK1	110	92	84	70	J12	H11
	INT11b	PP7	148	124	112	91	A10	A8
	INT12a	PC0	11	11	7	-	F4	F4
	INT12b	PL4	126	-	-	-	D16	-
	INT13a	PC1	10	10	6	-	F5	F5
	INT13b	PL5	125	-	-	-	E15	-
	INT14a	PC6	5	5	-	-	E4	E4
	INT14b	PM3	121	99	-	-	E13	F13
	INT15a	PC7	4	4	-	-	D4	D4
	INT15b	PM4	85	69	-	-	N12	L10

Table 3.17 Signal connection list (17/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
Advanced Programmable Motor Control Circuit	EMG0	PD6	54	46	42	35	N8	K8
		PV6	79	63	59	-	T11	N9
	OVV0	PD7	55	47	43	36	M9	L8
		PV7	78	62	58	-	R11	L9
	UO0	PD0	48	40	36	29	N5	L4
		PV0	115	97	89	-	F12	F10
	VO0	PD2	50	42	38	31	N6	K6
		PV2	113	95	87	-	G12	G11
	WO0	PD4	52	44	40	33	N7	L7
		PV4	81	65	61	-	R12	N10
	XO0	PD1	49	41	37	30	M6	L5
		PV1	114	96	88	-	G13	F11
	YO0	PD3	51	43	39	32	M7	L6
		PV3	112	94	86	-	H13	G10
	ZO0	PD5	53	45	41	34	M8	K7
		PV5	80	64	60	-	T12	P9
Consumer Electronics Control	CEC0	PT2	171	139	123	96	E6	E5
Real Time Clock	ALARM_N	PG2	131	107	95	74	C15	C13
	RTCOUT	PT3	31	31	27	22	H5	K4
Remote Control Signal preprocessor	RXIN0	PT3	31	31	27	22	H5	K4
	RXIN1	PT4	116	98	90	-	F13	E11
Multi-function DMA Controller Product Information	TRGIN2	PT3	31	31	27	22	H5	K4
High Speed DMA Controller Product Information	HDMAREQA	PB1	20	20	16	11	G2	H5
	HDMAREQB	PK1	110	92	84	70	J12	H11

Table 3.18 Signal connection list (18/18)

Related Reference Manual	Function pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
Debug Interface Boundary-Scan	TMS	PH4	89	73	65	51	R16	N14
	TCK	PH5	88	72	64	50	T15	P13
	TDO	PH6	87	71	63	49	R15	P12
	TDI	PH3	90	74	66	52	P15	N13
	TRST_N	PH7	86	70	62	48	R14	N12
	BSC	-	-	-	-	-	T16	P14
Debug Interface	SWDIO	PH4	89	73	65	51	R16	N14
	SWCLK	PH5	88	72	64	50	T15	P13
	SWV	PH6	87	71	63	49	R15	P12
	TRACECLK	PG6	95	79	71	57	M16	L14
	TRACEDATA0	PG7	94	78	70	56	M15	L13
	TRACEDATA1	PH0	93	77	69	55	N16	L11
	TRACEDATA2	PH1	92	76	68	54	N15	M13
	TRACEDATA3	PH2	91	75	67	53	P16	M14
Non Break Debug Interface	NBDCLK	PG6	95	79	71	57	M16	L14
	NBDDATA0	PG7	94	78	70	56	M15	L13
	NBDDATA1	PH0	93	77	69	55	N16	L11
	NBDDATA2	PH1	92	76	68	54	N15	M13
	NBDDATA3	PH2	91	75	67	53	P16	M14
	NBDSYNC	PH3	90	74	66	52	P15	N13
Clock Control and Operation Mode	X1	PY0	45	37	33	26	T2	P2
	X2	PY1	46	38	34	27	T3	P3
	XT1	PY2	44	36	32	25	P1	M1
	XT2	PY3	43	35	31	24	N1	L1
	EHCLKIN	PY0	45	37	33	26	T2	P2
	ELCLKIN	PY2	44	36	32	25	P1	M1
Flash Memory	BOOT_N	PY4	30	30	26	21	M2	K2

4. Registers

The following registers should be set appropriately to use the ports.

Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

”x” and ”n” in the following table show a port name and a function number, respectively.

Register Name		TYPE	Setting Value	Description
[PxDATA]	Data Register	R/W	0 or 1	Read from and write to a port.
[PxCR]	Output Control Register	R/W	0: Output disabled 1: Output enabled	Output control.
[PxFRn]	Function Register n	R/W	0: PORT 1: Function	Function setting. When 1 is set, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled.
[PxOD]	Open-Drain Control Register	R/W	0: CMOS 1: Open-drain	Programmable open-drain control. The programmable open-drain is a pseudo open-drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** = 1.
[PxPUP]	Pull-up Control Register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up control.
[PxPDN]	Pull-down Control Register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down control.
[PxIE]	Input Control Register	R/W	0: Input disabled 1: Input enabled	Input control. It takes maximum 100ns that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled.

4.1. List of Register

When the bit which is assigned to no functions is read, 0 is returned. The write to the bit is ignored.

Table 4.1 Ports base address

Peripheral function		Channel/Unit	Base address
Input/output ports	PA	-	0x400E0000
	PB	-	0x400E0100
	PC	-	0x400E0200
	PD	-	0x400E0300
	PE	-	0x400E0400
	PF	-	0x400E0500
	PG	-	0x400E0600
	PH	-	0x400E0700
	PJ	-	0x400E0800
	PK	-	0x400E0900
	PL	-	0x400E0A00
	PM	-	0x400E0B00
	PN	-	0x400E0C00
	PP	-	0x400E0D00
	PR	-	0x400E0E00
	PT	-	0x400E0F00
	PU	-	0x400E1000
	PV	-	0x400E1100
	PW	-	0x400E1200
	PY	-	0x400E1300

Table 4.2 Register List

Register Name	Address (Base+)	Port A	Port B	Port C	Port D	Port E
Data Register	0x0000	*[PADATA]*	*[PBDATA]*	*[PCDATA]*	*[PDDATA]*	*[PEDATA]*
Output Control Register	0x0004	*[PACR]*	*[PBCR]*	*[PCCR]*	*[PDCR]*	*[PECR]*
Function Register 1	0x0008	*[PAFR1]*	*[PBFR1]*	*[PCFR1]*	*[PDFR1]*	*[PEFR1]*
Function Register 2	0x000C	*[PAFR2]*	*[PBFR2]*	-	*[PDFR2]*	*[PEFR2]*
Function Register 3	0x0010	*[PAFR3]*	*[PBFR3]*	*[PCFR3]*	*[PDFR3]*	*[PEFR3]*
Function Register 4	0x0014	-	-	-	*[PDFR4]*	*[PEFR4]*
Function Register 5	0x0018	*[PAFR5]*	*[PBFR5]*	*[PCFR5]*	*[PDFR5]*	*[PEFR5]*
Function Register 6	0x001C	*[PAFR6]*	*[PBFR6]*	-	*[PDFR6]*	-
Function Register 7	0x0020	*[PAFR7]*	-	-	*[PDFR7]*	*[PEFR7]*
Open-Drain Control Register	0x0028	*[PAOD]*	*[PBOD]*	*[PCOD]*	*[PDOD]*	*[PEOD]*
Pull-up Control Register	0x002C	*[PAPUP]*	*[PBPUP]*	*[PCPUP]*	*[PDPUP]*	*[PEPUP]*
Pull-down Control Register	0x0030	*[PAPDN]*	*[PBPDN]*	*[PCPDN]*	*[PDPDN]*	*[PEPDN]*
Input Control Register	0x0038	*[PAIE]*	*[PBIE]*	*[PCIE]*	*[PDIE]*	*[PEIE]*

Register Name	Address (Base+)	Port F	Port G	Port H	Port J	Port K
Data Register	0x0000	*[PFDATA]*	*[PGDATA]*	*[PHDATA]*	*[PJDATA]*	*[PKDATA]*
Output Control Register	0x0004	*[PFCR]*	*[PGCR]*	*[PHCR]*	*[PJCR]*	*[PKCR]*
Function Register 1	0x0008	*[PFFR1]*	*[PGFR1]*	*[PHFR1]*	-	*[PKFR1]*
Function Register 2	0x000C	-	*[PGFR2]*	-	*[PJFR2]*	*[PKFR2]*
Function Register 3	0x0010	-	*[PGFR3]*	*[PHFR3]*	*[PJFR3]*	*[PKFR3]*
Function Register 4	0x0014	-	*[PGFR4]*	*[PHFR4]*	-	*[PKFR4]*
Function Register 5	0x0018	-	*[PGFR5]*	*[PHFR5]*	*[PJFR5]*	-
Function Register 6	0x001C	-	-	-	-	*[PKFR6]*
Function Register 7	0x0020	*[PFFR7]*	*[PGFR7]*	-	*[PJFR7]*	*[PKFR7]*
Open-Drain Control Register	0x0028	*[PFOD]*	*[PGOD]*	*[PHOD]*	*[PJOD]*	*[PKOD]*
Pull-up Control Register	0x002C	*[PFPUP]*	*[PGPUP]*	*[PHPUP]*	*[PJPUP]*	*[PKPUP]*
Pull-down Control Register	0x0030	*[PFPDN]*	*[PGPDN]*	*[PHPDN]*	*[PJPDN]*	*[PKPDN]*
Input Control Register	0x0038	*[PFIE]*	*[PGIE]*	*[PHIE]*	*[PJIE]*	*[PKIE]*

Register Name	Address (Base+)	Port L	Port M	Port N	Port P	Port R
Data Register	0x0000	*[PLDATA]*	*[PMDATA]*	*[PNDATA]*	*[PPDATA]*	*[PRDATA]*
Output Control Register	0x0004	*[PLCR]*	*[PMCR]*	*[PNCR]*	*[PPCR]*	*[PRCR]*
Function Register 1	0x0008	*[PLFR1]*	-	-	-	-
Function Register 2	0x000C	*[PLFR2]*	*[PMFR2]*	-	*[PPFR2]*	*[PRFR2]*
Function Register 3	0x0010	*[PLFR3]*	*[PMFR3]*	-	*[PPFR3]*	*[PRFR3]*
Function Register 4	0x0014	-	*[PMFR4]*	-	-	-
Function Register 5	0x0018	-	*[PMFR5]*	-	*[PPFR5]*	-
Function Register 6	0x001C	*[PLFR6]*	*[PMFR6]*	-	-	-
Function Register 7	0x0020	*[PLFR7]*	*[PMFR7]*	-	-	-
Open-Drain Control Register	0x0028	*[PLOD]*	*[PMOD]*	*[PNOD]*	*[PPOD]*	*[PROD]*
Pull-up Control Register	0x002C	*[PLPUP]*	*[PMPUP]*	*[PNPUP]*	*[PPPUP]*	*[PRPUP]*
Pull-down Control Register	0x0030	*[PLPDN]*	*[PMPDN]*	*[PNPDN]*	*[PPPDN]*	*[PRPDN]*
Input Control Register	0x0038	*[PLIE]*	*[PMIE]*	*[PNIE]*	*[PPIE]*	*[PRIE]*

Register Name	Address (Base+)	Port T	Port U	Port V	Port W	Port Y
Data Register	0x0000	*[PTDATA]*	*[PUDATA]*	*[PVDATA]*	*[PWDATA]*	*[PYDATA]*
Output Control Register	0x0004	*[PTCR]*	*[PUCR]*	*[PVCR]*	*[PWCR]*	*[PYCR]*
Function Register 1	0x0008	*[PTFR1]*	-	-	-	*[PYFR1]*
Function Register 2	0x000C	*[PTFR2]*	*[PUFR2]*	*[PVFR2]*	-	-
Function Register 3	0x0010	*[PTFR3]*	*[PUFR3]*	*[PVFR3]*	*[PWFR3]*	-
Function Register 4	0x0014	-	-	*[PVFR4]*	*[PWFR4]*	*[PYFR4]*
Function Register 5	0x0018	-	-	*[PVFR5]*	*[PWFR5]*	-
Function Register 6	0x001C	*[PTFR6]*	-	*[PVFR6]*	*[PWFR6]*	-
Function Register 7	0x0020	*[PTFR7]*	*[PUFR7]*	*[PVFR7]*	*[PWFR7]*	-
Open-Drain Control Register	0x0028	*[PTOD]*	*[PUOD]*	*[PVOD]*	*[PWOD]*	*[PYOD]*
Pull-up Control Register	0x002C	*[PTPUP]*	*[PUPUP]*	*[PVPUP]*	*[PWPUP]*	*[PYPUP]*
Pull-down Control Register	0x0030	*[PTPDN]*	*[PUPDN]*	*[PVPDN]*	*[PWPDN]*	*[PYPDN]*
Input Control Register	0x0038	*[PTIE]*	*[PUIE]*	*[PVIE]*	*[PWIE]*	*[PYIE]*

Note: Do not access the addresses described as "-"

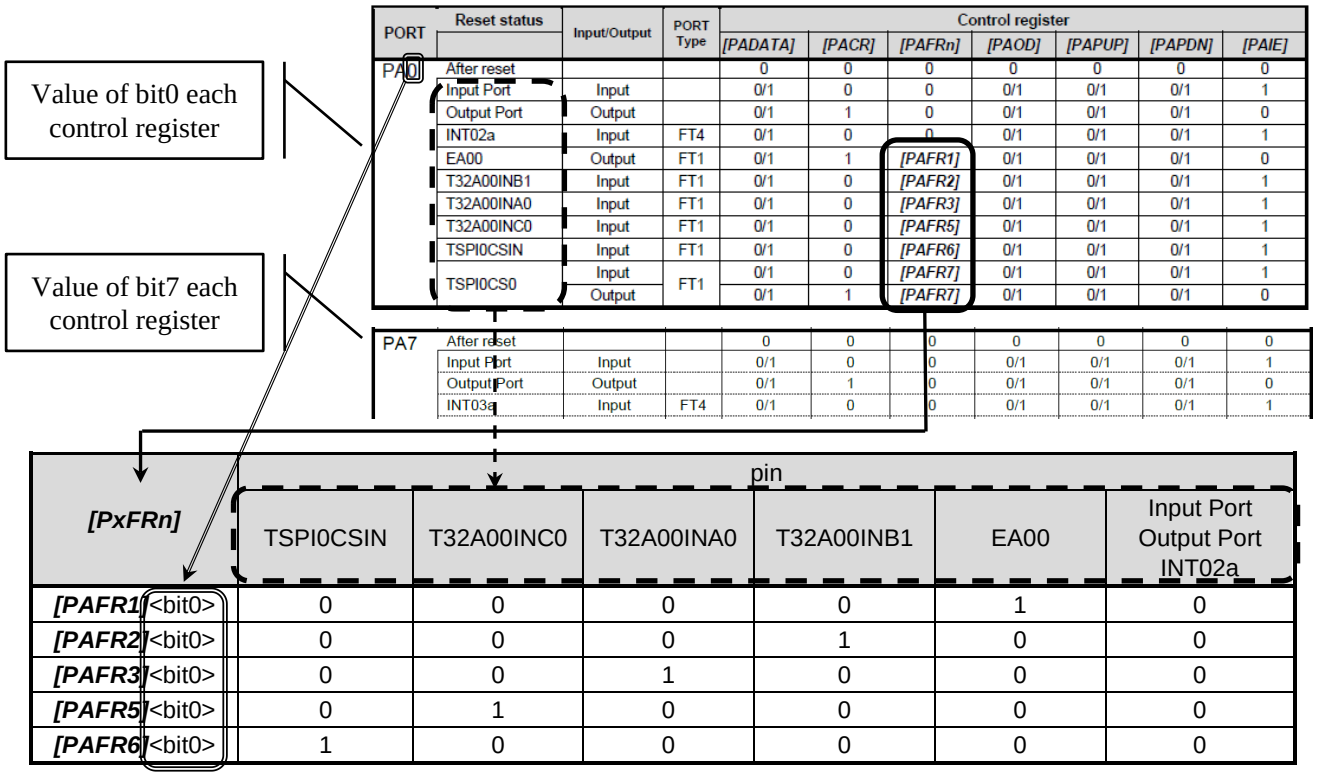
4.2. List of Port Functions and Settings

It is explained about viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the N/A in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.



PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	[PACR]	[PAFRn]	[PAOD]	[PAPUP]	[PAPDN]	[PAIE]
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA00	Output	FT1	0/1	1	[PAFR1]	0/1	0/1	0/1	0
	T32A00INB1	Input	FT1	0/1	0	[PAFR2]	0/1	0/1	0/1	1
	T32A00INA0	Input	FT1	0/1	0	[PAFR3]	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1	0/1	0	[PAFR5]	0/1	0/1	0/1	1
	TSPI0CSIN	Input	FT1	0/1	0	[PAFR6]	0/1	0/1	0/1	1
	TSPI0CS0	Input	FT1	0/1	0	[PAFR7]	0/1	0/1	0/1	1
		Output		0/1	1	[PAFR7]	0/1	0/1	0/1	0
PA7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1

[PxFRn]	TSPI0CSIN	T32A00INC0	T32A00INA0	T32A00INB1	EA00	Input Port Output Port INT02a
[PAFR1]<bit0>	0	0	0	0	1	0
[PAFR2]<bit0>	0	0	0	1	0	0
[PAFR3]<bit0>	0	0	1	0	0	0
[PAFR5]<bit0>	0	1	0	0	0	0
[PAFR6]<bit0>	1	0	0	0	0	0

4.2.1. Setting of using the alternated pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and enable output control register (***[PxCR]***<bit m>=1), then set the peripheral functions. If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), then set the peripheral functions.

To use peripheral functions such as I^2C, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), then set the peripheral function.

- When multiple functions are assigned same pin, please choose only one function for usage.
- When same function are assigned multiple pins, please the function use exclusively.

4.2.2. PORT A

Table 4.3 Port A registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA00	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A00INB1	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	T32A00INA0	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	TSPI0CSIN	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
	TSPI0CS0	Output	FT1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
PA1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA01	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA02	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A00OUTB	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FT1	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1
PA3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA03	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A00INA1	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	T32A00INB0	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A00INC1	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	TSPI2CS1	Output	FT1	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
	TSPI0TXD	Output	FT2	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
PA4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA04	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A01INB1	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	TSPI0CS1	Output	FT1	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
	TSPI2TXD	Output	FT2	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0

PA5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA05	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A01OUTA	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FT1	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
	TSPI0CS2	Output	FT1	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
	TSPI2RXD	Input	FT1	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1
PA6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA06	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A01OUTB	Output	FT1	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	TSPI0CS3	Output	FT1	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
	TSPI2SCK	Input	FT1	0/1	0	***[PAFR7]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PAFR7]***	0/1	0/1	0/1	0
PA7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA07	Output	FT1	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	T32A01INA1	Input	FT1	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	T32A01INB0	Input	FT1	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	TSPI2CSIN	Input	FT1	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
	TSPI2CS0	Output	FT1	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0

4.2.3. PORT B

Table 4.4 Port B registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBUP]*	*[PBPDN]*	*[PBIE]*
PB0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT04a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA08	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A02INB1	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	T32A02INA0	Input	FT1	0/1	0	***[PBFR3]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
PB1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA09	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A02INA1	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	T32A02INB0	Input	FT1	0/1	0	***[PBFR3]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
	HDMAREQA	Input	FT1	0/1	0	***[PBFR6]***	0/1	0/1	0/1	1
PB2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA10	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A02OUTA	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1	0/1	1	***[PBFR5]***	0/1	0/1	0/1	0
PB3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA11	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A02OUTB	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
PB4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA12	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FT1	0/1	1	***[PBFR5]***	0/1	0/1	0/1	0
PB5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA13	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A03OUTB	Output	FT1	0/1	1	***[PBFR3]***	0/1	0/1	0/1	0
PB6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT06a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA14	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A03INB1	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	T32A03INA0	Input	FT1	0/1	0	***[PBFR3]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1

PB7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA15	Output	FT1	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	T32A03INA1	Input	FT1	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	T32A03INB0	Input	FT1	0/1	0	***[PBFR3]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FT1	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1

4.2.4. PORT C

Table 4.5 Port C registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT12a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA16	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	T32A08INA0	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A08INC0	Input	FT1	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
PC1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT13a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA17	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	T32A08INB0	Input	FT1	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A08INC1	Input	FT1	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
PC2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA18	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	T32A08OUTA	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A08OUTC	Output	FT1	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
PC3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA19	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	T32A08OUTB	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
PC4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA20	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	T32A10OUTA	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A10OUTC	Output	FT1	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
PC5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EA21	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	T32A10OUTB	Output	FT1	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
PC6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT14a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA22	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
PC7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT15a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EA23	Output	FT1	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0

4.2.5. PORT D

Table 4.6 Port D registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED00/EAD00	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A04INB1	Input	FT1	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	T32A04INA0	Input	FT1	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1
	TSPI4CS0	Output	FT1	0/1	1	***[PDFR4]***	0/1	0/1	0/1	0
	T32A04INC0	Input	FT1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	TSPI4CSIN	Input	FT1	0/1	0	***[PDFR6]***	0/1	0/1	0/1	1
	UO0	Output	FT2	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
PD1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED01/EAD01	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A04INA1	Input	FT1	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	T32A04INB0	Input	FT1	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1
	TSPI4SCK	Input	FT1	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR4]***	0/1	0/1	0/1	0
	T32A04INC1	Input	FT1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	XO0	Output	FT2	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
PD2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED02/EAD02	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A04OUTA	Output	FT1	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	TSPI4RXD	Input	FT1	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
	T32A04OUTC	Output	FT1	0/1	1	***[PDFR5]***	0/1	0/1	0/1	0
	VO0	Output	FT2	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
PD3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED03/EAD03	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A04OUTB	Output	FT1	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	TSPI4TXD	Output	FT1	0/1	1	***[PDFR4]***	0/1	0/1	0/1	0
	YO0	Output	FT2	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
PD4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED04/EAD04	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A05OUTA	Output	FT1	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FT1	0/1	1	***[PDFR5]***	0/1	0/1	0/1	0
	WO0	Output	FT2	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0

PD5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED05/EAD05	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A05OUTB	Output	FT1	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	ZO0	Output	FT2	0/1	1	***[PDFR7]***	0/1	0/1	0/1	0
PD6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED06/EAD06	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A05INB1	Input	FT1	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	T32A05INA0	Input	FT1	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1
	T32A05INC0	Input	FT1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	EMG_N	Input	FT1	0/1	0	***[PDFR7]***	0/1	0/1	0/1	1
PD7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED07/EAD07	Input	FT14	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PDFR1]***	0/1	0/1	0/1	0
	T32A05INA1	Input	FT1	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	T32A05INB0	Input	FT1	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1
	T32A05INC1	Input	FT1	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1
	OVV0_N	Input	FT1	0/1	0	***[PDFR7]***	0/1	0/1	0/1	1

4.2.6. PORT E

Table 4.7 Port E registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED08/EAD08	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA23	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A06INB1	Input	FT1	0/1	0	***[PEFR2]***	0/1	0/1	0/1	1
	T32A06OUTB	Output	FT1	0/1	1	***[PEFR3]***	0/1	0/1	0/1	0
	T32A06INA1	Input	FT1	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	UT0RTS_N	Output	FT1	0/1	1	***[PEFR7]***	0/1	0/1	0/1	0
PE1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED09/EAD09	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA22	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A06OUTA	Output	FT1	0/1	1	***[PEFR3]***	0/1	0/1	0/1	0
	T32A06OUTC	Output	FT1	0/1	1	***[PEFR5]***	0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1	0/1	0	***[PEFR7]***	0/1	0/1	0/1	1
PE2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED10/EAD10	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA21	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A06INA0	Input	FT1	0/1	0	***[PEFR3]***	0/1	0/1	0/1	1
	T32A06INC0	Input	FT1	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	UT0RXD	Input	FT1	0/1	0	***[PEFR7]***	0/1	0/1	0/1	1
PE3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED11/EAD11	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA20	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A06INB0	Input	FT1	0/1	0	***[PEFR3]***	0/1	0/1	0/1	1
	T32A06INC1	Input	FT1	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1	0/1	1	***[PEFR7]***	0/1	0/1	0/1	0
PE4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED12/EAD12	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA19	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A07INA0	Input	FT1	0/1	0	***[PEFR3]***	0/1	0/1	0/1	1
	T32A07INC0	Input	FT1	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	ISDAIN0	Input	FT15	0/1	0	0	0/1	0/1	0/1	1

PE5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED13/EAD13	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA18	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A07INB0	Input	FT1	0/1	0	***[PEFR3]***	0/1	0/1	0/1	1
	T32A07INC1	Input	FT1	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	ISDAIN1	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
PE6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED14/EAD14	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA17	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A07OUTA	Output	FT1	0/1	1	***[PEFR3]***	0/1	0/1	0/1	0
	T32A07OUTC	Output	FT1	0/1	1	***[PEFR5]***	0/1	0/1	0/1	0
	ISDAIN2	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
PE7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ED15/EAD15	Input	FT14	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
	EA16	Output	FT1	0/1	1	***[PEFR4]***	0/1	0/1	0/1	0
	T32A07INB1	Input	FT1	0/1	0	***[PEFR2]***	0/1	0/1	0/1	1
	T32A07OUTB	Output	FT1	0/1	1	***[PEFR3]***	0/1	0/1	0/1	0
	T32A07INA1	Input	FT1	0/1	0	***[PEFR5]***	0/1	0/1	0/1	1
	ISDAIN3	Input	FT15	0/1	0	0	0/1	0/1	0/1	1

4.2.7. PORT F

Table 4.8 Port F registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT04b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	ERD_N	Output	FT1	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
PF1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EWR_N	Output	FT1	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
PF2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C1SDA	I/O	FT1	0/1	1	***[PFFR7]***	1	0/1	0/1	1
PF3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C1SCL	I/O	FT1	0/1	1	***[PFFR7]***	1	0/1	0/1	1
PF4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ECS2_N	Output	FT1	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
PF5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ECS3_N	Output	FT1	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
PF6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EBELL_N	Output	FT1	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0
PF7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EBELH_N	Output	FT1	0/1	1	***[PFFR1]***	0/1	0/1	0/1	0

4.2.8. PORT G

Table 4.9 Port G registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT08a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EALE	Output	FT1	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1	0/1	1	***[PGFR5]***	0/1	0/1	0/1	0
PG1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT09a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	EWAIT_N	Input	FT1	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
	UT2RXD	Input	FT1	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
PG2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2RTS_N	Output	FT1	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
	ALARM_N	Output	FT1	0/1	1	***[PGFR4]***	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	I2C0SDA	I/O	FT1	0/1	1	***[PGFR7]***	1	0/1	0/1	1
PG3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	TRGIN0	Input	FT1	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	UT2RTS_N	Output	FT1	0/1	1	***[PGFR5]***	0/1	0/1	0/1	0
	I2C0SCL	I/O	FT1	0/1	1	***[PGFR7]***	1	0/1	0/1	1
PG4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02OUTB	Output	FT1	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	FUT0IROUT	Output	FT1	0/1	1	***[PGFR4]***	0/1	0/1	0/1	0
	FUT0TXD	Output	FT1	0/1	1	***[PGFR5]***	0/1	0/1	0/1	0
	I2C2SDA	I/O	FT1	0/1	1	***[PGFR7]***	1	0/1	0/1	1
PG5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02OUTA	Output	FT1	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
	FUT0IRIN	Input	FT1	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	FUT0RXD	Input	FT1	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	I2C2SCL	I/O	FT1	0/1	1	***[PGFR7]***	1	0/1	0/1	1

PG6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TRACECLK	Output	FT1	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	NBDCLK	Input	FT3	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	FUT0RTS_N	Output	FT1	0/1	1	***[PGFR5]***	0/1	0/1	0/1	0
PG7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TRACEDATA0	Output	FT1	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	NBDDATA0	I/O	FT2b	0/1	1	***[PGFR4]***	0/1	0/1	0/1	1
	FUT0CTS_N	Input	FT1	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1

4.2.9. PORT H

Table 4.10 Port H registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PHDATA]	*[PHCR]*	*[PHFRn]*	*[PHOD]*	*[PHPUP]*	*[PHPDN]*	*[PHIE]*
PH0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TRACEDATA1	Output	FT1	0/1	1	***[PHFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FT1	0/1	0	***[PHFR3]***	0/1	0/1	0/1	1
	NBDDATA1	I/O	FT2b	0/1	1	***[PHFR4]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PHFR5]***	0/1	0/1	0/1	0
PH1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TRACEDATA2	Output	FT1	0/1	1	***[PHFR1]***	0/1	0/1	0/1	0
	UT1TXDA	Output	FT1	0/1	1	***[PHFR3]***	0/1	0/1	0/1	0
	NBDDATA2	I/O	FT2b	0/1	1	***[PHFR4]***	0/1	0/1	0/1	1
	UT1RXD	Input	FT1	0/1	0	***[PHFR5]***	0/1	0/1	0/1	1
PH2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TRACEDATA3	Output	FT1	0/1	1	***[PHFR1]***	0/1	0/1	0/1	0
	UT1RTS_N	Output	FT1	0/1	1	***[PHFR3]***	0/1	0/1	0/1	0
	NBDDATA3	I/O	FT2b	0/1	1	***[PHFR4]***	0/1	0/1	0/1	1
	UT1CTS_N	Input	FT1	0/1	0	***[PHFR5]***	0/1	0/1	0/1	1
PH3	After reset (TDI)	Input	FT2	0	0	***[PHFR1]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1	0/1	0	***[PHFR3]***	0/1	0/1	0/1	1
	NBDSYNC	Input	FT3	0/1	0	***[PHFR4]***	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PHFR5]***	0/1	0/1	0/1	0
PH4	After reset (TMS/SWDIO)	I/O	FT2	0	1 (Note)	***[PHFR1]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PHFR3]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1	0/1	1	***[PHFR5]***	0/1	0/1	0/1	0
PH5	After reset (TCK/SWCLK)	Input	FT2	0	0	***[PHFR1]***	0	0	1	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0TXDA	Output	FT1	0/1	1	***[PHFR3]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1	0/1	0	***[PHFR5]***	0/1	0/1	0/1	1
PH6	After reset (TDO/SWV)	Output	FT2	0	1 (Note)	***[PHFR1]***	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0RTS_N	Output	FT1	0/1	1	***[PHFR3]***	0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1	0/1	0	***[PHFR5]***	0/1	0/1	0/1	1
PH7	After reset (TRST_N)	Input	FT3	0	0	***[PHFR1]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1	0/1	0	***[PHFR3]***	0/1	0/1	0/1	1
	UT0RTS_N	Output	FT1	0/1	1	***[PHFR5]***	0/1	0/1	0/1	0

Note: When receive the command from TOOL, it becomes output.

4.2.10. PORT J

Table 4.11 Port J registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PJDATA]	*[PJCR]*	*[PJFRn]*	*[PJOD]*	*[PJPUP]*	*[PJPDN]*	*[PJIE]*
PJ0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5RXD	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	UT5TXDA	Output	FT1	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5TXDA	Output	FT1	0/1	1	***[PJFR3]***	0/1	0/1	0/1	0
	UT5RXD	Input	FT1	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
PJ2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5RTS_N	Output	FT1	0/1	1	***[PJFR3]***	0/1	0/1	0/1	0
	UT5CTS_N	Input	FT1	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
	I2C4SCL	I/O	FT1	0/1	1	***[PJFR7]***	1	0/1	0/1	1
PJ3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT5CTS_N	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	UT5RTS_N	Output	FT1	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
	I2C4SDA	I/O	FT1	0/1	1	***[PJFR7]***	1	0/1	0/1	1
PJ4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03INA0	Input	FT1	0/1	0	***[PJFR2]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	FUT0TXD	Output	FT1	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ5	After reset	Input		0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03INB0	Input	FT1	0/1	0	***[PJFR2]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FT1	0/1	0	***[PJFR3]***	0/1	0/1	0/1	1
	FUT0RXD	Input	FT1	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
PJ6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	FUT1TXD	Output	FT1	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
	I2C3SDA	I/O	FT1	0/1	1	***[PJFR7]***	1	0/1	0/1	1
PJ7	After reset	Input		0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	FUT1RXD	Input	FT1	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
	I2C3SCL	I/O	FT1	0/1	1	***[PJFR7]***	1	0/1	0/1	1

4.2.11. PORT K

Table 4.12 Port K registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PKDATA]	*[PKCR]*	*[PKFRn]*	*[PKOD]*	*[PKPUP]*	*[PKPDN]*	*[PKIE]*
PK0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT10a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	ISDAOUT	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	T32A00INA0	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	SMI0CS1_N	Output	FT1	0/1	1	***[PKFR6]***	0/1	0/1	0/1	0
PK1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT11a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	ISDBOUT	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	T32A00INB0	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A00INC1	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	HDMAREQB	Input	FT1	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
PK2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ECS0_N	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	SMI0D0	I/O	FT2	0/1	1	***[PKFR6]***	0/1	0/1	0/1	1
PK3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ECS1_N	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	SMI0D1	I/O	FT2	0/1	1	***[PKFR6]***	0/1	0/1	0/1	1
PK4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS1	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	TSPI3TXD	Output	FT2	0/1	1	***[PKFR4]***	0/1	0/1	0/1	0
	SMI0D2	I/O	FT2	0/1	1	***[PKFR6]***	0/1	0/1	0/1	1
PK5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS2	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	TSPI3RXD	Input	FT1	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
	SMI0D3	I/O	FT2	0/1	1	***[PKFR6]***	0/1	0/1	0/1	1

PK6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1CS3	Output	FT1	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	T32A01INA0	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	TSPI3SCK	Input	FT1	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PKFR4]***	0/1	0/1	0/1	0
	SMI0CLK	Output	FT1	0/1	1	***[PKFR6]***	0/1	0/1	0/1	0
PK7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A01INB0	Input	FT1	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FT1	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
	TSPI3CS0	Output	FT1	0/1	1	***[PKFR4]***	0/1	0/1	0/1	0
	SMI0CS0_N	Output	FT1	0/1	1	***[PKFR6]***	0/1	0/1	0/1	0
	TSPI3CSIN	Input	FT1	0/1	0	***[PKFR7]***	0/1	0/1	0/1	1

4.2.12. PORT L

Table 4.13 Port L registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PLDATA]	*[PLCR]*	*[PLFRn]*	*[PLOD]*	*[PLPUP]*	*[PLPDN]*	*[PLIE]*
PL0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01a	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A02INA0	Input	FT1	0/1	0	***[PLFR2]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FT1	0/1	0	***[PLFR3]***	0/1	0/1	0/1	1
	TSPI1CSIN	Input	FT1	0/1	0	***[PLFR6]***	0/1	0/1	0/1	1
	TSPI1CS0	Output	FT1	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1SCK	Input	FT1	0/1	0	***[PLFR7]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1RXD	Input	FT1	0/1	0	***[PLFR7]***	0/1	0/1	0/1	1
PL3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A02INB0	Input	FT1	0/1	0	***[PLFR2]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FT1	0/1	0	***[PLFR3]***	0/1	0/1	0/1	1
	TSPI3CS1	Output	FT1	0/1	1	***[PLFR6]***	0/1	0/1	0/1	0
	TSPI1TXD	Output	FT2	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT12b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A08OUTA	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0
	T32A08OUTC	Output	FT1	0/1	1	***[PLFR3]***	0/1	0/1	0/1	0
PL5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT13b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A08OUTB	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0
PL6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT03b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A09OUTA	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0
	T32A09OUTC	Output	FT1	0/1	1	***[PLFR3]***	0/1	0/1	0/1	0
PL7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TRGIN1	Input	FT1	0/1	0	***[PLFR1]***	0/1	0/1	0/1	1
	T32A09OUTB	Output	FT1	0/1	1	***[PLFR2]***	0/1	0/1	0/1	0

4.2.13. PORT M

Table 4.14 Port M registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PMDATA]	*[PMCR]*	*[PMFRn]*	*[PMOD]*	*[PMPUP]*	*[PMPDN]*	*[PMIE]*
PM0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C3SDA	I/O	FT1	0/1	1	***[PMFR4]***	1	0/1	0/1	1
	UT4RXD	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TSPI6TXD	Output	FT2	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
	UT4TXDA	Output	FT1	0/1	1	***[PMFR7]***	0/1	0/1	0/1	0
PM1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	I2C3SCL	I/O	FT1	0/1	1	***[PMFR4]***	1	0/1	0/1	1
	UT4TXDA	Output	FT1	0/1	1	***[PMFR5]***	0/1	0/1	0/1	0
	TSPI6RXD	Input	FT1	0/1	0	***[PMFR6]***	0/1	0/1	0/1	1
	UT4RXD	Input	FT1	0/1	0	***[PMFR7]***	0/1	0/1	0/1	1
PM2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A11OUTA	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	T32A11OUTC	Output	FT1	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	UT4RTS_N	Output	FT1	0/1	1	***[PMFR5]***	0/1	0/1	0/1	0
	TSPI6SCK	Input	FT1	0/1	0	***[PMFR6]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
	UT4CTS_N	Input	FT1	0/1	0	***[PMFR7]***	0/1	0/1	0/1	1
PM3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT14b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A11OUTB	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	TSPI6CSIN	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	UT4CTS_N	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TSPI6CS0	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
	UT4RTS_N	Output	FT1	0/1	1	***[PMFR7]***	0/1	0/1	0/1	0
PM4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT15b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A06OUTB	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	TSPI7CSIN	Input	FT1	0/1	0	***[PMFR4]***	0/1	0/1	0/1	1
	TSPI7CS0	Output	FT1	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
	FUT1CTS_N	Input	FT1	0/1	0	***[PMFR7]***	0/1	0/1	0/1	1
PM5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A06OUTA	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	T32A06OUTC	Output	FT1	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	TSPI7SCK	Input	FT1	0/1	0	***[PMFR6]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
	FUT1RTS_N	Output	FT1	0/1	1	***[PMFR7]***	0/1	0/1	0/1	0

PM6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A07OUTA	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	T32A07OUTC	Output	FT1	0/1	1	***[PMFR3]***	0/1	0/1	0/1	0
	I2C4SDA	I/O	FT1	0/1	1	***[PMFR4]***	1	0/1	0/1	1
	FUT1IRIN	Input	FT1	0/1	0	***[PMFR5]***	0/1	0/1	0/1	1
	TSPI7RXD	Input	FT1	0/1	0	***[PMFR6]***	0/1	0/1	0/1	1
	FUT1RXD	Input	FT1	0/1	0	***[PMFR7]***	0/1	0/1	0/1	1
PM7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A07OUTB	Output	FT1	0/1	1	***[PMFR2]***	0/1	0/1	0/1	0
	I2C4SCL	I/O	FT1	0/1	1	***[PMFR4]***	1	0/1	0/1	1
	FUT1IROUT	Output	FT1	0/1	1	***[PMFR5]***	0/1	0/1	0/1	0
	TSPI7TXD	Output	FT2	0/1	1	***[PMFR6]***	0/1	0/1	0/1	0
	FUT1TXD	Output	FT1	0/1	1	***[PMFR7]***	0/1	0/1	0/1	0

4.2.14. PORT N

Table 4.15 Port N registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PNDATA]	*[PNCR]*	*[PNFRn]*	*[PNOD]*	*[PNPUP]*	*[PNPDN]*	*[PNIE]*
PN0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA00(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PN1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA01(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PN2	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA02(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PN3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA03(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PN4	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA04(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PN5	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA05(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PN6	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA06(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0
PN7	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA07(Note)	Input	FT5	0/1	0	N/A	0/1	0	0	0

Note: When using analog input(AINAx), ***[PNCR]*** should be output disable “0”,***[PNIE]*** should be input disable “0” , ***[PNPUP]*** should be pull-up disable”0” and ***[PNPDN]*** should be pull-down disable “0”.

4.2.15. PORT P

Table 4.16 Port P registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PPDATA]	*[PPCR]*	*[PPFRn]*	*[PPOD]*	*[PPPUP]*	*[PPPDN]*	*[PPIE]*
PP0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA08(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A04INA0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A04INC0	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A04INB1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1
PP1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA09(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A04INB0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A04INC1	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A04INA1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1
PP2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA10(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A05INA0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A05INC0	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A05INB1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1
PP3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA11(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A05INB0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A05INC1	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A05INA1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1
PP4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA12(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A06INA0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A06INC0	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A06INB1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1
PP5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA13(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A06INB0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A06INC1	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A06INA1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1
PP6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA14(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	INT10b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A07INA0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A07INC0	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A07INB1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1

PP7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA15(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	INT11b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A07INB0	Input	FT1	0/1	0	***[PPFR2]***	0/1	0/1	0/1	1
	T32A07INC1	Input	FT1	0/1	0	***[PPFR3]***	0/1	0/1	0/1	1
	T32A07INA1	Input	FT1	0/1	0	***[PPFR5]***	0/1	0/1	0/1	1

Note: When using analog input(AINAx), ***[PPCR]*** should be output disable “0”,***[PPIE]*** should be input disable “0” , ***[PPPUP]*** should be pull-up disable”0” and ***[PPPDN]*** should be pull-down disable “0”.

4.2.16. PORT R

Table 4.17 Port R registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PRDATA]	*[PRCR]*	*[PRFRn]*	*[PROD]*	*[PRPUP]*	*[PRPDN]*	*[PRIE]*
PR0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA16(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A08INA0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A08INC0	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
PR1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA17(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A08INB0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A08INC1	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
PR2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA18(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A09INA0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A09INC0	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
PR3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA19(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A09INB0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A09INC1	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
PR4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA20(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A10INA0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A10INC0	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
PR5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA21(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A10INB0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A10INC1	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
PR6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA22(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A11INA0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A11INC0	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1
PR7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	AINA23(Note)	Input	FT5	0/1	0	0	0/1	0	0	0
	T32A11INB0	Input	FT1	0/1	0	***[PRFR2]***	0/1	0/1	0/1	1
	T32A11INC1	Input	FT1	0/1	0	***[PRFR3]***	0/1	0/1	0/1	1

Note: When using analog input(AINAx), ***[PRCR]*** should be output disable “0”,***[PRIE]*** should be input disable “0” , ***[PRPUP]*** should be pull-up disable”0” and ***[PRPDN]*** should be pull-down disable “0”.

4.2.17. PORT T

Table 4.18 Port T registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PTDATA]	*[PTCR]*	*[PTFRn]*	*[PTOD]*	*[PTPUP]*	*[PTPDN]*	*[PTIE]*
PT0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	DAC0 (Note)	Output	FT13	0/1	0	N/A	0/1	0	0	0
PT1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	DAC1 (Note)	Output	FT13	0/1	0	N/A	0/1	0	0	0
PT2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	CEC0	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
		I/O	FT1	0/1	1	***[PTFR7]***	0/1	0/1	0/1	1
PT3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	RTCOUT	Output	FT1	0/1	1	***[PTFR1]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FT1	0/1	1	***[PTFR2]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FT1	0/1	1	***[PTFR3]***	0/1	0/1	0/1	0
	RXIN0	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	TRGIN2	Input	FT1	0/1	0	***[PTFR6]***	0/1	0/1	0/1	1
PT4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT01b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	RXIN1	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
PT5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT02b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A03OUTB	Output	FT1	0/1	1	***[PTFR2]***	0/1	0/1	0/1	0

Note: When using analog output, ***[PTCR]*** should be output disable “0”,***[PTIE]*** should be input disable “0” , ***[PTPUP]*** should be pull-up disable”0” and ***[PTPDN]*** should be pull-down disable “0”.

4.2.18. PORT U

Table 4.19 Port U registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PUDATA]	*[PUCR]*	*[PUFRn]*	*[PUOD]*	*[PUPUP]*	*[PUPDN]*	*[PUIE]*
PU0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A12OUTA	Output	FT1	0/1	1	***[PUFR2]***	0/1	0/1	0/1	0
	T32A12OUTC	Output	FT1	0/1	1	***[PUFR3]***	0/1	0/1	0/1	0
	UT4TXDA	Output	FT1	0/1	1	***[PUFR7]***	0/1	0/1	0/1	0
PU1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A12OUTB	Output	FT1	0/1	1	***[PUFR2]***	0/1	0/1	0/1	0
	UT4RXD	Input	FT1	0/1	0	***[PUFR7]***	0/1	0/1	0/1	1
PU2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT06b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A12INA0	Input	FT1	0/1	0	***[PUFR2]***	0/1	0/1	0/1	1
	T32A12INC0	Input	FT1	0/1	0	***[PUFR3]***	0/1	0/1	0/1	1
	UT4CTS_N	Input	FT1	0/1	0	***[PUFR7]***	0/1	0/1	0/1	1
PU3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A12INB0	Input	FT1	0/1	0	***[PUFR2]***	0/1	0/1	0/1	1
	T32A12INC1	Input	FT1	0/1	0	***[PUFR3]***	0/1	0/1	0/1	1
	UT4RTS_N	Output	FT1	0/1	1	***[PUFR7]***	0/1	0/1	0/1	0
PU4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT08b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A13INB0	Input	FT1	0/1	0	***[PUFR2]***	0/1	0/1	0/1	1
	T32A13INC1	Input	FT1	0/1	0	***[PUFR3]***	0/1	0/1	0/1	1
	UT3RTS_N	Output	FT1	0/1	1	***[PUFR7]***	0/1	0/1	0/1	0
PU5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT09b	Input	FT4	0/1	0	0	0/1	0/1	0/1	1
	T32A13INA0	Input	FT1	0/1	0	***[PUFR2]***	0/1	0/1	0/1	1
	T32A13INC0	Input	FT1	0/1	0	***[PUFR3]***	0/1	0/1	0/1	1
	UT3CTS_N	Input	FT1	0/1	0	***[PUFR7]***	0/1	0/1	0/1	1
PU6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A13OUTA	Output	FT1	0/1	1	***[PUFR2]***	0/1	0/1	0/1	0
	T32A13OUTC	Output	FT1	0/1	1	***[PUFR3]***	0/1	0/1	0/1	0
	UT3RXD	Input	FT1	0/1	0	***[PUFR7]***	0/1	0/1	0/1	1
PU7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A13OUTB	Output	FT1	0/1	1	***[PUFR2]***	0/1	0/1	0/1	0
	UT3TXDA	Output	FT1	0/1	1	***[PUFR7]***	0/1	0/1	0/1	0

4.2.19. PORT V

Table 4.20 Port V registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PVDATA]	*[PVCR]*	*[PVFRn]*	*[PVOD]*	*[PVPUP]*	*[PVPDN]*	*[PVIE]*
PV0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A09INA0	Input	FT1	0/1	0	***[PVFR2]***	0/1	0/1	0/1	1
	T32A09INC0	Input	FT1	0/1	0	***[PVFR3]***	0/1	0/1	0/1	1
	ISDBIN0	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	UO0	Output	FT2	0/1	1	***[PVFR5]***	0/1	0/1	0/1	0
	UT3RXD	Input	FT1	0/1	0	***[PVFR6]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FT1	0/1	1	***[PVFR7]***	0/1	0/1	0/1	0
PV1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A09INB0	Input	FT1	0/1	0	***[PVFR2]***	0/1	0/1	0/1	1
	T32A09INC1	Input	FT1	0/1	0	***[PVFR3]***	0/1	0/1	0/1	1
	ISDBIN1	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	XO0	Output	FT2	0/1	1	***[PVFR5]***	0/1	0/1	0/1	0
	UT3TXDA	Output	FT1	0/1	1	***[PVFR6]***	0/1	0/1	0/1	0
	UT3RXD	Input	FT1	0/1	0	***[PVFR7]***	0/1	0/1	0/1	1
PV2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A09OUTA	Output	FT1	0/1	1	***[PVFR2]***	0/1	0/1	0/1	0
	T32A09OUTC	Output	FT1	0/1	1	***[PVFR3]***	0/1	0/1	0/1	0
	ISDBIN2	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	VO0	Output	FT2	0/1	1	***[PVFR5]***	0/1	0/1	0/1	0
	UT3RTS_N	Output	FT1	0/1	1	***[PVFR6]***	0/1	0/1	0/1	0
	UT3CTS_N	Input	FT1	0/1	0	***[PVFR7]***	0/1	0/1	0/1	1
PV3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A09OUTB	Output	FT1	0/1	1	***[PVFR2]***	0/1	0/1	0/1	0
	ISDBIN3	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	YO0	Output	FT2	0/1	1	***[PVFR5]***	0/1	0/1	0/1	0
	UT3CTS_N	Input	FT1	0/1	0	***[PVFR6]***	0/1	0/1	0/1	1
	UT3RTS_N	Output	FT1	0/1	1	***[PVFR7]***	0/1	0/1	0/1	0
PV4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04OUTB	Output	FT1	0/1	1	***[PVFR2]***	0/1	0/1	0/1	0
	TSPI5RXD	Input	FT1	0/1	0	***[PVFR4]***	0/1	0/1	0/1	1
	WO0	Output	FT2	0/1	1	***[PVFR5]***	0/1	0/1	0/1	0
	I2C2SCL	I/O	FT1	0/1	1	***[PMFR6]***	1	0/1	0/1	1
	UT1RXD	Input	FT1	0/1	0	***[PVFR7]***	0/1	0/1	0/1	1
PV5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A04OUTA	Output	FT1	0/1	1	***[PVFR2]***	0/1	0/1	0/1	0
	T32A04OUTC	Output	FT1	0/1	1	***[PVFR3]***	0/1	0/1	0/1	0
	TSPI5TXD	Output	FT2	0/1	1	***[PVFR4]***	0/1	0/1	0/1	0
	ZO0	Output	FT2	0/1	1	***[PVFR5]***	0/1	0/1	0/1	0
	I2C2SDA	I/O	FT1	0/1	1	***[PVFR6]***	1	0/1	0/1	1
	UT1TXDA	Output	FT1	0/1	1	***[PVFR7]***	0/1	0/1	0/1	0

PV6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05OUTA	Output	FT1	0/1	1	***[PVFR2]***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FT1	0/1	1	***[PVFR3]***	0/1	0/1	0/1	0
	TSPI5SCK	Input	FT1	0/1	0	***[PVFR4]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PVFR4]***	0/1	0/1	0/1	0
	EMG0	Input	FT1	0/1	0	***[PVFR5]***	0/1	0/1	0/1	1
	UT1CTS_N	Input	FT1	0/1	0	***[PVFR7]***	0/1	0/1	0/1	1
PV7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A05OUTB	Output	FT1	0/1	1	***[PVFR2]***	0/1	0/1	0/1	0
	TSPI5CS0	Output	FT1	0/1	1	***[PVFR4]***	0/1	0/1	0/1	0
	OVV0	Output	FT1	0/1	1	***[PVFR5]***	0/1	0/1	0/1	0
	TSPI5CSIN	Input	FT1	0/1	0	***[PVFR6]***	0/1	0/1	0/1	1
	UT1RTS_N	Output	FT1	0/1	1	***[PVFR7]***	0/1	0/1	0/1	0

4.2.20. PORT W

Table 4.21 Port W registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PWDATA]	*[PWCR]*	*[PWFRn]*	*[PWOD]*	*[PWPUP]*	*[PWPDN]*	*[PWIE]*
PW0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI8CS0	Output	FT1	0/1	1	***[PWFR4]***	0/1	0/1	0/1	0
	T32A00OUTB	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
	TSPI8CSIN	Input	FT1	0/1	0	***[PWFR6]***	0/1	0/1	0/1	1
PW1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI8SCK	Input	FT1	0/1	0	***[PWFR4]***	0/1	0/1	0/1	1
		Output		0/1	1	***[PWFR4]***	0/1	0/1	0/1	0
	T32A00OUTA	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FT1	0/1	1	***[PWFR7]***	0/1	0/1	0/1	0
PW2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI8RXD	Input	FT1	0/1	0	***[PWFR4]***	0/1	0/1	0/1	1
	T32A01OUTA	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FT1	0/1	1	***[PWFR7]***	0/1	0/1	0/1	0
PW3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI8TXD	Output	FT2	0/1	1	***[PWFR4]***	0/1	0/1	0/1	0
	T32A01OUTB	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
PW4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A11INA1	Input	FT1	0/1	0	***[PWFR3]***	0/1	0/1	0/1	1
	T32A10OUTB	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
	ISDCIN0	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	T32A10INA0	Input	FT1	0/1	0	***[PWFR7]***	0/1	0/1	0/1	1
PW5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A10OUTA	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
	ISDCIN1	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	T32A10OUTC	Output	FT1	0/1	1	***[PWFR7]***	0/1	0/1	0/1	0
PW6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A11OUTA	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
	ISDCIN2	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	T32A11OUTC	Output	FT1	0/1	1	***[PWFR7]***	0/1	0/1	0/1	0
PW7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A10INA1	Input	FT1	0/1	0	***[PWFR3]***	0/1	0/1	0/1	1
	T32A11OUTB	Output	FT1	0/1	1	***[PWFR5]***	0/1	0/1	0/1	0
	ISDCIN3	Input	FT15	0/1	0	0	0/1	0/1	0/1	1
	T32A11INA0	Input	FT1	0/1	0	***[PWFR7]***	0/1	0/1	0/1	1

4.2.21. PORT Y

Table 4.22 Port Y registers setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PYDATA]	*[PYCR]*	*[PYFRn]*	*[PYOD]*	*[PYPUP]*	*[PYPDN]*	*[PYIE]*
PY0	After reset			0	N/A	N/A	N/A	0	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	0/1	0/1	1
	X1	Input	FT10	0/1	N/A	N/A	N/A	0	0	0
	EHCLKIN	Input	FT10	0/1	N/A	N/A	N/A	0	0	0
PY1	After reset			0	N/A	N/A	N/A	0	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	0/1	0/1	1
	X2	Output	FT10	0/1	N/A	N/A	N/A	0	0	0
PY2	After reset			0	N/A	N/A	N/A	0	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	0/1	0/1	1
	XT1	Input	FT10	0/1	N/A	N/A	N/A	0	0	0
	ELCLKIN	Input	FT10	0/1	N/A	N/A	N/A	0	0	1
PY3	After reset			0	N/A	N/A	N/A	0	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	0/1	0/1	1
	XT2	Output	FT10	0/1	N/A	N/A	N/A	0	0	0
PY4	During reset (BOOT_N)	Input	FT16	0	0	0	0	1 (Note1)	0	1 (Note1)
	After reset			0	0	0	0	0	0	0 (Note2)
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0 (Note2)
	ISDCOUT	Output	FT1	0/1	1	***[PYFR1]***	0/1	0/1	0/1	0 (Note2)
	EEXBCLK	Output	FT1	0/1	1	***[PYFR4]***	0/1	0/1	0/1	0 (Note2)

Note1: ***[PYPUP]*** and ***[PYIE]*** are enable during reset by the reset pin(RESET_N) or POR, Therefore, BOOT_N signal can be input.

Note2: Do not set “1” to ***[PYIE]*** register of PY4.

5. Block Diagrams of Ports

The port has eleven types of circuits, FT1 to FT5, FT10, FT13 to FT16. Each circuit diagram is shown in the following page and after. The dot line block shows an equivalent circuit which is described in “Datasheet”.

The “I/O Reset” shown in the circuit diagram is described the power on reset(POR) or the reset pin(RESET_N). Although, “I/O Reset” of debug pins(TMS/SWDIO.TDI,TDO/SWV,TCK/SWCLK,TRST_N) is the power on reset(POR) only.

5.1. Type FT1

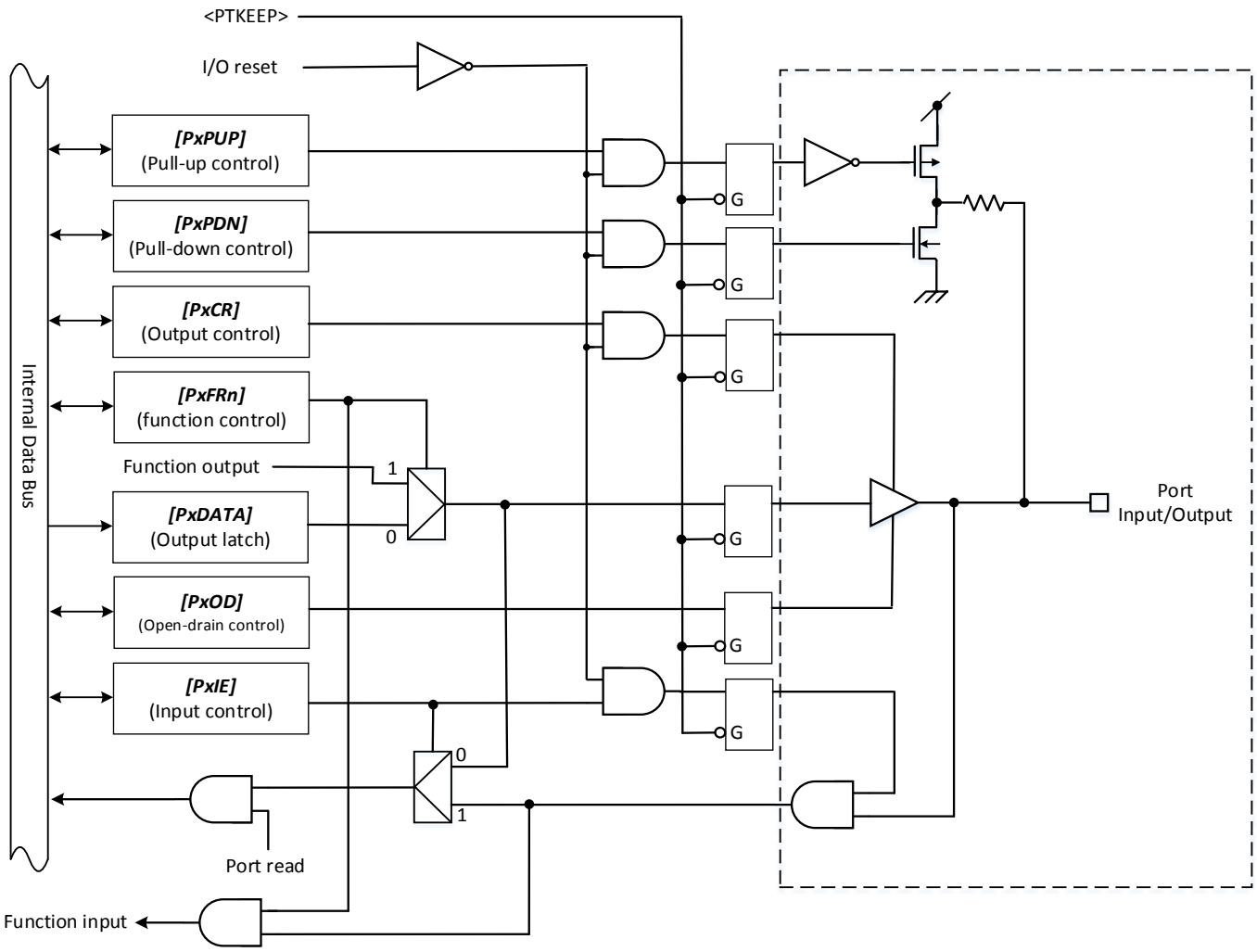


Figure 5.1 Port Type FT1

5.2. Type FT2

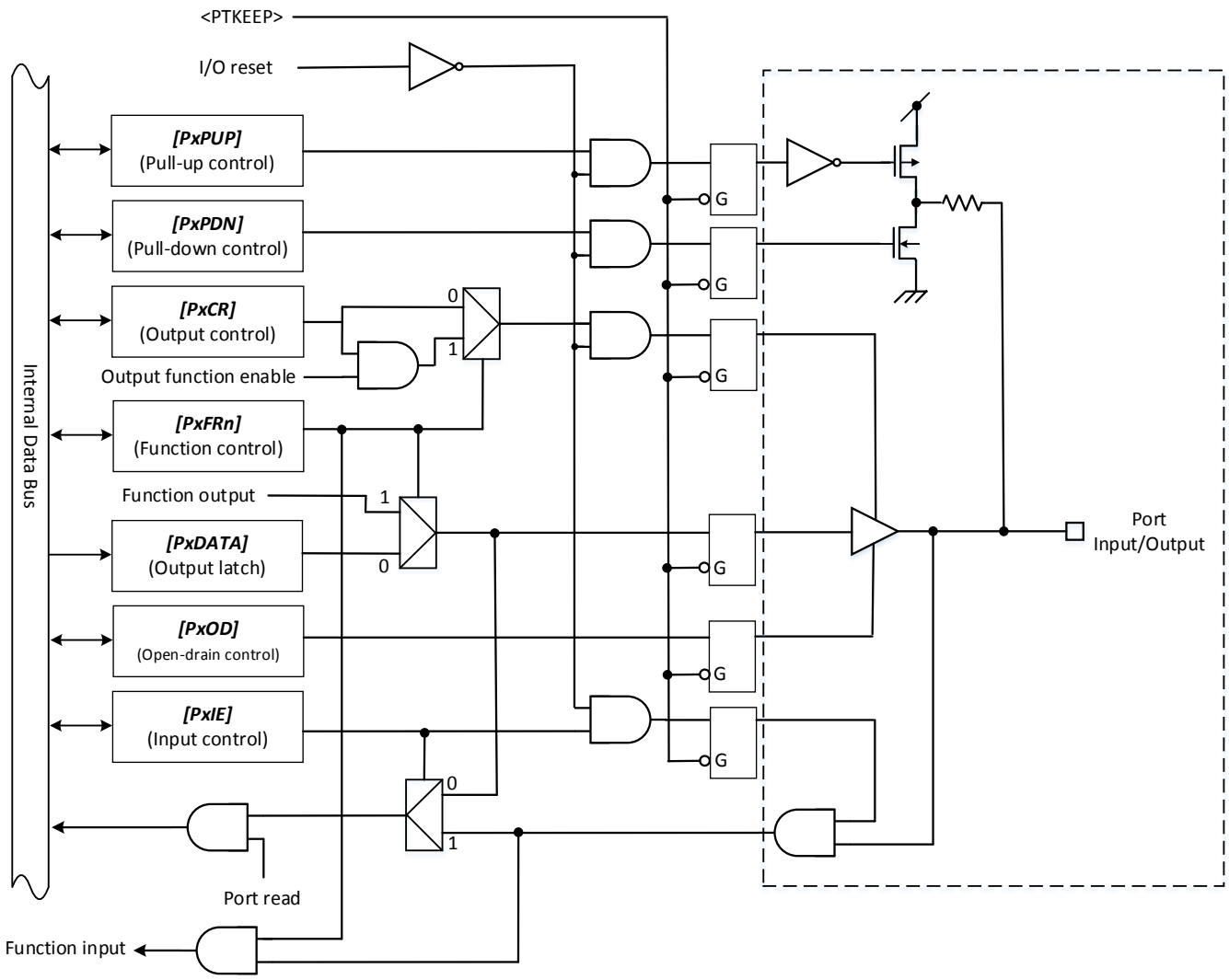


Figure 5.2 Port Type FT2

5.3. Type FT2b

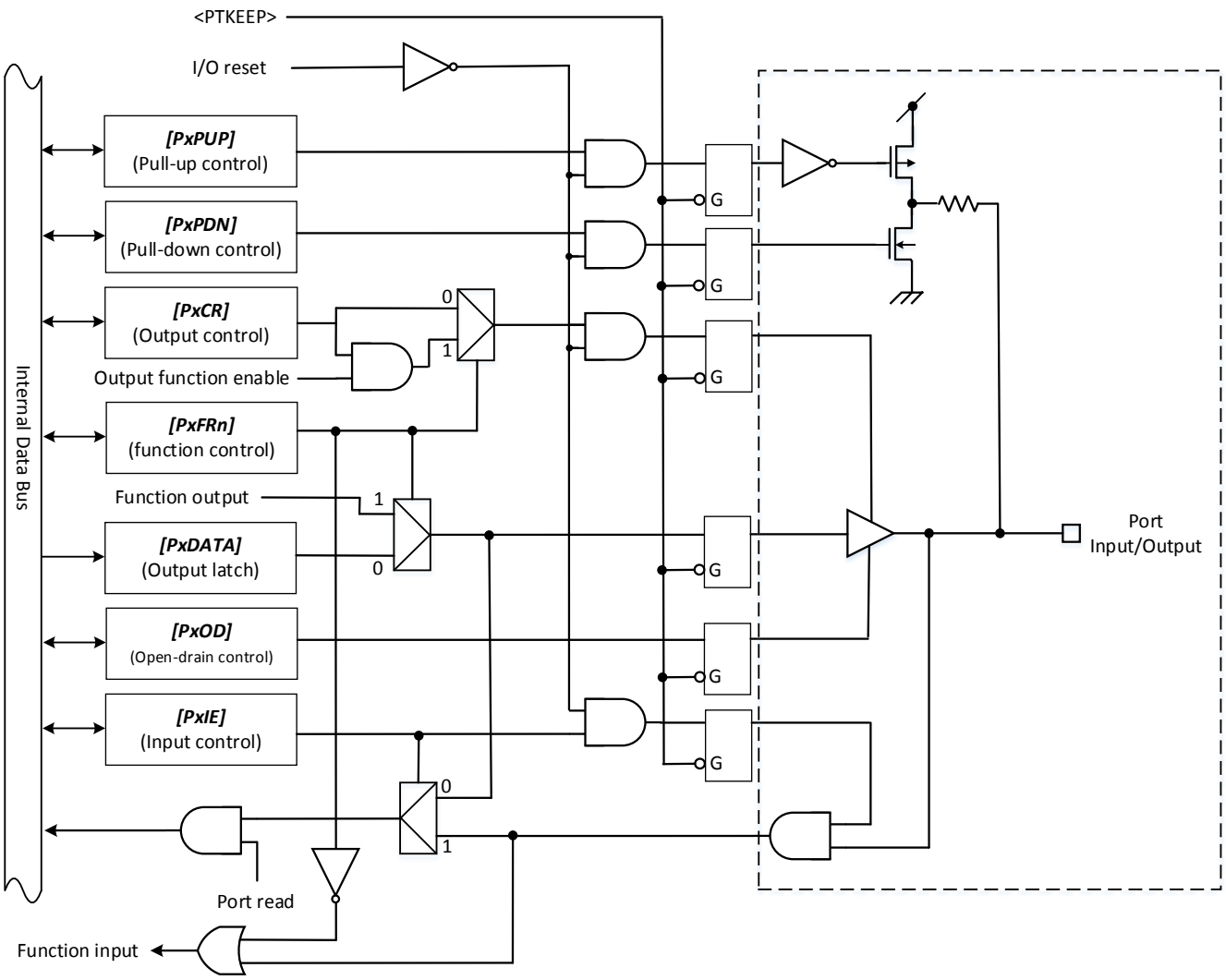
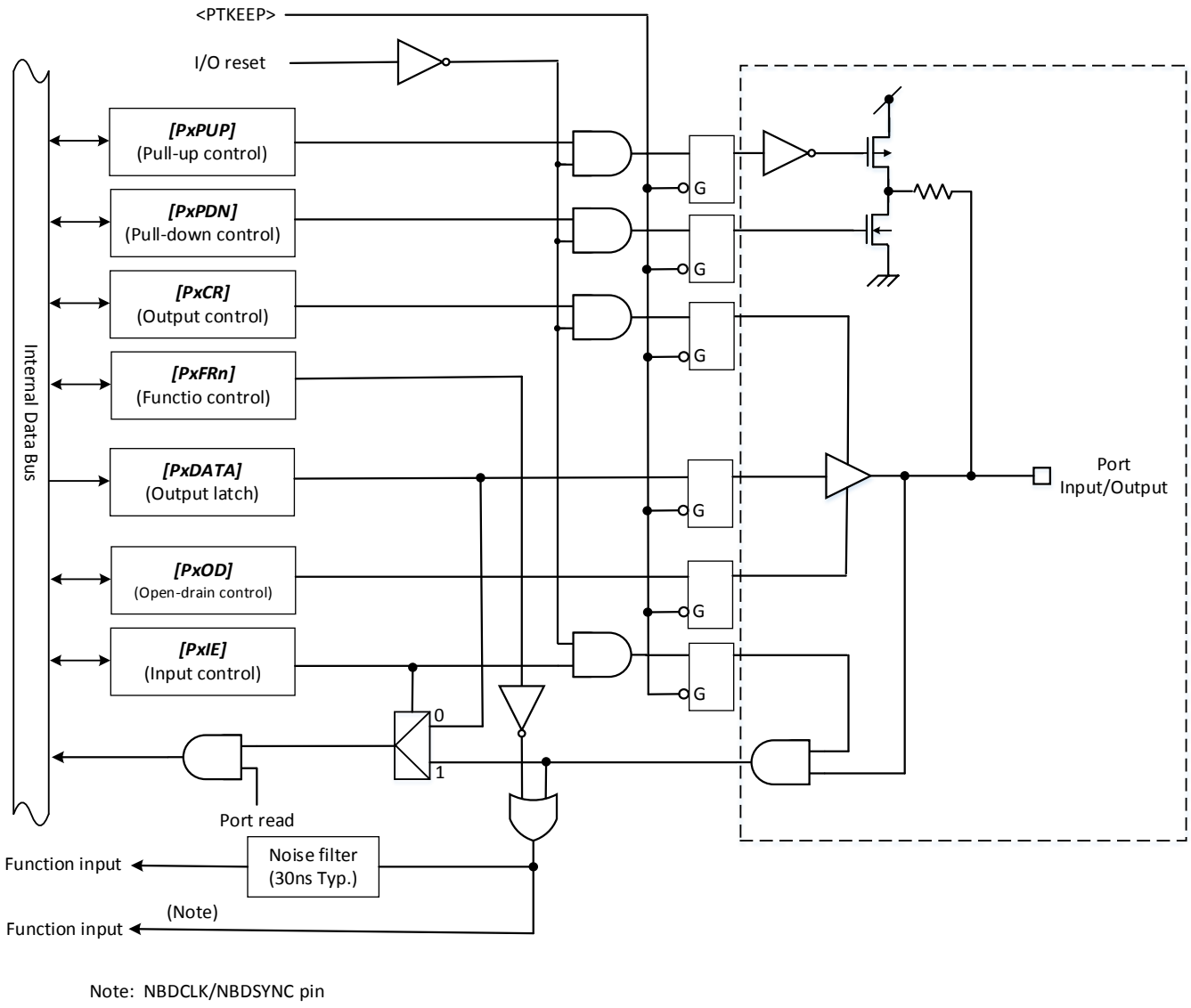


Figure 5.3 Port Type FT2b

5.4. Type FT3



Note: NBDCLK/NBDSYNC pin

Figure 5.4 Port Type FT3

5.5. Type FT4

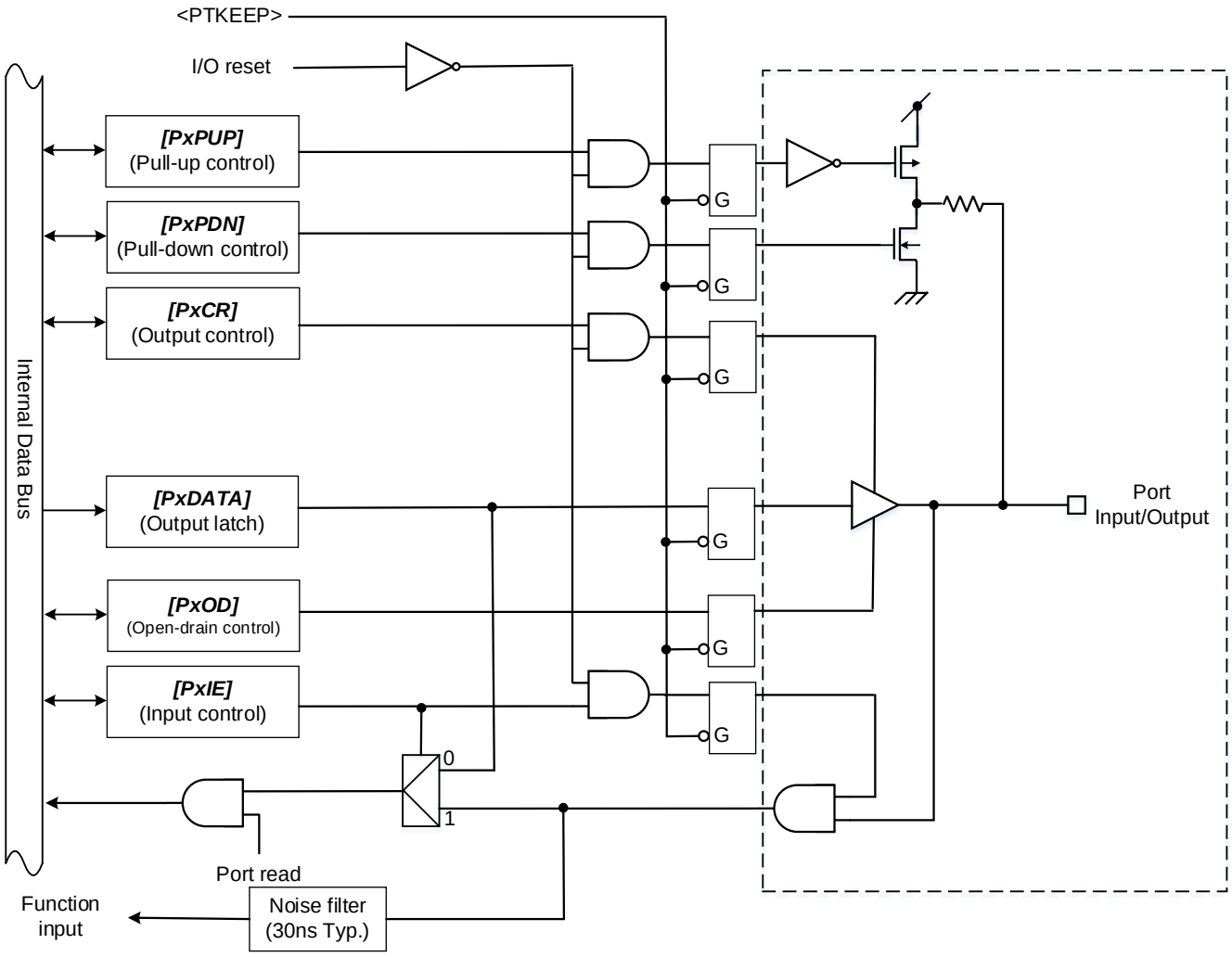


Figure 5.5 Port Type FT4

5.6. Type FT5

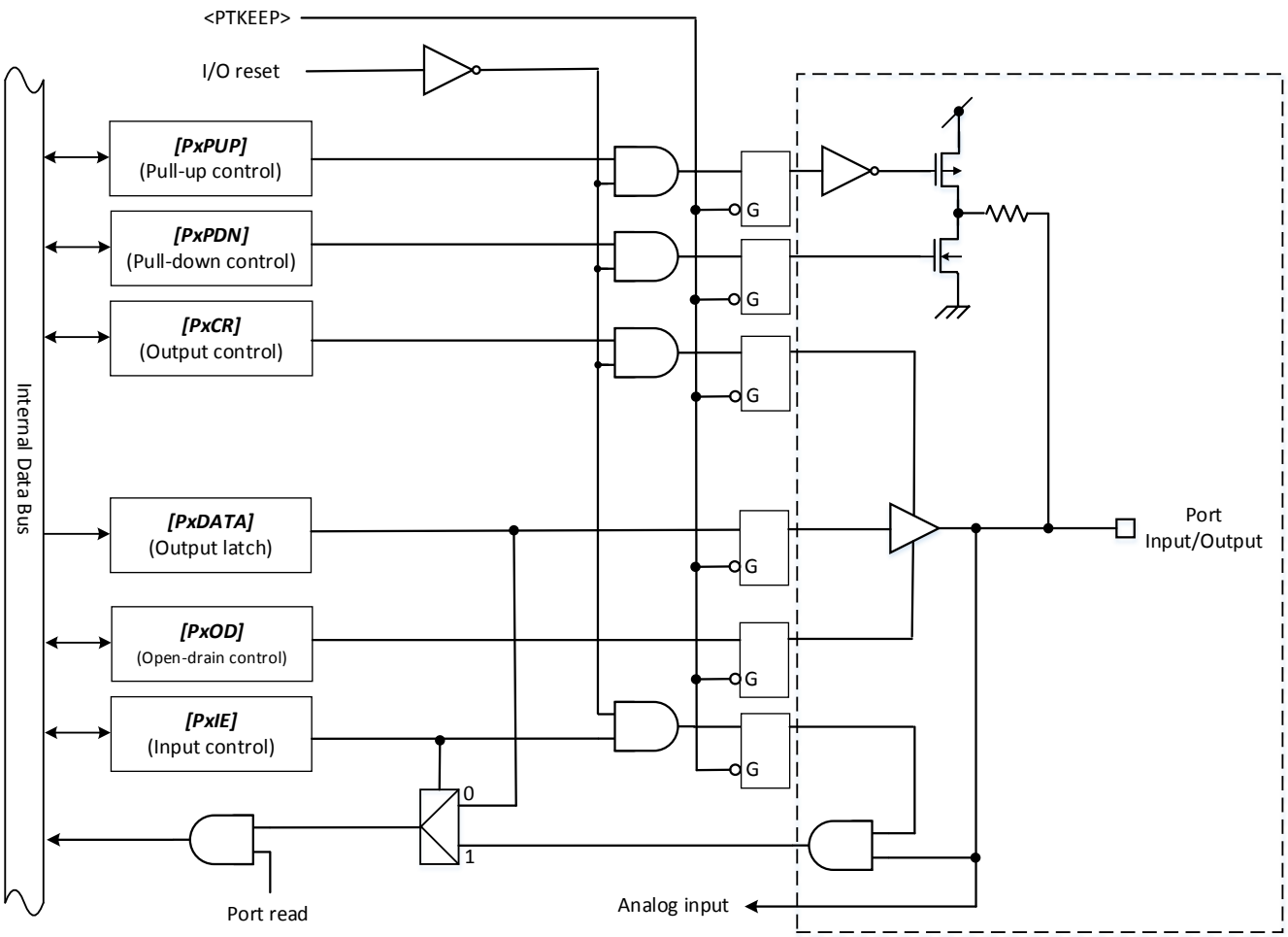


Figure 5.6 Port Type FT5

5.7. Type FT10

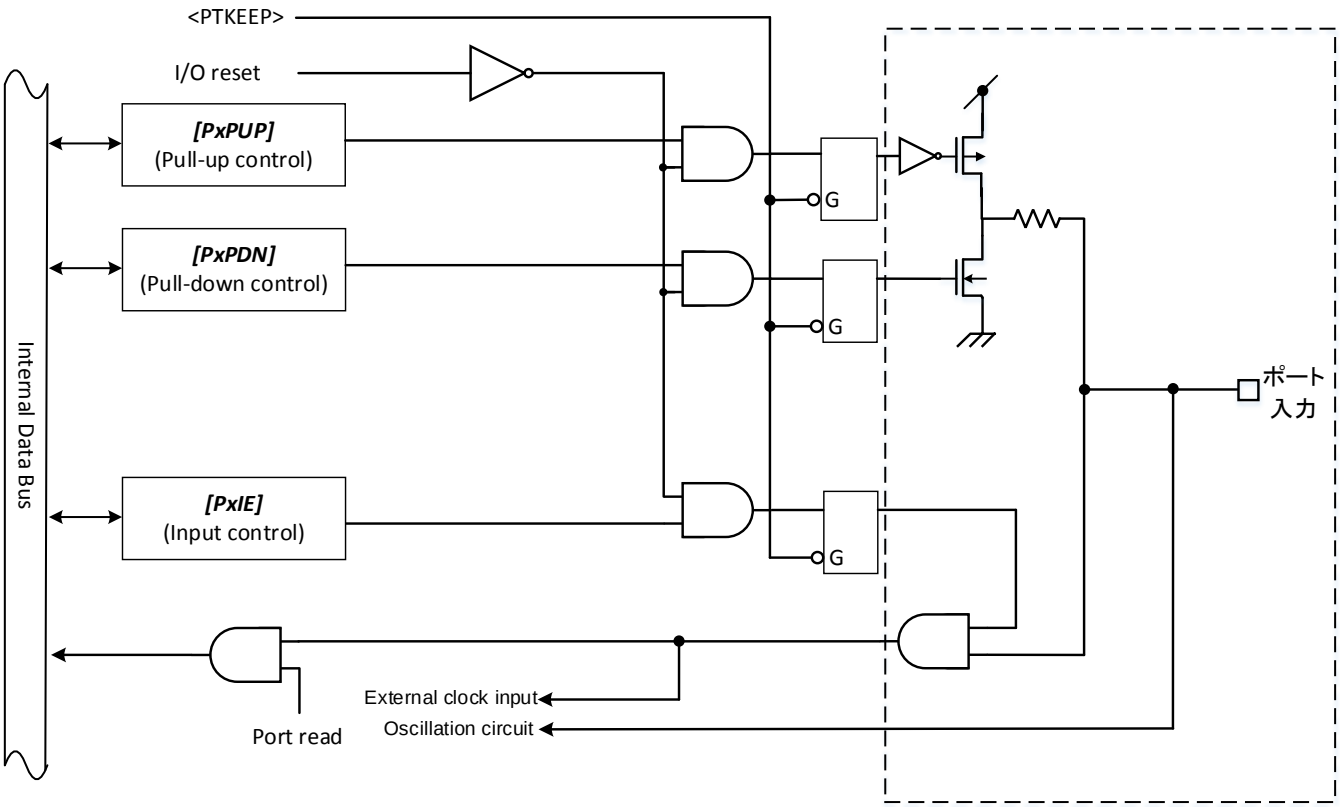


Figure 5.7 Port Type FT10

5.8. Type FT13

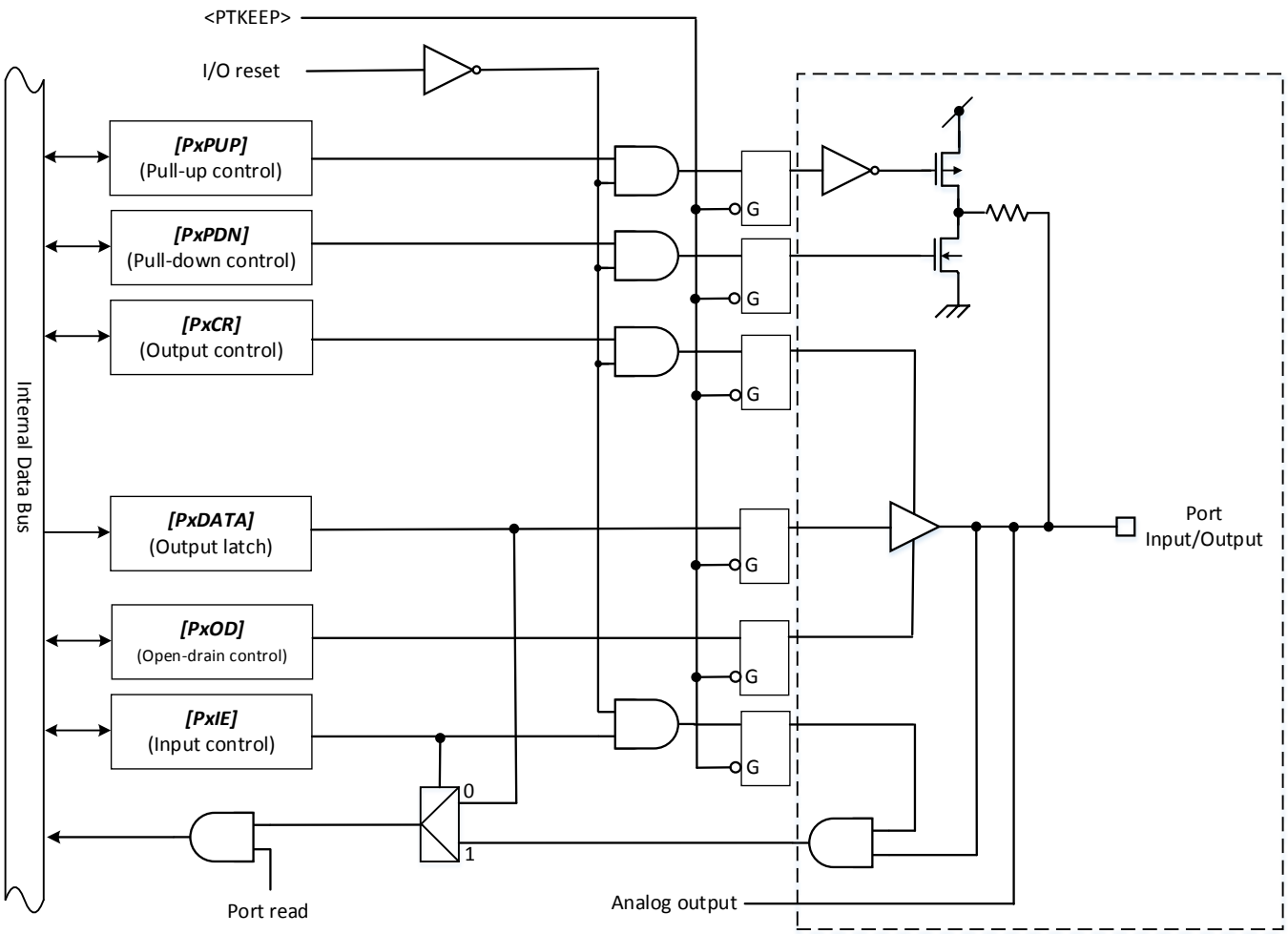


Figure 5.8 Port Type FT13

5.9. Type FT14

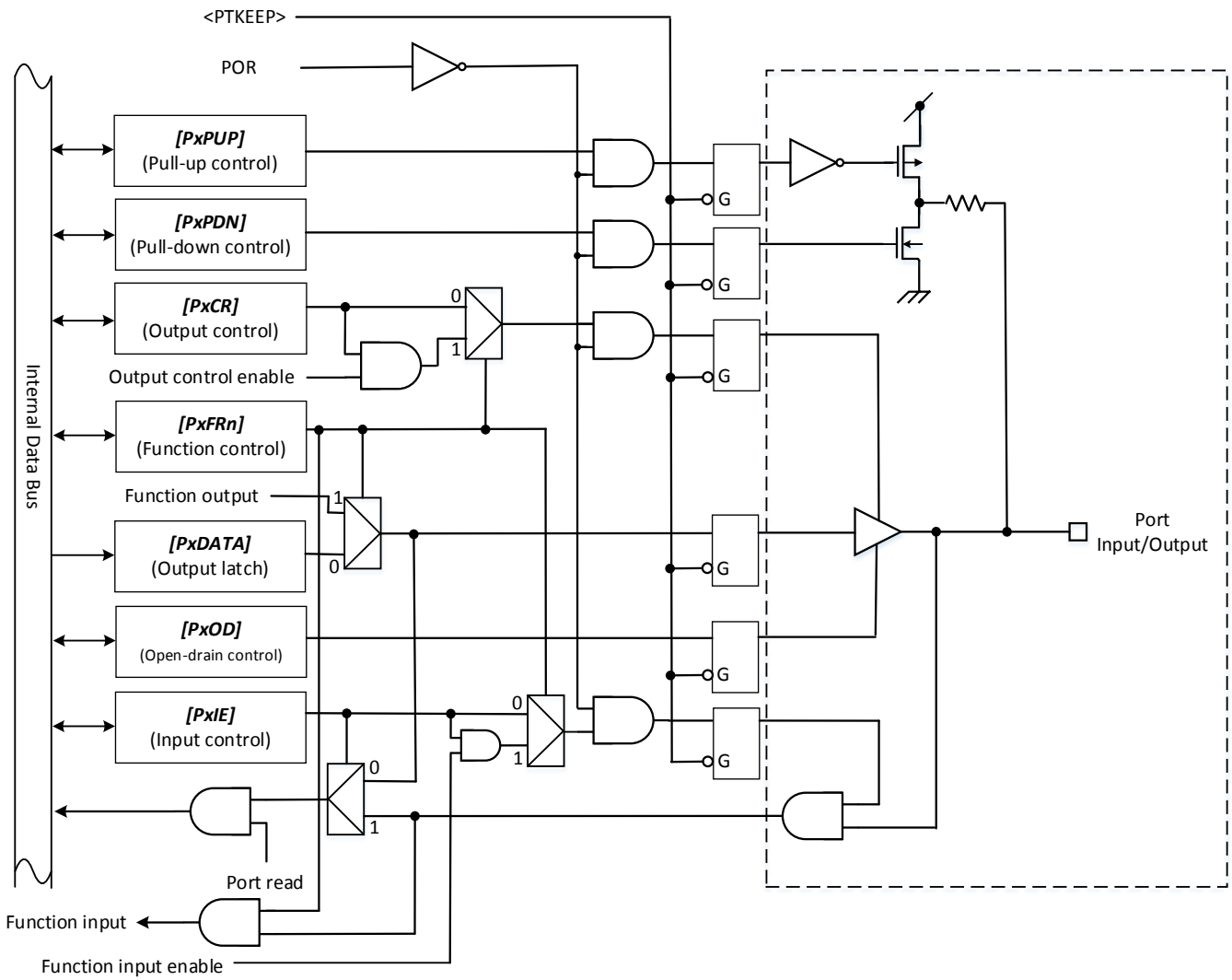


Figure 5.9 Port Type FT14

5.10. Type FT15

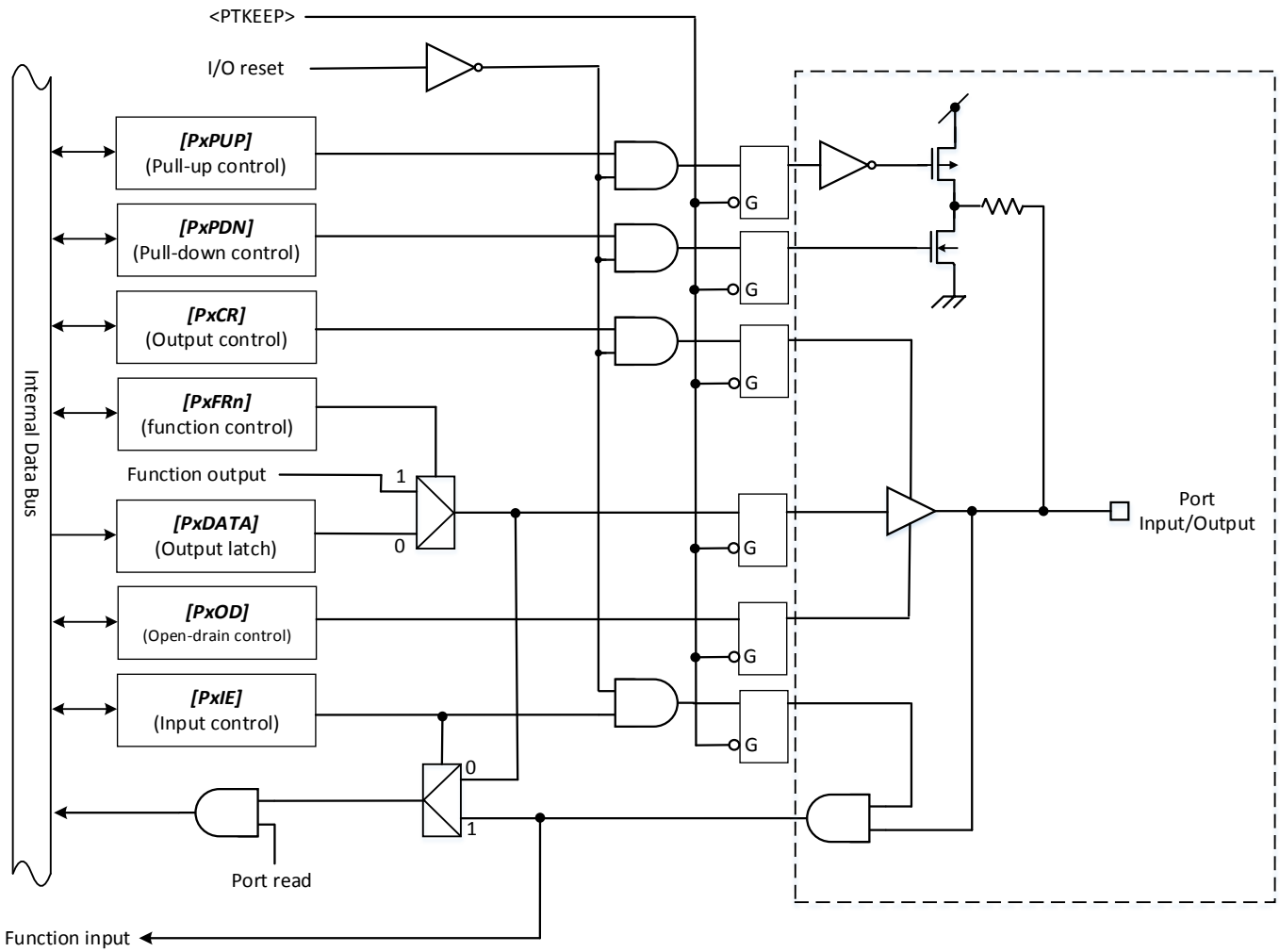


Figure 5.10 Port Type FT15

5.11. Type FT16

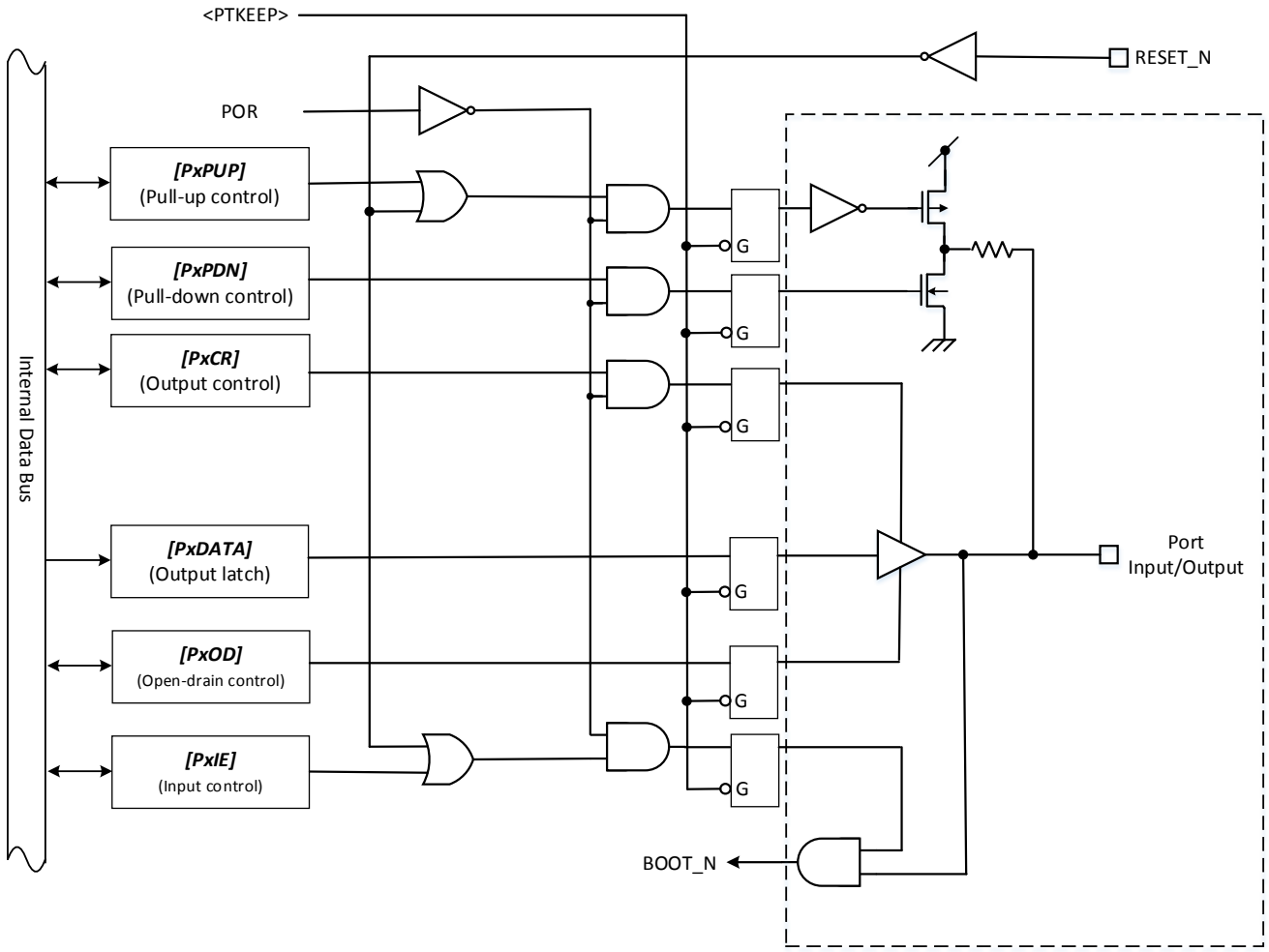


Figure 5.11 Port Type FT16

6. Precaution

6.1. pin status during a reset period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins(PH3 to PH7) are debug pin status.
- PY4(BOOT_N) is enabled for input and pull-up after pin reset or POR release. When “PY 4” is “High” at the later rising edge of "fixed time after release of POR reset" or "reset pin release", it becomes single chip mode and starts up from internal flash memory. When PY4 is “Low”, the device enters single BOOT mode and boots from the internal BOOT ROM program.

6.2. Unused pins

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important points of using debug interface pins used as general-purpose ports

After releasing reset, if the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer reference manual of “Flash memory”.

7. Revision history

Table 7.1 Revision history

Revision	Date	Description
1.0	2017-12-26	First release
2.0	2018-03-14	-3 Signal connection list Modified function pin name TCK to TCK/SWCLK, TDO to TDO/SWV, SWDIO to TMS/SWDIO in Table 3.18. -4.1 List of Register Modified Function Register 7 of Port J/K/M, ***[PDFR6]*** to ***[PJFR7]***, ***[PEFR7]*** to ***[PKFR7], [PGFR7]*** to ***[PMFR7]***. Modified Open Drain Control Register of Port Y, "-" to ***[PYOD]*** -4.2 List of Port Functions and Settings Modified PxFRn to ***[PxFRn]*** -4.2.6 PORT E Modified ***[PDFR1]*** to ***[PEFR1]***of ED/EAD pin -4.2.8 PORT G Modified NBDCLK of Port Type, FT3 to FT2b -4.2.8 PORT K Modified SMI0SCK to SMI0CLK -4.2.19 PORT V Modified PMFR4 to ***[PVFR4]*** of TSPI5SCK -4.2.21 PORT Y Modified "during reset" value of ***[PYPUP]***/***[PYIE]*** of PY4, "0" to "1". Added Note1).
2.1	2018-08-23	- Conventions Modified explanation of trademark - 3. Single connection list Modified function pin name RTCCLK to RTCOUT in Table 3.17 -4.2 List of Port Functions and Settings Added arrow between upper and lower tables - 4.2.2 PORT A Deleted Input line of TSPI0CS0/TSPI0CS1/TSPI0CS2/ TSPI0CS3/TSPI2CS0 Modified pin name TSPI0CLK to TSPI0SCK - 4.2.2 PORT D Deleted Input line of TSPI4CS0 - 4.2.6 PORT E Modified UT0RTS_N Input to Output, 0 to 1 of ***[PECR]***, 1 to 0 of ***[PEIE]*** - 4.2.8 PORT G Modified UT2RTS_N Input to Output, 0 to 1 of ***[PGCR]***, 1 to 0 of ***[PGIE]*** Modified Port Type of NBDCLK, FT2b to FT3 - 4.2.9 PORT H Modified Port Type of NBDSYNC, FT2b to FT3 Modified UT1RTS_N/UT0RTS_N Input to Output, 0 to 1 of ***[PHCR]***, 1 to 0 of ***[PHIE]*** Modified UT1CTS_N Output to Input, 1 to 0 of ***[PHCR]***, 0 to 1 of ***[PHIE]*** - 4.2.11 PORT K Deleted Input line of SMI0CS1_N/TSPI1CS1/TSPI1CS2/TSPI1CS3/TSPI3CS0 Modified Port Type of SIM0D0, FT1 to FT2 - 4.2.12 PORT L Modified pin name, TPI1SCK to TSPI1SCK Deleted Input line of TSPI3CS1 - 4.2.13 PORT M Deleted Input line of TSPI6CS0 - 4.2.17 PORT T Modified pin name RTCCLK to RTCOUT - 4.2.18 PORT U Modified ***[PUCR]*** of UT4RTS_N 0 to 1 - 5.4 Type FT3 Modified Note - RESTRICTIONS ON PRODUCT USE Replaced
2.2	2018-10-22	-1. Outlines Modified typ.to Typ. of Description of Interrupt control in Table 1.1.

		-4.2.2 PORT A Corrected ***[PAIE]*** of T32A00OUTA, 1 to 0. Corrected ***[PAIE]*** of TSPI0SCK Output, 1 to 0. -4.2.8 PORT G Corrected ***[PGCR]*** of I2C2SCL, 0 to 1. -4.2.10 PORT J Corrected ***[PJIE]*** of UT5CTS_N (PJ2), 0 to 1. Corrected ***[PJIE]*** of FUT1TXD, 1 to 0. -4.2.11 PORT K Corrected ***[PKIE]*** of SMI0CLK, 1 to 0. -4.2.14 PORT N Modified Note -4.2.15 PORT P Modified Note -4.2.16 PORT R Modified Note -4.2.19 PORT V Corrected ***[PVCR]*** of UT1TXDA, 0 to 1. - whole Modified Open Drain to Open-Drain
2.3	2019-06-06	-1. Outlines Corrected Chip select output pin of Serial Peripheral interface : “2 pins” to “4 pins” Corrected Function Classification : “Debug pin” to “Debug pins”, “Control pin” to “Control pins” -4.2 List of Port Functions and Settings Modified 1 to “1”, 0 to “0”, 0/1 to “0/1” -4.2.7 PORT F Corrected ***[PxOD]*** of I2C1SDA/I2C1SCL: “0/1” to “1” -4.2.8 PORT G Corrected ***[PxOD]*** of I2C0SDA/I2C0SCL/I2C1SDA/I2C1SCL: “0/1” to “1” -4.2.9 PORT H Corrected initial value of PH3 : “0/1” to “0” -4.2.10 PORT J Corrected ***[PxOD]*** of I2C4SDA/I2C4SCL/I2C3SDA/I2C3SCL: “0/1” to “1” -4.2.13 PORT M Corrected ***[PxOD]*** of I2C3SDA/I2C3SCL/I2C4SDA/I2C4SCL: “0/1” to “1” -4.2.19 PORT V Corrected ***[PxOD]*** of I2C2SDA/I2C2SCL: “0/1” to “1” -4.2.21 PORT Y Corrected PORT Type of BOOT_N: FT6 to FT16 -5. Block Diagrams of Ports Added description -5.11 Type FT16 Replaced FT6 to FT16

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