32-bit RISC Microcontroller

TMPM4G Group(1)

Reference manual
Memory Map
(MMAP-M4G(1))

Revision 1.1

2018-06

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Table

Preface

Related document

Document name
Arm® documentation set for the Arm Cortex®-M4

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

The Flash memory uses the Super Flash® technology under the license of Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
AO	constant energization region(8bit Bus)
APB	Advanced Peripheral Bus
A-PMD	Advanced Programmable Motor Control Circuit
CEC	Consumer Electronics Control
CG	Clock control & Generations
DAC	Digital to Analog Converter
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EBIF	External Bus Interface
FUART	Full Universal Asynchronous Receiver Transmitter
HDMAC	High Speed DMAC
I^2C	Inter-Integrated Circuit
IA(INTIF)	Interrupt control register A
IB(INTIF)	Interrupt control register B
INT	Interrupt
IMN	Interrupt Monitor
IO	IO Bus(32bit Peripheral Bus)
ISD	Interval Sensor Detection
LTTMR	Long Term Timer
LVD	Voltage Detection Circuit
MDMAC	Multi-purpose DMAC
NBDIF	Non Break Debug Interface
OFD	Oscillation Frequency Detector
RLM	Low Speed Oscillation / Power Supply Control / Reset
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial Memory Interface
T32A	32-bit Timer Event Counter
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Toshiba Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter

1. Memory Map

The memory maps for TMPM4G group (1) are based on the Arm Cortex-M4(with FPU) processor core memory map.
The internal ROM, internal RAM and special function registers (SFR) of TMPM4G group(1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4(with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register area is the processor core's internal register region.

For more information on each region, see the "Arm documentation set Cortex-M4".

Note that access to regions indicated as "Fault" causes a memory fault if memory faults are enabled, or causes a hard fault if memory faults are disabled. Also, do not access the vendor-specific region.

1.1. TMPM4GxF15

- Code Flash : 1536KB
- RAM : 192KB+2KB (Backup RAM)
- Data Flash : 32KB
- Target product : TMPM4G9F15FG, TMPM4G9F15XBG, TMPM4G8F15FG, TMPM4G8F15XBG

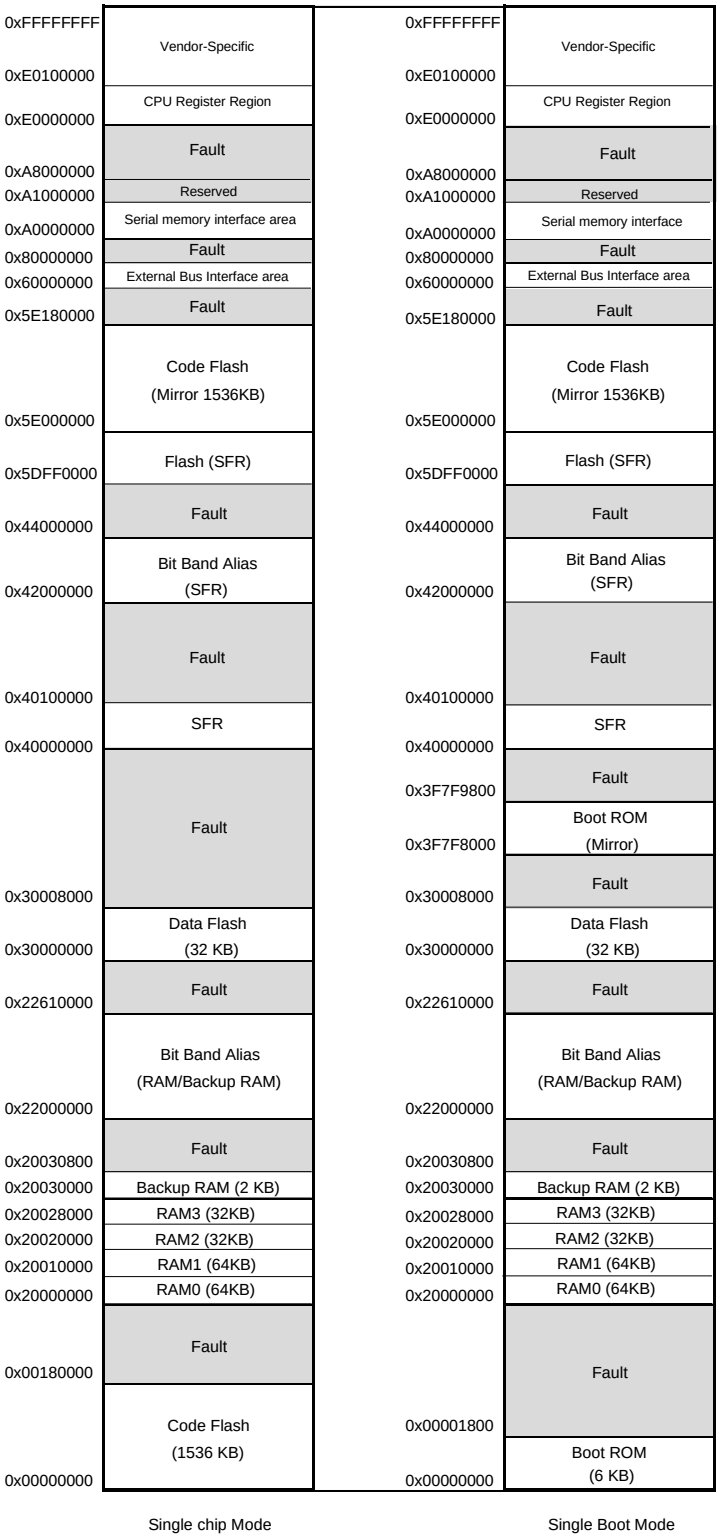


Figure 1.1 TMPM4GxF15

1.2. TMPM4GxF10

- Code Flash : 1024KB
- RAM : 192KB+2KB (Backup RAM)
- Data Flash : 32KB
- Target product : TMPM4G9F10FG, TMPM4G9F10XBG, TMPM4G8F10FG, TMPM4G8F10XBG, TMPM4G7F10FG, TMPM4G6F10FG

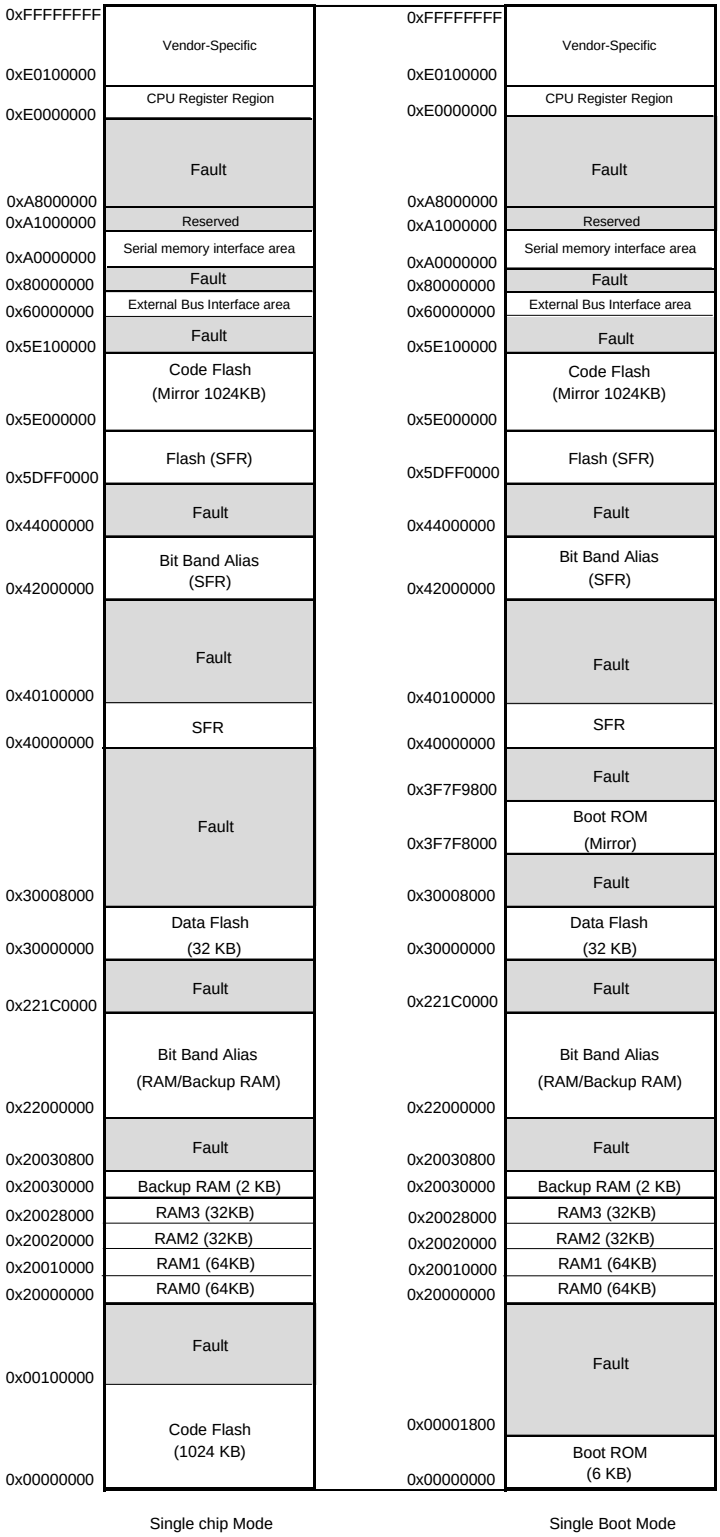


Figure 1.2 TMPM4GxF10

1.3. TMPM4GxFE

- Code Flash : 768KB
- RAM : 128KB+2KB (Backup RAM)
- Data Flash : 32KB
- Target product : TMPM4G9FEFG, TMPM4G9FEXBG, TMPM4G8FEFG, TMPM4G8FEXBG, TMPM4G7FEFG, TMPM4G6FEFG

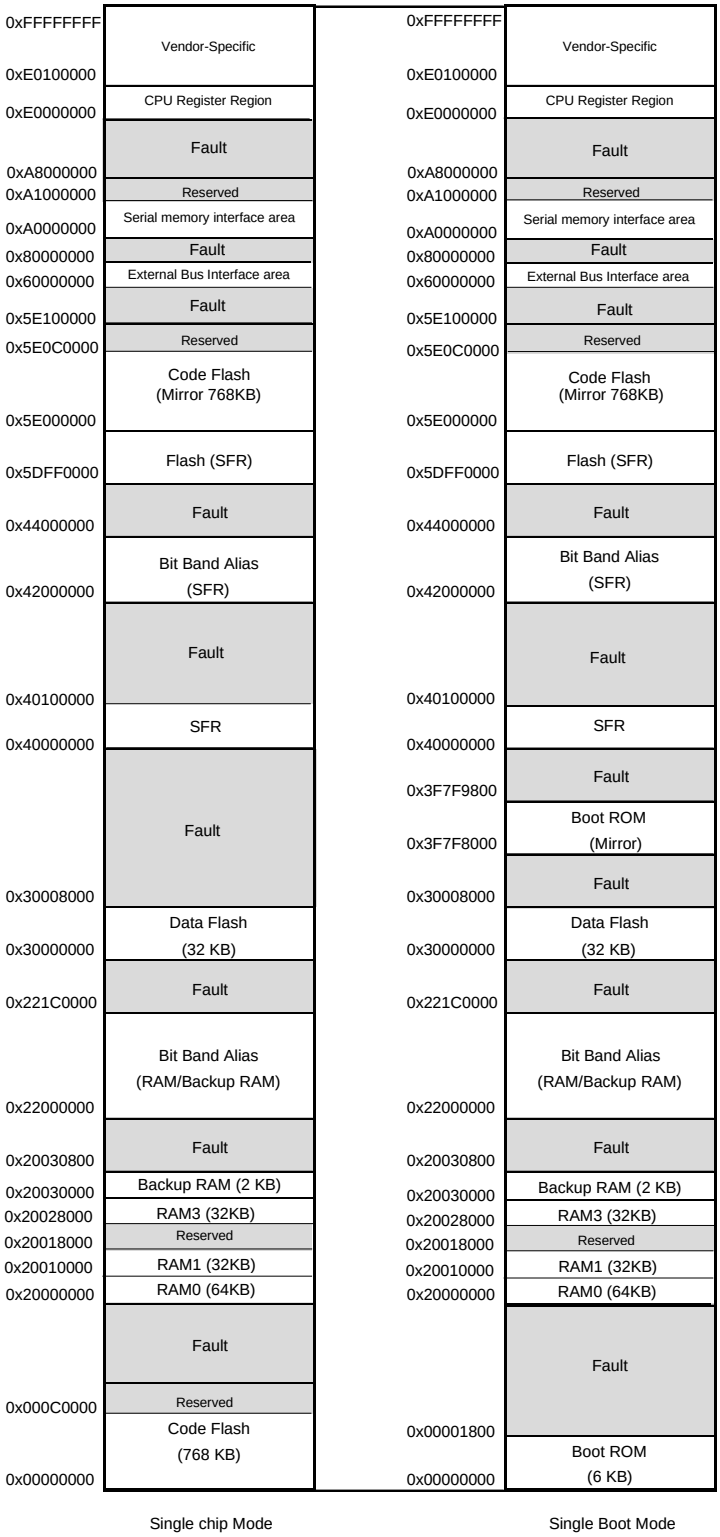


Figure 1.3 TMPM4GxFE

1.4. TMPM4GxFD

- Code Flash : 512KB
- RAM : 128KB+2KB (Backup RAM)
- Data Flash : 32KB
- Target product : TMPM4G9FDFG, TMPM4G9FDXBG, TMPM4G8FDFG, TMPM4G8FDXBG, TMPM4G7FDFG, TMPM4G6FDFG

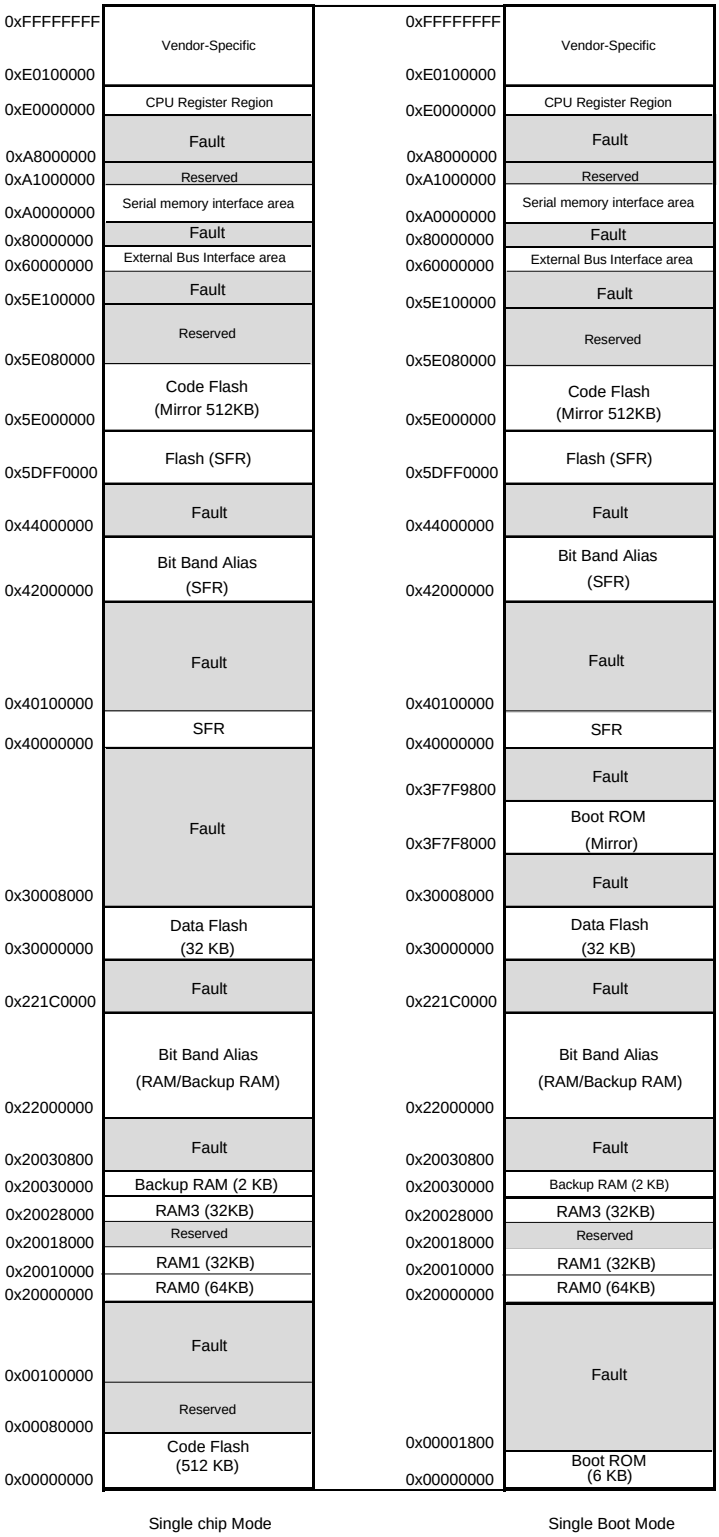


Figure 1.4 TMPM4GxFD

2. Bus Matrix

This microcontroller consists of CPU core of the main master, High-speed DMA controller (HDMAC), and a sub-master. The sub-master consists of Multi-function DMA controller (MDMAC) and NBDIF.

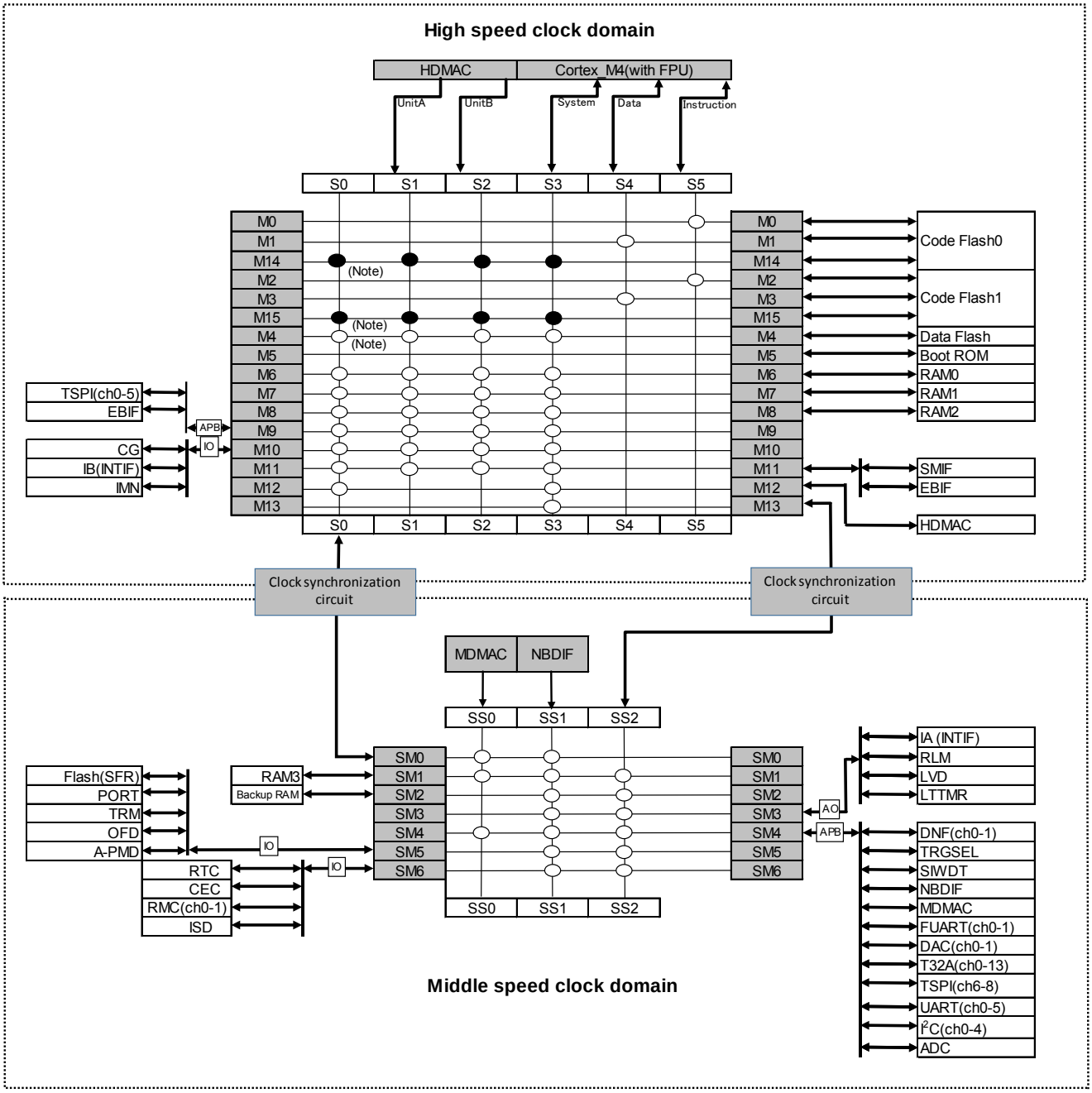
The signals of the main master are connected to the slave ports (S0 to S5) of the bus matrix. In the bus matrix, the signals of the slave ports are selectively connected to the master ports (M0 to M15). Both ○ and ● in the following figures mean “connected”, and ● shows a connection to a mirror area. The master ports are connected to sub-master and peripheral devices.

The signals of the sub-master are connected to the slave ports (SS0 to SS2) of the bus matrix. In the bus matrix, the signals of the slave ports are selectively connected to the sub ports (SM0 to SM6). Both ○ and ● in the following figures mean “connected”. The sub ports are connected to main master and peripheral devices.

When multiple slaves are connected to the same master line in the bus matrix and multiple slaves are accessed at the same time, the access to the slave with the smallest slave number from the master is prioritized.

2.1. Structure

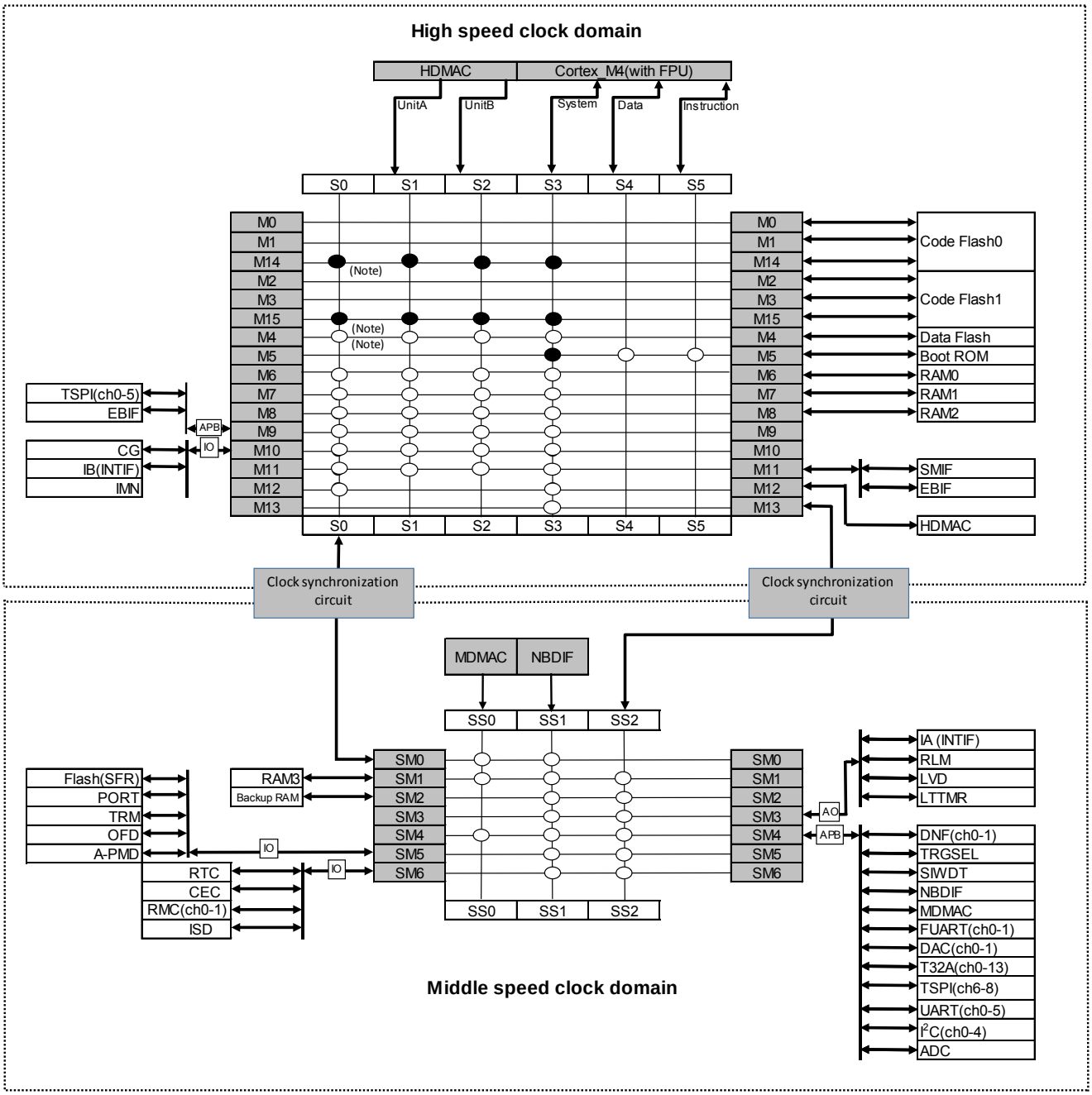
2.1.1. Single chip mode



Note: NBDIF are not connected to M4, M14, nor M15.

Figure 2.1 Single chip mode

2.1.2. Single boot mode



Note: NBDIF are not connected to M4, M14, nor M15.

Figure 2.2 Single boot mode

2.2. Connection table

2.2.1. Code area / SRAM area / SMIF area / External bus area

2.2.1.1. TMPM4GxF15

(1) Single chip mode

Table 2.1 TMPM4GxF15 Single chip mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Code Flash0	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x00100000	Code Flash1	M2	Fault	Fault	Fault	Fault	-	Fault	✓
		M3	Fault	Fault	Fault	Fault	-	✓	Fault
0x00180000	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M8	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x20030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x22610000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Code Flash1 (Mirror)	M15	✓	Fault	✓	✓	✓	-	-
0x5E180000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(2) Single boot mode

Table 2.2 TMPM4GxF15 Single boot mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M5	Fault	Fault	Fault	Fault	✓	✓	✓
0x00001800	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M8	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x22030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22610000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Code Flash1 (Mirror)	M15	✓	Fault	✓	✓	✓	-	-
0x5E180000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.1.2. TMPM4GxF10

(1) Single chip mode

Table 2.3 TMPM4GxF10 Single chip mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Code Flash0	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x00100000	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M8	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x20030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(2) Single boot mode

Table 2.4 TMPM4GxF10 Single boot mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M5	Fault	Fault	Fault	Fault	✓	✓	✓
0x00001800	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20020000	RAM2	M8	✓	✓	✓	✓	✓	-	-
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x22030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.1.3. TMPM4GxFE

(1) Single chip mode

Table 2.5 TMPM4GxFE Single chip mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Code Flash0	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x000C0000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x00100000	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20018000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x20030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(2) Single boot mode

Table 2.6 TMPM4GxFE Single boot mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M5	Fault	Fault	Fault	Fault	✓	✓	✓
0x00001800	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20018000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x22030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.1.4. TMPM4GxFD

(1) Single chip mode

Table 2.7 TMPM4GxFD Single chip mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Code Flash0	M0	Fault	Fault	Fault	Fault	-	Fault	✓
		M1	Fault	Fault	Fault	Fault	-	✓	Fault
0x00080000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x00100000	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20018000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x20030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	✓	✓	✓	✓	✓	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
0x30008000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

(2) Single boot mode

Table 2.8 TMPM4GxFD Single boot mode

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x00000000	Boot ROM	M5	Fault	Fault	Fault	Fault	✓	✓	✓
0x00001800	Fault	-	Fault	Fault	Fault	Fault	-	Fault	Fault
0x20000000	RAM0	M6	✓	✓	✓	✓	✓	-	-
0x20010000	RAM1	M7	✓	✓	✓	✓	✓	-	-
0x20018000	Reserved	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x20028000	RAM3	SM1	✓	✓	Fault	Fault	✓	-	-
0x20030000	Backup RAM	SM2	Fault	✓	Fault	Fault	✓	-	-
0x22030800	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x22000000	Bit band alias	-	Fault	Fault	Fault	Fault	Fault	-	-
0x221C0000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x30000000	Data Flash	M4	✓	Fault	✓	✓	✓	-	-
For the address of this area, refer to "Table 2.9 Peripheral area".									
0x5E000000	Code Flash0 (Mirror)	M14	✓	Fault	✓	✓	✓	-	-
0x5E100000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0x60000000	External Bus Interface area	M11	✓	✓	✓	✓	✓	-	-
0x80000000	Fault	-	Fault	Fault	Fault	Fault	Fault	-	-
0xA0000000	Serial memory interface area	M11	✓	✓	✓	✓	✓	-	-

✓: Accessible, - : No access, Fault: Fault occurred

2.2.2. Peripheral area

Table 2.9 Peripheral area

Start Address	Slave		Sub master		Main master				
			MDMAC unitA	NBDIF	HDMAC unitA	HDMAC unitB	Core S-Bus	Core D-Bus	Core I-Bus
			SS0	SS1	S1	S2	S3	S4	S5
0x40000000	HDMAC(unitA to B)	M12	✓	✓	Fault	Fault	✓	✓	✓
0x40002000	Fault	-	Fault	Fault	Fault	Fault	Fault	✓	✓
0x4000C000	SMIF	M11	✓	✓	✓	✓	✓	✓	✓
0x4000D000	Fault	-	Fault	Fault	Fault	Fault	Fault	✓	✓
0x4003E000	IA (INTIF)	SM3	Fault	✓	Fault	Fault	✓	✓	✓
0x4003E400	RLM	SM3	Fault	✓	Fault	Fault	✓	✓	✓
0x4003EC00	LVD	SM3	Fault	✓	Fault	Fault	✓	✓	✓
0x4003FF00	LTTMR	SM3	Fault	✓	Fault	Fault	✓	✓	✓
0x4006A000	TSPI(ch0 to 5)	M9	✓	✓	✓	✓	✓	✓	✓
0x40076000	EBIF	M9	✓	✓	✓	✓	✓	✓	✓
0x40083000	CG	M10	✓	✓	✓	✓	✓	✓	✓
0x40083200	IB (INTIF)	M10	✓	✓	✓	✓	✓	✓	✓
0x40083300	IMN	M10	✓	✓	✓	✓	✓	✓	✓
0x400A0200	DNF(ch0 to 1)	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400A0400	TRGSEL	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400A0600	SIWDT	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400A2000	NBDIF	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400A4000	MDMAC	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400A8000	FUART(ch0 to 1)	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400BA000	ADC	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400BC800	DAC(ch0 to 1)	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400C1000	T32A (ch0 to 13)	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400CB800	TSPI(ch6 to 8)	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400CE000	UART(ch0 to 5)	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400D1000	I^2C(ch0 to 4)	SM4	✓	✓	Fault	Fault	✓	✓	✓
0x400E0000	PORT	SM5	Fault	✓	Fault	Fault	✓	✓	✓
0x400E3100	TRM	SM5	Fault	✓	Fault	Fault	✓	✓	✓
0x400E4000	OFD	SM5	Fault	✓	Fault	Fault	✓	✓	✓
0x400E4800	RTC	SM6	Fault	✓	Fault	Fault	✓	✓	✓
0x400E8000	CEC	SM6	Fault	✓	Fault	Fault	✓	✓	✓
0x400E8100	RMC(ch0 to 1)	SM6	Fault	✓	Fault	Fault	✓	✓	✓
0x400E9000	A-PMD	SM5	Fault	✓	Fault	Fault	✓	✓	✓
0x400F0000	ISD	SM6	Fault	✓	Fault	Fault	✓	✓	✓
0x40100000	Fault	-	Fault	Fault	Fault	Fault	Fault	✓	✓
0x42000000	Bit Band Alias	-	Fault	Fault	Fault	Fault	✓	✓	✓
0x44000000	Fault	-	Fault	Fault	Fault	Fault	Fault	✓	✓
0x5DFF0000	Flash (SFR)	SM5	Fault	✓	Fault	Fault	✓	✓	✓

✓: Accessible, - : No access, Fault: Fault occurred

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2018-01-16	First release
1.1	2018-06-25	2.1.1. Single chip mode Corrected: Figure 2.1 Added channel number to peripheral function. 2.1.2. Single boot mode Corrected: Figure 2.2 M5-S3 point "○"->"●" Added channel number to peripheral function. 2.2.1.1. TMPM4GxF15 Corrected: Table 2.1, Table 2.2 2.2.1.2. TMPM4GxF10 Corrected: Table 2.3, Table 2.4 2.2.1.3. TMPM4GxFE Corrected: Table 2.5, Table 2.6 2.2.1.4. TMPM4GxFD Corrected: Table 2.7, Table 2.8 2.2.2. Peripheral area Corrected: Table 2.9

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**