32-Bit RISC Microcontroller

TMPM4G Group(1)

Reference Manual
Product Information
(PINFO-M4G(1))

Revision 3.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-" , follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviation

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
CEC	Consumer Electronics Control
CG	Clock control and Generations
DAC	Digital to Analog Converter
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EBIF	External Bus Interface
EHOSC	External High Speed Oscillator
ELOSC	External Low Speed Oscillator
fsys	frequency of SYSTEM Clock
FUART	Full Universal Asynchronous Receiver Transmitter
HDMAC	High speed DMAC
IHOSC	Internal High Speed Oscillator
I^2C	Inter-Integrated Circuit
INT	Interrupt
ISD	Interval Sensor Detection
LTTMR	Long Term Timer
LVD	Voltage Detection Circuit
MDMAC	Multi-Function DMA controller
NBDIF	Non Break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RMC	Remote Control Signal Preprocessor
RLM	Reset LOSC<Low Power> Manager
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
SMIF	Serial memory interface
T32A	32-bit Timer Event Counter
TRGSEL	Trigger Selection circuit
TSPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

This chapter describes the information which relates to peripheral functions about the channel or unit count, the pin information, and the product specific function. Use this document together with Reference manuals for peripheral functions.

2. Information of Peripheral Function

2.1. Register Base Address

The register base address type of TMPM4G group(1) is shown below.

Table 2.1 Type of the register base address (1/3)

Peripheral function			Base address type (✓: Available, -: N/A)			Base Address
			TYPE1	TYPE2	TYPE3	
High speed DMA controller	HDMAC (unit A,B)	unit A	✓	-	-	0x40000000
		unit B				0x40001000
Serial Memory Interface	SMIF	ch 0	✓	-	-	0x4000C000
Voltage Detection Circuit	LVD	-	✓	-	-	0x4003EC00
Long Term Timer	LTTMR	ch 0	✓	-	-	0x4003FF00
Serial Peripheral Interface	TSPI (ch 0 to 5)	ch 0	-	-	✓	0x4006A000
		ch 1				0x4006A400
		ch 2				0x4006A800
		ch 3				0x4006AC00
		ch 4				0x4006B000
		ch 5				0x4006B400
External Bus Interface	EBIF	-	-	-	✓	0x40076000
Digital Noise Filter Circuit	DNF (unit A,B)	unit A	-	✓	-	0x400A0200
		unit B				0x400A0300
Trigger Selector	TRGSEL	ch 0	-	✓	-	0x400A0400
Clock Selective Watchdog Timer	SIWDT	ch 0	-	✓	-	0x400A0600
Non Break Debug Interface	NBD	-	-	✓	-	0x400A2000
Multi-Function DMA controller	MDMAC	unit A	-	✓	-	0x400A4000
Full Universal Asynchronous Receiver Transmitter Circuit	FUART (ch 0,1)	ch 0	-	✓	-	0x400A8000
		ch 1				0x400A9000
12-bit Analog to Digital Converter	ADC	unit A	-	✓	-	0x400BA000
8-bit Digital to Analog Converter	DAC (ch 0,1)	ch 0	-	✓	-	0x400BC800
		ch 1				0x400BC900

Table 2.2 Type of the register base address (2/3)

Peripheral function			Base address type (✓: Available, -: N/A)			Base Address
			TYPE1	TYPE2	TYPE3	
32-bit Timer Event Counter	T32A (ch 0 to13)	ch 0	-	✓	-	0x400C1000
		ch 1				0x400C1400
		ch 2				0x400C1800
		ch 3				0x400C1C00
		ch 4				0x400C2000
		ch 5				0x400C2400
		ch 6				0x400C2800
		ch 7				0x400C2C00
		ch 8				0x400C3000
		ch 9				0x400C3400
		ch 10				0x400C3800
		ch 11				0x400C3C00
		ch 12				0x400C4000
		ch 13				0x400C4400
Serial Peripheral Interface	TSPI (ch 6 to 8)	ch 6	-	✓	-	0x400CB800
		ch 7				0x400CBC00
		ch 8				0x400CC000
Asynchronous Serial Communication Circuit	UART (ch 0 to 5)	ch 0	-	✓	-	0x400CE000
		ch 1				0x400CE400
		ch 2				0x400CE800
		ch 3				0x400CEC00
		ch 4				0x400CF000
		ch 5				0x400CF400
I^2C Interface	I^2C (ch 0 to 4)	ch 0	-	✓	-	0x400D1000
		ch 1				0x400D2000
		ch 2				0x400D3000
		ch 3				0x400D4000
		ch 4				0x400D5000

Table 2.3 Type of the register base address (3/3)

Peripheral function			Base address type (✓: Available, -: N/A)			Base Address
			TYPE1	TYPE2	TYPE3	
Trimming Circuit	TRM	-	-	✓	-	0x400E3100
Oscillation Frequency Detector	OFD	-	-	✓	-	0x400E4000
Real Time Clock	RTC	-	-	✓	-	0x400E4800
Consumer Electronics Control Circuit	CEC	ch 0	-	✓	-	0x400E8000
Remote Control Signal Preprocessor	RMC (ch 0,1)	ch 0	-	✓	-	0x400E8100
		ch 1				0x400E8200
Advanced Programmable Motor Control Circuit	A-PMD	ch 0	-	✓	-	0x400E9000
Interval Sensor Detection Circuit	ISD (unit A to C)	unit A	-	✓	-	0x400F0000
		unit B				0x400F0100
		unit C				0x400F0200
Flash Memory	FLASH	-	✓	-	-	0x5DFF0000

Each peripheral function should be developed using the type of the base address.

2.2. Trigger Selector (TRGSEL)

The trigger selector is the circuit which selects the one trigger and outputs the trigger signal to the peripheral function from two or more triggers inputted from the peripheral function, the port, etc.

The trigger selected from eight triggers by ***[TSEL0CRn]*** <INSELm> is outputted to the peripheral function of a connection destination.

Figure 2.1 shows an example of the trigger selector connection. One of TSPI, UART, I^2C, and T32A triggers is selected and connected to DMA controller via the trigger selector. ***[TSEL0CR0]***<INSEL0> controls the input trigger selection, enable or disable of the edge detection, the setting of the conditions of the edge detection, and enable or disable of the trigger output.

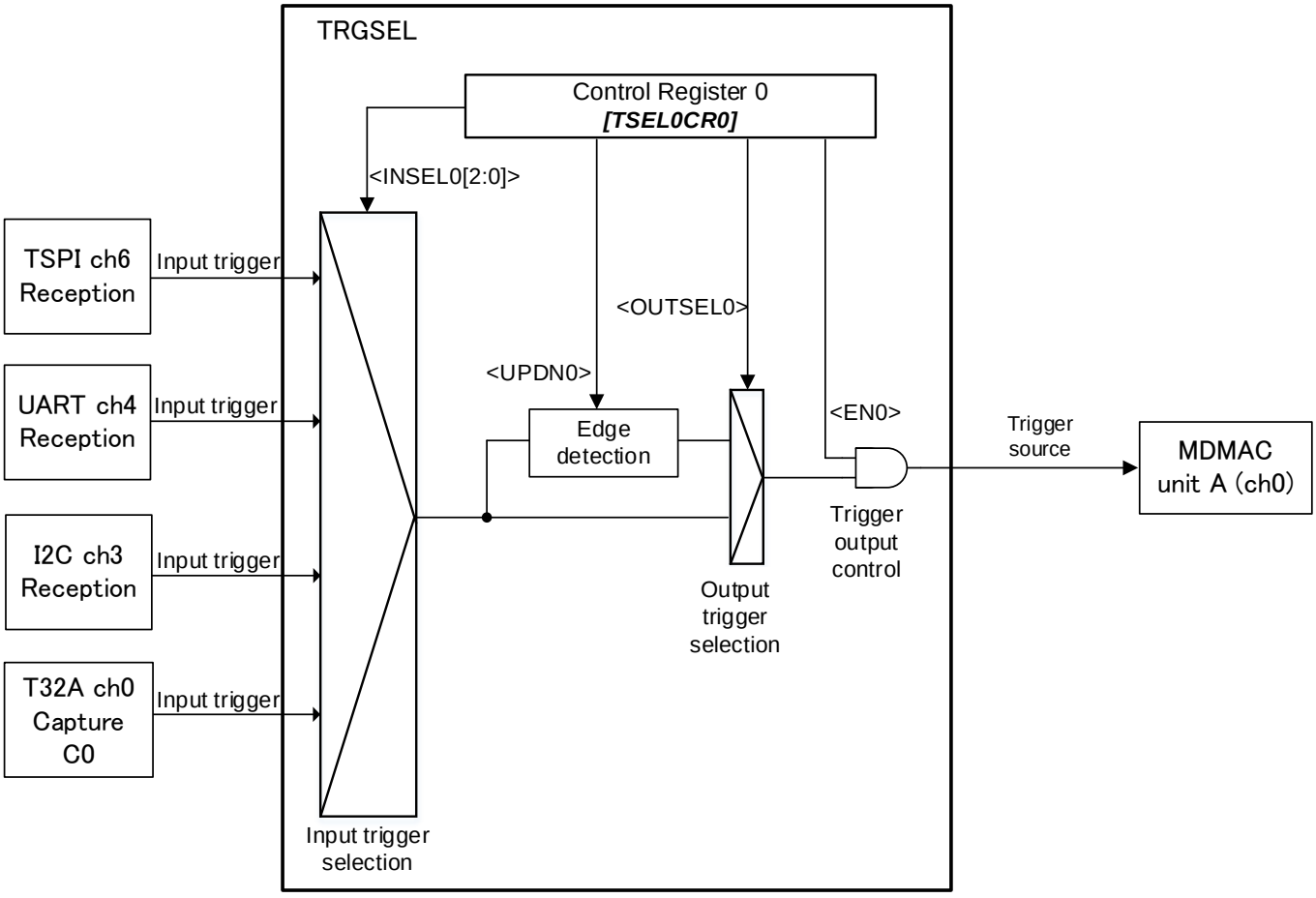

Figure 2.1 Example of the trigger selector connection

2.2.1. Trigger Selector per Product

TMPM4G group (1) trigger group selector consists of 14 control registers (***[TSEL0CR0-13]***), and can control 56 triggers.

The control register, the connection destination, and correspondence products are shown in the following table.

Table 2.4 List of the trigger selectors per product (1/6)

Register	Bit Symbol	Trigger source	Input trigger	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
[TSEL0CR0]	INSEL0[2:0]	MDMACA ch0	-TSPI ch6 receive DMA request	✓	✓	-	-
			-UART ch4 reception DMA request	✓	✓	-	-
			-I²C ch3 receiving DMA request	✓	✓	-	-
			-T32A ch0 DMA request at capture A0 register	✓	✓	✓	✓
	INSEL1[2:0]	MDMACA ch1	-TSPI ch6 transmit DMA request	✓	✓	-	-
			-UART ch4 transmission DMA request	✓	✓	-	-
			-I²C ch3 transmitting DMA request	✓	✓	-	-
			-T32A ch0 DMA request at match C0 register	✓	✓	✓	✓
	INSEL2[2:0]	MDMACA ch2	-TSPI ch7 receive DMA request	✓	✓	-	-
			-FUART ch1 reception DMA request	✓	✓	-	-
			-I²C ch4 receiving DMA request	✓	✓	-	-
	INSEL3[2:0]	MDMACA ch3	-TSPI ch7 transmit DMA request	✓	✓	-	-
			-FUART ch1 transmission DMA request	✓	✓	-	-
			-I²C ch4 transmitting DMA request	✓	✓	-	-
[TSEL0CR1]	INSEL4[2:0]	MDMACA ch4	-TSPI ch8 receive DMA request	✓	-	-	-
			-T32A ch0 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch0 DMA request at match C1 register	✓	✓	✓	✓
	INSEL5[2:0]	MDMACA ch5	-TSPI ch8 transmit DMA request	✓	-	-	-
			-T32A ch0 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch0 DMA request at capture B0 register	✓	✓	✓	✓
	INSEL6[2:0]	MDMACA ch6	-T32A ch1 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch1 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch1 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch1 DMA request at match C0 register	✓	✓	✓	✓
	INSEL7[2:0]	MDMACA ch7	-T32A ch1 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch1 DMA request at capture B0 register	✓	✓	✓	✓
			-UART ch0 reception DMA request	✓	✓	✓	✓
			-I²C ch0 receiving DMA request	✓	✓	✓	✓

Table 2.5 List of the trigger selectors per product (2/6)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)			
	Bit Symbol			M4G9	M4G8	M4G7	M4G6
[TSEL0CR2]	INSEL8[2:0]	MDMACA ch8	-T32A ch2 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch2 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch2 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch2 DMA request at match C0 register	✓	✓	✓	✓
	INSEL9[2:0]	MDMACA ch9	-T32A ch2 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch2 DMA request at capture B0 register	✓	✓	✓	✓
			-UART ch0 transmission DMA request	✓	✓	✓	✓
			-I^2C ch0 transmitting DMA request	✓	✓	✓	✓
	INSEL10[2:0]	MDMACA ch10	-T32A ch3 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch3 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch3 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch3 DMA request at match C0 register	✓	✓	✓	✓
	INSEL11[2:0]	MDMACA ch11	-T32A ch3 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch3 DMA request at capture B0 register	✓	✓	✓	✓
			-UART ch1 reception DMA request	✓	✓	✓	✓
			-I^2C ch1 receiving DMA request	✓	✓	✓	✓
[TSEL0CR3]	INSEL12[2:0]	MDMACA ch12	-T32A ch4 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch4 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch4 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch4 DMA request at match C0 register	✓	✓	✓	✓
	INSEL13[2:0]	MDMACA ch13	-T32A ch4 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch4 DMA request at capture B0 register	✓	✓	✓	✓
			-UART ch1 transmission DMA request	✓	✓	✓	✓
			-I^2C ch1 transmitting DMA request	✓	✓	✓	✓
	INSEL14[2:0]	MDMACA ch14	-T32A ch5 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch5 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch5 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch5 DMA request at match C0 register	✓	✓	✓	✓
	INSEL15[2:0]	MDMACA ch15	-T32A ch5 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch5 DMA request at capture B0 register	✓	✓	✓	✓
			-FUART ch0 transmission DMA request	✓	✓	✓	✓
			-I^2C ch2 transmitting DMA request	✓	✓	✓	✓

Table 2.6 List of the trigger selectors per product (3/6)

Register	Bit Symbol	Trigger source	Input trigger	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
[TSEL0CR4]	INSEL16[2:0]	MDMACA ch16	-T32A ch6 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch6 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch6 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch6 DMA request at match C0 register	✓	✓	✓	✓
	INSEL17[2:0]	MDMACA ch17	-T32A ch6 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch6 DMA request at capture B0 register	✓	✓	✓	✓
			-FUART ch0 reception DMA request	✓	✓	✓	✓
			-I^2C ch2 receiving DMA request	✓	✓	✓	✓
	INSEL18[2:0]	MDMACA ch18	-T32A ch7 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch7 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch7 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch7 DMA request at match C0 register	✓	✓	✓	✓
	INSEL19[2:0]	MDMACA ch19	-T32A ch7 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch7 DMA request at capture B0 register	✓	✓	✓	✓
			-UART ch2 reception DMA request	✓	✓	✓	✓
			-ADC unit A general purpose trigger DMA request	✓	✓	✓	✓
[TSEL0CR5]	INSEL20[2:0]	MDMACA ch20	-T32A ch8 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch8 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch8 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch8 DMA request at match C0 register	✓	✓	✓	✓
	INSEL21[2:0]	MDMACA ch21	-T32A ch8 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch8 DMA request at capture B0 register	✓	✓	✓	✓
			-UART ch2 transmission DMA request	✓	✓	✓	✓
			-ADC unit A Highest priority DMA request	✓	✓	✓	✓
	INSEL22[2:0]	MDMACA ch22	-T32A ch9 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch9 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch9 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch9 DMA request at match C0 register	✓	✓	✓	✓
	INSEL23[2:0]	MDMACA ch23	-T32A ch9 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch9 DMA request at capture B0 register	✓	✓	✓	✓
			-T32A ch9 DMA request at capture A1 register	✓	✓	✓	✓
			-T32A ch9 DMA request at capture B1 register	✓	✓	✓	✓

Table 2.7 List of the trigger selectors per product (4/6)

Register	Bit Symbol	Trigger source	Input trigger	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
[TSEL0CR6]	INSEL24[2:0]	MDMACA ch24	-T32A ch10 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch10 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch10 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch10 DMA request at capture C0 register	✓	✓	✓	✓
	INSEL25[2:0]	MDMACA ch25	-T32A ch10 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch10 DMA request at capture B0 register	✓	✓	✓	✓
			-T32A ch10 DMA request at capture A1 register	✓	✓	✓	✓
			-T32A ch10 DMA request at capture B1 register	✓	✓	✓	✓
	INSEL26[2:0]	MDMACA ch26	-T32A ch11 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch11 DMA request at match C1 register	✓	✓	✓	✓
			-T32A ch11 DMA request at capture A0 register	✓	✓	✓	✓
			-T32A ch11 DMA request at capture C0 register	✓	✓	✓	✓
	INSEL27[2:0]	MDMACA ch27	-T32A ch11 DMA request at match B1 register	✓	✓	✓	✓
			-T32A ch11 DMA request at capture B0 register	✓	✓	✓	✓
			-T32A ch11 DMA request at capture A1 register	✓	✓	✓	✓
			-T32A ch11 DMA request at capture B1 register	✓	✓	✓	✓
[TSEL0CR7]	INSEL28[2:0]	MDMACA ch28	-T32A ch12 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch12 DMA request at match C1 register	✓	✓	✓	✓
			-UART ch3 reception DMA request	✓	✓	✓	-
	INSEL29[2:0]	MDMACA ch29	-T32A ch12 DMA request at match B1 register	✓	✓	✓	✓
			-UART ch3 transmission DMA request	✓	✓	✓	-
			-A-PMD ch0 PWM interrupt	✓	✓	✓	✓
	INSEL30[2:0]	MDMACA ch30	-T32A ch13 DMA request at match A1 register	✓	✓	✓	✓
			-T32A ch13 DMA request at match C1 register	✓	✓	✓	✓
			-UART ch5 reception DMA request	✓	-	-	-
	INSEL31[2:0]	MDMACA ch31	-T32A ch13 DMA request at match B1 register	✓	✓	✓	✓
			-UART ch5 transmission DMA request	✓	-	-	-
			-TRGIN2 (PT3 pin)	✓	✓	✓	✓

Table 2.8 List of the trigger selectors per product (5/6)

Register	Bit Symbol	Trigger source	Input trigger	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
[TSEL0CR8]	INSEL32[2:0]	ADC	-A-PMD ch0 ADC synchronous trigger output 0	✓	✓	✓	✓
			-A-PMD ch0 ADC synchronous trigger output 1	✓	✓	✓	✓
			-A-PMD ch0 ADC synchronous trigger output 2	✓	✓	✓	✓
			-A-PMD ch0 ADC synchronous trigger output 3	✓	✓	✓	✓
			-INSEL37 output	✓	✓	✓	✓
			-INSEL38 output	✓	✓	✓	✓
	INSEL33[2:0]	ADC	-A-PMD ch0 ADC synchronous trigger output 0	✓	✓	✓	✓
			-A-PMD ch0 ADC synchronous trigger output 1	✓	✓	✓	✓
			-A-PMD ch0 ADC synchronous trigger output 2	✓	✓	✓	✓
			-A-PMD ch0 ADC synchronous trigger output 3	✓	✓	✓	✓
			-INSEL37 output	✓	✓	✓	✓
			-INSEL38 output	✓	✓	✓	✓
	INSEL34[2:0]	T32A ch8 timer A	-ELOSC low speed clock	✓	✓	✓	✓
	INSEL35[2:0]	T32A ch13 timer A	-RMC ch0 trigger output	✓	✓	✓	✓
			-T32A ch2 timer register A0 match trigger	✓	✓	✓	✓
[TSEL0CR9]	INSEL36[2:0]	T32A ch13 timer B	-RMC ch1 trigger output	✓	✓	✓	-
			-T32A ch2 timer register A0 match trigger	✓	✓	✓	✓
	INSEL37[2:0]	INSEL32 ,INSEL33	-T32A ch9 timer register A1 match trigger	✓	✓	✓	✓
			-T32A ch9 timer register B1 match trigger	✓	✓	✓	✓
			-T32A ch10 timer register A1 match trigger	✓	✓	✓	✓
			-T32A ch10 timer register B1 match trigger	✓	✓	✓	✓
			-T32A ch11 timer register A1 match trigger	✓	✓	✓	✓
			-T32A ch11 timer register B1 match trigger	✓	✓	✓	✓
			-TRGIN0 (PG3 pin)	✓	✓	✓	✓
			-TRGIN1 (PL7 pin)	✓	-	-	-
	INSEL38[2:0]	INSEL32 ,INSEL33	-T32A ch9 timer register A1 match trigger	✓	✓	✓	✓
			-T32A ch9 timer register B1 match trigger	✓	✓	✓	✓
			-T32A ch10 timer register A1 match trigger	✓	✓	✓	✓
			-T32A ch10 timer register B1 match trigger	✓	✓	✓	✓
			-T32A ch11 timer register A1 match trigger	✓	✓	✓	✓
			-T32A ch11 timer register B1 match trigger	✓	✓	✓	✓
			-TRGIN0 (PG3 pin)	✓	✓	✓	✓
			-TRGIN1 (PL7 pin)	✓	-	-	-
	INSEL39[2:0]	T32A ch5 timer A	-T32A ch9 timer register A0 match trigger	✓	✓	✓	✓
			-T32A ch13 timer register A0 match trigger	✓	✓	✓	✓

Table 2.9 List of the trigger selectors per product (6/6)

Register		Trigger source	Input trigger	Product table (✓: Available, -: N/A)			
	Bit Symbol			M4G9	M4G8	M4G7	M4G6
[TSEL0CR10]	INSEL40[2:0]	T32A ch5 timer B	-T32A ch9 timer register A0 match trigger	✓	✓	✓	✓
			-T32A ch13 timer register A0 match trigger	✓	✓	✓	✓
	INSEL41[2:0]	T32A ch6 timer A	-T32A ch10 timer register A0 match trigger	✓	✓	✓	✓
			-T32A ch13 timer register B0 match trigger	✓	✓	✓	✓
	INSEL42[2:0]	T32A ch6 timer B	-T32A ch10 timer register A0 match trigger	✓	✓	✓	✓
			-T32A ch13 timer register B0 match trigger	✓	✓	✓	✓
	INSEL43[2:0]	T32A ch7 timer A	-T32A ch11 timer register A0 match trigger	✓	✓	✓	✓
			-T32A ch13 timer register B0 match trigger	✓	✓	✓	✓
[TSEL0CR11]	INSEL44[2:0]	T32A ch7 timer B	-T32A ch11 timer register A0 match trigger	✓	✓	✓	✓
			-T32A ch13 timer register B0 match trigger	✓	✓	✓	✓
	INSEL45[2:0]	T32A ch8 timer B	-T32A ch4 timer B output	✓	✓	✓	✓
			-T32A ch8 timer A output	✓	✓	✓	✓
	INSEL46[2:0]	T32A ch0 timer A	-TSPI ch0 transmit completion	✓	✓	✓	✓
			-UART ch0 transmission completion trigger	✓	✓	✓	✓
			-T32A ch12 timer register A0 match trigger	✓	✓	✓	✓
	INSEL47[2:0]	T32A ch0 timer B	-TSPI ch0 receive completion	✓	✓	✓	✓
			-UART ch0 reception completion trigger	✓	✓	✓	✓
			-T32A ch12 timer register A0 match trigger	✓	✓	✓	✓
[TSEL0CR12]	INSEL48[2:0]	T32A ch1 timer A	-TSPI ch1 transmit completion	✓	✓	✓	✓
			-UART ch1 transmission completion	✓	✓	✓	✓
			-T32A ch12 timer register A0 match trigger	✓	✓	✓	✓
	INSEL49[2:0]	T32A ch1 timer B	-TSPI ch1 receive completion	✓	✓	✓	✓
			-UART ch1 reception completion trigger	✓	✓	✓	✓
			-T32A ch12 timer register A0 match trigger	✓	✓	✓	✓
	INSEL50[2:0]	T32A ch2 timer A	-TSPI ch2 transmit completion	✓	✓	✓	✓
			-UART ch2 transmission completion trigger	✓	✓	✓	✓
			-T32A ch12 timer register B0 match trigger	✓	✓	✓	✓
	INSEL51[2:0]	T32A ch2 timer B	-TSPI ch2 receive completion	✓	✓	✓	✓
			-UART ch2 reception completion trigger	✓	✓	✓	✓
			-T32A ch12 timer register B0 match trigger	✓	✓	✓	✓
[TSEL0CR13]	INSEL52[2:0]	T32A ch3 timer A	-TSPI ch3 transmit completion	✓	✓	✓	✓
			-T32A ch12 timer register B0 match trigger	✓	✓	✓	✓
	INSEL53[2:0]	T32A ch3 timer B	-TSPI ch3 receive completion	✓	✓	✓	✓
			-T32A ch12 timer register B0 match trigger	✓	✓	✓	✓
	INSEL54[2:0]	T32A ch4 timer A	-TSPI ch4 transmit completion	✓	✓	✓	✓
			-T32A ch13 timer register A0 match trigger	✓	✓	✓	✓
	INSEL55[2:0]	T32A ch4 timer B	-TSPI ch4 receive completion	✓	✓	✓	✓
			-T32A ch13 timer register A0 match trigger	✓	✓	✓	✓

2.2.2. Operation and setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), and fc supply stop registers (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

Setting procedure of trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger subdevice bit (***[TSEL0CRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Selection of edge detection conditions (***[TSEL0CRn]*** <UPDNm>)

For the selected input trigger signal, select detection of rising edge or falling edge.

To select the edge detection condition, set with the edge detection condition bit (***[TSEL0CRn]*** <UPDNm>) of the control register.

The following shows the trigger signal which needs edge detection.

- External trigger input (TRGIN0, TRGIN1, and TRGIN2)
- ELOSC low speed clock (fs)

(3) Selection of a trigger output (***[TSEL0CRn]***<OUTSELm>)

Selection of an output without or with edge detection is performed.

Please set up selection of a trigger output in the selection bit (***[TSEL0CRn]***<OUTSELm>) of a control register.

(4) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set as "1".

2.2.3. List of Registers

The control registers and their addresses are shown in the following tables.

Peripheral function		Channel/Unit	Base address
			TYPE 2
Trigger Selector	TRGSEL	ch0	0x400A0400

Register name		Address (Base+)
Control Register 0	***[TSEL0CR0]***	0x0000
Control Register 1	***[TSEL0CR1]***	0x0004
Control Register 2	***[TSEL0CR2]***	0x0008
Control Register 3	***[TSEL0CR3]***	0x000C
Control Register 4	***[TSEL0CR4]***	0x0010
Control Register 5	***[TSEL0CR5]***	0x0014
Control Register 6	***[TSEL0CR6]***	0x0018
Control Register 7	***[TSEL0CR7]***	0x001C
Control Register 8	***[TSEL0CR8]***	0x0020
Control Register 9	***[TSEL0CR9]***	0x0024
Control Register 10	***[TSEL0CR10]***	0x0028
Control Register 11	***[TSEL0CR11]***	0x002C
Control Register 12	***[TSEL0CR12]***	0x0030
Control Register 13	***[TSEL0CR13]***	0x0034

2.2.4. Details of Registers

The following chapters show the details of a register.

The corresponding signal name is shown in parentheses in the column “Description”.

2.2.4.1. *[TSEL0CR0]* (Control Register 0)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL3[2:0]	000	R/W	Input trigger selection (MDMAC A ch3) 000: TSPI ch7 transmit DMA request (TSPI7TX_DMA) 001: FUART ch1 transmission DMA request (FUART1TX_DMAREQ) 010: I^{2}C ch4 transmitting DMA request (I2C4TXDMAREQ) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN3	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL3	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN3	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL2[2:0]	000	R/W	Input trigger selection (MDMAC A ch2) 000: TSPI ch7 receive DMA request (TSPI7RX_DMA) 001: FUART ch1 reception DMA request (FUART1RX_DMAREQ) 010: I^{2}C ch4 receiving DMA request (I2C4RXDMAREQ) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN2	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL2	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN2	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL1[2:0]	000	R/W	Input trigger selection (MDMAC A ch1) 000: TSPI ch6 transmit DMA request (TSPI6TX_DMA) 001: UART ch4 transmission DMA request (UART4TX_DMAREQ) 010: I^{2}C ch3 transmitting DMA request (I2C3TXDMAREQ) 011: T32A ch0 DMA request at match C0 register (T32A00DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN1	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL1	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN1	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL0[2:0]	000	R/W	Input trigger selection (MDMAC A ch0) 000: TSPI ch6 receive DMA request (TSPI6RX_DMA) 001: UART ch4 reception DMA request (UART4RX_DMAREQ) 010: I^{2}C ch3 receiving DMA request (I2C3RXDMAREQ) 011: T32A ch0 DMA request at capture A0 register (T32A00DMAREQCAPA0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN0	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL0	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN0	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.2. *[TSEL0CR1]* (Control Register 1)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL7[2:0]	000	R/W	Input trigger selection (MDMAC A ch7) 000: T32A ch1 DMA request at match B1 register (T32A01DMAREQCMPB1) 001: T32A ch1 DMA request at capture B0 register (T32A01DMAREQCAPB0) 010: UART ch0 reception DMA request (UART0RX_DMAREQ) 011: I^2C ch0 receiving DMA request (I2C0RXDMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN7	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL7	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN7	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL6[2:0]	000	R/W	Input trigger selection (MDMAC A ch6) 000: T32A ch1 DMA request at match A1 register (T32A01DMAREQCMPA1) 001: T32A ch1 DMA request at match C1 register (T32A01DMAREQCMPC1) 010: T32A ch1 DMA request at capture A0 register (T32A01DMAREQCAPA0) 011: T32A ch1 DMA request at capture C0 register (T32A01DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN6	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL6	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN6	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL5[2:0]	000	R/W	Input trigger selection (MDMAC A ch5) 000: TSPI ch8 transmit DMA request (TSPI8TX_DMA) 001: T32A ch0 DMA request at match B1 register (T32A00DMAREQCMPB1) 010: T32A ch0 DMA request at capture B0 register (T32A00DMAREQCAPB0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN5	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL5	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN5	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL4[2:0]	000	R/W	Input trigger selection (MDMAC A ch4) 000: TSPI ch8 receive DMA request (TSPI8RX_DMA) 001: T32A ch0 DMA request at match A1 register (T32A00DMAREQCMPA1) 010: T32A ch0 DMA request at match C1 register (T32A00DMAREQCMPC1) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN4	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL4	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN4	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.3. *[TSEL0CR2]* (Control Register 2)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL11[2:0]	000	R/W	Input trigger selection (MDMAC A ch11) 000: T32A ch3 DMA request at match B1 register (T32A03DMAREQCMPB1) 001: T32A ch3 DMA request at capture B0 register (T32A03DMAREQCAPB0) 010: UART ch1 reception DMA request (UART1RX_DMAREQ) 011: I^2C ch1 receiving DMA request (I2C1RXDMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN11	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL11	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN11	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL10[2:0]	000	R/W	Input trigger selection (MDMAC A ch10) 000: T32A ch3 DMA request at match A1 register (T32A03DMAREQCMPA1) 001: T32A ch3 DMA request at match C1 register (T32A03DMAREQCMPC1) 010: T32A ch3 DMA request at capture A0 register (T32A03DMAREQCAPA0) 011: T32A ch3 DMA request at match C0 register (T32A03DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN10	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL10	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN10	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL9[2:0]	000	R/W	Input trigger selection (MDMAC A ch9) 000: T32A ch2 DMA request at match B1 register (T32A02DMAREQCMPB1) 001: T32A ch2 DMA request at capture B0 register (T32A02DMAREQCAPB0) 010: UART ch0 transmission DMA request (UART0TX_DMAREQ) 011: I^2C ch0 transmitting DMA request (I2C0TXDMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN9	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL9	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN9	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL8[2:0]	000	R/W	Input trigger selection (MDMAC A ch8) 000: T32A ch2 DMA request at match A1 register (T32A02DMAREQCMPA1) 001: T32A ch2 DMA request at match C1 register (T32A02DMAREQCMPC1) 010: T32A ch2 DMA request at capture A0 register (T32A02DMAREQCAPA0) 011: T32A ch2 DMA request at capture C0 register (T32A02DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN8	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL8	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN8	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.4. *[TSEL0CR3]* (Control Register 3)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL15[2:0]	000	R/W	Input trigger selection (MDMAC A ch15) 000: T32A ch5 DMA request at match B1 register (T32A05DMAREQCMPB1) 001: T32A ch5 DMA request at capture B0 register (T32A05DMAREQCAPB0) 010: FUART ch0 transmission DMA request (FUART0TX_DMAREQ) 011: I^2C ch2 transmitting DMA request (I2C2TXDMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN15	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL15	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN15	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL14[2:0]	000	R/W	Input trigger selection (MDMAC A ch14) 000: T32A ch5 DMA request at match A1 register (T32A05DMAREQCMPA1) 001: T32A ch5 DMA request at match C1 register (T32A05DMAREQCMPC1) 010: T32A ch5 DMA request at capture A0 register (T32A05DMAREQCAPA0) 011: T32A ch5 DMA request at capture C0 register (T32A05DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN14	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL14	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN14	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL13[2:0]	000	R/W	Input trigger selection (MDMAC A ch13) 000: T32A ch4 DMA request at match B1 register (T32A04DMAREQCMPB1) 001: T32A ch4 DMA request at capture B0 register (T32A04DMAREQCAPB0) 010: UART ch1 transmission DMA request (UART1TX_DMAREQ) 011: I^2C ch1 transmitting DMA request (I2C1TXDMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN13	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL13	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN13	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL12[2:0]	000	R/W	Input trigger selection (MDMAC A ch12) 000: T32A ch4 DMA request at match A1 register (T32A04DMAREQCMPA1) 001: T32A ch4 DMA request at match C1 register (T32A04DMAREQCMPC1) 010: T32A ch4 DMA request at capture A0 register (T32A04DMAREQCAPA0) 011: T32A ch4 DMA request at capture C0 register (T32A04DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN12	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL12	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN12	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.5. *[TSEL0CR4]* (Control Register 4)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL19[2:0]	000	R/W	Input trigger selection (MDMAC A ch19) 000: T32A ch7 DMA request at match B1 register (T32A07DMAREQCMPB1) 001: T32A ch7 DMA request at capture B0 register (T32A07DMAREQCAPB0) 010: UART ch2 reception DMA request (UART2RX_DMAREQ) 011: ADC unit A general purpose trigger DMA request (ADATRG_DMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN19	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL19	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN19	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL18[2:0]	000	R/W	Input trigger selection (MDMAC A ch18) 000: T32A ch7 DMA request at match A1 register (T32A07DMAREQCMPA1) 001: T32A ch7 DMA request at match C1 register (T32A07DMAREQCMPC1) 010: T32A ch7 DMA request at capture A0 register (T32A07DMAREQCAPA0) 011: T32A ch7 DMA request at capture C0 register (T32A07DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN18	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL18	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN18	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL17[2:0]	000	R/W	Input trigger selection (MDMAC A ch17) 000: T32A ch6 DMA request at match B1 register (T32A06DMAREQCMPB1) 001: T32A ch6 DMA request at capture B0 register (T32A06DMAREQCAPB0) 010: FUART ch0 reception DMA request (FUART0RX_DMAREQ) 011: I^2C ch2 receiving DMA request (I2C2RXDMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN17	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL17	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN17	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL16[2:0]	000	R/W	Input trigger selection (MDMAC A ch16) 000: T32A ch6 DMA request at match A1 register (T32A06DMAREQCMPA1) 001: T32A ch6 DMA request at match C1 register (T32A06DMAREQCMPC1) 010: T32A ch6 DMA request at capture A0 register (T32A06DMAREQCAPA0) 011: T32A ch6 DMA request at capture C0 register (T32A06DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN16	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL16	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN16	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.6. *[TSEL0CR5]* (Control Register 5)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL23[2:0]	000	R/W	Input trigger selection (MDMAC A ch23) 000: T32A ch9 DMA request at match B1 register (T32A09DMAREQCMPB1) 001: T32A ch9 DMA request at capture B0 register (T32A09DMAREQCAPB0) 010: T32A ch9 DMA request at capture A1 register (T32A09DMAREQCAPA1) 011: T32A ch9 DMA request at capture B1 register (T32A09DMAREQCAPB1) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN23	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL23	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN23	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL22[2:0]	000	R/W	Input trigger selection (MDMAC A ch22) 000: T32A ch9 DMA request at match A1 register (T32A09DMAREQCMPA1) 001: T32A ch9 DMA request at match C1 register (T32A09DMAREQCMPC1) 010: T32A ch9 DMA request at capture A0 register (T32A09DMAREQCAPA0) 011: T32A ch9 DMA request at capture C0 register (T32A09DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN22	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL22	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN22	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL21[2:0]	000	R/W	Input trigger selection (MDMAC A ch21) 000: T32A ch8 DMA request at match B1 register (T32A08DMAREQCMPB1) 001: T32A ch8 DMA request at capture B0 register (T32A08DMAREQCAPB0) 010: UART ch2 transmission DMA request (UART2TX_DMAREQ) 011: ADC unit A Highest priority DMA request (ADAHP_DMAREQ) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN21	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL21	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN21	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL20[2:0]	000	R/W	Input trigger selection (MDMAC A ch20) 000: T32A ch8 DMA request at match A1 register (T32A08DMAREQCMPA1) 001: T32A ch8 DMA request at match C1 register (T32A08DMAREQCMPC1) 010: T32A ch8 DMA request at capture A0 register (T32A08DMAREQCAPA0) 011: T32A ch8 DMA request at capture C0 register (T32A08DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN20	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL20	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN20	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.7. *[TSEL0CR6]* (Control Register 6)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL27[2:0]	000	R/W	Input trigger selection (MDMAC A ch27) 000: T32A ch11 DMA request at match B1 register (T32A11DMAREQCMPB1) 001: T32A ch11 DMA request at capture B0 register (T32A11DMAREQCAPB0) 010: T32A ch11 DMA request at capture A1 register (T32A11DMAREQCAPA1) 011: T32A ch11 DMA request at capture B1 register (T32A11DMAREQCAPB1) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN27	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL27	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN27	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL26[2:0]	000	R/W	Input trigger selection (MDMAC A ch26) 000: T32A ch11 DMA request at match A1 register (T32A11DMAREQCMPA1) 001: T32A ch11 DMA request at match C1 register (T32A11DMAREQCMPC1) 010: T32A ch11 DMA request at capture A0 register (T32A11DMAREQCAPA0) 011: T32A ch11 DMA request at capture C0 register (T32A11DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN26	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL26	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN26	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL25[2:0]	000	R/W	Input trigger selection (MDMAC A ch25) 000: T32A ch10 DMA request at match B1 register (T32A10DMAREQCMPB1) 001: T32A ch10 DMA request at capture B0 register (T32A10DMAREQCAPB0) 010: T32A ch10 DMA request at capture A1 register (T32A10DMAREQCAPA1) 011: T32A ch10 DMA request at capture B1 register (T32A10DMAREQCAPB1) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN25	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL25	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN25	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL24[2:0]	000	R/W	Input trigger selection (MDMAC A ch24) 000: T32A ch10 DMA request at match A1 register (T32A10DMAREQCMPA1) 001: T32A ch10 DMA request at match C1 register (T32A10DMAREQCMPC1) 010: T32A ch10 DMA request at capture A0 register (T32A10DMAREQCAPA0) 011: T32A ch10 DMA request at capture C0 register (T32A10DMAREQCAPC0) 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN24	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL24	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN24	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.8. *[TSEL0CR7]* (Control Register 7)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL31[2:0]	000	R/W	Input trigger selection (MDMAC A ch31) 000: T32A ch13 DMA request at match B1 register (T32A13DMAREQCMPB1) 001: UART ch5 transmission DMA request (UART5TX_DMAREQ) 010: TRGIN2 (PT3 pin) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved. When “010” (TRGIN2) is selected, <OUTSEL31> should be set to “1” (An edge is detected.).
27	-	0	R	Read as “0”.
26	UPDN31	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL31	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN31	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL30[2:0]	000	R/W	Input trigger selection (MDMAC A ch30) 000: T32A ch13 DMA request at match A1 register (T32A13DMAREQCMPA1) 001: T32A ch13 DMA request at match C1 register (T32A13DMAREQCMPC1) 010: UART ch5 reception DMA request (UART5RX_DMAREQ) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN30	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL30	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN30	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL29[2:0]	000	R/W	Input trigger selection (MDMAC A ch29) 000: T32A ch12 DMA request at match B1 register (T32A12DMAREQCMPB1) 001: UART ch3 transmission DMA request (UART3TX_DMAREQ) 010: A-PMD ch0 PWM interrupt (INTPWM0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN29	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL29	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN29	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL28[2:0]	000	R/W	Input trigger selection (MDMAC A ch28) 000: T32A ch12 DMA request at match A1 register (T32A12DMAREQCMPA1) 001: T32A ch12 DMA request at match C1 register (T32A12DMAREQCMPC1) 010: UART ch3 reception DMA request (UART3RX_DMAREQ) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN28	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL28	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN28	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.9. *[TSEL0CR8]* (Control Register 8)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL35[2:0]	000	R/W	Input trigger selection (T32A ch13 timer A) 000: RMC ch0 trigger output (RMC0TRG) 001: T32A ch2 timer register A0 match trigger (T32A02TRGOUTCMPA0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN35	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL35	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN35	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL34[2:0]	000	R/W	Input trigger selection (T32A ch8 timer A) 000: ELOSC low speed clock (fs) 001: Reserved. 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved. When “000” (ELOSC low speed clock) is selected, <OUTSEL34> should be set to “1” (An edge is detected.).
19	-	0	R	Read as “0”.
18	UPDN34	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL34	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN34	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL33[2:0]	000	R/W	Input trigger selection (ADC) 000: A-PMD ch0 ADC synchronous trigger output 0 (PMD0TRG0) 001: A-PMD ch0 ADC synchronous trigger output 1 (PMD0TRG1) 010: A-PMD ch0 ADC synchronous trigger output 2 (PMD0TRG2) 011: A-PMD ch0 ADC synchronous trigger output 3 (PMD0TRG3) 100: Reserved 101: Reserved 110: TRGSEL37 output (TRGSEL0OUT37) 111: TRGSEL38 output (TRGSEL0OUT38)
11	-	0	R	Read as “0”.
10	UPDN33	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL33	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN33	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL32[2:0]	000	R/W	Input trigger selection (ADC) 000: A-PMD ch0 ADC synchronous trigger output 0 (PMD0TRG0) 001: A-PMD ch0 ADC synchronous trigger output 1 (PMD0TRG1) 010: A-PMD ch0 ADC synchronous trigger output 2 (PMD0TRG2) 011: A-PMD ch0 ADC synchronous trigger output 3 (PMD0TRG3) 100: Reserved 101: Reserved 110: TRGSEL37 output (TRGSEL0OUT37) 111: TRGSEL38 output (TRGSEL0OUT38)
3	-	0	R	Read as “0”.
2	UPDN32	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL32	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN32	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.10. *[TSEL0CR9]* (Control Register 9)

Bit	Bit Symbol	After Reset	Type	Description
31	-	-	-	Read as “0”.
30:28	INSEL39[2:0]	000	R/W	Input trigger selection (T32A ch5 timer A) 000: T32A ch9 timer register A0 match trigger (T32A09TRGOUTCMPA0) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN39	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL39	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN39	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL38[2:0]	000	R/W	Input trigger selection (INSEL32,INSEL33) 000: T32A ch9 timer register A1 match trigger (T32A09TRGOUTCMPA1) 001: T32A ch9 timer register B1 match trigger (T32A09TRGOUTCMPB1) 010: T32A ch10 timer register A1 match trigger (T32A10TRGOUTCMPA1) 011: T32A ch10 timer register B1 match trigger (T32A10TRGOUTCMPB1) 100: T32A ch11 timer register A1 match trigger (T32A11TRGOUTCMPA1) 101: T32A ch11 timer register B1 match trigger (T32A11TRGOUTCMPB1) 110: TRGIN0 (PG3 pin) 111: TRGIN1 (PL7 pin) When “110” (TRGIN0) or “111” (TRGIN1) is selected, <OUTSEL38> should be set to “1” (An edge is detected.).
19	-	0	R	Read as “0”.
18	UPDN38	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL38	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN38	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL37[2:0]	000	R/W	Input trigger selection (INSEL32,INSEL33) 000: T32A ch9 timer register A1 match trigger (T32A09TRGOUTCMPA1) 001: T32A ch9 timer register B1 match trigger (T32A09TRGOUTCMPB1) 010: T32A ch10 timer register A1 match trigger (T32A10TRGOUTCMPA1) 011: T32A ch10 timer register B1 match trigger (T32A10TRGOUTCMPB1) 100: T32A ch11 timer register A1 match trigger (T32A11TRGOUTCMPA1) 101: T32A ch11 timer register B1 match trigger (T32A11TRGOUTCMPB1) 110: TRGIN0 (PG3 pin) 111: TRGIN1 (PL7 pin) When “110” (TRGIN0) or “111” (TRGIN1) is selected, <OUTSEL37> should be set to “1” (An edge is detected.).
11	-	0	R	Read as “0”.
10	UPDN37	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL37	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN37	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL36[2:0]	000	R/W	Input trigger selection (T32A ch13 timer B) 000: RMC ch1 trigger output (RMC1TRG) 001: T32A ch2 timer register A0 match trigger (T32A02TRGOUTCMPA0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN36	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL36	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN36	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.11. *[TSEL0CR10]* (Control Register 10)

Bit	Bit Symbol	After Reset	Type	Description
31	-	-	-	Read as “0”.
30:28	INSEL43[2:0]	000	R/W	Input trigger selection (T32A ch7 timer A) 000: T32A ch11 timer register A0 match trigger (T32A11TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN43	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL43	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN43	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL42[2:0]	000	R/W	Input trigger selection (T32A ch6 timer B) 000: T32A ch10 timer register A0 match trigger (T32A10TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN42	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL42	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN42	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL41[2:0]	000	R/W	Input trigger selection (T32A ch6 timer A) 000: T32A ch10 timer register A0 match trigger (T32A10TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN41	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL41	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN41	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL40[2:0]	000	R/W	Input trigger selection (T32A ch5 timer B) 000: T32A ch9 timer register A0 match trigger (T32A09TRGOUTCMPA0) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN40	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL40	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN40	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.12. *[TSEL0CR11]* (Control Register 11)

Bit	Bit Symbol	After Reset	Type	Description
31	-	-	-	Read as “0”.
30:28	INSEL47[2:0]	000	R/W	Input trigger selection (T32A ch0 timer B) 000: TSPI ch0 recieve completion (TSPI0RXDEND) 001: UART ch0 reception completion trigger (UART0RXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN47	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL47	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN47	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL46[2:0]	000	R/W	Input trigger selection (T32A ch0 timer A) 000: TSPI ch0 transmit completion (TSPI0TXDEND) 001: UART ch0 transmission completion trigger (UART0TXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN46	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL46	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN46	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL45[2:0]	000	R/W	Input trigger selection (T32A ch8 timer B) 000: T32A ch4 timer B output (T32A04OUTB) 001: T32A ch8 timer A output (T32A08OUTA) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN45	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL45	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN45	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL44[2:0]	000	R/W	Input trigger selection (T32A ch7 timer B) 000: T32A ch11 timer register A0 match trigger (T32A11TRGOUTCMPA0) 001: T32A ch13 timer register B0 match trigger (T32A13TRGOUTCMPB0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN44	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL44	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN44	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.13. *[TSEL0CR12]* (Control Register 12)

Bit	Bit Symbol	After Reset	Type	Description
31	-	-	-	Read as “0”.
30:28	INSEL51[2:0]	000	R/W	Input trigger selection (T32A ch2 timer B) 000: TSPI ch2 recive completion (TSPI2RXDEND) 001: UART ch2 reception completion trigger (UART2RXTRG) 010: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN51	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL51	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN51	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL50[2:0]	000	R/W	Input trigger selection (T32A ch2 timer A) 000: TSPI ch2 transmit completion (TSPI2TXDEND) 001: UART ch2 transmission completion trigger (UART2TXTRG) 010: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN50	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL50	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN50	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	-	0	R	Read as “0”.

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL49[2:0]	000	R/W	Input trigger selection (T32A ch1 timer B) 000: TSPI ch1 recieve completion (TSPI1RXDEND) 001: UART ch1 reception completion trigger (UART1RXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN49	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL49	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN49	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL48[2:0]	000	R/W	Input trigger selection (T32A ch1 timer A) 000: TSPI ch1 transmit completion (TSPI1TXDEND) 001: UART ch1 transmission completion trigger (UART1TXTRG) 010: T32A ch12 timer register A0 match trigger (T32A12TRGOUTCMPA0) 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN48	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL48	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN48	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.14. *[TSEL0CR13]* (Control Register 13)

Bit	Bit Symbol	After Reset	Type	Description
31	-	0	R	Read as “0”.
30:28	INSEL55[2:0]	000	R/W	Input trigger selection (T32A ch4 timer B) 000: TSPI ch4 transmt completion (TSPI4TXDEND) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
27	-	0	R	Read as “0”.
26	UPDN55	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
25	OUTSEL55	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
24	EN55	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	-	0	R	Read as “0”.
22:20	INSEL54[2:0]	000	R/W	Input trigger selection (T32A ch4 timer A) 000: TSPI ch4 transmit completion (TSPI4TXDEND) 001: T32A ch13 timer register A0 match trigger (T32A13TRGOUTCMPA0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
19	-	0	R	Read as “0”.
18	UPDN54	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
17	OUTSEL54	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
16	EN54	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

Bit	Bit Symbol	After Reset	Type	Description
15	-	0	R	Read as “0”.
14:12	INSEL53[2:0]	000	R/W	Input trigger selection (T32A ch3 timer B) 000: TSPI ch3 receive completion (TSPI3RXDEND) 001: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
11	-	0	R	Read as “0”.
10	UPDN53	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
9	OUTSEL53	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
8	EN53	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	-	0	R	Read as “0”.
6:4	INSEL52[2:0]	000	R/W	Input trigger selection (T32A ch3 timer A) 000: TSPI ch3 transmit completion (TSPI3TXDEND) 001: T32A ch12 timer register B0 match trigger (T32A12TRGOUTCMPB0) 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
3	-	0	R	Read as “0”.
2	UPDN52	0	R/W	Edge detection condition 0: Rising edge is detected. 1: Falling edge is detected.
1	OUTSEL52	0	R/W	Output trigger selection 0: No edge detection 1: An edge is detected.
0	EN52	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.3. Clock Selective Watchdog Timer (SIWDT)

2.3.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.10 SIWDT built-in channel

Product	SIWDT channel (✓: Available, -: N/A)
	Channel 0
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.3.2. Count clock

The SIWDT can select the clock to count. The clock which can be selected as the following table is shown.

Table 2.11 SIWDT count clock

Clock	Signal name	Selection
System clock	fsys	It selects by the ***[SIWD0MOD]***<WDCLS> register.
Internal High Speed Oscillator1 Clock (Note1)	f_{IHOSC1}	
Internal High Speed Oscillator2 Clock (Note2)	f_{IHOSC2}	

Note1: The oscillation control register is ***[CGOSCCR]***<IHOSC1EN>.
Note2: The oscillation control register is ***[RLMLOSCCR]***<POSCEN>.

2.3.3. Protect function

TMPM4G group (1) does not support protect A mode. To use the protect function, use protect B mode.

2.3.4. Oscillation clock protection function

TMPM4G group (1) has no oscillation clock protect function.

Therefore, ***[SIWDxOSCCR]*** (oscillation clock protect control register) can not be used.

2.4. Oscillation Frequency Detection Circuit (OFD)

2.4.1. Built-in list

The following table shows the built-in list for each product.

Table 2.12 OFD buitl-in list

Product	Built-in OFD (✓:Available, -: N/A)
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.4.2. Reference clock

The OFD operates with the clock in the following table as the reference clock.

Table 2.13 OFD reference clock

Reference clock	Signal name	Divide value
Internal High speed oscillator 2	f_{IHOSC2}	128

Note: The oscillation control register is ***[RLMLOSCCR]***<POSCEN>.

2.4.3. Detection object clock

The OFD selects clock to monitor from the detection object clock of the following table.

Table 2.14 OFD clock for detection

Detection target clock		Signal name
Input signal	External High speed oscillator clock	f_{EHOSC}
	Selected clock by the ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> in CG(Clock control block)	fc

2.5. Debug Interface

2.5.1. Debugging interface terminal list of each product.

Table 2.15 Debugging interface terminal list

Debug pin (Signal name)	Port	Product table (✓: Available, -: N/A)			
		M4G9	M4G8	M4G7	M4G6
SWDIO	PH4	✓	✓	✓	✓
TMS					
SWCLK	PH5	✓	✓	✓	✓
TCK					
SWV	PH6	✓	✓	✓	✓
TDO					
TDI	PH3	✓	✓	✓	✓
TRST_N	PH7	✓	✓	✓	✓
TRACECLK	PG6	✓	✓	✓	✓
TRACEDATA0	PG7	✓	✓	✓	✓
TRACEDATA1	PH0	✓	✓	✓	✓
TRACEDATA2	PH1	✓	✓	✓	✓
TRACEDATA3	PH2	✓	✓	✓	✓

2.6. Non break Debug Interface (NBDIF)

2.6.1. Support products

The NBDIF is supported by the following products.

Table 2.16 NBDIF support product

Product	NBDIF support (✓: Supportted, -: Unsupported)
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.6.2. List of NBDIF pins in each product

Table 2.17 NBDIF pins list

NBDIF pin (Signal name)	Port	Product table (✓: Available, -: N/A)			
		M4G9	M4G8	M4G7	M4G6
NBDCLK	PG6	✓	✓	✓	✓
NBDDATA0	PG7	✓	✓	✓	✓
NBDDATA1	PH0	✓	✓	✓	✓
NBDDATA2	PH1	✓	✓	✓	✓
NBDDATA3	PH2	✓	✓	✓	✓
NBDSYNC	PH3	✓	✓	✓	✓

2.7. Flash Memory

2.7.1. Clock for the programming/erasing

As for flash memory, the clock of the following tables is used for programming/erasing of the code flash or the data flash.

Table 2.18 Clock for programming/erasing

Clock for programming/erasing
f_{IHOSC1}

Note: The oscillation control register is ***[CGOSCCR]***<IHOSC1EN>.

2.7.2. The code flash block configuration of each product

The code flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.19 The code flash (Block) of each product

FLASH I/F	Area	Block name		TMPM4G9F15FG TMPM4G9F15XBG TMPM4G8F15FG TMPM4G8F15XBG	TMPM4G9F10FG TMPM4G9F10XBG TMPM4G8F10FG TMPM4G8F10XBG TMPM4G7F10FG TMPM4G6F10FG	TMPM4G9FEFG TMPM4G9FEXBG TMPM4G8FEFG TMPM4G8FEXBG TMPM4G7FEFG TMPM4G6FEFG	TMPM4G9FDFG TMPM4G9FDXBG TMPM4G8FDFG TMPM4G8FDXBG TMPM4G7FDFG TMPM4G6FDFG	Block size (KB)
0	0	Block0	PG0	✓	✓	✓	✓	4
			PG1	✓	✓	✓	✓	4
			PG2	✓	✓	✓	✓	4
			PG3	✓	✓	✓	✓	4
			PG4	✓	✓	✓	✓	4
			PG5	✓	✓	✓	✓	4
			PG6	✓	✓	✓	✓	4
			PG7	✓	✓	✓	✓	4
		Block1		✓	✓	✓	✓	32
		Block2		✓	✓	✓	✓	32
		Block3		✓	✓	✓	✓	32
		Block4		✓	✓	✓	✓	32
		Block5		✓	✓	✓	✓	32
		Block6		✓	✓	✓	✓	32
		Block7		✓	✓	✓	✓	32
		Block8		✓	✓	✓	✓	32
		Block9		✓	✓	✓	✓	32
		Block10		✓	✓	✓	✓	32
		Block11		✓	✓	✓	✓	32
		Block12		✓	✓	✓	✓	32
		Block13		✓	✓	✓	✓	32
		Block14		✓	✓	✓	✓	32
		Block15		✓	✓	✓	✓	32

0	1	Block16	✓	✓	✓	-	32
		Block17	✓	✓	✓	-	32
		Block18	✓	✓	✓	-	32
		Block19	✓	✓	✓	-	32
		Block20	✓	✓	✓	-	32
		Block21	✓	✓	✓	-	32
		Block22	✓	✓	✓	-	32
		Block23	✓	✓	✓	-	32
		Block24	✓	✓	-	-	32
		Block25	✓	✓	-	-	32
		Block26	✓	✓	-	-	32
		Block27	✓	✓	-	-	32
		Block28	✓	✓	-	-	32
		Block29	✓	✓	-	-	32
		Block30	✓	✓	-	-	32
		Block31	✓	✓	-	-	32
1	2	Block0	PG0	✓	-	-	-	4
			PG1	✓	-	-	-	4
			PG2	✓	-	-	-	4
			PG3	✓	-	-	-	4
			PG4	✓	-	-	-	4
			PG5	✓	-	-	-	4
			PG6	✓	-	-	-	4
			PG7	✓	-	-	-	32
		Block1		✓	-	-	-	32
		Block2		✓	-	-	-	32
		Block3		✓	-	-	-	32
		Block4		✓	-	-	-	32
		Block5		✓	-	-	-	32
		Block6		✓	-	-	-	32
		Block7		✓	-	-	-	32
		Block8		✓	-	-	-	32
		Block9		✓	-	-	-	32
		Block10		✓	-	-	-	32
		Block11		✓	-	-	-	32
		Block12		✓	-	-	-	32
		Block13		✓	-	-	-	32
		Block14		✓	-	-	-	32
		Block15		✓	-	-	-	32

Note: ✓: Available, -: N/A

2.7.3. The data flash block configuration of each product

The data flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.20 The data flash (Block) of each product

FLASH I/F	Area	Block name	TMPM4G9F15FG TMPM4G9F15XBG TMPM4G8F15FG TMPM4G8F15XBG	TMPM4G9F10FG TMPM4G9F10XBG TMPM4G8F10FG TMPM4G8F10XBG TMPM4G7F10FG TMPM4G6F10FG	TMPM4G9FEFG TMPM4G9FEXBG TMPM4G8FEFG TMPM4G8FEXBG TMPM4G7FEFG, TMPM4G6FEFG	TMPM4G9FDFG TMPM4G9FDXBG TMPM4G8FDFG TMPM4G8FDXBG TMPM4G7FDFG TMPM4G6FDFG	Block size (KB)
2	4	Block0	✓	✓	✓	✓	4
		Block1	✓	✓	✓	✓	4
		Block2	✓	✓	✓	✓	4
		Block3	✓	✓	✓	✓	4
		Block4	✓	✓	✓	✓	4
		Block5	✓	✓	✓	✓	4
		Block6	✓	✓	✓	✓	4
		Block7	✓	✓	✓	✓	4

Note: ✓: Available, -: N/A

2.7.4. Single boot use resource

The peripheral function of the following table is used in single boot.

Table 2.21 Single boot use resource

Peripheral function	Channel	Pin name
BOOT	-	PY4 (BOOT_N)
UART	ch 0	PH4/PH5 (UT0TXDA/UT0RXD),
T32A	ch 0	-

The single boot mode can be set by reset release from the RESET_N pin or from the power on reset (POR).

The range of the RAM address transmitted by the RAM loader command should use the following table.

Table 2.22 The end address in which RAM transmission is possible

Product name	The end address in which RAM transmission is possible
TMPM4G9F15FG TMPM4G9F15XBG TMPM4G8F15FG TMPM4G8F15XBG TMPM4G9F10FG TMPM4G9F10XBG TMPM4G8F10FG TMPM4G8F10XBG TMPM4G7F10FG TMPM4G6F10FG	0x20000400 to 0x2001FFFF
TMPM4G9FEFG TMPM4G9FEXBG TMPM4G8FEFG TMPM4G8FEXBG TMPM4G7FEFG TMPM4G6FEFG TMPM4G9FDFG TMPM4G9FDXBG TMPM4G8FDFG TMPM4G8FDXBG TMPM4G7FDFG TMPM4G6FDFG	0x20000400 to 0x20017FFF

2.8. HDMA Controller (HDMAC)

2.8.1. Built-in unit

Built-in unit per product are shown in the following table.

Table 2.23 HDMAC built-in unit

Product	HDMAC unit (✓: Available, -: N/A)	
	unit A	unit B
M4G9	✓	✓
M4G8	✓	✓
M4G7	✓	✓
M4G6	✓	✓

2.8.2. DMA transfer request list

A DMA transfer request list is shown in the following table.

"-" in a table does not have an applicable function.

Table 2.24 HDMAC DMA transfer request list: unit A

Ch No.	Single transfer request		Burst transfer request	
		Signal name		Signal name
0	TSPI ch0 receive DMA request	TSPI0RX_DMA	TSPI ch0 receive DMA request	TSPI0RX_DMA
1	TSPI ch0 transmit DMA request	TSPI0TX_DMA	TSPI ch0 transmit DMA request	TSPI0TX_DMA
2	TSPI ch2 receive DMA request	TSPI2RX_DMA	TSPI ch2 receive DMA request	TSPI2RX_DMA
3	TSPI ch2 transmit DMA request	TSPI2TX_DMA	TSPI ch2 transmit DMA request	TSPI2TX_DMA
4	TSPI ch4 receive DMA request	TSPI4RX_DMA	TSPI ch4 receive DMA request	TSPI4RX_DMA
5	TSPI ch4 transmit DMA request	TSPI4TX_DMA	TSPI ch4 transmit DMA request	TSPI4TX_DMA
6	-	-	SMIF ch0 interrupt	INTSMI0
7	-	-	-	-
8	-	-	-	-
9	-	-	-	-
10	-	-	-	-
11	-	-	-	-
12	-	-	-	-
13	-	-	-	-
14	-	-	-	-
15	-	-	PB1 (HDMAREQA) Trigger input (Note)	PB1 (HDMAREQA)

Note: When DMA request is done, "High" level should be input to Port PB1 for the interval of 2 x fsysh cycles or more.

Table 2.25 HDMAC DMA transfer request list: unit B

Ch No.	Single transfer request		Burst transfer request	
		Signal name		Signal name
0	TSPI ch1 receive DMA request	TSPI1RX_DMA	TSPI ch1 receive DMA request	TSPI1RX_DMA
1	TSPI ch1 transmit DMA request	TSPI1TX_DMA	TSPI ch1 transmit DMA request	TSPI1TX_DMA
2	TSPI ch3 receive DMA request	TSPI3RX_DMA	TSPI ch3 receive DMA request	TSPI3RX_DMA
3	TSPI ch3 transmit DMA request	TSPI3TX_DMA	TSPI ch3 transmit DMA request	TSPI3TX_DMA
4	TSPI ch5 receive DMA request (Note1)	TSPI5RX_DMA	TSPI ch5 receive DMA request (Note1)	TSPI5RX_DMA
5	TSPI ch5 transmit DMA request (Note1)	TSPI5TX_DMA	TSPI ch5 transmit DMA request (Note1)	TSPI5TX_DMA
6	-	-	-	-
7	-	-	-	-
8	-	-	-	-
9	-	-	-	-
10	-	-	-	-
11	-	-	-	-
12	-	-	-	-
13	-	-	-	-
14	-	-	-	-
15	-	-	PK1 (HDMAREQB) Trigger input (Note2)	PK1 (HDMAREQB)

Note1: M4G6 product does not have this function.

Note2: When DMA request is done, “High” level should be input to Port PK1 for the interval of 2 x fsysh cycles or more.

2.9. MDMA Controller (MDMAC)

2.9.1. Built-in unit

Built-in unit per product are shown in the following table.

Table 2.26 MDMAC built-in unit

Product	MDMAC unit (✓: Available, -: N/A)
	unit A
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.9.2. DMA transfer request list

A DMAC transfer request list is shown in the following table.
The channel which has a register name in the trigger selector column of a table should select the request used by a trigger selector. "-" in a table does not have an applicable function.

Table 2.27 MDMAC DMA transfer request list: unit A (1/4)

Channel	Single transfer request			Burst transfer request	
	Trigger selector		Signal name		Signal name
ch0	***[TSEL0CR0]*** <INSEL0[2:0]> (Note1)	TSPI ch6 receive DMA request (Note3) (Note4)	TSPI6RX_DMA	-	-
		UART ch4 reception DMA request (Note3) (Note4)	UART4RX_DMAREQ		
		I^2C ch3 receiving DMA request (Note3) (Note4)	I2C3RXDMAREQ		
		T32A ch0 DMA request at capture A0 register	T32A00DMAREQCAPA0		
ch1	***[TSEL0CR0]*** <INSEL1[2:0]> (Note1)	TSPI ch6 transmit DMA request (Note3) (Note4)	TSPI6TX_DMA	-	-
		UART ch4 transmission DMA request (Note3) (Note4)	UART4TX_DMAREQ		
		I^2C ch3 transmitting DMA request (Note3) (Note4)	I2C3TXDMAREQ		
		T32A ch0 DMA request at capture C0 register	T32A00DMAREQCAPC0		
ch2	***[TSEL0CR0]*** <INSEL2[2:0]> (Note1)	TSPI ch7 receive DMA request (Note3) (Note4)	TSPI7RX_DMA	-	-
		FUART ch1 reception DMA request (Note3) (Note4)	FUART1RX_DMAREQ		
		I^2C ch4 receiving DMA request (Note3) (Note4)	I2C4RXDMAREQ		
ch3	***[TSEL0CR0]*** <INSEL3[2:0]> (Note1)	TSPI ch7 transmit DMA request (Note3) (Note4)	TSPI7TX_DMA	-	-
		FUART ch1 transmission DMA request (Note3) (Note4)	FUART1TX_DMAREQ		
		I^2C ch4 transmitting DMA request (Note3) (Note4)	I2C4TXDMAREQ		
ch4	***[TSEL0CR1]*** <INSEL4[2:0]> (Note1)	TSPI ch8 receive DMA request (Note2) (Note3) (Note4)	TSPI8RX_DMA	-	-
		T32A ch0 DMA request at comparison match A1 register	T32A00DMAREQCMPA1		
		T32A ch0 DMA request at comparison match C1 register	T32A00DMAREQCMPC1		
ch5	***[TSEL0CR1]*** <INSEL5[2:0]> (Note1)	TSPI ch8 transmit DMA request (Note2) (Note3) (Note4)	TSPI8TX_DMA	-	-
		T32A ch0 DMA request at comparison match B1 register	T32A00DMAREQCMPB1		
		T32A ch0 DMA request at capture B0 register	T32A00DMAREQCAPB0		

Note1: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to " 2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: M4G8 product does not have this function.

Note3: M4G7 product does not have this function.

Note4: M4G6 product does not have this function.

Table 2.28 MDMAC DMA transfer request list: unit A (2/4)

Channel	Single transfer request			Burst transfer request	
	Trigger Selector		Signal name		Signal name
ch6	***[TSEL0CR1]*** <INSEL6[2:0]> (Note)	T32A ch1 DMA request at match A1 register	T32A01DMAREQCMPA1	-	-
		T32A ch1 DMA request at match C1 register	T32A01DMAREQCMPC1		
		T32A ch1 DMA request at capture A0 register	T32A01DMAREQCAPA0		
		T32A ch1 DMA request at capture C0 register	T32A01DMAREQCAPC0		
ch7	***[TSEL0CR1]*** <INSEL7[2:0]> (Note)	T32A ch1 DMA request at match B1 register	T32A01DMAREQCMPB1	-	-
		T32A ch1 DMA request at capture B0 register	T32A01DMAREQCAPB0		
		UART ch0 reception DMA request	UART0RX_DMAREQ		
		I^2C ch0 receiving DMA request	I2C0RXDMAREQ		
ch8	***[TSEL0CR2]*** <INSEL8[2:0]> (Note)	T32A ch2 DMA request at match A1 register	T32A02DMAREQCMPA1	-	-
		T32A ch2 DMA request at match C1 register	T32A02DMAREQCMPC1		
		T32A ch2 DMA request at capture A0 register	T32A02DMAREQCAPA0		
		T32A ch2 DMA request at capture C0 register	T32A02DMAREQCAPC0		
ch9	***[TSEL0CR2]*** <INSEL9[2:0]> (Note)	T32A ch2 c DMA request at match B1 register	T32A02DMAREQCMPB1	-	-
		T32A ch2 DMA request at capture B0 register	T32A02DMAREQCAPB0		
		UART ch0 transmission DMA request	UART0TX_DMAREQ		
		I^2C ch0 transmitting DMA request	I2C0TXDMAREQ		
ch10	***[TSEL0CR2]*** <INSEL10[2:0]> (Note)	T32A ch3 DMA request at match A1 register	T32A03DMAREQCMPA1	-	-
		T32A ch3 DMA request at match C1 register	T32A03DMAREQCMPC1		
		T32A ch3 DMA request at capture A0 register	T32A03DMAREQCAPA0		
		T32A ch3 DMA request at capture C0 register	T32A03DMAREQCAPC0		
ch11	***[TSEL0CR2]*** <INSEL11[2:0]> (Note)	T32A ch3 DMA request at match B1 register	T32A03DMAREQCMPB1	-	-
		T32A ch3 DMA request at capture B0 register	T32A03DMAREQCAPB0		
		UART ch1 reception DMA request	UART1RX_DMAREQ		
		I^2C ch1 receiving DMA request	I2C1RXDMAREQ		
ch12	***[TSEL0CR3]*** <INSEL12[2:0]> (Note)	T32A ch4 DMA request at match A1 register	T32A04DMAREQCMPA1	-	-
		T32A ch4 DMA request at match C1 register	T32A04DMAREQCMPC1		
		T32A ch4 DMA request at capture A0 register	T32A04DMAREQCAPA0		
		T32A ch4 DMA request at capture C0 register	T32A04DMAREQCAPC0		
ch13	***[TSEL0CR3]*** <INSEL13[2:0]> (Note)	T32A ch4 DMA request at match B1 register	T32A04DMAREQCMPB1	-	-
		T32A ch4 DMA request at capture B0 register	T32A04DMAREQCAPB0		
		UART ch1 transmission DMA request	UART1TX_DMAREQ		
		I^2C ch1 transmitting DMA request	I2C1TXDMAREQ		
ch14	***[TSEL0CR3]*** <INSEL14[2:0]> (Note)	T32A ch5 DMA request at match A1 register	T32A05DMAREQCMPA1	-	-
		T32A ch5 DMA request at match C1 register	T32A05DMAREQCMPC1		
		T32A ch5 DMA request at capture A0 register	T32A05DMAREQCAPA0		
		T32A ch5 DMA request at capture C0 register	T32A05DMAREQCAPC0		
ch15	***[TSEL0CR3]*** <INSEL15[2:0]> (Note)	T32A ch5 DMA request at match B1 register	T32A05DMAREQCMPB1	-	-
		T32A ch5 DMA request at capture B0 register	T32A05DMAREQCAPB0		
		FUART ch0 transmission DMA request	FUART0TX_DMAREQ		
		I^2C ch2 transmitting DMA request	I2C2TXDMAREQ		
ch16	***[TSEL0CR4]*** <INSEL16[2:0]> (Note)	T32A ch6 DMA request at match A1 register	T32A06DMAREQCMPA1	-	-
		T32A ch6 DMA request at match C1 register	T32A06DMAREQCMPC1		
		T32A ch6 DMA request at capture A0 register	T32A06DMAREQCAPA0		
		T32A ch6 DMA request at capture C0 register	T32A06DMAREQCAPC0		

Note: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to " 2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.29 MDMAC DMA transfer request list: unit A (3/4)

Channel	Single transfer request			Burst transfer request	
	Trigger sector		Signal name		Signal name
ch17	***[TSEL0CR4]*** <INSEL17[2:0]> (Note)	T32A ch6 DMA request at match B1 register	T32A06DMAREQCMPB1	-	-
		T32A ch6 DMA request at capture B0 register	T32A06DMAREQCAPB0		
		FUART ch0 reception DMA request	FUART0RX_DMAREQ		
		I^2C ch2 receiving DMA request	I2C2RXDMAREQ		
ch18	***[TSEL0CR4]*** <INSEL18[2:0]> (Note)	T32A ch7 DMA request at match A1 register	T32A07DMAREQCMPA1	-	-
		T32A ch7 DMA request at match C1 register	T32A07DMAREQCMPC1		
		T32A ch7 DMA request at capture A0 register	T32A07DMAREQCAPA0		
		T32A ch7 DMA request at capture C0 register	T32A07DMAREQCAPC0		
ch19	***[TSEL0CR4]*** <INSEL19[2:0]> (Note)	T32A ch7 DMA request at match B1 register	T32A07DMAREQCMPB1	-	-
		T32A ch7 DMA request at capture B0 register	T32A07DMAREQCAPB0		
		UART ch2 reception DMA request	UART2RX_DMAREQ		
		ADC unit A general purpose trigger DMA request	ADATRG_DMAREQ		
ch20	***[TSEL0CR5]*** <INSEL20[2:0]> (Note)	T32A ch8 DMA request at match A1 register	T32A08DMAREQCMPA1	-	-
		T32A ch8 DMA request at match C1 register	T32A08DMAREQCMPC1		
		T32A ch8 DMA request at capture A0 register	T32A08DMAREQCAPA0		
		T32A ch8 DMA request at capture C0 register	T32A08DMAREQCAPC0		
ch21	***[TSEL0CR5]*** <INSEL21[2:0]> (Note)	T32A ch8 DMA request at match B1 register	T32A08DMAREQCMPB1	-	-
		T32A ch8 DMA request at capture B0 register	T32A08DMAREQCAPB0		
		UART ch2 transmission DMA request	UART2TX_DMAREQ		
		ADC unit A Highest priority conversion	ADAHP_DMAREQ		
ch22	***[TSEL0CR5]*** <INSEL22[2:0]> (Note)	T32A ch9 DMA request at match A1 register	T32A09DMAREQCMPA1	-	-
		T32A ch9 DMA request at match C1 register	T32A09DMAREQCMPC1		
		T32A ch9 DMA request at capture A0 register	T32A09DMAREQCAPA0		
		T32A ch9 DMA request at capture C0 register	T32A09DMAREQCAPC0		
ch23	***[TSEL0CR5]*** <INSEL23[2:0]> (Note)	T32A ch9 DMA request at match B1 register	T32A09DMAREQCMPB1	-	-
		T32A ch9 DMA request at capture B0 register	T32A09DMAREQCAPB0		
		T32A ch9 DMA request at capture A1 register	T32A09DMAREQCAPA1		
		T32A ch9 DMA request at capture B1 register	T32A09DMAREQCAPB1		
ch24	***[TSEL0CR6]*** <INSEL24[2:0]> (Note)	T32A ch10 DMA request at match A1 register	T32A10DMAREQCMPA1	-	-
		T32A ch10 DMA request at match C1 register	T32A10DMAREQCMPC1		
		T32A ch10 DMA request at capture A0 register	T32A10DMAREQCAPA0		
		T32A ch10 DMA request at capture C0 register	T32A10DMAREQCAPC0		
ch25	***[TSEL0CR6]*** <INSEL25[2:0]> (Note)	T32A ch10 DMA request at match B1 register	T32A10DMAREQCMPB1	-	-
		T32A ch10 DMA request at capture B0 register	T32A10DMAREQCAPB0		
		T32A ch10 DMA request at capture A1 register	T32A10DMAREQCAPA1		
		T32A ch10 DMA request at capture B1 register	T32A10DMAREQCAPB1		
ch26	***[TSEL0CR6]*** <INSEL26[2:0]> (Note)	T32A ch11 DMA request at match A1 register	T32A11DMAREQCMPA1	-	-
		T32A ch11 DMA request at match C1 register	T32A11DMAREQCMPC1		
		T32A ch11 DMA request at capture A0 register	T32A11DMAREQCAPA0		
		T32A ch11 DMA request at capture C0 register	T32A11DMAREQCAPC0		
ch27	***[TSEL0CR6]*** <INSEL27[2:0]> (Note)	T32A ch11 DMA request at match B1 register	T32A11DMAREQCMPB1	-	-
		T32A ch11 DMA request at capture B0 register	T32A11DMAREQCAPB0		
		T32A ch11 DMA request at capture A1 register	T32A11DMAREQCAPA1		
		T32A ch11 DMA request at capture B1 register	T32A11DMAREQCAPB1		

Note: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to "2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Table 2.30 MDMAC DMA transfer request list: unit A (4/4)

Channel	Single transfer request			Burst transfer request	
	Trigger Selector		Signal name		Signal name
ch28	***[TSEL0CR7]*** <INSEL28[2:0]> (Note1)	T32A ch12 DMA request at match A1 register	T32A12DMAREQCMPA1	-	-
		T32A ch12 DMA request at match C1 register	T32A12DMAREQCMPC1		
		UART ch3 reception DMA request (Note4)	UART3RX_DMAREQ		
ch29	***[TSEL0CR7]*** <INSEL29[2:0]> (Note1)	T32A ch12 DMA request at match B1 register	T32A12DMAREQCMPB1	-	-
		UART ch3 transmission DMA request (Note4)	UART3TX_DMAREQ		
		A-PMD ch0 PWM interrupt	INTPWM0		
ch30	***[TSEL0CR7]*** <INSEL30[2:0]> (Note1)	T32A ch13 DMA request at match A1 register	T32A13DMAREQCMPA1	-	-
		T32A ch13 DMA request at match C1 register	T32A13DMAREQCMPC1		
		UART ch5 reception DMA request (Note2) (Note3) (Note4)	UART5RX_DMAREQ		
ch31	***[TSEL0CR7]*** <INSEL31[2:0]> (Note1)	T32A ch13 DMA request at match B1 register	T32A13DMAREQCMPB1	-	-
		UART ch5 transmission DMA request (Note2) (Note3) (Note4)	UART5TX_DMAREQ		
		TRGIN2 (PT3 pin) (Note5)	TRGIN2		

Note1: Ch0 to ch31 select the trigger source of a DMA transfer request by a trigger selector. Please refer to " 2.2. Trigger Selector (TRGSEL)" for the detailed connection.

Note2: M4G8 product does not have this function.

Note3: M4G7 product does not have this function.

Note4: M4G6 product does not have this function.

Note5: When DMA request is done, "High" level should be input to Port PT3 for the interval of 3 x fsysm cycles or more.

2.10. Advanced Programmable Motor Control Circuit (A-PMD)

2.10.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.31 A-PMD built-in channel

Product	A-PMD channel (✓: Available, -: N/A)
	Channel 0
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.10.2. Function pin and port

The functional terminal is assigned to the following ports.

Table 2.32 A-PMD functional pin

Channel	Function pin		Signal name	Port	Product table (✓: Available, -: N/A)			
					M4G9	M4G8	M4G7	M4G6
ch0	XO0	Output	XO0	PD1	✓	✓	✓	✓
				PV1	✓	✓	✓	-
	YO0	Output	YO0	PD3	✓	✓	✓	✓
				PV3	✓	✓	✓	-
	ZO0	Output	ZO0	PD5	✓	✓	✓	✓
				PV5	✓	✓	✓	-
	UO0	Output	UO0	PD0	✓	✓	✓	✓
				PV0	✓	✓	✓	-
	VO0	Output	VO0	PD2	✓	✓	✓	✓
				PV2	✓	✓	✓	-
	WO0	Output	WO0	PD4	✓	✓	✓	✓
				PV4	✓	✓	✓	-
	EMG0	Input	EMG0	PD6	✓	✓	✓	✓
				PV6	✓	✓	✓	-
	OVV0	Input	OVV0	PD7	✓	✓	✓	✓
				PV7	✓	✓	✓	-

2.10.3. DMA Request

The A-PMD has the DMA request shown in the following table.

Table 2.33 A-PMD DMA request

Channel	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch0	PWM interrupt	INTPWM0	***[TSEL0CR7]*** <INSEL29[2:0]>	29	✓	-

Note: ✓: Available, -: Not available.

2.10.4. Internal signal connection specification

Some internal signals are connected to a peripheral function in the A-PMD, as shown in the following table.

2.10.4.1. ADC connection

Table 2.34 A-PMD inside connection list: Output

I/O	Function output		Output destination		
		Signal name	Trigger Selector		Signal name
Output	ADC synchronous trigger outpu 0	PMD0TRG0	***[TSEL0CR8]*** <INSEL32[2:0]>	ADC ch0 Highest priority trigger input	AD0HPTRGIN
	ADC synchronous trigger outpu 1	PMD0TRG1			
	ADC synchronous trigger outpu 2	PMD0TRG2			
	ADC synchronous trigger outpu 3	PMD0TRG3			
	ADC synchronous trigger outpu 0	PMD0TRG0	***[TSEL0CR8]*** <INSEL33[2:0]>	ADC ch0 General purpose trigger DMA request input	AD0TRGIN
	ADC synchronous trigger outpu 1	PMD0TRG1			
	ADC synchronous trigger outpu 2	PMD0TRG2			
	ADC synchronous trigger outpu 3	PMD0TRG3			

2.11. 12-bit Analog to Digital Converter (ADC)

2.11.1. Built-in unit

Built-in unit per product are shown in the following table.

Table 2.35 ADC built-in unit

Product	ADC unit (✓: Available, -: N/A)
	unit A
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.11.2. Function pin and port

The functional pin is assigned to the port of the following table.

There is also a channel which does not have a functional pin by a product.

Table 2.36 ADC function pin and port

Input channel	Function pin (Signal name)	Port	Product table (✓: Available, -: N/A)			
			M4G9	M4G8	M4G7	M4G6
ch0	AINA00	PN0	✓	✓	✓	✓
ch1	AINA01	PN1	✓	✓	✓	✓
ch2	AINA02	PN2	✓	✓	✓	✓
ch3	AINA03	PN3	✓	✓	✓	✓
ch4	AINA04	PN4	✓	✓	✓	✓
ch5	AINA05	PN5	✓	✓	✓	✓
ch6	AINA06	PN6	✓	✓	✓	✓
ch7	AINA07	PN7	✓	✓	✓	✓
ch8	AINA08	PP0	✓	✓	✓	✓
ch9	AINA09	PP1	✓	✓	✓	✓
ch10	AINA10	PP2	✓	✓	✓	✓
ch11	AINA11	PP3	✓	✓	✓	✓
ch12	AINA12	PP4	✓	✓	✓	✓
ch13	AINA13	PP5	✓	✓	✓	✓
ch14	AINA14	PP6	✓	✓	✓	✓
ch15	AINA15	PP7	✓	✓	✓	✓
ch16	AINA16	PR0	✓	✓	✓	-
ch17	AINA17	PR1	✓	✓	✓	-
ch18	AINA18	PR2	✓	✓	✓	-
ch19	AINA19	PR3	✓	✓	✓	-
ch20	AINA20	PR4	✓	✓	-	-
ch21	AINA21	PR5	✓	✓	-	-
ch22	AINA22	PR6	✓	✓	-	-
ch23	AINA23	PR7	✓	✓	-	-

2.11.3. Analog reference pins

The analog reference pins (VREFHA, VREFLA) are shared with the analog power supply pins (AVDD3, AVSS).

2.11.4. Clock for the ADC conversion

The clock which shows the 12-bit Analog to Digital Converter in the following table at the conversion clock is used.

Table 2.37 ADC clock for the conversion

Clock for the conversion
ADCLK

2.11.5. Set of mode setting register 2

Please be sure to set up the value of the following table about the setting value of the mode setting register 2 (***[ADxMOD2]***).

Table 2.38 ADC set of mode setting register 2

Register name	Value
[ADxMOD2]<MOD2[31:0]>	0x00000000

2.11.6. DMA request

A 12-bit Analog to Digital Converter has the DMA request shown in the following table.

Table 2.39 ADC DMA request

Unit	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
A	General purpose trigger DMA request	ADATRG_DMAREQ	***[TSEL0CR4]*** <INSEL19[2:0]>	19	✓	-
	Highest priority DMA request	ADAHP_DMAREQ	***[TSEL0CR5]*** <INSEL21[2:0]>	21	✓	-

Note: ✓: Available, -: Not available.

2.11.7. Monitoring functions

The monitoring function supports the functions shown in the following table.

Table 2.40 ADC supported monitoring functions

Function	Support (✓: Supportted, -: Unsupported)
Monitor Function 0	✓
Monitor Function 1	✓
Monitor Function 2	-
Monitor Function 3	-

2.11.8. Internal signal connection specification

2.11.8.1. Start trigger connection specification

The 12-bit Analog to Digital Converter has a conversion function by the trigger signal.

The input trigger signal which has a register name in the trigger selector column of the following table should select the input trigger used by a trigger selector.

Table 2.41 ADC start-up trigger connection specification

Connection destination (Signal name)	Start-up trigger		
	Trigger Selector	Input trigger signal	Signal name
ADAHPTRGIN	***[TSEL0CR8]*** <INSEL32[2:0]> (Note)	ADC synchronous trigger output trigger 0	PMD0TRG0
		ADC synchronous trigger output trigger 1	PMD0TRG1
		ADC synchronous trigger output trigger 2	PMD0TRG2
		ADC synchronous trigger output trigger 3	PMD0TRG3
		TRGSEL 37 output	TRGSEL0OUT37
		TRGSEL 38 output	TRGSEL0OUT38
ADATRGIN	***[TSEL0CR8]*** <INSEL33[2:0]> (Note)	ADC synchronous trigger output trigger 0	PMD0TRG0
		ADC synchronous trigger output trigger 1	PMD0TRG1
		ADC synchronous trigger output trigger 2	PMD0TRG2
		ADC synchronous trigger output trigger 3	PMD0TRG3
		TRGSEL 37 output	TRGSEL0OUT37
		TRGSEL 38 output	TRGSEL0OUT38

Note: Select the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to “ 2.2. Trigger Selector (TRGSEL) ”.

Table 2.42 ADC start-up trigger connection Specification (TRGSEL37 and 38 outputs)

Connection destination (Signal name)	Start-up trigger		
	Trigger Selector	Input trigger signal	Signal name
TRGSEL 37 output (TRGSEL0OUT37)	***[TSEL0CR9]*** <INSEL37[2:0]> (Note)	T32A ch9 timer register A1 match trigger	T32A09TRGOUTCMPA1
		T32A ch9 timer register B1 match trigger	T32A09TRGOUTCMPB1
		T32A ch10 timer register A1 match trigger	T32A10TRGOUTCMPA1
		T32A ch10 timer register B1 match trigger	T32A10TRGOUTCMPB1
		T32A ch11 timer register A1 match trigger	T32A11TRGOUTCMPA1
		T32A ch11 timer register B1 match trigger	T32A11TRGOUTCMPB1
		TRGIN0 (PG3 pin)	-
		TRGIN1 (PL7 pin)	-
TRGSEL 38 output (TRGSEL0OUT38)	***[TSEL0CR9]*** <INSEL38[2:0]> (Note)	T32A ch9 timer register A1 match trigger	T32A09TRGOUTCMPA1
		T32A ch9 timer register B1 match trigger	T32A09TRGOUTCMPB1
		T32A ch10 timer register A1 match trigger	T32A10TRGOUTCMPA1
		T32A ch10 timer register B1 match trigger	T32A10TRGOUTCMPB1
		T32A ch11 timer register A1 match trigger	T32A11TRGOUTCMPA1
		T32A ch11 timer register B1 match trigger	T32A11TRGOUTCMPB1
		TRGIN0 (PG3 pin)	-
		TRGIN1 (PL7 pin)	-

Note: Select the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

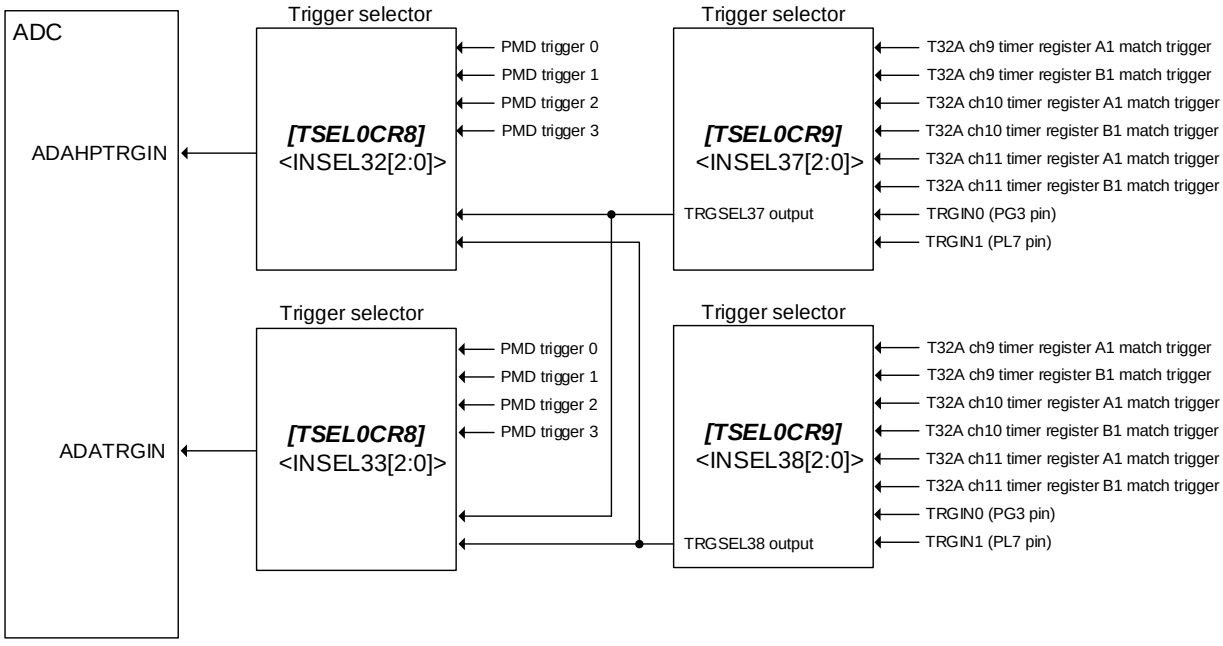

Figure 2.2 ADC start-up trigger connection diagram

2.12. 8-bit Digital to Analog Converter (DAC)

2.12.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.43 DAC built-in channel

Product	DAC channel (✓: Available, -: N/A)	
	Channel 0	Channel 1
M4G9	✓	✓
M4G8	✓	✓
M4G7	✓	✓
M4G6	✓	✓

2.12.2. Function pin and port

The functional terminal is assigned to the following ports.

Table 2.44 DAC function pin and port

Channel	Function pin (Signal name)	Port	Product table (✓: Available, -: N/A)			
			M4G9	M4G8	M4G7	M4G6
ch0	DAC0	PT0	✓	✓	✓	✓
ch1	DAC1	PT1	✓	✓	✓	✓

2.13. Voltage Detection Circuit (LVD)

2.13.1. Built-in list

The following table shows the built-in list for each product.

Table 2.45 LVD Built-in list

Product	Built-in LVD (✓: Available, -: N/A)
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.13.2. LVD detection power supply

A voltage detecting circuit monitors the power supply of the following table.

Table 2.46 LVD detection power supply

LVD detection power supply	Power supply name
Digital power source terminal	DVDD3

2.14. 32-bit Timer Event Counter (T32A)

2.14.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.47 T32A built-in channel

Product	T32A channel (✓: Available, -: N/A)													
	channel 0	channel 1	channel 2	channel 3	channel 4	channel 5	channel 6	channel 7	channel 8	channel 9	channel 10	channel 11	channel 12	channel 13
M4G9	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M4G8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M4G7	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M4G6	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

2.14.2. Function pin and port

The functional pin is assigned to the port of the following tables.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.48 T32A functional pin and port (1/4)

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch0	T32A00INA0	Input	PA0 / PK0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A00INA1	Input	PA3	✓	✓	✓	✓
	T32A00OUTA	Output	PA1 / PW1	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A00INB0	Input	PA3 / PK1	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A00INB1	Input	PA0	✓	✓	✓	✓
	T32A00OUTB	Output	PA2 / PW0	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A00INC0	Input	PA0 / PK0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A00INC1	Input	PA3 / PK3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A00OUTC	Output	PA1 / PW1	✓ / ✓	✓ / -	✓ / -	✓ / -
ch1	T32A01INA0	Input	PA4 / PK6	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A01INA1	Input	PA7	✓ / ✓	✓ / ✓	✓	✓
	T32A01OUTA	Output	PA5 / PW2	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A01INB0	Input	PA7 / PK7	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A01INB1	Input	PA4	✓ / ✓	✓ / ✓	✓	✓
	T32A01OUTB	Output	PA6 / PW3	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A01INC0	Input	PA4 / PK6	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A01INC1	Input	PA7 / PK7	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A01OUTC	Output	PA5 / PW2	✓ / ✓	✓ / -	✓ / -	✓ / -

Table 2.49 T32A functional pin and port (2/4)

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch2	T32A02INA0	Input	PB0 / PL0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A02INA1	Input	PB1	✓	✓	✓	✓
	T32A02OUTA	Output	PB2 / PG5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A02INB0	Input	PB1 / PL3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A02INB1	Input	PB0	✓	✓	✓	✓
	T32A02OUTB	Output	PB3 / PG4	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A02INC0	Input	PB0 / PL0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A02INC1	Input	PB1 / PL3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A02OUTC	Output	PB2 / PG5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
ch3	T32A03INA0	Input	PB6 / PJ4	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A03INA1	Input	PB7	✓	✓	✓	✓
	T32A03OUTA	Output	PB4 / PT3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A03INB0	Input	PB7 / PJ5	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A03INB1	Input	PB6	✓	✓	✓	✓
	T32A03OUTB	Output	PB5 / PT5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
	T32A03INC0	Input	PB6 / PJ4	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A03INC1	Input	PB7 / PJ5	✓ / ✓	✓ / -	✓ / -	✓ / -
	T32A03OUTC	Output	PB4 / PT3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
ch4	T32A04INA0	Input	PD0 / PP0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A04INA1	Input	PD1 / PP1	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A04OUTA	Output	PD2 / PV5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
	T32A04INB0	Input	PD1 / PP1	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A04INB1	Input	PD0 / PP0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A04OUTB	Output	PD3 / PV4	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
	T32A04INC0	Input	PD0 / PP0	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A04INC1	Input	PD1 / PP1	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A04OUTC	Output	PD2 / PV5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
ch5	T32A05INA0	Input	PD6 / PP2	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A05INA1	Input	PD7 / PP3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A05OUTA	Output	PD4 / PV6	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
	T32A05INB0	Input	PD7 / PP3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A05INB1	Input	PD6 / PP2	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A05OUTB	Output	PD5 / PV7	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
	T32A05INC0	Input	PD6 / PP2	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A05INC1	Input	PD7 / PP3	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A05OUTC	Output	PD4 / PV6	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
ch6	T32A06INA0	Input	PE2 / PP4	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A06INA1	Input	PE0 / PP5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A06OUTA	Output	PE1 / PM5	✓ / ✓	✓ / ✓	✓ / -	✓ / -
	T32A06INB0	Input	PE3 / PP5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A06INB1	Input	PE0 / PP4	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A06OUTB	Output	PE0 / PM4	✓ / ✓	✓ / ✓	✓ / -	✓ / -
	T32A06INC0	Input	PE2 / PP4	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A06INC1	Input	PE3 / PP5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A06OUTC	Output	PE1 / PM5	✓ / ✓	✓ / ✓	✓ / -	✓ / -

Table 2.50 T32A functional pin and port (3/4)

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch7	T32A07INA0	Input	PE4 / PP6	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A07INA1	Input	PE7 / PP7	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A07OUTA	Output	PE6 / PM6	✓ / ✓	✓ / ✓	✓ / -	✓ / -
	T32A07INB0	Input	PE5 / PP7	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A07INB1	Input	PE7 / PP6	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A07OUTB	Output	PE7 / PM7	✓ / ✓	✓ / ✓	✓ / -	✓ / -
	T32A07INC0	Input	PE4 / PP6	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A07INC1	Input	PE5 / PP7	✓ / ✓	✓ / ✓	✓ / ✓	✓ / ✓
	T32A07OUTC	Output	PE6 / PM6	✓ / ✓	✓ / ✓	✓ / -	✓ / -
ch8	T32A08INA0	Input	PC0 / PR0	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A08OUTA	Output	PC2 / PL4	✓ / ✓	✓ / -	✓ / -	- / -
	T32A08INB0	Input	PC1 / PR1	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A08OUTB	Output	PC3 / PL5	✓ / ✓	✓ / -	✓ / -	- / -
	T32A08INC0	Input	PC0 / PR0	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A08INC1	Input	PC1 / PR1	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A08OUTC	Output	PC2 / PL4	✓ / ✓	✓ / -	✓ / -	- / -
ch9	T32A09INA0	Input	PR2 / PV0	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A09OUTA	Output	PL6 / PV2	✓ / ✓	- / ✓	- / ✓	- / -
	T32A09INB0	Input	PR3 / PV1	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A09OUTB	Output	PL7 / PV3	✓ / ✓	- / ✓	- / ✓	- / -
	T32A09INC0	Input	PR2 / PV0	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A09INC1	Input	PR3 / PV1	✓ / ✓	✓ / ✓	✓ / ✓	- / -
	T32A09OUTC	Output	PL6 / PV2	✓ / ✓	- / ✓	- / ✓	- / -
ch10	T32A10INA0	Input	PR4 / PW4	✓ / ✓	✓ / -	- / -	- / -
	T32A10INA1	Input	PW7	✓	-	-	-
	T32A10OUTA	Output	PC4 / PW5	✓ / ✓	✓ / -	- / -	- / -
	T32A10INB0	Input	PR5	✓	✓	-	-
	T32A10OUTB	Output	PC5 / PW4	✓ / ✓	✓ / -	- / -	- / -
	T32A10INC0	Input	PR4	✓	✓	-	-
	T32A10INC1	Input	PR5	✓	✓	-	-
	T32A10OUTC	Output	PC4 / PW5	✓ / ✓	✓ / -	- / -	- / -
ch11	T32A11INA0	Input	PR6 / PW7	✓ / ✓	✓ / -	- / -	- / -
	T32A11INA1	Input	PW4	✓	-	-	-
	T32A11OUTA	Output	PM2 / PW6	✓ / ✓	✓ / -	- / -	- / -
	T32A11INB0	Input	PR7	✓	✓	-	-
	T32A11OUTB	Output	PM3 / PW7	✓ / ✓	✓ / -	- / -	- / -
	T32A11INC0	Input	PR6	✓	✓	-	-
	T32A11INC1	Input	PR7	✓	✓	-	-
	T32A11OUTC	Output	PM2 / PW6	✓ / ✓	✓ / -	- / -	- / -

Table 2.51 T32A functional pin and port (4/4)

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch12	T32A12INA0	Input	PU2	✓	-	-	-
	T32A12OUTA	Output	PU0	✓	-	-	-
	T32A12INB0	Input	PU3	✓	-	-	-
	T32A12OUTB	Output	PU1	✓	-	-	-
	T32A12INC0	Input	PU2	✓	-	-	-
	T32A12INC1	Input	PU3	✓	-	-	-
	T32A12OUTC	Output	PU0	✓	-	-	-
ch13	T32A13INA0	Input	PU5	✓	-	-	-
	T32A13OUTA	Output	PU6	✓	-	-	-
	T32A13INB0	Input	PU4	✓	-	-	-
	T32A13OUTB	Output	PU7	✓	-	-	-
	T32A13INC0	Input	PU5	✓	-	-	-
	T32A13INC1	Input	PU4	✓	-	-	-
	T32A13OUTC	Output	PU6	✓	-	-	-

2.14.3. Clock for prescaler

The clock shown in the table below is used as the prescaler clock for T32A.

Table 2.52 T32A clock for prescaler

Clock for prescaler
ΦT0m

2.14.4. Internal signal connection specification

The following table shows the internal signals connected to the T32A.

2.14.4.1. Capture/counter channel connection specification

The following table shows the capture trigger signals connected to the T32A.

The input trigger signal which has a register name in the trigger selector column of the following table should select the input trigger used by a trigger selector.

Table 2.53 4 input trigger connection

Channel	Timer	Function (Intput)	Signal name	Trigger Selector	ch	Timer	Function (Output)	Signal name
ch12	A	Internal trigger (Register A0 match)	T32A12TRGOUTCMPA0	***[TSEL0CR11]*** <INSEL46[2:0]>	0	A	Internal trigger input	T32A00TRGINAPCK
				[TSEL0CR11] <INSEL47[2:0]>	0	B		T32A00TRGINBPCK
				[TSEL0CR12] <INSEL48[2:0]>	1	A		T32A01TRGINAPCK
				[TSEL0CR12] <INSEL49[2:0]>	1	B		T32A01TRGINBPCK
ch12	B	Internal trigger (Register B0 match)	T32A12TRGOUTCMPB0	***[TSEL0CR12]*** <INSEL50[2:0]>	2	A	Internal trigger input	T32A02TRGINAPCK
				[TSEL0CR12] <INSEL51[2:0]>	2	B		T32A02TRGINBPCK
				[TSEL0CR13] <INSEL52[2:0]>	3	A		T32A03TRGINAPCK
				[TSEL0CR13] <INSEL53[2:0]>	3	B		T32A03TRGINBPCK
ch13	A	Internal trigger (Register A0 match)	T32A13TRGOUTCMPA0	***[TSEL0CR13]*** <INSEL54[2:0]>	4	A	Internal trigger input	T32A04TRGINAPCK
				[TSEL0CR13] <INSEL55[2:0]>	4	B		T32A04TRGINBPCK
				[TSEL0CR9] <INSEL39[2:0]>	5	A		T32A05TRGINAPCK
				[TSEL0CR10] <INSEL40[2:0]>	5	B		T32A05TRGINBPCK
ch13	B	Internal trigger (Register B0 match)	T32A13TRGOUTCMPB0	***[TSEL0CR10]*** <INSEL41[2:0]>	6	A	Internal trigger input	T32A06TRGINAPCK
				[TSEL0CR10] <INSEL42[2:0]>	6	B		T32A06TRGINBPCK
				[TSEL0CR10] <INSEL43[2:0]>	7	A		T32A07TRGINAPCK
				[TSEL0CR11] <INSEL44[2:0]>	7	B		T32A07TRGINBPCK
ch2	A	Internal trigger (Register A0 match)	T32A02TRGOUTCMPA0	-	12	A	Internal trigger input	T32A12TRGINAPCK
				-	12	B		T32A12TRGINBPCK
				[TSEL0CR8] <INSEL35[2:0]>	13	A		T32A13TRGINAPCK
				[TSEL0CR9] <INSEL36[2:0]>	13	B		T32A13TRGINBPCK
ch12	C	Internal trigger (Register C0 match)	T32A12TRGOUTCMPC0	-	0	C	Internal trigger input	T32A00TRGINCPCK
				-	1	C		T32A01TRGINCPCK
				-	2	C		T32A02TRGINCPCK
				-	3	C		T32A03TRGINCPCK

ch13	C	Internal trigger (Register C0 match)	T32A13TRGOUTCMPC0	-	4	C	Internal trigger input	T32A04TRGINCPCK
				-	5	C		T32A05TRGINCPCK
				-	6	C		T32A06TRGINCPCK
				-	7	C		T32A07TRGINCPCK

Note: -: Not available.

Table 2.54 T32A timer output trigger connection

T32A				Trigger Selector	T32A			
Channel	Timer	Function (Output)	Signal name		ch	Timer	Function (Input)	Signal name
ch4	A	Timer output	T32A04OUTA	-	8	A	Another timer output	T32A08TRGINAPHCK
ch4	B	Timer output	T32A04OUTB	***[TSEL0CR11]*** <INSEL45[2:0]>	8	B	Another timer output	T32A08TRGINBPHCK
ch5	A	Timer output	T32A05OUTA	-	9	A	Another timer output	T32A09TRGINAPHCK
ch5	B	Timer output	T32A05OUTB	-	9	B	Another timer output	T32A09TRGINBPHCK
ch6	A	Timer output	T32A06OUTA	-	10	A	Another timer output	T32A10TRGINAPHCK
ch6	B	Timer output	T32A06OUTB	-	10	B	Another timer output	T32A10TRGINBPHCK
ch7	A	Timer output	T32A07OUTA	-	11	A	Another timer output	T32A11TRGINAPHCK
ch7	B	Timer output	T32A07OUTB	-	11	B	Another timer output	T32A11TRGINBPHCK

Note: -: Not available.

2.14.4.2. Synchronous control connection specification

The timer synchronous connection specification of a T32A is shown in the following tables.

Table 2.55 T32A synchronous control connection specification (1/3)

Channel	Master			Slave			
	Timer	Function (Output)	Signal name	ch	Timer	Function (Output)	Signal name
ch0	A	Synchronous start output A	T32A00SYNCSTARTOUTA	0	B	Synchronous start B	T32A00SYNCSTARTB
				1	A	Synchronous start A	T32A01SYNCSTARTA
				1	B	Synchronous start B	T32A01SYNCSTARTB
		Synchronous stop output A	T32A00SYNCSTOPOUTA	0	B	Synchronous stop B	T32A00SYNCSTOPB
				1	A	Synchronous stop A	T32A01SYNCSTOPA
				1	B	Synchronous stop B	T32A01SYNCSTOPB
		Synchronous reload output A	T32A00SYNCRELOADOUTA	0	B	Synchronous reload B	T32A00SYNCRELOADB
				1	A	Synchronous reload A	T32A01SYNCRELOADA
				1	B	Synchronous reload B	T32A01SYNCRELOADB
ch0	C	Synchronous start output C	T32A00SYNCSTARTOUTC	1	C	Synchronous start C	T32A01SYNCSTARTC
		Synchronous stop output C	T32A00SYNCSTOPOUTC	1	C	Synchronous stop C	T32A01SYNCSTOPC
		Synchronous reload output C	T32A00SYNCRELOADOUTC	1	C	Synchronous reload C	T32A01SYNCRELOADC
ch2	A	Synchronous start output A	T32A02SYNCSTARTOUTA	2	B	Synchronous start B	T32A02SYNCSTARTB
				3	A	Synchronous start A	T32A03SYNCSTARTA
				3	B	Synchronous start B	T32A03SYNCSTARTB
		Synchronous stop output A	T32A02SYNCSTOPOUTA	2	B	Synchronous stop B	T32A02SYNCSTOPB
				3	A	Synchronous stop A	T32A03SYNCSTOPA
				3	B	Synchronous stop B	T32A03SYNCSTOPB
		Synchronous reload output A	T32A02SYNCRELOADOUTA	2	B	Synchronous reload B	T32A02SYNCRELOADB
				3	A	Synchronous reload A	T32A03SYNCRELOADA
				3	B	Synchronous reload B	T32A03SYNCRELOADB
ch2	C	Synchronous start output A	T32A02SYNCSTARTOUTC	3	C	Synchronous start C	T32A03SYNCSTARTC
		Synchronous stop output A	T32A02SYNCSTOPOUTC	3	C	Synchronous stop C	T32A03SYNCSTOPC
		Synchronous reload output A	T32A02SYNCRELOADOUTC	3	C	Synchronous reload C	T32A03SYNCRELOADC

Table 2.56 T32A synchronous control connection specification (2/3)

Channel	Master			Slave			
	Timer	Function (Output)	Signal name	ch	Timer	Function (Output)	Signal name
ch4	A	Synchronous start output A	T32A04SYNCSTARTOUTA	4	B	Synchronous start B	T32A04SYNCSTARTB
				5	A	Synchronous start A	T32A05SYNCSTARTA
				5	B	Synchronous start B	T32A05SYNCSTARTB
		Synchronous stop output A	T32A04SYNCSTOPOUTA	4	B	Synchronous stop B	T32A04SYNCSTOPB
				5	A	Synchronous stop A	T32A05SYNCSTOPA
				5	B	Synchronous stop B	T32A05SYNCSTOPB
		Synchronous reload output A	T32A04SYNCRELOADOUTA	4	B	Synchronous reload B	T32A04SYNCRELOADB
				5	A	Synchronous reload A	T32A05SYNCRELOADA
				5	B	Synchronous reload B	T32A05SYNCRELOADB
ch4	C	Synchronous start output C	T32A04SYNCSTARTOUTC	5	C	Synchronous start C	T32A05SYNCSTARTC
		Synchronous stop output C	T32A04SYNCSTOPOUTC	5	C	Synchronous stop C	T32A05SYNCSTOPC
		Synchronous reload output C	T32A04SYNCRELOADOUTC	5	C	Synchronous reload C	T32A05SYNCRELOADC
ch6	A	Synchronous start output A	T32A06SYNCSTARTOUTA	6	B	Synchronous start B	T32A06SYNCSTARTB
				7	A	Synchronous start A	T32A07SYNCSTARTA
				7	B	Synchronous start B	T32A07SYNCSTARTB
		Synchronous stop output A	T32A06SYNCSTOPOUTA	6	B	Synchronous stop B	T32A06SYNCSTOPB
				7	A	Synchronous stop A	T32A07SYNCSTOPA
				7	B	Synchronous stop B	T32A07SYNCSTOPB
		Synchronous reload output A	T32A06SYNCRELOADOUTA	6	B	Synchronous reload B	T32A06SYNCRELOADB
				7	A	Synchronous reload A	T32A07SYNCRELOADA
				7	B	Synchronous reload B	T32A07SYNCRELOADB
ch6	C	Synchronous start output C	T32A06SYNCSTARTOUTC	7	C	Synchronous start C	T32A07SYNCSTARTC
		Synchronous stop output C	T32A06SYNCSTOPOUTC	7	C	Synchronous stop C	T32A07SYNCSTOPC
		Synchronous reload output C	T32A06SYNCRELOADOUTC	7	C	Synchronous reload C	T32A07SYNCRELOADC
ch8	A	Synchronous start output A	T32A08SYNCSTARTOUTA	8	B	Synchronous start B	T32A08SYNCSTARTB
				9	A	Synchronous start A	T32A09SYNCSTARTA
				9	B	Synchronous start B	T32A09SYNCSTARTB
		Synchronous stop output A	T32A08SYNCSTOPOUTA	8	B	Synchronous stop B	T32A08SYNCSTOPB
				9	A	Synchronous stop A	T32A09SYNCSTOPA
				9	B	Synchronous stop B	T32A09SYNCSTOPB
		Synchronous reload output A	T32A08SYNCRELOADOUTA	8	B	Synchronous reload B	T32A08SYNCRELOADB
				9	A	Synchronous reload A	T32A09SYNCRELOADA
				9	B	Synchronous reload B	T32A09SYNCRELOADB
ch8	C	Synchronous start output C	T32A08SYNCSTARTOUTC	9	C	Synchronous start C	T32A09SYNCSTARTC
		Synchronous stop output C	T32A08SYNCSTOPOUTC	9	C	Synchronous stop C	T32A09SYNCSTOPC
		Synchronous reload output C	T32A08SYNCRELOADOUTC	9	C	Synchronous reload C	T32A09SYNCRELOADC

Table 2.57 T32A synchronous control connection specification (3/3)

channel	Master			Slave			
	Timer	Function (Output)	Signal name	ch	Timer	Function (Output)	Signal name
ch10	A	Synchronous start output A	T32A10SYNCSTARTOUTA	10	B	Synchronous start B	T32A10SYNCSTARTB
				11	A	Synchronous start A	T32A11SYNCSTARTA
				11	B	Synchronous start B	T32A11SYNCSTARTB
		Synchronous stop output A	T32A10SYNCSTOPOUTA	10	B	Synchronous stop B	T32A10SYNCSTOPB
				11	A	Synchronous stop A	T32A11SYNCSTOPA
				11	B	Synchronous stop B	T32A11SYNCSTOPB
		Synchronous reload output A	T32A10SYNCRELOADOUTA	10	B	Synchronous reload B	T32A10SYNCRELOADB
				11	A	Synchronous reload A	T32A11SYNCRELOADA
				11	B	Synchronous reload B	T32A11SYNCRELOADB
ch10	C	Synchronous start output C	T32A10SYNCSTARTOUTC	11	C	Synchronous start C	T32A11SYNCSTARTC
		Synchronous stop output C	T32A10SYNCSTOPOUTC	11	C	Synchronous stop C	T32A11SYNCSTOPC
		Synchronous reload output C	T32A10SYNCRELOADOUTC	11	C	Synchronous reload C	T32A11SYNCRELOADC
ch12	A	Synchronous start output A	T32A12SYNCSTARTOUTA	12	B	Synchronous start B	T32A12SYNCSTARTB
				13	A	Synchronous start A	T32A13SYNCSTARTA
				13	B	Synchronous start B	T32A13SYNCSTARTB
		Synchronous stop output A	T32A12SYNCSTOPOUTA	12	B	Synchronous stop B	T32A12SYNCSTOPB
				13	A	Synchronous stop A	T32A13SYNCSTOPA
				13	B	Synchronous stop B	T32A13SYNCSTOPB
		Synchronous reload output A	T32A12SYNCRELOADOUTA	12	B	Synchronous reload B	T32A12SYNCRELOADB
				13	A	Synchronous reload A	T32A13SYNCRELOADA
				13	B	Synchronous reload B	T32A13SYNCRELOADB
ch12	C	Synchronous start output C	T32A12SYNCSTARTOUTC	13	C	Synchronous start C	T32A13SYNCSTARTC
		Synchronous stop output C	T32A12SYNCSTOPOUTC	13	C	Synchronous stop C	T32A13SYNCSTOPC
		Synchronous reload output C	T32A12SYNCRELOADOUTC	13	C	Synchronous reload C	T32A13SYNCRELOADC

2.14.4.3. T32A timer channel reload trigger connection specification

Table 2.58 T32A reload trigger connection

T32A				Trigger Selector	T32A			
channel	Timer	Function (Output)	Signal name		ch	Timer	Function (Input)	Signal name
ch9	A	Internal trigger (Register A0 match)	T32A09TRGOUTCMPA0	***[TSEL0CR9]*** <INSEL39[2:0]>	5	A	Internal trigger input	T32A05TRGINAPCK
				[TSEL0CR10] <INSEL40[2:0]>	5	B		T32A05TRGINBPCK
				-	9	B		T32A09TRGINBPCK
ch10	A	Internal trigger (Register A0 match)	T32A10TRGOUTCMPA0	***[TSEL0CR10]*** <INSEL41[2:0]>	6	A	Internal trigger input	T32A06TRGINAPCK
				[TSEL0CR10] <INSEL42[2:0]>	6	B		T32A06TRGINBPCK
				-	10	B		T32A10TRGINBPCK
ch11	A	Internal trigger (Register A0 match)	T32A11TRGOUTCMPA0	***[TSEL0CR10]*** <INSEL43[2:0]>	7	A	Internal trigger input	T32A07TRGINAPCK
				[TSEL0CR11] <INSEL44[2:0]>	7	B		T32A07TRGINBPCK
				-	11	B		T32A11TRGINBPCK

2.14.4.4. TSPI/UART - T32A connection specification

Table 2.59 T32A TSPI/UART - T32A Connection Specification

TSPI		Trigger Selector	T32A			
Function (Output)	Signal name		channel	Timer	Function (Input)	Signal name
TSPI ch0 transmt completion	TSPI0TXDEND	***[TSEL0CR11]*** <INSEL46[2:0]>	ch0	A	Internal trigger input	T32A00TRGINAPCK
UART ch0 transmission completion trigger	UART0TXTRG					
TSPI ch0 receive completion	TSPI0RXDEND	***[TSEL0CR11]*** <INSEL47[2:0]>	ch0	B	Internal trigger input	T32A00TRGINBPCK
UART ch0 reception completion trigger	UART0RXTRG					
TSPI ch1 transmit completion	TSPI1TXDEND	***[TSEL0CR12]*** <INSEL48[2:0]>	ch1	A	Internal trigger input	T32A01TRGINAPCK
UART ch1 transmission completion trigger	UART1TXTRG					
TSPI ch1 receive completion	TSPI1RXDEND	***[TSEL0CR12]*** <INSEL49[2:0]>	ch1	B	Internal trigger input	T32A01TRGINBPCK
UART ch1 reception completion trigger	UART1RXTRG					
TSPI ch2 transmit completion	TSPI2TXDEND	***[TSEL0CR12]*** <INSEL50[2:0]>	ch2	A	Internal trigger input	T32A02TRGINAPCK
UART ch2 transmission completion trigger	UART2TXTRG					
TSPI ch2 receive completion	TSPI2RXDEND	***[TSEL0CR12]*** <INSEL51[2:0]>	ch2	B	Internal trigger input	T32A02TRGINBPCK
UART ch2 reception completion trigger	UART2RXTRG					
TSPI ch3 transmit completion	TSPI3TXDEND	***[TSEL0CR13]*** <INSEL52[2:0]>	ch3	A	Internal trigger input	T32A03TRGINAPCK
TSPI ch3 receive completion	TSPI3RXDEND	***[TSEL0CR13]*** <INSEL53[2:0]>	ch3	B	Internal trigger input	T32A03TRGINBPCK
TSPI ch4 transmit completion	TSPI4TXDEND	***[TSEL0CR13]*** <INSEL54[2:0]>	ch4	A	Internal trigger input	T32A04TRGINAPCK
TSPI ch4 receive completion	TSPI4RXDEND	***[TSEL0CR13]*** <INSEL55[2:0]>	ch4	B	Internal trigger input	T32A04TRGINBPCK

Note: -: Not available.

2.14.4.5. T32A - ISD connection specification

Table 2.60 T32A T32A – ISD connection specification

T32A				ISD		
channel	Timer	Function (Output)	Signal name	unit	Function (Input)	Signal name
ch9	A	Ttimer A output	T32A09OUTA	A	Timer trigger A for clock source	ISDACLKTRG
				B	Timer trigger B for clock source	ISDBCLKTRG
				C	Timer trigger C for clock source	ISDCCLKTRG

2.14.4.6. ELOSC low speed clock – T32A connection specification

Table 2.61 T32A ELOSC low speed Clock – T32A connection specification

-		Trigger Selector	T32A			
Function (Output)	Signal name		channel	Timer	Function (Input)	Signal name
ELOSC low speed clock	fs	***[TSEL0CR8]*** INSEL34[2:0]	ch8	A	Internal trigger input	T32A08TRGINAPCK

2.14.5. Pulse count correspondence classified by product List

In the T32A, as shown in the following tables, correspondence of a pulse counter changes with products.

Table 2.62 T32A pulse count support list

Channel	Product table (-: Not available)			
	M4G9	M4G8	M4G7	M4G6
ch0	2-phase pulse count 1-pahse pulse count			
ch1	2-phase pulse count 1-pahse pulse count			
ch2	2-phase pulse count 1-pahse pulse count			
ch3	2-phase pulse count 1-pahse pulse count			
ch4	2-phase pulse count 1-pahse pulse count			
ch5	2-phase pulse count 1-pahse pulse count			
ch6	2-phase pulse count 1-pahse pulse count			
ch7	2-phase pulse count 1-pahse pulse count			
ch8	2-phase pulse count 1-pahse pulse count			-
ch9	2-phase pulse count 1-pahse pulse count			-
ch10	2-phase pulse count 1-pahse pulse count		-	
ch11	2-phase pulse count 1-pahse pulse count		-	
ch12	2-phase pulse count 1-pahse pulse count	-		
ch13	2-phase pulse count 1-pahse pulse count	-		

2.14.6. DMA Request

The T32A has the DMA request shown in the following tables.

When there is mention of the register name in the trigger selector column of the table, please select a request to use with a trigger selector.

Table 2.63 T32A DMA request (1/3)

Channel	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch0	DMA request at capture A0 register	T32A00DMAREQCAPA0	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	DMA request at capture C0 register	T32A00DMAREQCAPC0	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR1]*** <INSEL4[2:0]>	4	✓	-
	DMA request at match C1 register	T32A00DMAREQCMPC1				
	DMA request at match B1 register	T32A00DMAREQCMPB1	***[TSEL0CR1]*** <INSEL5[2:0]>	5	✓	-
	DMA request at capture B0 register	T32A00DMAREQCAPB0				
ch1	DMA request at match A1 register	T32A01DMAREQCMPA1	***[TSEL0CR1]*** <INSEL6[2:0]>	6	✓	-
	DMA request at match C1 register	T32A01DMAREQCMPC1				
	DMA request at capture A0 register	T32A01DMAREQCAPA0				
	DMA request at capture C0 register	T32A01DMAREQCAPC0				
	DMA request at match B1 register	T32A01DMAREQCMPB1	***[TSEL0CR1]*** <INSEL7[2:0]>	7	✓	-
	DMA request at capture B0 register	T32A01DMAREQCAPB0				
ch2	DMA request at match A1 register	T32A02DMAREQCMPA1	***[TSEL0CR2]*** <INSEL8[2:0]>	8	✓	-
	DMA request at match C1 register	T32A02DMAREQCMPC1				
	DMA request at capture A0 register	T32A02DMAREQCAPA0				
	DMA request at capture C0 register	T32A02DMAREQCAPC0				
	DMA request at match B1 register	T32A02DMAREQCMPB1	***[TSEL0CR2]*** <INSEL9[2:0]>	9	✓	-
	DMA request at capture B0 register	T32A02DMAREQCAPB0				
ch3	DMA request at match A1 register	T32A03DMAREQCMPA1	***[TSEL0CR2]*** <INSEL10[2:0]>	10	✓	-
	DMA request at match C1 register	T32A03DMAREQCMPC1				
	DMA request at capture A0 register	T32A03DMAREQCAPA0				
	DMA request at capture C0 register	T32A03DMAREQCAPC0				
	DMA request at match B1 register	T32A03DMAREQCMPB1	***[TSEL0CR2]*** <INSEL11[2:0]>	11	✓	-
	DMA request at capture B0 register	T32A03DMAREQCAPB0				
ch4	DMA request at match A1 register	T32A04DMAREQCMPA1	***[TSEL0CR3]*** <INSEL12[2:0]>	12	✓	-
	DMA request at match C1 register	T32A04DMAREQCMPC1				
	DMA request at capture A0 register	T32A04DMAREQCAPA0				
	DMA request at capture C0 register	T32A04DMAREQCAPC0				
	DMA request at match B1 register	T32A04DMAREQCMPB1	***[TSEL0CR3]*** <INSEL13[2:0]>	13	✓	-
	DMA request at Capture B0 register	T32A04DMAREQCAPB0				
ch5	DMA request at match A1 register	T32A05DMAREQCMPA1	***[TSEL0CR3]*** <INSEL14[2:0]>	14	✓	-
	DMA request at match C1 register	T32A05DMAREQCMPC1				
	DMA request at capture A0 register	T32A05DMAREQCAPA0				
	DMA request at capture C0 register	T32A05DMAREQCAPC0				
	DMA request at match B1 register	T32A05DMAREQCMPB1	***[TSEL0CR3]*** <INSEL15[2:0]>	15	✓	-
	DMA request at capture B0 register	T32A05DMAREQCAPB0				

Note: ✓: Available, -: Not available.

Table 2.64 T32A DMA request (2/3)

Channel	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch6	DMA request at match A1 register	T32A06DMAREQCMPA1	***[TSEL0CR4]*** <INSEL16[2:0]>	16	✓	-
	DMA request at match C1 register	T32A06DMAREQCMPC1				
	DMA request at Capture A0 register	T32A06DMAREQCAPA0				
	DMA request at Capture C0 register	T32A06DMAREQCAPC0				
	DMA request at match B1 register	T32A06DMAREQCMPB1	***[TSEL0CR4]*** <INSEL17[2:0]>	17	✓	-
	DMA request at Capture B0 register	T32A06DMAREQCAPB0				
ch7	DMA request at match A1 register	T32A07DMAREQCMPA1	***[TSEL0CR4]*** <INSEL18[2:0]>	18	✓	-
	DMA request at match C1 register	T32A07DMAREQCMPC1				
	DMA request at Capture A0 register	T32A07DMAREQCAPA0				
	DMA request at Capture C0 register	T32A07DMAREQCAPC0				
	DMA request at match B1 register	T32A07DMAREQCMPB1	***[TSEL0CR4]*** <INSEL19[2:0]>	19	✓	-
	DMA request at Capture B0 register	T32A07DMAREQCAPB0				
ch8	DMA request at match A1 register	T32A08DMAREQCMPA1	***[TSEL0CR5]*** <INSEL20[2:0]>	20	✓	-
	DMA request at match C1 register	T32A08DMAREQCMPC1				
	DMA request at Capture A0 register	T32A08DMAREQCAPA0				
	DMA request at Capture C0 register	T32A08DMAREQCAPC0				
	DMA request at match B1 register	T32A08DMAREQCMPB1	***[TSEL0CR5]*** <INSEL21[2:0]>	21	✓	-
	DMA request at Capture B0 register	T32A08DMAREQCAPB0				
ch9	DMA request at match A1 register	T32A09DMAREQCMPA1	***[TSEL0CR5]*** <INSEL22[2:0]>	22	✓	-
	DMA request at match C1 register	T32A09DMAREQCMPC1				
	DMA request at Capture A0 register	T32A09DMAREQCAPA0				
	DMA request at Capture C0 register	T32A09DMAREQCAPC0				
	DMA request at match B1 register	T32A09DMAREQCMPB1	***[TSEL0CR5]*** <INSEL23[2:0]>	23	✓	-
	DMA request at Capture B0 register	T32A09DMAREQCAPB0				
	DMA request at Capture A1 register	T32A09DMAREQCAPA1				
	DMA request at Capture B1 register	T32A09DMAREQCAPB1				
ch10	DMA request at match A1 register	T32A10DMAREQCMPA1	***[TSEL0CR6]*** <INSEL24[2:0]>	24	✓	-
	DMA request at match C1 register	T32A10DMAREQCMPC1				
	DMA request at Capture A0 register	T32A10DMAREQCAPA0				
	DMA request at Capture C0 register	T32A10DMAREQCAPC0				
	DMA request at match B1 register	T32A10DMAREQCMPB1	***[TSEL0CR6]*** <INSEL25[2:0]>	25	✓	-
	DMA request at Capture B0 register	T32A10DMAREQCAPB0				
	DMA request at Capture A1 register	T32A10DMAREQCAPA1				
	DMA request at Capture B1 register	T32A10DMAREQCAPB1				
ch11	DMA request at match A1 register	T32A11DMAREQCMPA1	***[TSEL0CR6]*** <INSEL26[2:0]>	26	✓	-
	DMA request at match C1 register	T32A11DMAREQCMPC1				
	DMA request at Capture A0 register	T32A11DMAREQCAPA0				
	DMA request at Capture C0 register	T32A11DMAREQCAPC0				
	DMA request at match B1 register	T32A11DMAREQCMPB1	***[TSEL0CR6]*** <INSEL27[2:0]>	27	✓	-
	DMA request at Capture B0 register	T32A11DMAREQCAPB0				
	DMA request at Capture A1 register	T32A11DMAREQCAPA1				
	DMA request at Capture B1 register	T32A11DMAREQCAPB1				

Note: ✓: Available, -: Not available.

Table 2.65 T32A DMA request (3/3)

Channel	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch12	DMA request at match A1 register	T32A12DMAREQCMPA1	***[TSEL0CR7]*** <INSEL28[2:0]>	28	✓	-
	DMA request at match C1 register	T32A12DMAREQCMPC1				
	DMA request at match B1 register	T32A12DMAREQCMPB1	***[TSEL0CR7]*** <INSEL29[2:0]>	29	✓	-
ch13	DMA request at match A1 register	T32A13DMAREQCMPA1	***[TSEL0CR7]*** <INSEL30[2:0]>	30	✓	-
	DMA request at match C1 register	T32A13DMAREQCMPC1				
	DMA request at match B1 register	T32A13DMAREQCMPB1	***[TSEL0CR7]*** <INSEL31[2:0]>	31	✓	-

Note: ✓: Available, -: Not available.

2.15. Real Time Clock (RTC)

2.15.1. Support products

The RTC is supported by the following products.

Table 2.66 RTC support product

Product	RTC support (✓: Supportted, -: Unsupported)
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.15.2. Function pin and port

The functional terminal is assigned to the following ports.

Table 2.67 RTC function pin and port

Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
			M4G9	M4G8	M4G7	M4G6
RTCALARM	Output	PG2	✓	✓	✓	✓
RTCCLK	Output	PT3	✓	✓	✓	✓

2.15.3. Watch count clock

The clock shown in the table below is used as the count clock for the watch.

Table 2.68 RTC count clock

Count clock
fs

2.16. Long Term Timer (LTTMR)

2.16.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.69 LTTMR built-in channel

Product	LTTMR channel (✓: Available, -: N/A)
	Channel 0
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.16.2. Count clock

The following clock is used as the count clock in the LTTMR.

Table 2.70 LTTMR count clock

Clock	Signal name
Internal high speed oscillator 2 (Note)	f_{IHOSC2}

Note: The oscillation control register is ***[RLMLOSCCR]***<POSCEN>.

2.16.3. Internal signal connection specification

2.16.3.1. CEC/RMC connection

Table 2.71 LTTMR CEC/RMC connection

Function (Output)		Input signal		
	Signal name	Channel	Function (Input)	Signal name
LTTMR0 interrupt	INTLTTMR0	CEC ch0	Timer trigger 0 for clock source	CEC0CLKTRG
		RMC ch0	Timer trigger 0 for clock source	TB0OUT
		RMC ch1	Timer trigger 1 for clock source	TB1OUT

2.17. Universal Asynchronous Receiver Transmitter (UART)

2.17.1. Built-in channel

The built-in channel for every product is shown in the following table.

In M4G Group (1), Maximum Communication speed of UART is 5.0 Mbps.

Table 2.72 UART built-in channel

Product	UART channel (✓: Available, -: N/A)					
	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
M4G9	✓	✓	✓	✓	✓	✓
M4G8	✓	✓	✓	✓	✓	-
M4G7	✓	✓	✓	✓	-	-
M4G6	✓	✓	✓	-	-	-

2.17.2. Function pin and port

The functional pin is assigned to the port of the following table.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.73 UART functional pin signal and port

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch0	UT0RXD	Input	PE2 / PH4 / PH5	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/✓
	UT0TXDA	Output	PE3 / PH5 / PH4	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/✓
	UT0CTS_N	Input	PE1 / PH7 / PH6	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/✓
	UT0RTS_N	Output	PE0 / PH6 / PH7	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/✓
ch1	UT1RXD	Input	PH0 / PH1 / PV4	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/-
	UT1TXDA	Output	PH1 / PH0 / PV5	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/-
	UT1CTS_N	Input	PH3 / PH2 / PV6	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/-
	UT1RTS_N	Output	PH2 / PH3 / PV7	✓/✓/✓	✓/✓/✓	✓/✓/✓	✓/✓/-
ch2	UT2RXD	Input	PG0 / PG1	✓/✓	✓/✓	✓/✓	✓/✓
	UT2TXDA	Output	PG1 / PG0	✓/✓	✓/✓	✓/✓	✓/✓
	UT2CTS_N	Input	PG3 / PG2	✓/✓	✓/✓	✓/✓	✓/✓
	UT2RTS_N	Output	PG2 / PG3	✓/✓	✓/✓	✓/✓	✓/✓
ch3	UT3RXD	Input	PU6 / PV0 / PV1	✓/✓/✓	-/✓/✓	-/✓/✓	- / - / -
	UT3TXDA	Output	PU7 / PV1 / PV0	✓/✓/✓	-/✓/✓	-/✓/✓	- / - / -
	UT3CTS_N	Input	PU5 / PV3 / PV2	✓/✓/✓	-/✓/✓	-/✓/✓	- / - / -
	UT3RTS_N	Output	PU4 / PV2 / PV3	✓/✓/✓	-/✓/✓	-/✓/✓	- / - / -
ch4	UT4RXD	Input	PM0 / PM1 / PU1	✓/✓/✓	✓/✓/-	- / - / -	- / - / -
	UT4TXDA	Output	PM1 / PM0 / PU0	✓/✓/✓	✓/✓/-	- / - / -	- / - / -
	UT4CTS_N	Input	PM3 / PM2 / PU2	✓/✓/✓	✓/✓/-	- / - / -	- / - / -
	UT4RTS_N	Output	PM2 / PM3 / PU3	✓/✓/✓	✓/✓/-	- / - / -	- / - / -
ch5	UT5RXD	Input	PJ0 / PJ1	✓/✓	- / -	- / -	- / -
	UT5TXDA	Output	PJ1 / PJ0	✓/✓	- / -	- / -	- / -
	UT5CTS_N	Input	PJ3 / PJ2	✓/✓	- / -	- / -	- / -
	UT5RTS_N	Output	PJ2 / PJ3	✓/✓	- / -	- / -	- / -

2.17.3. Half clock mode list for the each products

The half clock mode support is shown in the table below.

TMPM4G group (1) is support in 1-pin mode only.

Table 2.74 UART Half clock mode (1-pin mode) support list

Channel	Product table (✓: Available, -: N/A)			
	M4G9	M4G8	M4G7	M4G6
ch0	✓	✓	✓	✓
ch1	✓	✓	✓	✓
ch2	✓	✓	✓	✓
ch3	✓	✓	✓	-
ch4	✓	✓	-	-
ch5	✓	-	-	-

2.17.4. Clock for prescaler

The clock shown in the table below is used as the prescaler clock for UART.

Table 2.75 UART clock for prescaler

Clock
ΦT0m

2.17.5. DMA Request

The following table shows the DMA request in the UART

The request from MDMAC is always a single transfer request regardless of the fill level in the FIFO.

Table 2.76 UART DMA request

Channel	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch0	Reception DMA request	UART0RX_DMAREQ	***[TSEL0CR1]*** <INSEL7[2:0]>	7	✓	-
	Transmission DMA request	UART0TX_DMAREQ	***[TSEL0CR2]*** <INSEL9[2:0]>	9	✓	-
ch1	Reception DMA request	UART1RX_DMAREQ	***[TSEL0CR2]*** <INSEL11[2:0]	11	✓	-
	Transmission DMA request	UART1TX_DMAREQ	***[TSEL0CR3]*** <INSEL13[2:0]>	13	✓	-
ch2	Reception DMA request	UART2RX_DMAREQ	***[TSEL0CR4]*** <INSEL19[2:0]>	19	✓	-
	Transmission DMA request	UART2TX_DMAREQ	***[TSEL0CR5]*** <INSEL21[2:0]>	21	✓	-
ch3	Reception DMA request	UART3RX_DMAREQ	***[TSEL0CR7]*** <INSEL28[2:0]>	28	✓	-
	Transmission DMA request	UART3TX_DMAREQ	***[TSEL0CR7]*** <INSEL29[2:0]>	29	✓	-
ch4	Reception DMA request	UART4RX_DMAREQ	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	Transmission DMA request	UART4TX_DMAREQ	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
ch5	Reception DMA request	UART5RX_DMAREQ	***[TSEL0CR7]*** <INSEL30[2:0]>	30	✓	-
	Transmission DMA request	UART5TX_DMAREQ	***[TSEL0CR7]*** <INSEL31[2:0]>	31	✓	-

Note: ✓: Available, -: Not available.

2.17.6. Internal signal connection specification

The UART has the transmission function started by a trigger signal.

The trigger signal is selected from among the trigger sources in the following table by the trigger selector.

2.17.6.1. Trigger transmission signal connection specification

Table 2.77 UART trigger transmission signal connection specification

Channel	Signal name	Input trigger signal	
			Signal name
ch0	UART0TRGIN (Input)	T32A ch0 internal trigger (Register A1 match)	T32A00TRGOUTCMPA1
ch1	UART1TRGIN (Input)	T32A ch1 internal trigger (Register A1 match)	T32A01TRGOUTCMPA1
ch2	UART2TRGIN (Input)	T32A ch2 internal trigger (Register A1 match)	T32A02TRGOUTCMPA1

2.18. Full Universal Asynchronous Receiver Transmitter (FUART)

2.18.1. Built-in channel

The built-in channel for every product is shown in the following table.

In M4G Group (1), Maximum Communication speed of FUART is 2.5 Mbps.

Table 2.78 FUART built-in channel

Product	FUART channel (✓: Available, -: N/A)	
	Channel 0	Channel 1
M4G9	✓	✓
M4G8	✓	✓
M4G7	✓	-
M4G6	✓	-

2.18.2. Function pin and port

The functional pin is assigned to the port of the following table.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.79 FUART functional pin signal and port

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch0	FUT0RXD	Output	PG5 / PJ5	✓ / ✓	✓ / -	✓ / -	✓ / -
	FUT0TXD	Input	PG4 / PJ4	✓ / ✓	✓ / -	✓ / -	✓ / -
	FUT0CTS_N	Input	PG7	✓	✓	✓	✓
	FUT0RTS_N	Output	PG6	✓	✓	✓	✓
	FUT0IROUT	Output	PG4	✓	✓	✓	✓
	FUT0SI_SIRIN	Input	PG5	✓	✓	✓	✓
ch1	FUT1RXD	Output	PJ7 / PM6	✓ / ✓	- / ✓	- / -	- / -
	FUT1TXD	Input	PJ6 / PM7	✓ / ✓	- / ✓	- / -	- / -
	FUT1CTS_N	Input	PM4	✓	✓	-	-
	FUT1RTS_N	Output	PM5	✓	✓	-	-
	FUT1IROUT	Output	PM7	✓	✓	-	-
	FUT1SI_SIRIN	Input	PM6	✓	✓	-	-

2.18.3. Clock for Prescaler

The clock shown in the table below is used as the prescaler clock for FUART.

Table 2.80 FUART clock for prescaler

Clock
ΦT0m

2.18.4. DMA Request

The following table shows the DMA request in the FUART.

The request from MDMAC is always a single transfer request regardless of the fill level in the FIFO.

Table 2.81 FUART DMA request

Channel	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer request	Burst transfer request
ch0	Reception DMA request	FUART0RX_DMAREQ	***[TSEL0CR4]*** <INSEL17[2:0]>	17	✓	-
	Transmission DMA request	FUART0TX_DMAREQ	***[TSEL0CR3]*** <INSEL15[2:0]>	15	✓	-
ch1	Reception DMA request	FUART1RX_DMAREQ	***[TSEL0CR0]*** <INSEL2[2:0]>	2	✓	-
	Transmission DMA request	FUART1TX_DMAREQ	***[TSEL0CR0]*** <INSEL3[2:0]>	3	✓	-

Note: ✓: Available, -: Not available.

2.19. I²C Interface (I²C)

2.19.1. Built-in channel

The built-in channel for every product is shown in the following table.

In the M4G group (1), the I²C interface supports Standard mode and Fast mode.

Table 2.82 I²C interface built-in channel

Product	I²C interface channel (✓: Available, -: N/A)				
	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4
M4G9	✓	✓	✓	✓	✓
M4G8	✓	✓	✓	✓	✓
M4G7	✓	✓	✓	-	-
M4G6	✓	✓	✓	-	-

2.19.2. Function pin and port

The functional pin is assigned to the port of the following table.

Table 2.83 I²C interface function pin and port

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch0	I2C0SCL	I/O	PG3	✓	✓	✓	✓
	I2C0SDA	I/O	PG2	✓	✓	✓	✓
ch1	I2C1SCL	I/O	PF3	✓	✓	✓	✓
	I2C1SDA	I/O	PF2	✓	✓	✓	✓
ch2	I2C2SCL	I/O	PG5 / PV4	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
	I2C2SDA	I/O	PG4 / PV5	✓ / ✓	✓ / ✓	✓ / ✓	✓ / -
ch3	I2C3SCL	I/O	PJ7 / PM1	✓ / ✓	- / ✓	- / -	- / -
	I2C3SDA	I/O	PJ6 / PM0	✓ / ✓	- / ✓	- / -	- / -
ch4	I2C4SCL	I/O	PJ2 / PM7	✓ / ✓	- / ✓	- / -	- / -
	I2C4SDA	I/O	PJ3 / PM6	✓ / ✓	- / ✓	- / -	- / -

2.19.3. Clock for Prescaler

The I²C use the clock of following table as a prescaler clock.

Table 2.84 I²C interface clock for prescaler

Clock
fsysm

2.19.4. Communication speed

The communication speed of each channel is shown in the table below.

Table 2.85 I²C communication speed

Channel	Communication speed (✓: Available, -: N/A)	
	Standard mode (Max 100kbps)	Fast mode (Max 400kbps)
ch0	✓	✓
ch1	✓	✓
ch2	✓	✓
ch3	✓	✓
ch4	✓	✓

2.19.5. Wakeup Function

TMPM4G group(1) products do not support I²C wakeup function.

2.19.6. Noise Filter Selection

The channel 0 to 4 do not include an analog filter. Always use the filter digital.

Table 2.86 I²C interface filter selection

Channel	Filter selection: ***[I2CxOP]***<NLSEL>
ch0	Digital (0)
ch1	Digital (0)
ch2	Digital (0)
ch3	Digital (0)
ch4	Digital (0)

2.19.7. DMA Request

The following table shows the DMA request in the I^2C.

Table 2.87 I^2C interface DMA request

Channel	Request	Signal name	Trigger Selector	DMA request channel (MDMAC unit A)		
					Single transfer	Burst transfer
ch0	Receiving DMA request	I2C0RXDMAREQ	***[TSEL0CR1]*** <INSEL7[2:0]>	7	✓	-
	Transmitting DMA request	I2C0TXDMAREQ	***[TSEL0CR2]*** <INSEL9[2:0]>	9	✓	-
ch1	Receiving DMA request	I2C1RXDMAREQ	***[TSEL0CR2]*** <INSEL11[2:0]>	11	✓	-
	Transmitting DMA request	I2C1TXDMAREQ	***[TSEL0CR3]*** <INSEL13[2:0]>	13	✓	-
ch2	Receiving DMA request	I2C2RXDMAREQ	***[TSEL0CR4]*** <INSEL17[2:0]>	17	✓	-
	Transmitting DMA request	I2C2TXDMAREQ	***[TSEL0CR3]*** <INSEL15[2:0]>	15	✓	-
ch3	Receiving DMA request	I2C3RXDMAREQ	***[TSEL0CR0]*** <INSEL0[2:0]>	0	✓	-
	Transmitting DMA request	I2C3TXDMAREQ	***[TSEL0CR0]*** <INSEL1[2:0]>	1	✓	-
ch4	Receiving DMA request	I2C4RXDMAREQ	***[TSEL0CR0]*** <INSEL2[2:0]>	2	✓	-
	Transmitting DMA request	I2C4TXDMAREQ	***[TSEL0CR0]*** <INSEL3[2:0]>	3	✓	-

Note: ✓: Available, -: Not available.

2.20. Serial Peripheral Interface (TSPI)

2.20.1. Built-in channel

The built-in channel for every product is shown in the following table.

In M4G Group (1), Maximum Communication speed TSPI is 25 Mbps for channel 0 to 3 and 10Mbps for channel 4 to 8.

Table 2.88 TSPI built-in channel

Product	TSPI channel (✓: Available, -: N/A)								
	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
M4G9	✓	✓	✓	✓	✓	✓	✓	✓	✓
M4G8	✓	✓	✓	✓	✓	✓	✓	✓	-
M4G7	✓	✓	✓	✓	✓	✓	-	-	-
M4G6	✓	✓	✓	✓	✓	-	-	-	-

2.20.2. Function pin and port

The functional pin is assigned to the port of the following table.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.89 TSPI function pin and port (1/2)

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch0	TSPI0CSIN	Input	PA0	✓	✓	✓	✓
	TSPI0CS0	Output	PA0	✓	✓	✓	✓
	TSPI0CS1	Output	PA4	✓	✓	✓	✓
	TSPI0CS2	Output	PA5	✓	✓	✓	✓
	TSPI0CS3	Output	PA6	✓	✓	✓	✓
	TSPI0RXD	Input	PA2	✓	✓	✓	✓
	TSPI0TXD	Output	PA3	✓	✓	✓	✓
	TSPI0SCK	I/O	PA1	✓	✓	✓	✓
ch1	TSPI1CSIN	Input	PL0	✓	✓	✓	✓
	TSPI1CS0	Output	PL0	✓	✓	✓	✓
	TSPI1CS1	Output	PK4	✓	✓	✓	✓
	TSPI1CS2	Output	PK5	✓	✓	✓	✓
	TSPI1CS3	Output	PK6	✓	✓	✓	✓
	TSPI1RXD	Input	PL2	✓	✓	✓	✓
	TSPI1TXD	Output	PL3	✓	✓	✓	✓
	TSPI1SCK	I/O	PL1	✓	✓	✓	✓
ch2	TSPI2CSIN	Input	PA7	✓	✓	✓	✓
	TSPI2CS0	Output	PA7	✓	✓	✓	✓
	TSPI2CS1	Output	PA3	✓	✓	✓	✓
	TSPI2CS2	Output	-	-	-	-	-
	TSPI2CS3	Output	-	-	-	-	-
	TSPI2RXD	Input	PA5	✓	✓	✓	✓
	TSPI2TXD	Output	PA4	✓	✓	✓	✓
	TSPI2SCK	I/O	PA6	✓	✓	✓	✓
ch3	TSPI3CSIN	Input	PK7	✓	✓	✓	✓
	TSPI3CS0	Output	PK7	✓	✓	✓	✓
	TSPI3CS1	Output	PL3	✓	✓	✓	✓
	TSPI3CS2	Output	-	-	-	-	-
	TSPI3CS3	Output	-	-	-	-	-
	TSPI3RXD	Input	PK5	✓	✓	✓	✓
	TSPI3TXD	Output	PK4	✓	✓	✓	✓
	TSPI3SCK	I/O	PK6	✓	✓	✓	✓

Table 2.90 TSPI function pin and port (2/2)

Channel	Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
ch4	TSPI4CSIN	Input	PD0	✓	✓	✓	✓
	TSPI4CS0	Output	PD0	✓	✓	✓	✓
	TSPI4CS1	Output	-	-	-	-	-
	TSPI4CS2	Output	-	-	-	-	-
	TSPI4CS3	Output	-	-	-	-	-
	TSPI4RXD	Input	PD2	✓	✓	✓	✓
	TSPI4TXD	Output	PD3	✓	✓	✓	✓
	TSPI4SCK	I/O	PD1	✓	✓	✓	✓
ch5	TSPI5CSIN	Input	PV7	✓	✓	✓	-
	TSPI5CS0	Output	PV7	✓	✓	✓	-
	TSPI5CS1	Output	-	-	-	-	-
	TSPI5CS2	Output	-	-	-	-	-
	TSPI5CS3	Output	-	-	-	-	-
	TSPI5RXD	Input	PV4	✓	✓	✓	-
	TSPI5TXD	Output	PV5	✓	✓	✓	-
	TSPI5SCK	I/O	PV6	✓	✓	✓	-
ch6	TSPI6CSIN	Input	PM3	✓	✓	-	-
	TSPI6CS0	Output	PM3	✓	✓	-	-
	TSPI6CS1	Output	-	-	-	-	-
	TSPI6CS2	Output	-	-	-	-	-
	TSPI6CS3	Output	-	-	-	-	-
	TSPI6RXD	Input	PM1	✓	✓	-	-
	TSPI6TXD	Output	PM0	✓	✓	-	-
	TSPI6SCK	I/O	PM2	✓	✓	-	-
ch7	TSPI7CSIN	Input	PM4	✓	✓	-	-
	TSPI7CS0	Output	PM4	✓	✓	-	-
	TSPI7CS1	Output	-	-	-	-	-
	TSPI7CS2	Output	-	-	-	-	-
	TSPI7CS3	Output	-	-	-	-	-
	TSPI7RXD	Input	PM6	✓	✓	-	-
	TSPI7TXD	Output	PM7	✓	✓	-	-
	TSPI7SCK	I/O	PM5	✓	✓	-	-
ch8	TSPI8CSIN	Input	PW0	✓	-	-	-
	TSPI8CS0	Output	PW0	✓	-	-	-
	TSPI8CS1	Output	-	-	-	-	-
	TSPI8CS2	Output	-	-	-	-	-
	TSPI8CS3	Output	-	-	-	-	-
	TSPI8RXD	Input	PW2	✓	-	-	-
	TSPI8TXD	Output	PW3	✓	-	-	-
	TSPI8SCK	I/O	PW1	✓	-	-	-

2.20.3. Transfer mode list for the each products

The transfer modes which can be used with the product as TSPI is shown in the following tables differ.

Table 2.91 TSPI mode support list

Channel	Mode support (-: Unsupport)			
	M4G9	M4G8	M4G7	M4G6
ch0	SPI mode SIO mode			
ch1	SPI mode SIO mode			
ch2	SPI mode SIO mode			
ch3	SPI mode SIO mode			
ch4	SPI mode SIO mode			
ch5	SPI mode SIO mode			-
ch6	SPI mode SIO mode		-	-
ch7	SPI mode SIO mode		-	-
ch8	SPI mode SIO mode	-	-	-

2.20.4. *[TSPIxCR2]*<RXDLY> set value

For the setting value of TSPI control register 2 ([***TSPIxCR2]*** <RXDLY>), set the values in the following table.

Table 2.92 TSPI *[TSPIxCR2]*<RXDLY> set value

Register name	Value
[TSPIxCR2]<RXDLY>	1

2.20.5. Clock for Prescaler

The clock shown in the table below is used as the prescaler clock for TSPI.

Table 2.93 TSPI clock for prescaler

TSPI channel	Clock for prescaler
ch0 to 5	ΦT0h
ch6 to 8	ΦT0m

2.20.6. DMA Request

The following table shows the DMA request in the TSPI.

The request from MDMAC is always a single transfer request regardless of the fill level in the FIFO.

Table 2.94 TSPI DMA request

Channel	Request	Signal name	Trigger Selector	DMA request channel			
						Single transfer	Burst transfer
ch0	Receive DMA request	TSPI0RX_DMA	-	HDMAC unit A	0	✓	✓
	Transmit DMA request	TSPI0TX_DMA			1	✓	✓
ch1	Receive DMA request	TSPI1RX_DMA	-	HDMAC unit B	0	✓	✓
	Transmit DMA request	TSPI1TX_DMA			1	✓	✓
ch2	Receive DMA request	TSPI2RX_DMA	-	HDMAC unit A	2	✓	✓
	Transmit DMA request	TSPI2TX_DMA			3	✓	✓
ch3	Receive DMA request	TSPI3RX_DMA	-	HDMAC unit B	2	✓	✓
	Transmit DMA request	TSPI3TX_DMA			3	✓	✓
ch4	Receive DMA request	TSPI4RX_DMA	-	HDMAC unit A	4	✓	✓
	Transmit DMA request	TSPI4TX_DMA			5	✓	✓
ch5	Receive DMA request	TSPI5RX_DMA	-	HDMAC unit B	4	✓	✓
	Transmit DMA request	TSPI5TX_DMA			5	✓	✓
ch6	Receive DMA request	TSPI6RX_DMA	***[TSEL0CR0]*** <INSEL0[2:0]>	MDMAC unit A	0	✓	-
	Transmit DMA request	TSPI6TX_DMA	***[TSEL0CR0]*** <INSEL1[2:0]>		1	✓	-
ch7	Receive DMA request	TSPI7RX_DMA	***[TSEL0CR0]*** <INSEL2[2:0]>		2	✓	-
	Transmit DMA request	TSPIT7X_DMA	***[TSEL0CR0]*** <INSEL3[2:0]>		3	✓	-
ch8	Receive DMA request	TSPI8RX_DMA	***[TSEL0CR1]*** <INSEL4[2:0]>		4	✓	-
	Transmit DMA request	TSPI8TX_DMA	***[TSEL0CR1]*** <INSEL5[2:0]>		5	✓	-

Note: ✓: Available, -: Not available.

2.20.7. Internal signal connection specification

2.20.7.1. Trigger transmission signal connection specification

The TSPI has the transmission function started by a trigger signal.

The trigger signal is selected from among the trigger sources in the following table by the trigger selector.

Table 2.95 TSPI trigger transmission signal connection Specification

Channel		Trigger source	
	Signal name	Input trigger signal	Signal name
ch0	TSPI0TRG (Input)	T32A ch0 timer register A1 match trigger	T32A00TRGOUTCMPA1
ch1	TSPI1TRG (Input)	T32A ch1 timer register A1 match trigger	T32A01TRGOUTCMPA1
ch2	TSPI2TRG (Input)	T32A ch2 timer register A1 match trigger	T32A02TRGOUTCMPA1
ch3	TSPI3TRG (Input)	T32A ch3 timer register A1 match trigger	T32A03TRGOUTCMPA1
ch4	TSPI4TRG (Input)	T32A ch4 timer register A1 match trigger	T32A04TRGOUTCMPA1

Note: TSPI ch5 to ch8 have no connections.

2.21. Serial Memory Interface (SMIF)

2.21.1. Built-in channel

The built-in channel for every product is shown in the following table.

Table 2.96 SMIF built-in channel

Product	SMIF channel (✓: Available, -: N/A)
	Channel 0
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.21.2. Function pin and port

The functional pin is assigned to the port of the following table.

Table 2.97 SMIF function pin and port

Function pin (Signal name)	Port	Product table (✓: Available, -: N/A)			
		M4G9	M4G8	M4G7	M4G6
SMI0CS1_N	PK0	✓	✓	✓	✓
SMI0D0	PK2	✓	✓	✓	✓
SMI0D1	PK3	✓	✓	✓	✓
SMI0D2	PK4	✓	✓	✓	✓
SMI0D3	PK5	✓	✓	✓	✓
SMI0CLK	PK6	✓	✓	✓	✓
SMI0CS0_N	PK7	✓	✓	✓	✓

2.22. Consumer Electronics Control Circuit (CEC)

2.22.1. Built-in channel

The built-in channel for every product is shown in the following table.

Table 2.98 CEC built-in channel

Product	CEC channel (✓: Available, -: N/A)
	Channel 0
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.22.2. Function pin and port

The functional pin is assigned to the port of the following table.

Table 2.99 CEC function pin and port

Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
			M4G9	M4G8	M4G7	M4G6
CEC0	Input	PT2	✓	✓	✓	✓

2.22.3. Sampling Clock

The following clock can be used as the sampling clock for CEC.

Table 2.100 CEC sampling clock

Clock		Clock source	
	Signal name		Signal name
Low speed clock	fs	External low speed oscillator	fs
Timer trigger 0 for clock source	CEC0CLKTRG	LTTMR0 interrupt	INTLTTMR0

Note: The sampling clock should be selected by ***[CECxFSSEL]***<CECCLK>.

2.23. Remote Control Reception Circuit (RMC)

2.23.1. Built-in channel

The built-in channel for every product is shown in the following table.

Table 2.101 RMC built-in channel

Product	RMC channel (✓: Available, -: N/A)	
	Channel 0	Channel 1
M4G9	✓	✓
M4G8	✓	✓
M4G7	✓	✓
M4G6	✓	-

2.23.2. Function pin and port

The functional pin is assigned to the port of the following table.

Table 2.102 RMC function pin and port

Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
			M4G9	M4G8	M4G7	M4G6
RXIN0	Input	PT3	✓	✓	✓	✓
RXIN1	Input	PT4	✓	✓	✓	-

2.23.3. Sampling Clock

The following clock can be used as the sampling clock for RMC.

Table 2.103 RMC sampling clock

Channel	Clock		Clock source	
		Signal name		Signal name
ch0	Low speed clock	fs	External low speed oscillator	fs
	Timer trigger 0 for clock source	TB0OUT	LTTMR0 interrupt	INTLTTMR0
ch1	Low speed clock	fs	External low speed oscillator	fs
	Timer trigger 1 for clock source	TB1OUT	LTTMR0 interrupt	INTLTTMR0

Note: The sampling clocks should be selected by ***[RMC0FSSEL]***<RMCCLK> and ***[RMC1FSSEL]*** <RMCCLK>.

2.23.4. Internal signal connection specification

2.23.4.1. T32A Connection

Table 2.104 RMC T32A connection specification

Channel	Function output	Signal name	Trigger Selector	Output destination	Signal name
ch0	Trigger output	RMC0TRG	***[TSEL0CR8]*** <INSEL35[2:0]>	T32A13 timer A internal trigger input	T32A13TRGINAPCK
ch1	Trigger output	RMC1TRG	***[TSEL0CR9]*** <INSEL36[2:0]>	T32A13 timer B internal trigger input	T32A13TRGINBPCK

2.24. Digital Noise Filter Circuit (DNF)

2.24.1. Built-in unit

The built-in units for every product is shown in the following table.

Table 2.105 DNF built-in unit

Product	DNF unit (✓: Available, -: N/A)	
	unit A	unit B
M4G9	✓	✓
M4G8	✓	✓
M4G7	✓	✓
M4G6	✓	✓

2.24.2. External interrupt pin and DNF

The digital noise filter circuit supports the external interrupt pins as shown in the following table.

Table 2.106 External interrupt pin and DNF (unit A)

External interrupt pin (Pin name)	Port	unit	Setting register name	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
INT00a	PK7	A	***[DNFAENCR]***<NFEN0>	✓	✓	✓	✓
INT01a	PL0		***[DNFAENCR]***<NFEN1>	✓	✓	✓	✓
INT02a	PA0		***[DNFAENCR]***<NFEN2>	✓	✓	✓	✓
INT03a	PA7		***[DNFAENCR]***<NFEN3>	✓	✓	✓	✓
INT04a	PB0		***[DNFAENCR]***<NFEN4>	✓	✓	✓	✓
INT05a	PB1		***[DNFAENCR]***<NFEN5>	✓	✓	✓	✓
INT06a	PB6		***[DNFAENCR]***<NFEN6>	✓	✓	✓	✓
INT07a	PB7		***[DNFAENCR]***<NFEN7>	✓	✓	✓	✓
INT08a	PG0		***[DNFAENCR]***<NFEN8>	✓	✓	✓	✓
INT09a	PG1		***[DNFAENCR]***<NFEN9>	✓	✓	✓	✓
INT10a	PK0		***[DNFAENCR]***<NFEN10>	✓	✓	✓	✓
INT11a	PK1		***[DNFAENCR]***<NFEN11>	✓	✓	✓	✓
INT12a	PC0		***[DNFAENCR]***<NFEN12>	✓	✓	✓	-
INT13a	PC1		***[DNFAENCR]***<NFEN13>	✓	✓	✓	-
INT14a	PC6		***[DNFAENCR]***<NFEN14>	✓	✓	-	-
INT15a	PC7		***[DNFAENCR]***<NFEN15>	✓	✓	-	-

Table 2.107 External interrupt pin and DNF (unit B)

External interrupt pin (Pin name)	Port	unit	Setting register name	Product table (✓: Available, -: N/A)			
				M4G9	M4G8	M4G7	M4G6
INT00b	PT3	B	***[DNFBENCR]***<NFEN0>	✓	✓	✓	✓
INT01b	PT4		***[DNFBENCR]***<NFEN1>	✓	✓	✓	-
INT02b	PT5		***[DNFBENCR]***<NFEN2>	✓	✓	✓	-
INT03b	PL6		***[DNFBENCR]***<NFEN3>	✓	-	-	-
INT04b	PF0		***[DNFBENCR]***<NFEN4>	✓	✓	✓	✓
INT05b	PF7		***[DNFBENCR]***<NFEN5>	✓	✓	✓	✓
INT06b	PU2		***[DNFBENCR]***<NFEN6>	✓	-	-	-
INT07b	PU3		***[DNFBENCR]***<NFEN7>	✓	-	-	-
INT08b	PU4		***[DNFBENCR]***<NFEN8>	✓	-	-	-
INT09b	PU5		***[DNFBENCR]***<NFEN9>	✓	-	-	-
INT10b	PP6		***[DNFBENCR]***<NFEN10>	✓	✓	✓	✓
INT11b	PP7		***[DNFBENCR]***<NFEN11>	✓	✓	✓	✓
INT12b	PL4		***[DNFBENCR]***<NFEN12>	✓	-	-	-
INT13b	PL5		***[DNFBENCR]***<NFEN13>	✓	-	-	-
INT14b	PM3		***[DNFBENCR]***<NFEN14>	✓	✓	-	-
INT15b	PM4		***[DNFBENCR]***<NFEN15>	✓	✓	-	-

2.24.3. Sampling Source Clock

The following clock can be used as the sampling source clock for DNF.

Table 2.108 DNF sampling source clock

Sampling source clock
fc

2.25. Interval Sensor Detection Circuit (ISD)

2.25.1. Built-in unit

The built-in units for every product is shown in the following table.

Table 2.109 ISD built-in unit

Product	ISD unit (✓: Available, -: N/A)		
	unit A	unit B	unit C
M4G9	✓	✓	✓
M4G8	✓	✓	-
M4G7	✓	✓	-
M4G6	✓	-	-

2.25.2. Function pin and port

The functional pin is assigned to the port of the following table.

There is also a unit which does not have a functional pin by a product.

Table 2.110 ISD function pin and port

Unit	Function pin (Signal name)	Port	Product table (✓: Available, -: N/A)			
			M4G9	M4G8	M4G7	M4G6
A	ISDAIN0	PE4	✓	✓	✓	✓
	ISDAIN1	PE5	✓	✓	✓	✓
	ISDAIN2	PE6	✓	✓	✓	✓
	ISDAIN3	PE7	✓	✓	✓	✓
	ISDAOUT	PK0	✓	✓	✓	✓
B	ISDBIN0	PV0	✓	✓	✓	-
	ISDBIN1	PV1	✓	✓	✓	-
	ISDBIN2	PV2	✓	✓	✓	-
	ISDBIN3	PV3	✓	✓	✓	-
	ISDBOUT	PK1	✓	✓	✓	- (Note)
C	ISDCIN0	PW4	✓	-	-	-
	ISDCIN1	PW5	✓	-	-	-
	ISDCIN2	PW6	✓	-	-	-
	ISDCIN3	PW7	✓	-	-	-
	ISDCOUT	PY4	✓	- (Note)	- (Note)	- (Note)

Note: The function pin is existing, but it has no corresponding function.

2.25.3. Reference Clock

The ISD circuit can select the following clocks as a reference clock.

Table 2.111 ISD reference clock

Unit	Clock		Clock source	
		Signal name		Signal name
A	Low speed clock	fs	External low speed oscillator	fs
	Timer trigger A for clock source	ISDACLKTRG	T32A ch9 timer A output	T32A09OUTA
B	Low speed clock	fs	External low speed oscillator	fs
	Timer trigger B for clock source	ISDBCLKTRG	T32A ch9 timer A output	T32A09OUTA
C	Low speed clock	fs	External low speed oscillator	fs
	Timer trigger C for clock source	ISDCCLKTRG	T32A ch9 timer A output	T32A09OUTA

Note: The sampling clock should be selected by ***[ISDxCLKCR]***<SC> in each unit.

2.25.4. Internal signal connection specification

The following table shows the internal signals connected to the ISD.

Table 2.112 ISD control connection Specification

Unit	Master		Slave		
	Function (Output)	Signal name	unit	Function (Input)	Signal name
unit A	ISDASDO	Output timing connection to Slave unit	B	ISDBSDI	Output timing connection from Master unit A
			C	ISDCSDI	Output timing connection from Master unit A
	ISDATMO	Detection timing connection to Slave unit	B	ISDBTMI	Detection timing form Master unit A
			C	ISDCTMI	Detection timing form Master unit A

2.26. Boundary-scan (BSC)

2.26.1. Support products

The function support for every product is shown in the following table.

Table 2.113 Boundary scan support product

Product	Boundary scan support (✓: Supportted, -: Unsupported)
M4G9	✓ (Note1)
M4G8	✓ (Note2)
M4G7	-
M4G6	-

Note1: VFBGA177 package product only.
Note2: VFBGA145 package product only.

2.26.2. JTAG interfaces and port for the each products

Table 2.114 JTAG interfaces and port for the each products

Debug pin (Signal name)	Port	Product table (✓: Available, -: N/A)			
		M4G9	M4G8	M4G7	M4G6
TMS	PH4	✓	✓	✓	✓
TCK	PH5	✓	✓	✓	✓
TDO	PH6	✓	✓	✓	✓
TDI	PH3	✓	✓	✓	✓
TRST_N	PH7	✓	✓	✓	✓
BSC		✓ (Note1)	✓ (Note2)	-	-

Note1: LQFP176 package product is not supported.
Note2: LQFP144 package product is not supported.

2.26.3. Boundary-scan Order

The following tables show the order of the boundary-scan for the processor signals in the product.

Table 2.115 Boundary-scan order (1/4)

Order	Function name or Port name	Support (✓: Supportted, -: Unsupported)	
		M4G9 (177-pin product only)	M4G8 (145-pin product only)
-	TDI	✓	✓
1	PH2	✓	✓
2	PH1	✓	✓
3	PH0	✓	✓
4	PG7	✓	✓
5	PG6	✓	✓
6	PG5	✓	✓
7	PG4	✓	✓
8	PL3	✓	✓
9	PL2	✓	✓
10	PL1	✓	✓
11	PL0	✓	✓
12	PK7	✓	✓
13	PK6	✓	✓
14	PK5	✓	✓
15	PK4	✓	✓
16	PK3	✓	✓
17	PK2	✓	✓
18	PK1	✓	✓
19	PK0	✓	✓
20	PV3	✓	✓
21	PV2	✓	✓
22	PV1	✓	-
23	PV0	✓	-
24	PT4	✓	✓
25	PW7	✓	-
26	PW6	✓	-
27	PW5	✓	-
28	PW4	✓	-
29	PM3	✓	✓
30	PM2	✓	✓
31	PM1	✓	✓
32	PM0	✓	✓
33	PL5	✓	-
34	PL4	✓	-
35	PG0	✓	✓
36	PG1	✓	✓
37	PG2	✓	✓
38	PG3	✓	✓
39	PN0	✓	✓
40	PN1	✓	✓

Table 2.116 Boundary-scan order (2/4)

Order	Function name or Port name	Support (✓: Supportted, -: Unsupported)	
		M4G9 (177-pin product only)	M4G8 (145-pin product only)
41	PN2	✓	✓
42	PN3	✓	✓
43	PN4	✓	✓
44	PN5	✓	✓
45	PN6	✓	✓
46	PN7	✓	✓
47	PP0	✓	✓
48	PP1	✓	✓
49	PP2	✓	✓
50	PP3	✓	✓
51	PP4	✓	✓
52	PP5	✓	✓
53	PP6	✓	✓
54	PP7	✓	✓
55	PR0	✓	✓
56	PR1	✓	✓
57	PR2	✓	✓
58	PR3	✓	✓
59	PR4	✓	✓
60	PR5	✓	✓
61	PR6	✓	✓
62	PR7	✓	✓
63	PT0	✓	✓
64	PT1	✓	✓
65	PL7	✓	-
66	PL6	✓	-
67	PJ3	✓	-
68	PJ2	✓	-
69	PJ1	✓	-
70	PJ0	✓	-
71	PT2	✓	✓
72	PF0	✓	✓
73	PF1	✓	✓
74	PF2	✓	✓
75	PF3	✓	✓
76	PF4	✓	✓
77	PF5	✓	✓
78	PF6	✓	✓
79	PF7	✓	✓
80	PC7	✓	✓

Table 2.117 Boundary-scan order (3/4)

Order	Function name or Port name	Support (✓: Supportted, -: Unsupported)	
		M4G9 (177-pin product only)	M4G8 (145-pin product only)
81	PC6	✓	✓
82	PC5	✓	✓
83	PC4	✓	✓
84	PC3	✓	✓
85	PC2	✓	✓
86	PC1	✓	✓
87	PC0	✓	✓
88	PB7	✓	✓
89	PB6	✓	✓
90	PB5	✓	✓
91	PB4	✓	✓
92	PB3	✓	✓
93	PB2	✓	✓
94	PB1	✓	✓
95	PB0	✓	✓
96	PA7	✓	✓
97	PA6	✓	✓
98	PA5	✓	✓
99	PA4	✓	✓
100	PA3	✓	✓
101	PA2	✓	✓
102	PA1	✓	✓
103	PA0	✓	✓
104	PY4	✓	✓
105	PT3	✓	✓
106	PU0	✓	-
107	PU1	✓	-
108	PU2	✓	-
109	PU3	✓	-
110	PU4	✓	-
111	PU5	✓	-
112	PU6	✓	-
113	PU7	✓	-
114	PY3	✓	✓
115	PY2	✓	✓
116	PY1	✓	✓
117	PY0	✓	✓
118	PD0	✓	✓
119	PD1	✓	✓
120	PD2	✓	✓

Table 2.118 Boundary-scan order (4/4)

Order	Function name or Port name	Support (✓: Supportted, -: Unsupported)	
		M4G9 (177-pin product only)	M4G8 (145-pin product only)
121	PD3	✓	✓
122	PD4	✓	✓
123	PD5	✓	✓
124	PD6	✓	✓
125	PD7	✓	✓
126	PE0	✓	✓
127	PE1	✓	✓
128	PE2	✓	✓
129	PE3	✓	✓
130	PE4	✓	✓
131	PE5	✓	✓
132	PE6	✓	✓
133	PE7	✓	✓
134	PJ7	✓	-
135	PJ6	✓	-
136	PJ5	✓	-
137	PJ4	✓	-
138	PT5	✓	✓
139	PW3	✓	-
140	PW2	✓	-
141	PW1	✓	-
142	PW0	✓	-
143	PV7	✓	✓
144	PV6	✓	✓
145	PV5	✓	✓
146	PV4	✓	✓
147	PM7	✓	✓
148	PM6	✓	✓
149	PM5	✓	✓
150	PM4	✓	✓
-	TDO	✓	✓

2.27. Trimming Circuit (TRM)

2.27.1. Built-in list

The following table shows the built-in list for each product.

Table 2.119 TRM built-in list

Product	built-in TRM (✓: Available, -: N/A)
M4G9	✓
M4G8	✓
M4G7	✓
M4G6	✓

2.27.2. Target Oscillator

The object oscillator of a trimming circuit is an oscillator shown in the following table.

Table 2.120 TRM trimming oscillator

Object oscillator	Oscillator name
Internal high speed oscillator 1	IHOSC1

2.28. External Bus Interface (EBIF)

2.28.1. Function pin and port

The functional pin is assigned to the port of the following table.

There is also a unit which does not have a functional pin by a product.

Table 2.121 EBIF function pin and port

Function pin (Signal name)		Port	Product table (✓: Available, -: N/A)			
Separated bus	Multiplexed bus		M4G9	M4G8	M4G7	M4G6
EA00 to EA07	-	PA0 to PA7	✓	✓	✓	✓
EA08 to EA15	-	PB0 to PB7	✓	✓	✓	✓
EA16 to EA23	EA16 to EA23	PC0 to PC3 / PC4 to PC7	✓ / ✓	✓ / ✓	✓ / -	- / -
		PE7 to PE0	✓	✓	✓	✓
ED00 to ED15	EAD00 to EAD15	PD0 to PD7and PE0 to PE7	✓	✓	✓	✓
-	EALE	PG0	✓	✓	✓	✓
ERD_N		PF0	✓	✓	✓	✓
EWR_N		PF1	✓	✓	✓	✓
ECS0_N		PK2	✓	✓	✓	✓
ECS1_N		PK3	✓	✓	✓	✓
ECS2_N		PF4	✓	✓	✓	-
ECS3_N		PF5	✓	✓	✓	-
EBELL_N		PF6	✓	✓	✓	✓
EBELH_N		PF7	✓	✓	✓	✓
EWAIT_N		PG1	✓	✓	✓	✓
EEXBCLK		PY4	✓	✓	✓	✓

3. Revision History

Table 3.1 Revision history

Revision	Date	Description
1.0	2018-02-01	First release
2.0	2018-03-22	2.1. Register Base Address Corrected: Table 2.1, 2.3 Peripheral function unit / channel 2.2.1. Trigger Selector per Product Corrected: Table 2.4 to 2.7 Trigger source column “(unit A)”->”A” 2.2.2. Operation and setting Corrected: “For the selected input trigger signal, select detection of rising edge or falling edge.” Corrected: “To select the edge detection condition, set with the edge detection condition bit (***[TSEL0CRn]*** <UPDNm>) of the control register.” 2.2.4.1. ***[TSEL0CR0]*** to 2.2.4.14. ***[TSEL0CR13]*** Corrected: Description column “(unit A)”->”A” 2.5.1. Debugging interface terminal list of each product. Corrected: Table 2.15 2.8.2. DMA transfer request list Corrected: Table 2.24 Note: “2 x fsys” ->” 2 x fsysh” Corrected: Table 2.25 Note2: “HDMAC request”->” DMA request” “2 x fsys” ->” 2 x fsysh” 2.9.2. DMA transfer request list Corrected: “2.9.2. MDMA transfer request list” ->” 2.9.2. DMA transfer request list” Corrected: Table 2.30 Note5: “MDMAC request”->” DMA request” 2.10.3. DMA Request Corrcted: “Table 2.33 A-PDM DMA request”->” Table 2.33 A-PMD DMA request” Deleted: Table 2.33 Request column “A-PMD” 2.11.2. Function pin and port Corrected: Table 2.36 Input channel column “ch00 – ch09”->”ch0 – ch9” 2.11.6. DMA request Deleted: Table 2.39 Unit column “unit” , Request column “ADC” 2.16.3.1. CEC/RMC connection Corrected: 2.16.3.1 And 2.16.3.2 are integrated and amended to "2.16.3.1. CEC / RMC connection" Corrected: Table 2.71 and Table 2.72 are integrated and modified 2.20.6. DMA Request Deleted: DMA request channel column “'(MDMAC unit A)” 2.23.4.1. T32A Connection Corrected: Output destination column 2.25.2. Function pin and port 2.25. Interval Sensor Detection Circuit (ISD) Deleted: Table 2.109, 110, 111 Unit column “unit”
2.1	2018-05-28	2.1 Register Base Address Deleted Input/Output Ports from Table 2.3 2.14.4.3 T32A timer channel reload trigger connection specification Added “<>” to bit symbol name of Trigger Selector in Table 2.58 2.17.1 Built-in channel Added maximum communication speed of UART 2.18.1 Built-in channel Added maximum communication speed of FUART 2.19.1 Built-in channel Added support mode of I^2C interface 2.20.1 Built-in channel Added maximum communication speed of TSPI

3.0	2019-02-12	2.4.1. “Support products” → “ Built-in list” The expression changed. 2.13.1. “Support products” → “ Built-in list” The expression changed. 2.17.3. Half clock mode list for the each products Corrected: Half clock mode support 2.27.1. “Support products” → “ Built-in list” The expression changed. RESTRICTIONS ON PRODUCT USE Revised: Update
3.1	2019-06-17	Terms and Abbreviation Modified “Toshiba Serial Peripheral Interface” to “ Serial Peripheral Interface” 2.1 Register Base Address Corrected Base address type of SMIF: TYPE3 to TYPE1 2.14.4.1 Capture/counter channel connection specification Added Trigger Selection of ch2 in Table 2.53 Deleted Trigger Selection of ch5(TimerB) in Table 2.54

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