32-bit RISC Microcontroller

TMPM4G Group(1)

Reference Manual
Power Supply and Reset Operation
(RESET-M4G(1))

Revision 1.1

2018-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related document

Document name
The datasheet of each product (Electrical Characteristics)
Exception
Clock Control and Operation Mode
Oscillation Frequency Detector
Voltage Detection Circuit
Clock Selective Watchdog Timer
Flash Memory

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
SIWDT	Clock Selective Watchdog Timer

1. Outline

This section describe how to turn on power supply, a Power On Reset, and assert/deassert reset.

Function classification	Factor	Functional Description
Cold reset (Reset by turning on a power supply)	Power On Reset	Reset which occurs at the time of a power supply turning on or turning off.
	LVD reset	Reset which occurs below on the set-up voltage
	Reset pin	Reset by a RESET_N pin
Worm reset (Reset without turning on a power supply)	Internal reset	Reset by SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>
	Reset pin	Reset by a RESET_N pin
Reset by STOP2 mode release	Interruption	Reset which is performed to Main Power Domain during return operation from the STOP2 mode. (STOP2REQ)
	Reset pin	Reset by a RESET_N pin
Single boot start up	-	Start up program in the built-in boot ROM is used after the reset deassertion.

2. Function and Operation

Note: Refer to the "Electrical Characteristics" of a datasheet for the time and voltage of description of the symbol in a figure.

2.1. Cold reset

When turn on a power supply, the stabilization times for the built-in regulator, the built-in Flash memory, and the built-in high speed oscillator are necessary. The TXZ family automatically insert a wait time for the stabilization of these circuits.

2.1.1. Reset by a Power On Reset Circuit (without using a RESET_N pin)

After a supply voltage exceeds the release voltage of a Power On Reset (POR), internal reset is deasserted after "Internal initialization time" is elapsed. Please increase a supply voltage goes up into an operating voltage range before "Internal initialization time" is elapsed. The CPU operates after internal reset is released.

After a supply voltage exceeds the release voltage of a Power On Reset (POR), LVD continue to output reset to exceeds LVD release voltage. And internal reset gives priority during the time of "Internal initialization time". When rising time of a supply voltage beyond "Internal initialization time", please refer to "2.1.3. Reset by LVD".

For example, if the operating voltage of a circuit board is more than 2.7V, after Power On Reset released increase a supply voltage to 2.7V before "Internal initialization time" is elapsed.

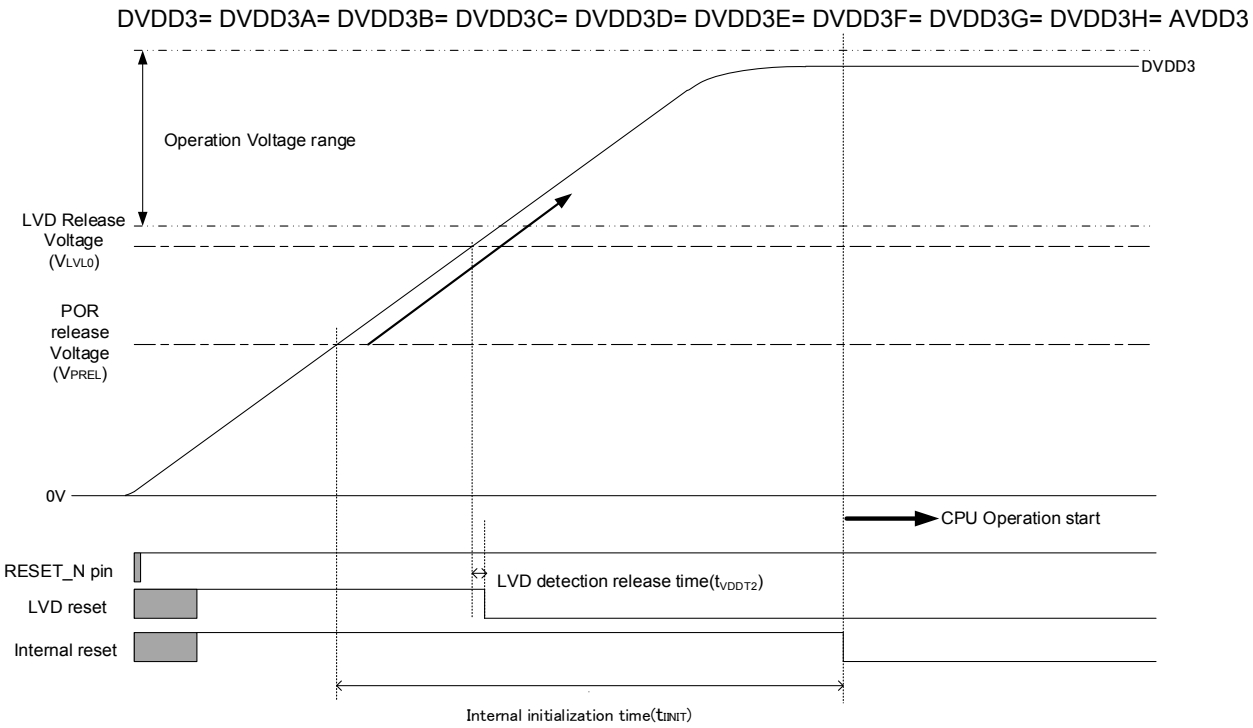

Figure 2.1 The reset operation by a Power On Reset Circuit

Note: When you use only a Power On Reset Circuit without RESET_N pin, the RESET_N pin should input "High" level or opened.

2.1.2. Reset by a RESET_N pin

When turn on a power supply, it can control the timing of reset release by using RESET_N pin.

After a supply voltage exceeds the release voltage of a Power On Reset and even after "Internal initialization time" elapsed and RESET_N pin is still "Low", internal reset is extended.
After a supply voltage goes up into an operating voltage range and a RESET_N pin becomes "High", Internal reset is deasserted after "CPU operation latency time" elapses.

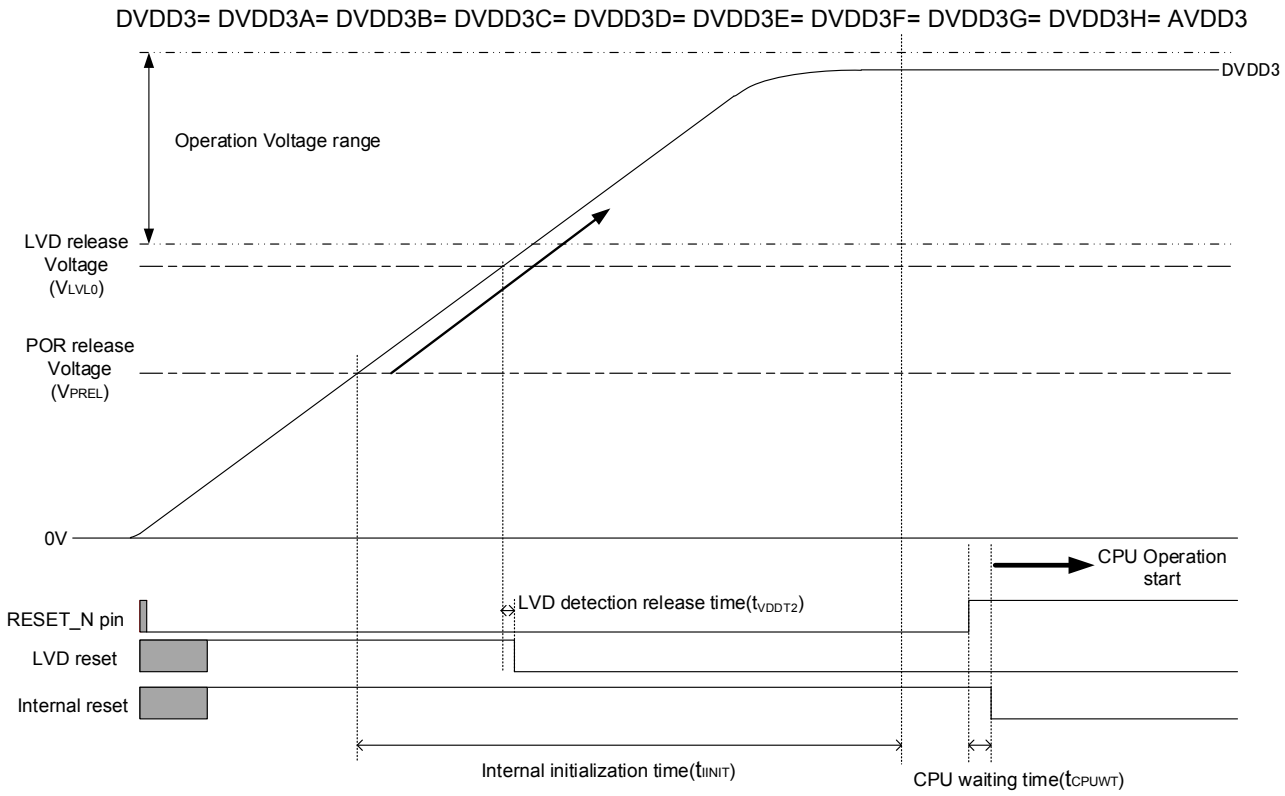

Figure 2.2 Reset operation by a RESET_N pin (1)

In case of RESET_N pin input change from "Low" to "High" before "Internal initialization time" elapses, internal reset signal is released after "Internal initialization time" elapses.
Please goes up a supply voltage into an operating voltage range before "Internal initialization time" elapses. The CPU operates after internal reset release.

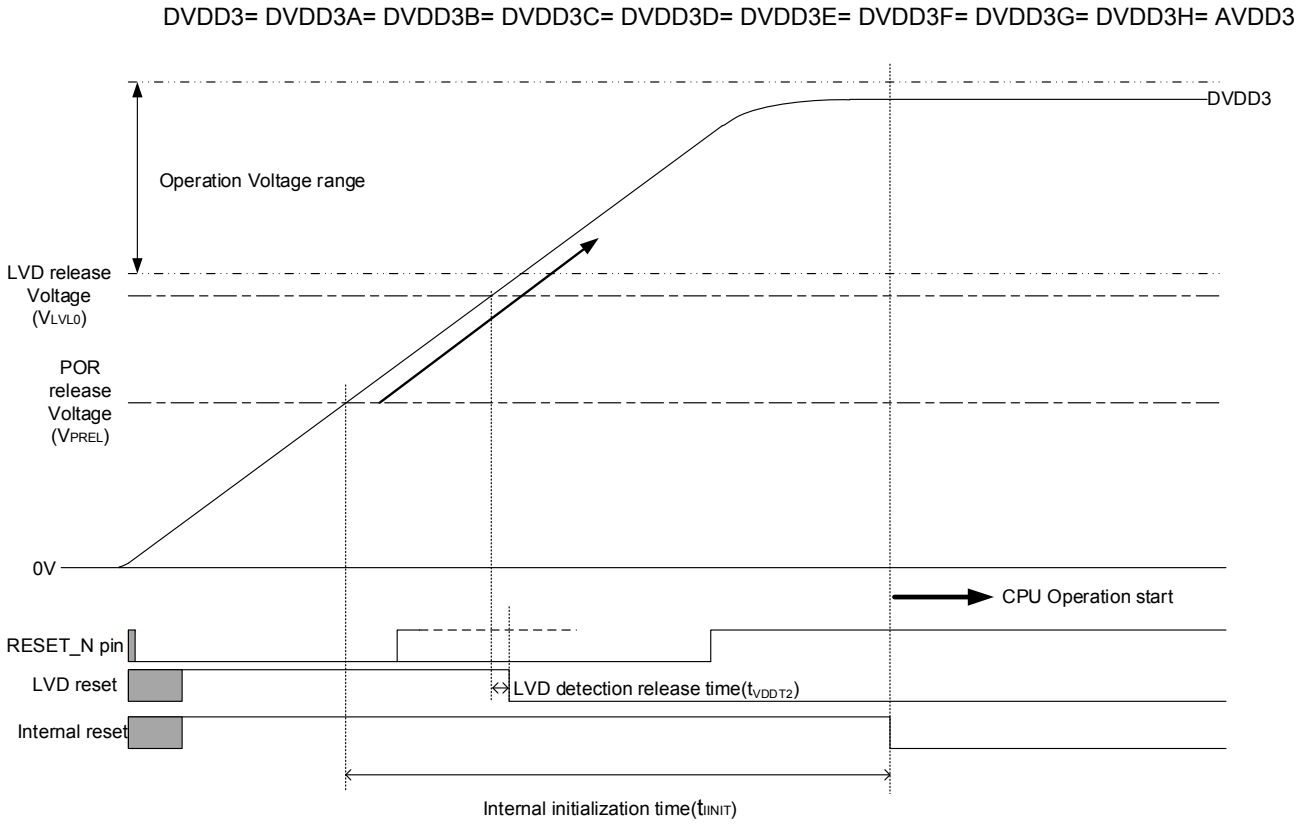

Figure 2.3 Reset operation by a RESET_N pin (2)

2.1.3. Reset by LVD

When the power supply voltage has not exceeded the LVD release voltage even after "Internal initialization time" elapses, LVD generates the reset signal and the reset state continues. After the power supply voltage exceeds the LVD release voltage and "LVD detection release time"+"CPU operation wait time" elapses, the internal reset is deasserted. And CPU starts operating. Refer to Reference Manual "Voltage detection circuit" for detail of LVD.

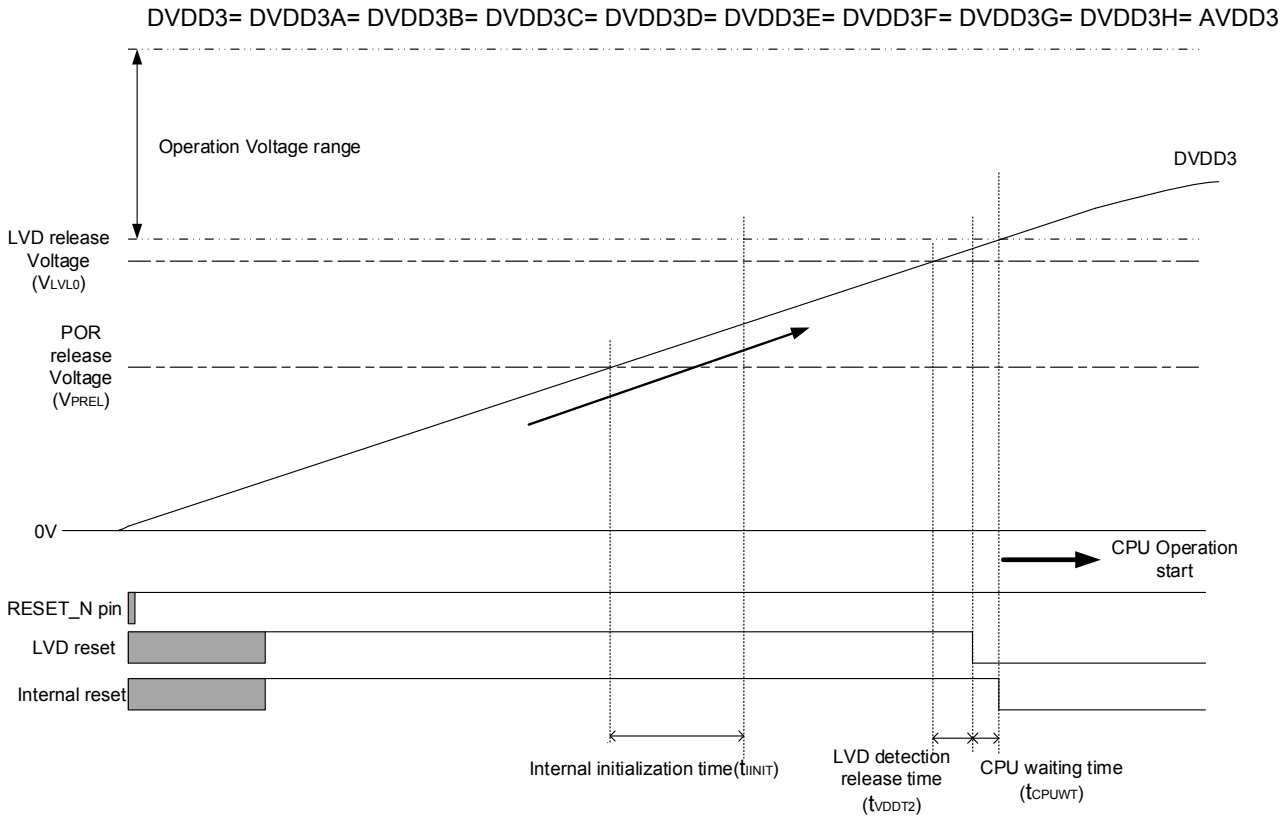

Figure 2.4 The reset operation by LVD reset

2.2. Warm reset

2.2.1. Warm reset by RESET_N pin

When resetting with the RESET_N pin, set the RESET_N pin to "Low" for at least 17.2µs or more while the power supply voltage is within the operating range.

When the "Low" period of a RESET_N pin is longer than "Internal processing time", after a RESET_N pin changes to "High", Internal reset is released after "CPU operation latency time" elapsed.

When the "Low" period of a RESET_N pin is shorter than "Internal processing time", after internal reset is extended and from a RESET_N pin changes "Low", Internal reset is release after "Internal processing time"+"CPU operation latency time" has elapsed, internal reset will be released.

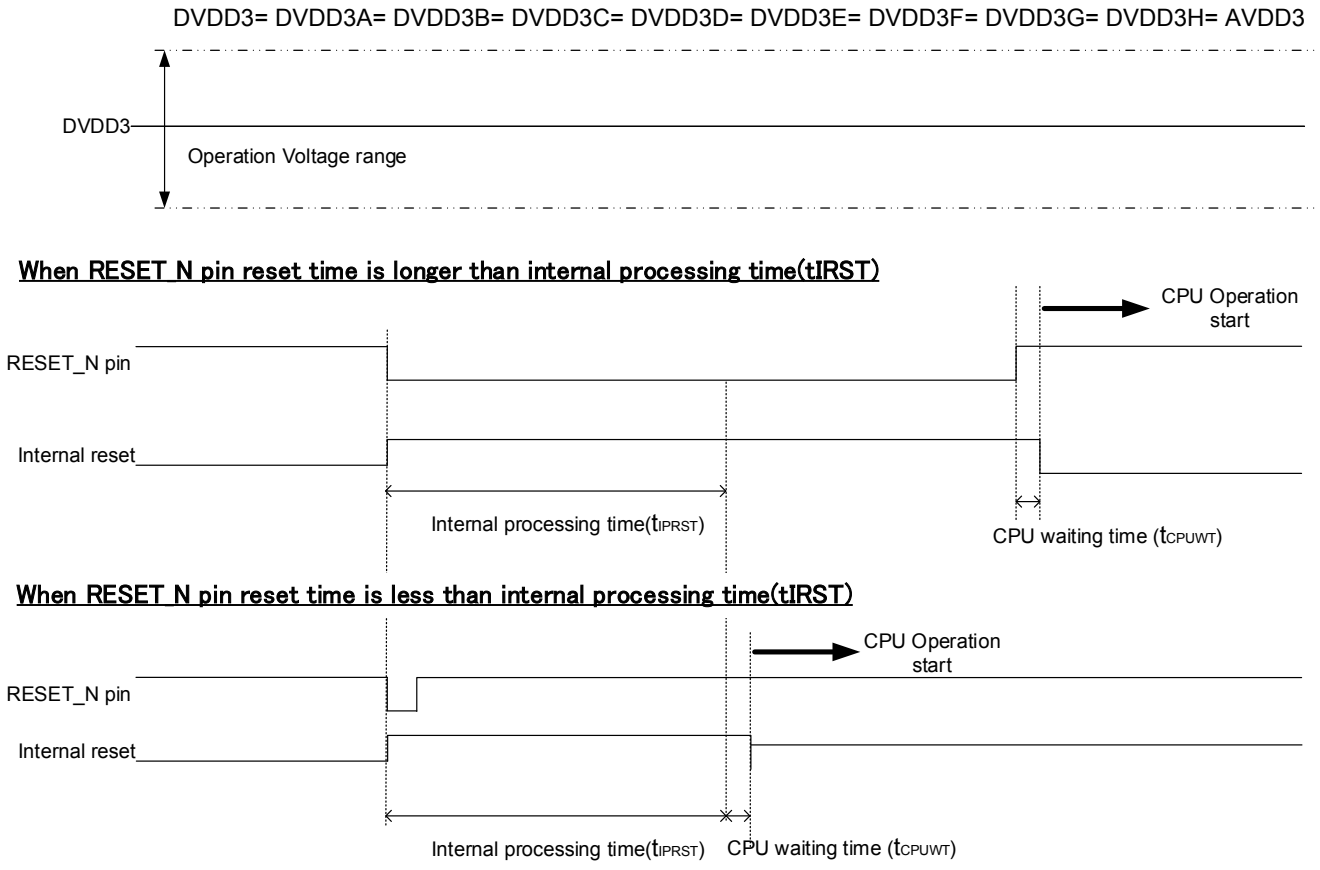

Figure 2.5 Warm reset action

2.2.2. Warm reset by internal reset

In case of reset asserted by internal factors, such as SIWDT, OFD, LVD, LOCKUP, and <SYSRESETREQ>, Internal reset is released after "Internal processing time"+"CPU operation latency time" elapsed.

2.3. Reset by STOP2 mode release

When RESET_N pin changed "Low" during STOP2 mode, STOP2 released. The power supply is turned on and assert reset to Main Power Domain. After RESET_N pin changes to "High", start operate in NORMAL mode. At that time, condition of CPU is as same as cold reset except ***[RLMLOSCCR]***,***[RLMRSTFLG0]***,***[RLMRSTFLG1]***.

When asserted interrupt request during STOP2 mode, also STOP2 released. The power supply is turned on and assert reset to Main Power Domain in the sequence of releasing STOP2 mode. Refer to "Clock Control and Operation Mode" of reference manual for the operation at the time of STOP2 release.

2.4. Starting in reset and single boot mode

For the details of the single mode, refer to "Flash memory" in Reference manual.

2.4.1. Start-up Using RESET_N Pin Signal

When "Low" is inputted to a BOOT_N pin, reset release (a RESET_N pin "Low" to "High"), "single boot mode" will be started.

When turn on power supply, the time of input "Low" to the RESET_N pin longer than "Internal initialization time". And deassert RESET_N pin to "High", after a supply voltage goes up into an operating voltage range.

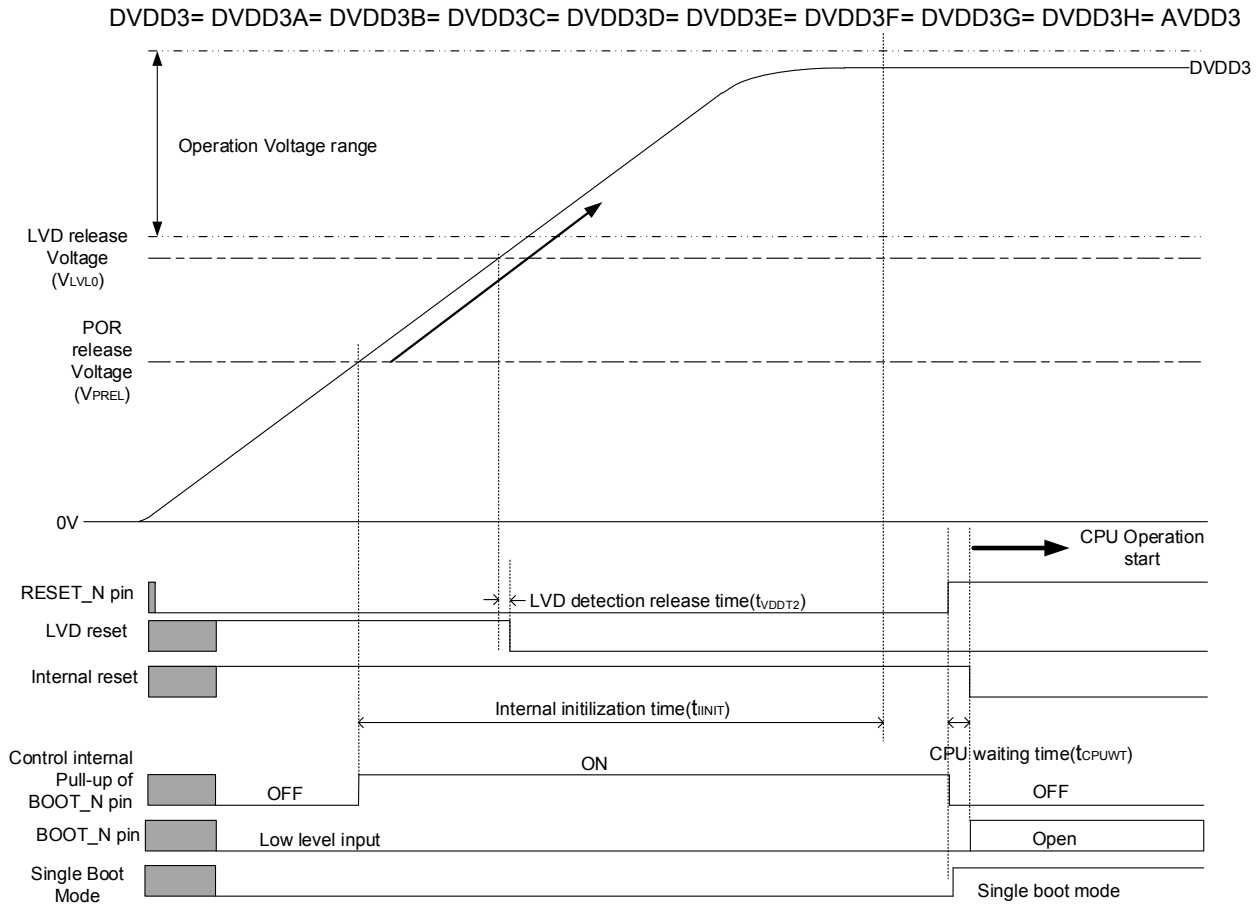

Figure 2.6 Starting in power supply is on and single boot mode

2.4.2. Start up by Power On Reset (Not Using RESET_N Pin Signal)

"Low" should be input to BOOT_N pin after the power is supplied. And after the internal reset is deasserted and the CPU operation starts, the single boot mode starts up.

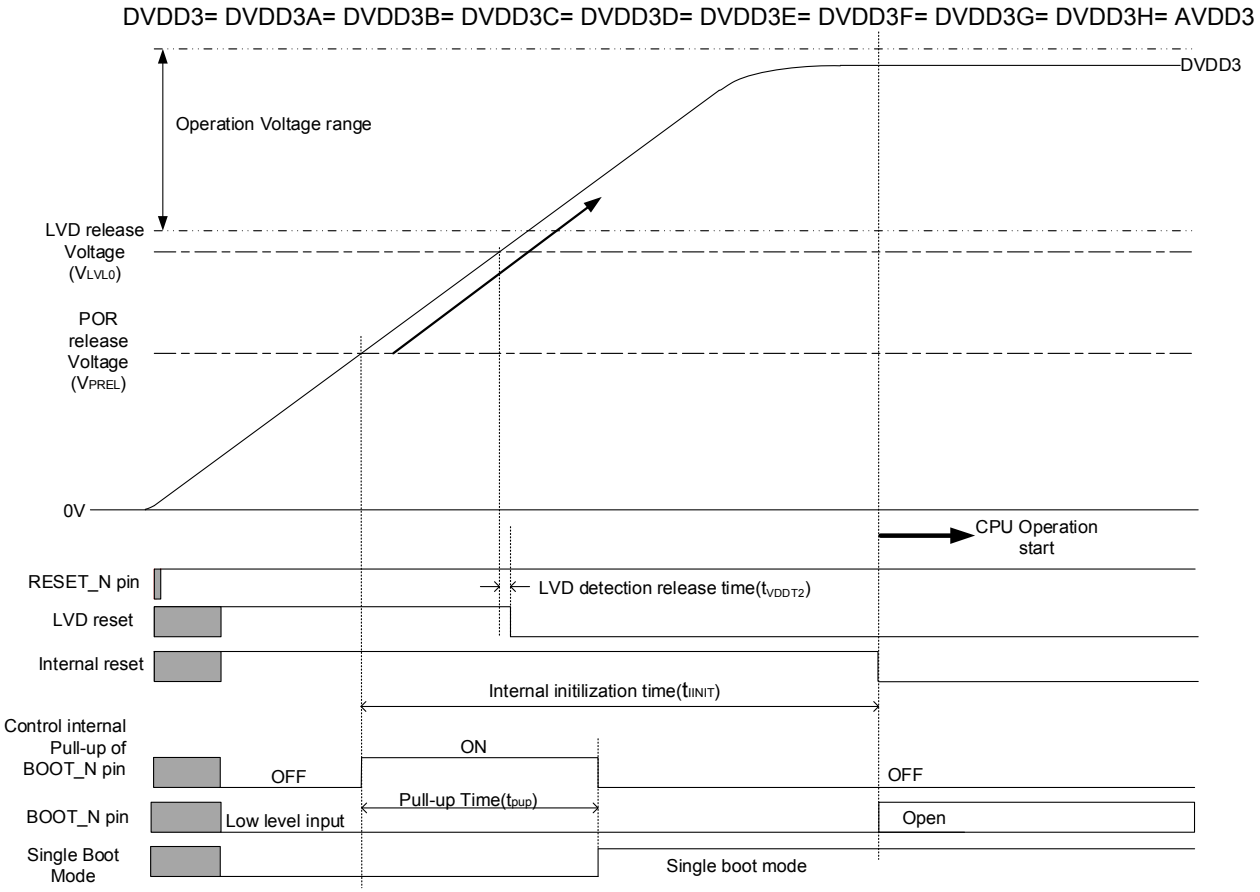

Figure 2.7 Starting single boot mode without using reset

2.4.3. Starting in the single boot mode when power supply is stable

When the supply voltage is stable within an operating voltage range, input "Low" to RESET_N pin for reset longer than "Internal processing time", during inputted "Low" to the BOOT_N pin. And deassert RESET_N pin to "High".

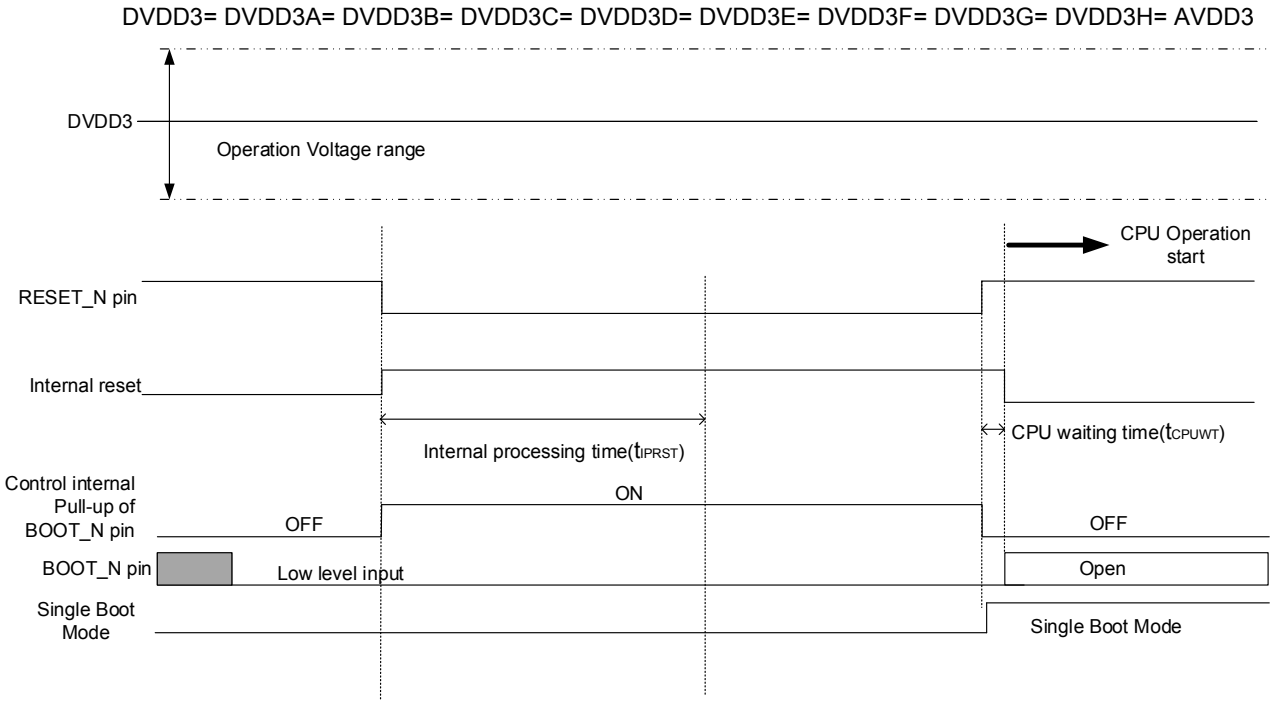

Figure 2.8 Starting in the single boot mode when power supply is stable

2.5. Power On Reset Circuit

The Power On Reset Circuit (POR) generates a reset signal when the power is turned on or turned off.

Note: The Power On Reset Circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electric characteristics.

The Power On Reset Circuit consists of a Detection voltage generation circuit, a Reference voltage generation circuit, and a Comparator.

The supply voltage has referred to DVDD3(= DVDD3A= DVDD3B= DVDD3C= DVDD3D= DVDD3E= DVDD3F= DVDD3G= DVDD3H).

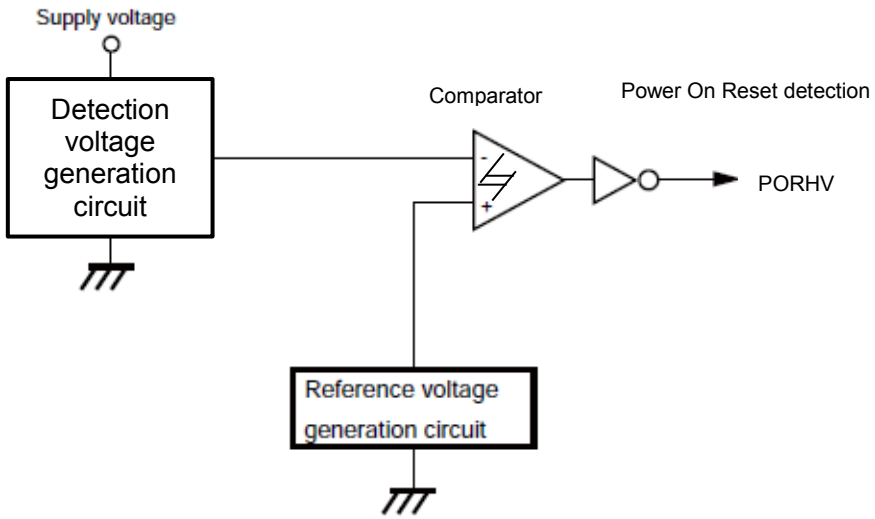

Figure 2.9 Power On Reset Circuit

2.5.1. Operation at the time of a power supply

When turn on power supply, while the power supply voltage is lower than Power On Reset Circuit release voltage (V_{PREL}), the Power On Reset detection signal is generated. Refer to "Figure 2.1 The reset operation by a Power On Reset Circuit" for detail.

While the Power On Reset signal is generated, the reset is asserted to the CPU and the peripherals.

2.5.2. Operation at the time of turn off

When turn off power supply or when the power supply voltage is lower than Power On Reset detection voltage(V_{PDET}), the Power On Reset detection signal is generated

While the Power On Reset signal is generated, the reset is asserted to the CPU and the peripherals.

2.6. About turn on power supply after turn off

(1) When using external reset circuit or internal LVD reset output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, reset is performed with an external reset circuit or built-in LVD (when the voltage is less than the set voltage). After that, from the state where the reset is applied, please follow the same constraints as when turning on the power and turned on the power supply voltage.

(2) When not using external reset circuit and internal LVD reset output

When the power supply is turned off and the power supply voltage drops below the operation guaranteed voltage, be sure to lower the power supply voltage below the Power On Reset detection voltage (V_{PDET}) and hold it for 200µs or more. After that, please follow the same constraints as when turning on the power and turned on the power supply voltage.
When the power supply voltage drops below the Power On Reset detection voltage (V_{PDET}) and cannot be held for 200µs or more, or when the same constraints as at power on cannot keep , the MCU may not operate properly.

2.7. After reset release

All of the control register of Cortex-M4(with FPU) core and the peripheral function control register (SFR) are initialized by reset. But depend on the reset factor, initialized range is different.

Please refer to "Table 2.1 A reset factor and the range initialized" for the initialized range by every reset factor.

The reset factor when reset occurs can be check by a reset flag register which are ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***. For detail of ***[RLMRSTFLG0]*** and ***[RLMRSTFLG1]***, please refer to "Exception" of reference manual.

After reset is released, TXZ-MCU starts operation by a clock of Internal High Speed Oscillator1(IHOSC1). External clock and PLL multiple circuit should be set if necessary.

2.7.1. A reset factor and the reset range

A reset factor and the range initialized is shown in Table 2.1.

Table 2.1 A reset factor and the range initialized

Registers and Peripheral function		Reset factors								
		Peripheral function		Cold Reset	Warm reset					
		Interru -ption factor	Reset Pin	POR	Reset Pin	OFD Reset	WDT Reset	LVD Reset	CPU <SYS RESET REQ> Reset	CPU LOCKUP Reset
	Reset signal name	STOP2 REQ	RESET_N	PORHV	RESET_N	OFD RSTOUT	WDT RSTOUT	LVD RSTOUT	SYS RESET REQ	LOCKUP RESET REQ
RTC	***[RTCSECR] [RTCMINR] [RTCHOURR] [RTCDAYR] [RTCDATER] [RTCMONTHR] [RTCYEARR] [RTCADJCTL] [RTCADJDAT] [RTCADJSIGN]***	-	-	-	-	-	-	-	-	-
	Except the above	-	✓	✓	✓	✓	✓	✓	✓	✓
Low speed oscillation Power control Reset flag	***[RLMSHTDNOP] [RLMPROTECT]***	-	✓	✓	✓	✓	✓	✓	✓	✓
	[RLMLOSCCR] [RLMRSTFLG0] [RLMRSTFLG1]	-	-	✓	-	-	-	-	-	-
Interruption Control	***[IAIMCxx] [IANIC00]***	-	✓	✓	✓	✓	✓	✓	✓	✓
	[IBIMCxxx] [IBNIC00]	✓	✓	✓	✓	✓	✓	✓	✓	✓
FLASH	***[FCSBMR]***	✓	✓	✓	-	-	-	-	-	-
Port	All the registers	✓	✓	✓	✓	✓	✓	✓	✓	✓
OFD		✓	✓	✓	✓	✓	✓	✓	✓	✓
LVD		-	✓	✓	✓	-	-	-	-	-
LTTMR, ISD, RMC, CEC		-	✓	✓	✓	✓	✓	✓	✓	✓
Debugging interface		✓	✓	✓	-	-	-	-	-	-
Except the above		✓	✓	✓	✓	✓	✓	✓	✓	✓

✓: it is initialized.
-: It is not initialized.

Note: When reset is performed, the data of built-in RAM will not be guaranteed.

3. Revision history

Table 3.1 Revision history

Revision	Date	Description
1.0	2018-01-23	First release
1.1	2018-07-09	- 1.: Deleted of "Table 1.1 Functional outline". - 2.1.3.: Corrected to "the internal initialization time" → "Internal initialization time". Corrected to "LVD release detection time" → "LVD detection release time" in Figure 2.4. - 2.5: Added "Comparator" in Figure 2.9. - 2.5.2.: Corrected to " Reset detection voltage" →" Reset detection voltage(V_{PDET})". - 2.6: Correction of description content .

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