32-bit RISC Microcontroller

TXZ/TXZ+ Family

Reference Manual
Advanced Programmable Motor Control Circuit
(A-PMD-C)

Revision 2.3

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related document

Document name
Input/Output Ports
Exception
Clock Control and Operation Mode
Product Information
12-bit Analog to Digital Converter

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
PMD	Programmable Motor Control Circuit
PWM	Pulse Width Modulation

1. Outlines

The advanced programmable motor control circuit (hereafter, abbreviated as PMD) can operate as a motor control circuit of 1 channel per unit. The following is a list of functions. The following is a list of functions.

Function Classification	Function	Operation
PWM output	Resolution	The count resolution of PWM carrier: 1/fsys. PWM frequency and duty setting: 15-bit fixed
	PWM carrier generation	The frequency range of the PWM carrier that can be generated is 0.076 to 156.245 kHz (at fsys =80 MHz), and the amplitude is 15-bit width. 4 types of PWM carrier waveform: Triangular waveform, Saw-tooth waveform, Inverse triangular waveform, Inverse saw-tooth waveform. Carrier waveform can be selected for each phase. The phase shift can be done between U and V phases, and between U and W phases in the PWM carriers.
	3-phase PWM wave generation	3-phase PWM is generated by comparing the PWM carrier with the duty setting. 3-phase PWM can be generated by selecting either 3-phase common duty or 3-phase independent duty.
	Conduction control	Each of the U/X, V/Y and W/Z phases can be selected PWM or high/low output. Upper-phase output and lower-phase output can be set to low active or high active. This function has the common PWM carrier waveform and generates independent 3-phase PWM (3-phase complementary PWM).
AD conversion start trigger	Synchronous trigger generation	The AD conversion start trigger can be output at an arbitrary timing synchronized with the PWM carrier.
Protection function	Protection control	Output prohibition function by protection signal input (OFF output or terminal output disabled). 2 types of protect control: EMG, OVV
	Dead time control	The dead time control inserts the dead time for preventing short circuit at switching between the upper and lower phases (U/X, V/Y, W/Z). The complementary PWM is output.
Buffer function	-	PWM period, Duty, Synchronous trigger timing, and 6 port output setting are double-buffered or triple-buffered. These setting can be changed during operation. Selectable update timing of execution buffer: Asynchronous, PWM center, PWM end, PWM center/end Selectable update timing of intermediate buffer: Asynchronous, PWM center, PWM end, PWM 1/4, PWM 3/4
Interrupt request	PWM interrupt	PWM interrupt request is generated at a synchronous timing with the PWM wave. Interrupt timing: PWM center or PWM end Interrupt period: Half PWM period, one PWM period, two PWM period, or four PWM period. Decimation control: Synchronous trigger generation and buffer update can be decimated according to interrupt cycle selection.
	EMG interrupt	This interrupt request is generated by the EMG protection of EMG input.
	OVV interrupt	This interrupt request is generated by the OVV protection of OVV input.

2. Configuration

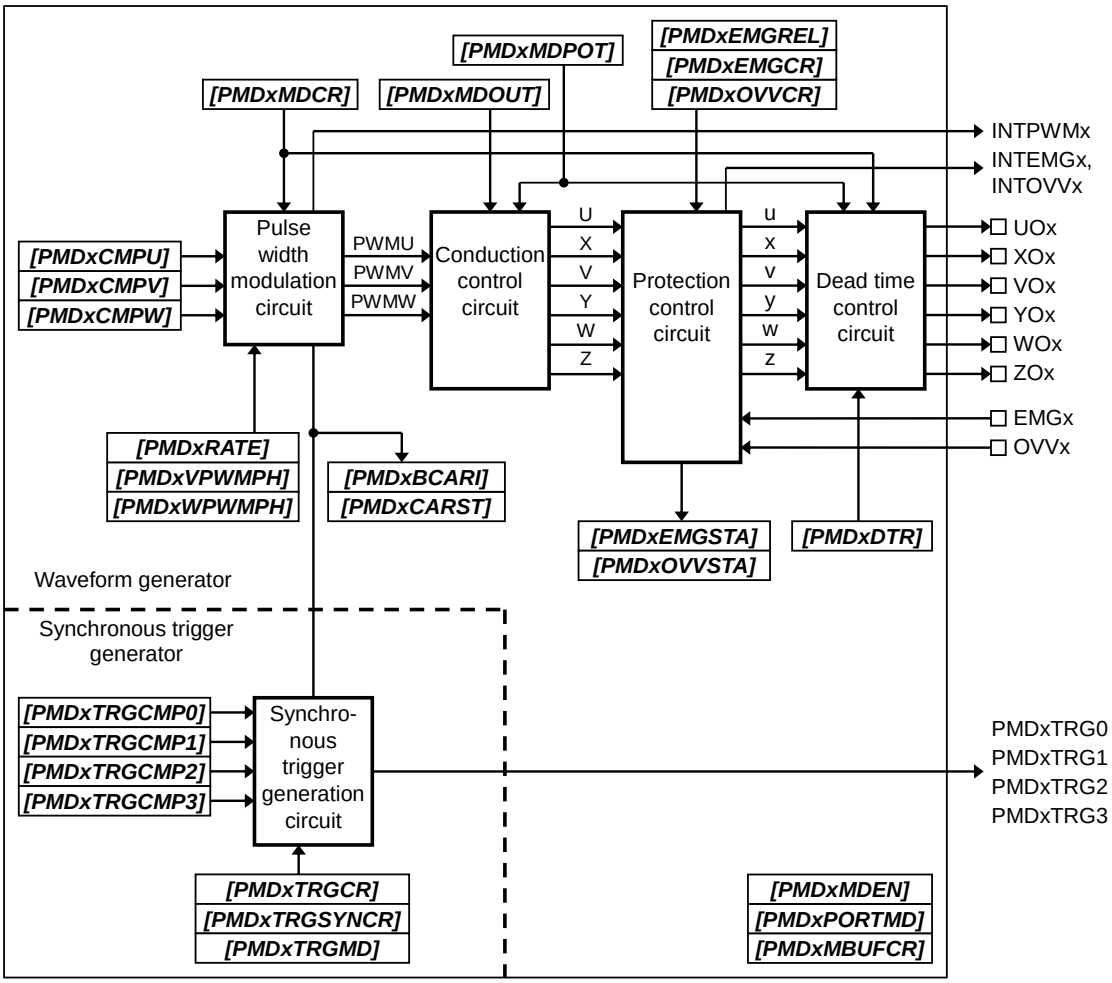

Figure 2.1 Block diagram of PMD circuit

Table 2.1 List of signals

No	Signal symbol	Signal name	I/O	Related Reference manual
1	UOx	U-phase output pin	Output	Product Information
2	XOx	X-phase output pin	Output	Product Information
3	VOx	V-phase output pin	Output	Product Information
4	YOx	Y-phase output pin	Output	Product Information
5	WOx	W-phase output pin	Output	Product Information
6	ZOx	Z-phase output pin	Output	Product Information
7	EMGx	EMG detection input	Input	Product Information
8	OVVx	OVV detection input	Input	Product Information
9	PMDxTRG0	ADC synchronous trigger output 0	Output	Product Information
10	PMDxTRG1	ADC synchronous trigger output 1	Output	Product Information
11	PMDxTRG2	ADC synchronous trigger output 2	Output	Product Information
12	PMDxTRG3	ADC synchronous trigger output 3	Output	Product Information
13	INTPWMx	PWM interrupt	Output	Exception
14	INTEMGx	EMG interrupt	Output	Exception
15	INTOVVx	OVV interrupt	Output	Exception

3. Function and Operation

PMD circuit consists of a wave generation circuit and a synchronous trigger generation circuit. The wave generation circuit includes a pulse width modulation circuit, a conduction control circuit, a protection control circuit, and a dead time control circuit.

- The pulse width modulation circuit generates PWM carrier waveforms and generates independent 3-phase PWM waveforms.
- The conduction control circuit determines the output patterns of the upper and lower phases of U, V, and W phases.
- The protection control circuit stops the outputs in emergency case when EMG or OVV signal is received.
- The dead time control circuit prevents from short-circuit at switching between the upper and lower phases.
- The synchronous trigger generation circuit generates 4 channel synchronous trigger signals to ADC.

3.1. Clock Supply

When using PMD, set an applicable clock enable bit to "1" (clock supply) in Clock supply and stop register A for fsys (***[CGFSYSENA]***, ***[CGFSYSMENA]***), Clock supply and stop register B for fsys (***[CGFSYSENB]***, ***[CGFSYSMENB]***), Clock supply and stop register C for fsys (***[CGFSYSMENC]***), and Clock supply and stop register for fc (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

3.2. Pulse Width Modulation Circuit

The pulse width modulation circuit consists of a PWM carrier generation circuit and 3-phase PWM generation circuit.

3.2.1. PWM Carrier Generation

The PWM carrier generation circuit integrates ***[PMDxRATE]*** register value to generate a basic carrier (saw-tooth wave), and generates each PWM carrier of 3 phases using the basic carrier.

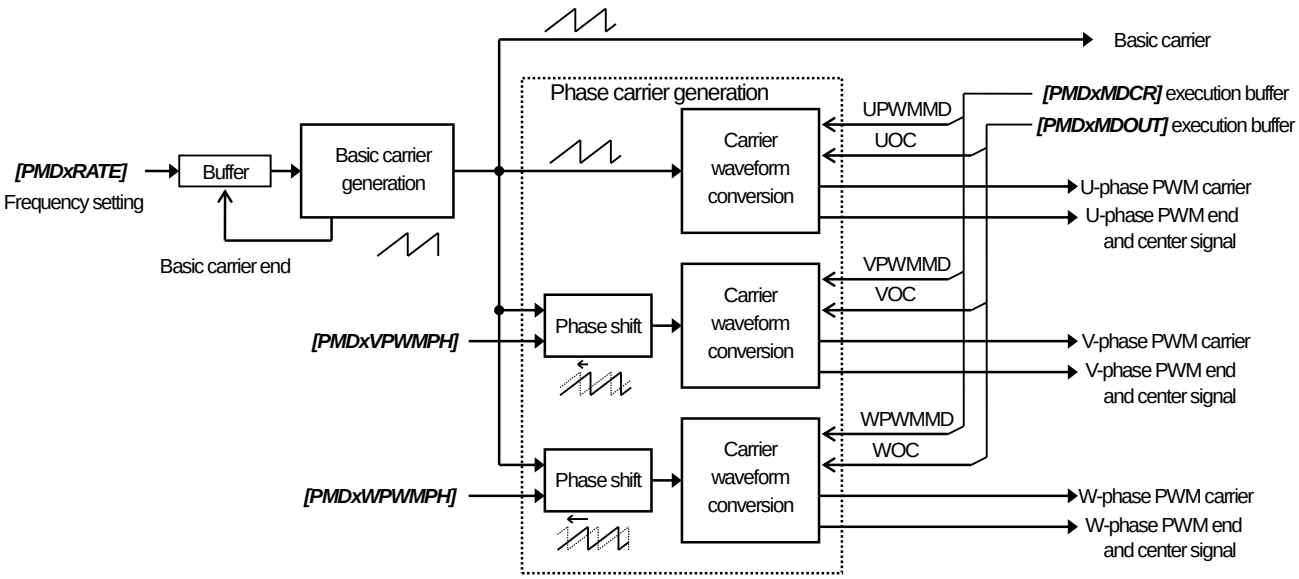

Figure 3.1 PWM carrier generation circuit

- Basic carrier generation

The PWM frequency should be set in ***[PMDxRATE]*** register. ***[PMDxRATE]*** register has a double-buffer structure. The execution buffer is updated every basic carrier end (refer to "4.2.6. ***[PMDxRATE]*** (PWM frequency register)").

The PWM frequency is calculated with the following formula:

$$\text{PWM frequency} = \frac{\text{fsys [Hz]}}{2^{24} / \textbf{\textit{[PMDxRATE]}}\ \text{value}}$$

Note: The decimal fraction is rounded off in the denominator.

The amplitude of the basic carrier is the same even when the frequency is changed, as shown in

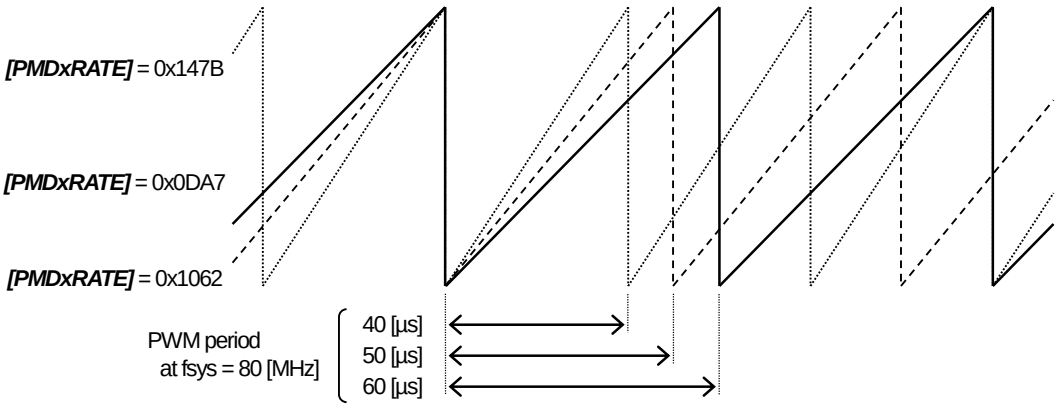

Figure 3.2 Basic carrier waveform

- Phase shift

The phase shift can be done between U and V phases, and between U and W phases in the PWM carriers. ***[PMDxVPWMPH]*** and ***[PMDxWPWMPH]*** registers can set the phase differences between U and V phases, and between U and W phases, respectively (refer to Figure 3.3).

The setting value of the phase shift is (the ratio to the PWM period) x 2^{15}.

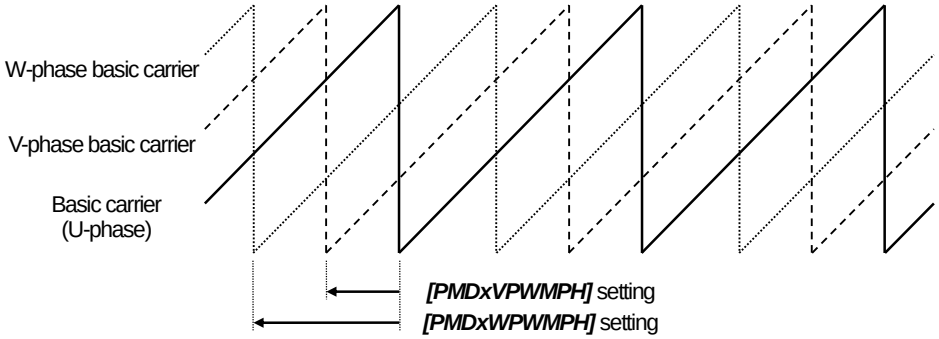

Figure 3.3 Phase shift diagram

- Each phase carrier generation

Each PWM phase carrier can select its waveform using the settings of <UPWMMD[1:0]>, <VPWMMD[1:0]>, and <WPWMMD[1:0]> in ***[PMDxMDCR]*** register. <UPWMMD[1:0]>, <VPWMMD[1:0]>, and <WPWMMD[1:0]> fields have a triple-buffer structure. The update timing of the execution buffer is shown in Table 3.1. For the update of the intermediate buffer, refer to "3.7. Buffer Operation".

The waveform of the PWM carrier can be selected from a saw-tooth wave, a triangular wave, an inverse saw-tooth wave, and an inverse triangular wave (refer to Figure 3.4). And the PWM carrier waveform is inversed when the conduction setting ***[PMDxMDOUT]***<UOC[1:0]>/<VOC[1:0]>/ <WOC[1:0]> is set to "00".

Table 3.1 Update control of execution buffers of <UPWMMD[1:0]>, <VPWMMD[1:0]>, and <WPWMMD[1:0]>

Setting *[PMDxMDPOT]*<PSYNCS[1:0]>	Update Timing
00	Asynchronous with PWM
01	Update at each PWM center
10	Update at each PWM end
11	Update at each PWM end and center

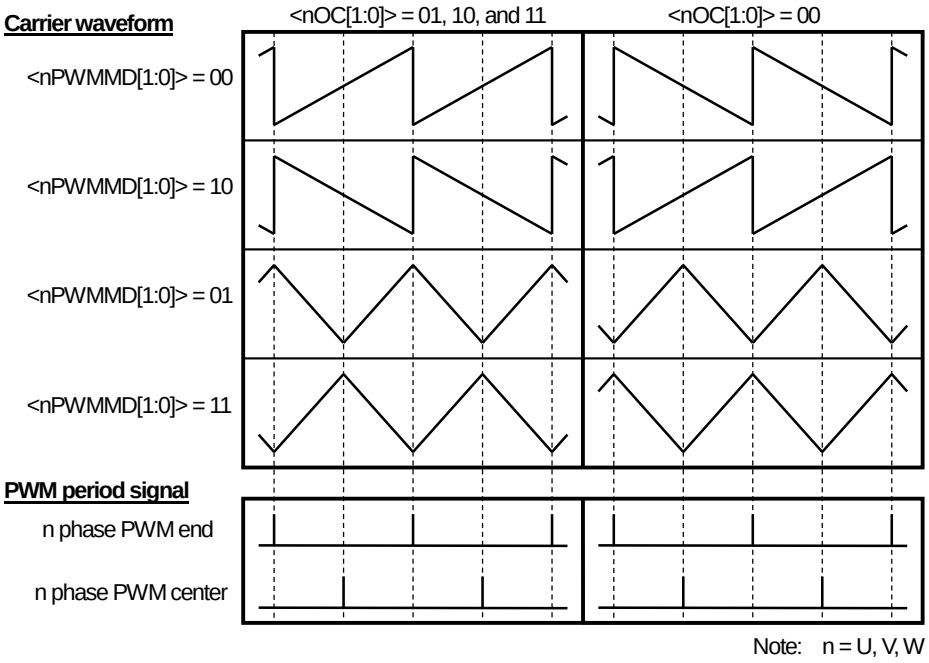

Figure 3.4 Converted carrier waveform output

3.2.2. 3 Phase PWM Wave Generation

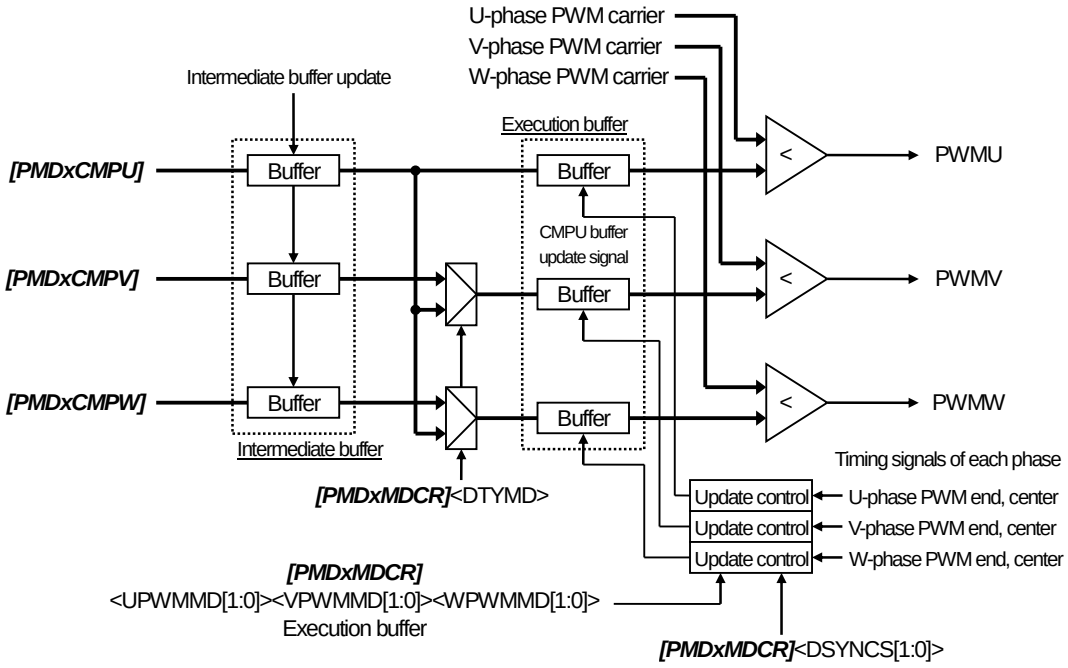

Figure 3.5 Generation circuit of 3-phase PWM waves

- Comparison function

  3 comparators compare the magnitudes of 3-phase PWM carries with the values in 3-phase PWM duty comparison registers (***[PMDxCMPU]***, ***[PMDxCMPV]***, and ***[PMDxCMPW]***) to generate PWM waves which have the expected duties.

  Each phase PWM duty comparison register has a triple-buffer structure. The value of each phase PWM duty comparison register is loaded to the execution buffer at a synchronous timing with the PWM period. The update at the half of the PWM period (Load every half period) can be selected (refer to Table 3.2). For the update of the intermediate buffer, refer to "3.7. Buffer Operation".

Table 3.2 Update control of the execution buffers in *[PMDxCMPU]*, *[PMDxCMPV]*, and *[PMDxCMPW]*

***[PMDxMDCR]* setting**		**Update timing**
<DSYNCS[1:0]>	**<INTPRD[1:0]>**	
00	01, 10, 11	Update at each PWM end
	00	Update at each PWM end and center
01	xx	Update at each PWM center
10	xx	Update at each PWM end
11	xx	Update at each PWM end and center

Note: xx: Don't care

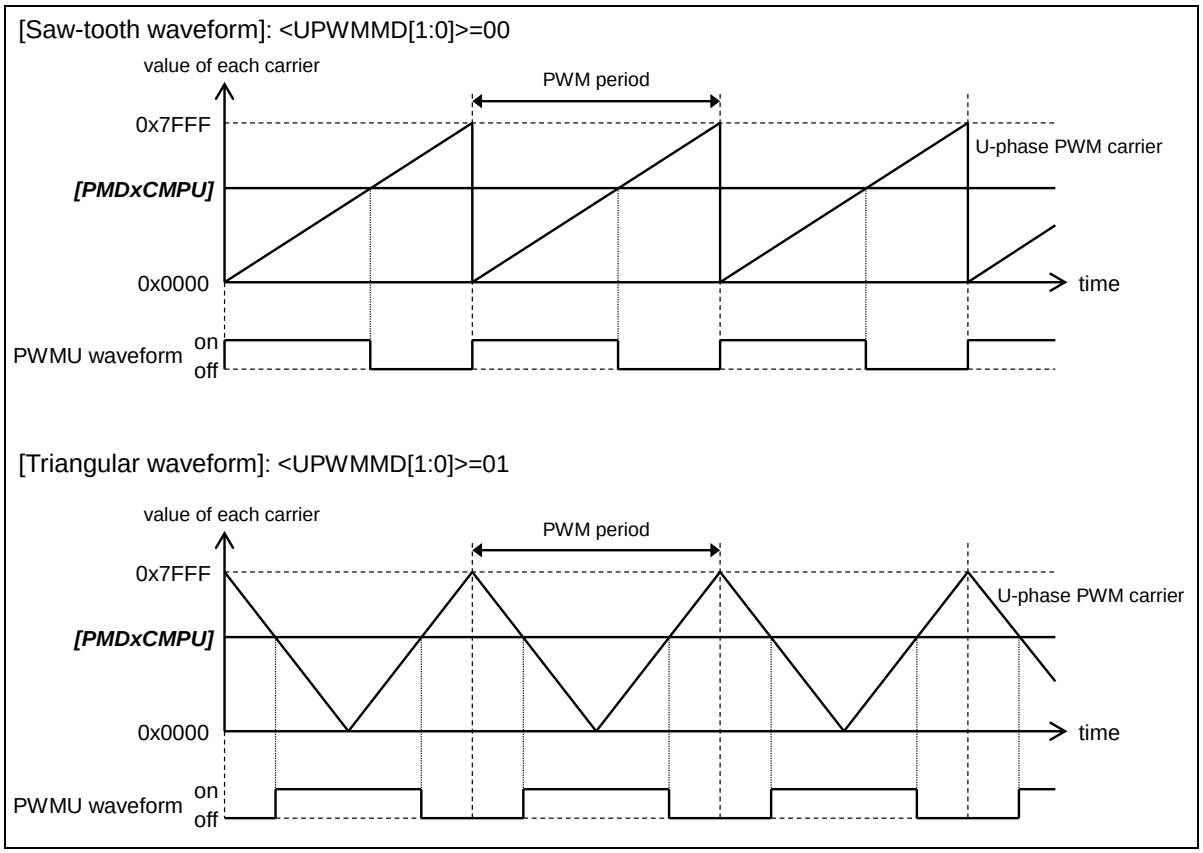

Figure 3.6 PWM waveform

- Waveform mode

  3-phase PWM waveforms can be generated in the following 2 modes by the duty mode selection ***[PMDxMDCR]***<DTYMD>.

  – 3-phase independent duty mode:

    3-phase PWM duty comparison registers are set to different values. Each PWM wave is generated independently. This mode is used to generate arbitrary driving waves such as sine waves.

  – 3-phase common duty mode:

    Only U-phase PWM duty comparison register is used. The register value controls all 3-phase PWM waves. These PWM waves become the same. This mode is used for the pulse control to drive a brushless DC motor.

- Interrupt procedure

  The pulse width modulation circuit generates a PWM interrupt request at a synchronous timing with the PWM period. The timing of the interrupt generation can be selected between U-phase PWM end and U-phase PWM center.

  The frequency of the PWM interrupt can be selected from every half of the PWM period, every PWM period, every second PWM period, and every fourth PWM period.

3.3. Conduction Control Circuit

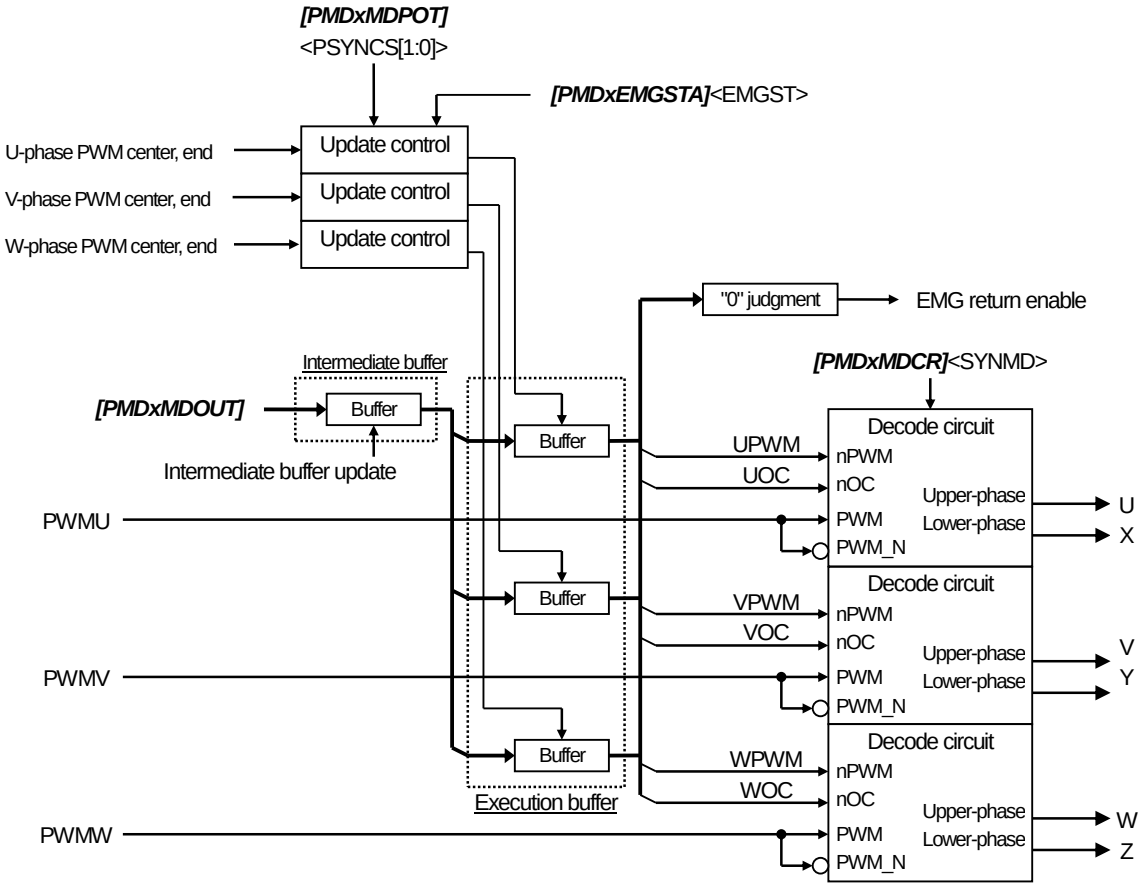

Figure 3.7 Conduction control circuit

The output ports are controlled by the settings of the PMD conduction control register ***[PMDxMDOUT]*** and the PMD output setting register ***[PMDxMDPOT]***. ***[PMDxMDOUT]*** has a triple-buffer structure. The update timing of its execution buffer can be selected between a synchronous timing with PWM period and an asynchronous one. And the update timing which is synchronous with the trigger input can also be set. The update timing is selected by ***[PMDxMDPOT]***<PSYNCS[1:0]>.

Each of 6 port outputs (Upper-phase output, UOx, VOx, and WOx, and lower-phase output, XOx, YOx, and ZOx) can be set separately to low active output and high active output by ***[PMDxMDPOT]***<POLH> and <POLL> (Refer to "3.5. Dead time Control Circuit"). And, each phase of U, V, and W can select between PWM output and high/low level output using ***[PMDxMDOUT]***<UPWM>, <VPWM>, and <WPWM>, respectively. When PWM output is selected, PWM wave is output, and when high/low output is selected, high level or low level is output. The selection of high or low is done by ***[PMDxMDOUT]***<UOC[1:0]>, <VOC[1:0]>, and <WOC[1:0]>. Table 3.3 shows the port outputs determined by the settings of the port output set by ***[PMDxMDOUT]*** and ***[PMDxMDPOT]***, and also by the setting of the port output mode set by PMD control register ***[PMDxMDCR]***.

Table 3.3 Decode circuit outputs according to *[PMDxMDOUT]* and *[PMDxMDCR]*<SYNTMD> setting

[PMDxMDCR]<SYNTMD> =0

		PWM output setting *[PMDxMDOUT]*<nPWM>			
		0: H/L output		1: PWM output	
		Upper-phase	Lower-phase	Upper-phase	Lower-phase
Conduction setting *[PMDxMDOUT]* <nOC[1:0]>	00	Low	Low	PWM	PWM_N
	01	Low	High	Low	PWM
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

[PMDxMDCR]<SYNTMD> =1

		PWM output setting *[PMDxMDOUT]*<nPWM>			
		0: H/L output		1: PWM output	
		Upper-phase	Lower-phase	Upper-phase	Lower-phase
Conduction setting *[PMDxMDOUT]* <nOC[1:0]>	00	Low	Low	PWM	PWM_N
	01	Low	High	Low	PWM_N
	10	High	Low	PWM	Low
	11	High	High	PWM	PWM_N

Note: n= U, V, W

3.4. Protection Control Circuit

The protection control circuit consists of a protection control unit and a protect output control unit.
The protection control unit consists of EMG protection control and OVV protection control circuits.

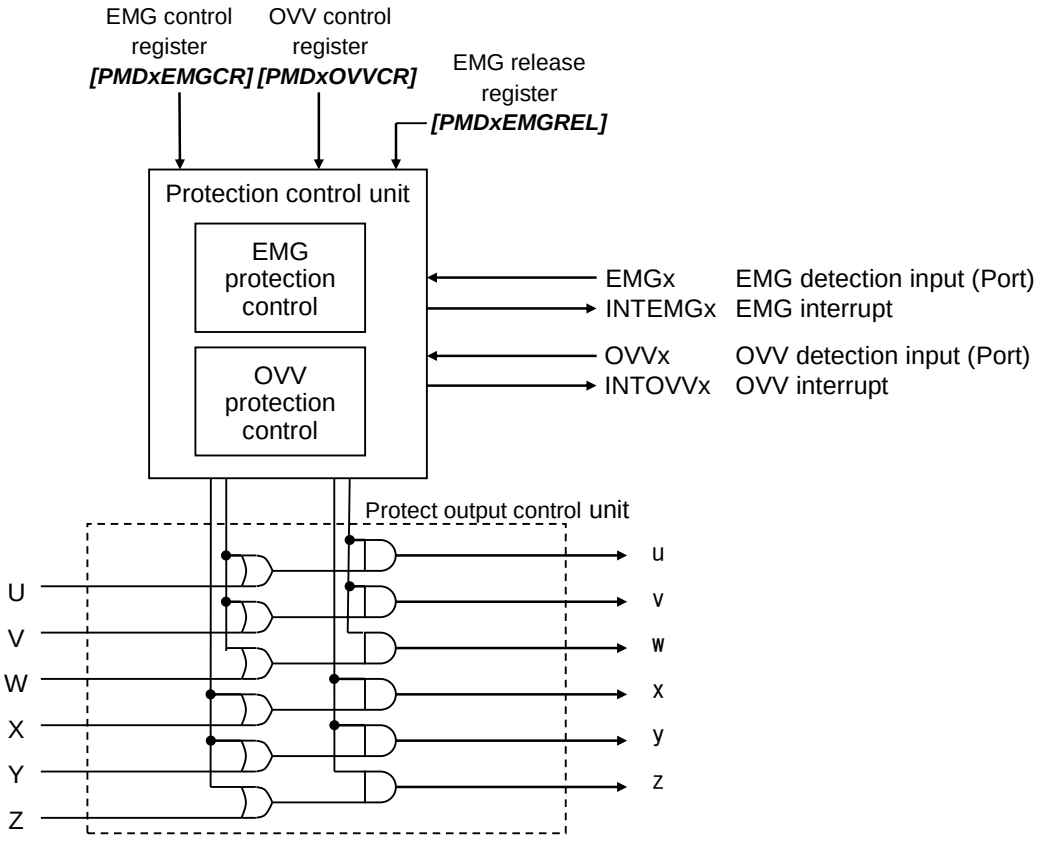

Figure 3.8 Protection control circuit

3.4.1. EMG Protection Control Circuit

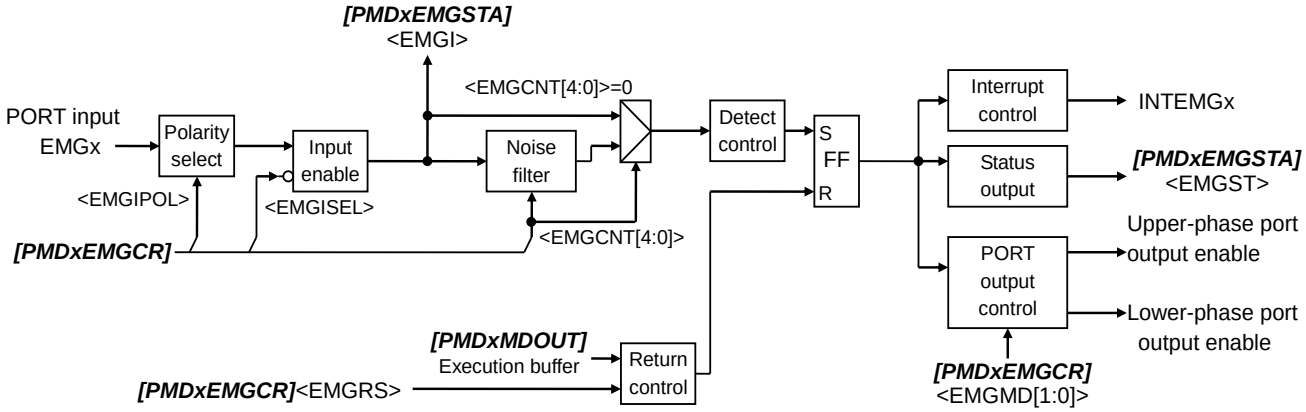

Figure 3.9 EMG protection control circuit

EMG protection control circuit is for emergency stop. The protection is enabled by ***[PMDxEMGCR]***<EMGEN> =1. When EMG input becomes active, the protection starts operating. The EMG protection is set by EMG control register ***[PMDxEMGCR]***.

Note: After reset, the EMG protection control circuit is enabled.

- EMG input

  EMGx pin is enabled / disabled as EMG input by ***[PMDxEMGCR]***<EMGISEL>. The active level is selected by ***[PMDxEMGCR]***<EMGIPOL> (EMGx input polarity selection).

  The noise filter is inserted in the EMG input. The noise detection time is selected with the EMG input detection time setting (***[PMDxEMGCR]***<EMGCNT[4:0]>). When <EMGCNT[4:0]> =00000 setting, the noise filter is bypassed.

  Note: When <EMGCNT[4:0]> or <EMGIPOL> is changed while EMG protection control circuit is enabled, it may become the protection state. Therefore, when these are changed, please execute "Return from the EMG protection".

- EMG protection operation

  When EMG input is active for a predetermined period (set by <EMGCNT[4:0]>), all 6 PWM outputs can be disabled immediately and EMG interrupt (INTEMGx) is generated. According to the setting of ***[PMDxEMGCR]***<EMGMD[1:0]>, the external output port status during protection operation is selected from all phase High-impedance, all lower-phase High-impedance / all upper-phase ON, all upper-phase High-impedance / all lower-phase ON.

  When ***[PMDxEMGSTA]***<EMGST> is "1", the device is in EMG protection state.

- Return from the EMG protection

  When all the port outputs are set to inactive (***[PMDxMDOUT]***<UPWM>, <VPWM>, <WPWM>, <UOC[1:0]>, <VOC[1:0]>, and <WOC[1:0]> are all "0") in EMG protection state and then ***[PMDxEMGCR]***<EMGRS> is set to "1", the device return from EMG protection state. When, however, EMG input is active, writing "1" to <EMGRS> is ignored. The return procedure should be done after EMG input becomes inactive. It is confirmed with reading ***[PMDxEMGSTA]***<EMGI>.

  Note: EMG return procedure after the reset deassertion

  EMGx pin is shared with a data port. The pin is the data port after the reset deassertion. EMG protection control circuit is enabled at the initial state. So, EMC protection may be active. The return from EMG protection state should be done as follows in the initial sequence:

  (1) EMG function should be selected by the port function register (***[PxFRn]***).
  (2) ***[PMDxEMGSTA]***<EMGI> should be read to confirm its value is "1".
  (3) ***[PMDxMDOUT]***<UPWM>, <VPWM>, <WPWM>, <UOC[1:0]>, <VOC[1:0]>, and <WOC[1:0]> should be set to "0" to set all port outputs to inactive state.
  (4) ***[PMDxEMGCR]***<EMGRS> should be set to "1" to return from EMG protection state.

- Disable of the EMG protection function

  In order to disable EMG function, EMG release register ***[PMDxEMGREL]*** should be set to "0x5A" and "0xA5" in order, then ***[PMDxEMGCR]***<EMGEN> should be set to "0". These 3 instructions should be executed continuously to prevent wrong disabling of the EMG protection control circuit.

3.4.2. OVV Protection Control Circuit

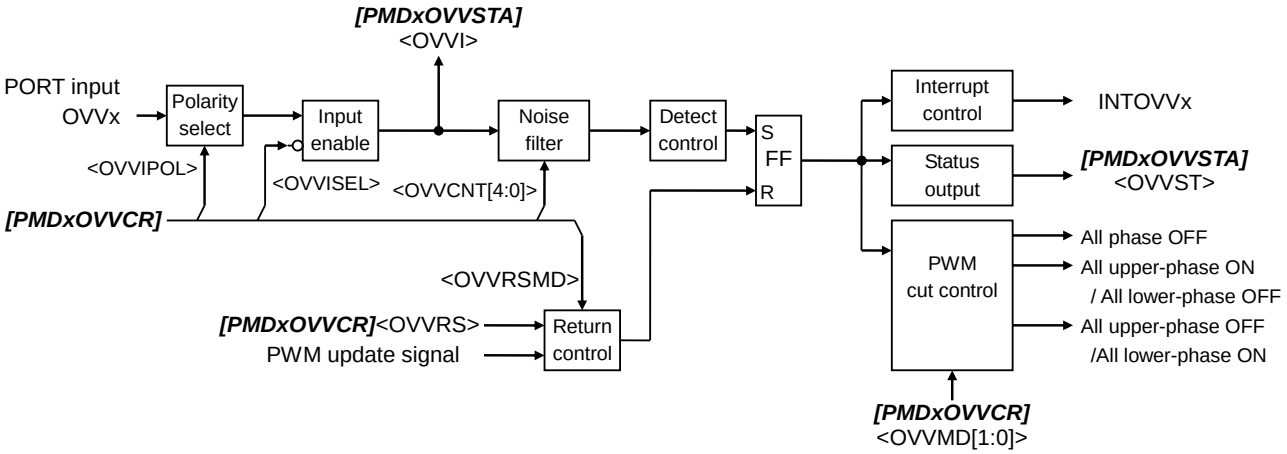

Figure 3.10 OVV protection control circuit

The OVV protection control circuit is enabled by ***[PMDxOVVCR]***<OVVEN> =1. When OVV input becomes active, the protection starts operating. This protection is set by OVV control register (***[PMDxOVVCR]***).

- OVV input

  OVVx pin is enabled / disabled as OVV input by ***[PMDxOVVCR]***<OVVISEL>. The active level is selected by <OVVIPOL> in OVVx input (Port) polarity selection register.

  The noise filter is inserted in the OVV input. The noise detection time is selected with the OVV input detection time setting (***[PMDxOVVCR]***<OVVCNT[4:0]>).

  Note: When <OVVCNT[4:0]> or <OVVIPOL> is changed while OVV protection control circuit is enabled, it may become the protection state. Therefore, when these are changed, please execute "Return from the OVV protection".

- OVV protection operation

  OVV protection control circuit fixes 6 port outputs in the conduction control block to high level or low level, when OVV input is active for a predetermined period (set by <OVVCNT[4:0]>). And OVV interrupt (INTOVVx) is generated. ***[PMDxOVVCR]***<OVVMD[1:0]> setting selects from all lower-phase OFF/all upper-phase ON, all upper-phase OFF/all lower-phase ON, and all phase OFF.

  When ***[PMDxOVVSTA]***<OVVST> is "1", the device is in OVV protection state.

- Return from the OVV protection

  When ***[PMDxOVVCR]***<OVVRS> is set to "1", the device returns from OVV protection state. When, however, OVV input is active, writing "1" to <OVVRS> is ignored. The return procedure should be done after OVV input becomes inactive. It is confirmed with reading ***[PMDxOVVSTA]***<OVVI>.

  When OVV return operation selection <OVVRSMD> =0, the auto return is enabled. After OVV input becomes inactive, the return is done at the synchronous timing with U-phase PWM period (the state of the port can be checked by reading ***[PMDxOVVSTA]***<OVVI>). The device returns automatically from OVV protection state at U-phase PWM end. When, however, half PWM period interrupt is set, the timing is the PWM end and center.

- Disable of the OVV protection control circuit

  In order to disable OVV function, EMG release register ***[PMDxEMGREL]*** should be set to "0x5A" and "0xA5" in order, then ***[PMDxOVVCR]***<OVVEN> should be set to "0". These 3 instructions should be executed continuously to prevent the OVV protection control circuit from being inadvertently disabled.

3.4.3. Protection control when using the debug tool

When using the debug tool, PMD output ports can be disabled when CPU is stopped by the debug halt. However, when the EMG occurs, port outputs are controlled depending on the setting of ***[PMDxEMGCR]***<EMGMD[1:0]>.

In the debug halt, whether the port output becomes High-impedance or PMD output is selected by ***[PMDxPORTMD]***<PORTMD[1:0]> setting.

3.5. Dead time Control Circuit

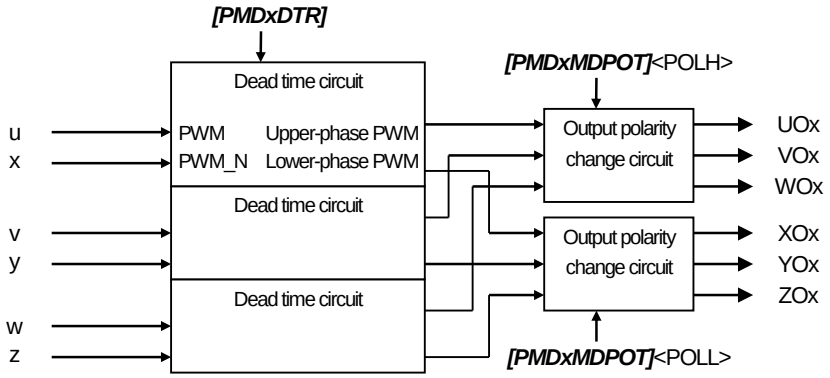

Figure 3.11 Dead time control circuit

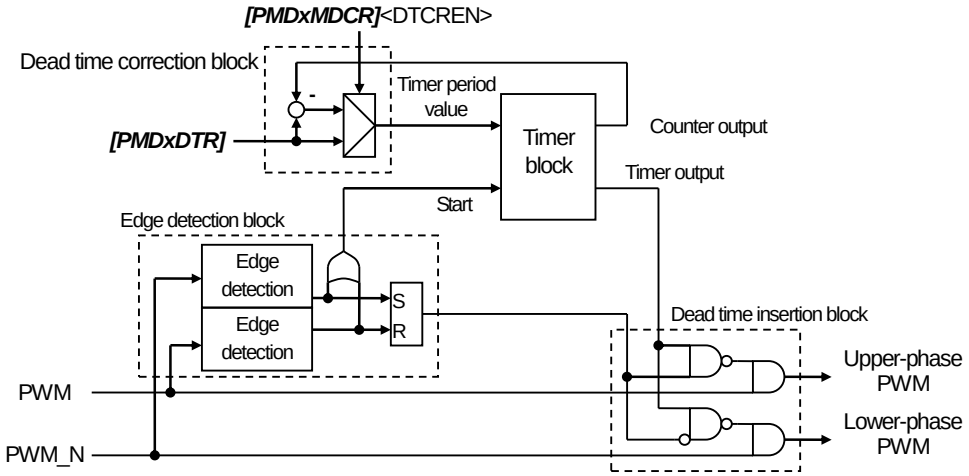

Figure 3.12 Dead time circuit

The dead time control circuit consists of dead time circuits and output polarity change circuits (refer to Figure 3.11). The dead time circuit includes an edge detection block, a timer block, a dead time insertion block, and a dead time correction block (refer to Figure 3.12).

The dead time circuit delays ON timing to prevent from the short-circuit between the upper-phase and the lower-phase for U, V, and W phases, when both the upper-phase and the lower-phase invert their signals at the same time. The unit of the delay time is 4/fsys (50 ns at 80 MHz, 10-bit resolution). The delay time is set to the dead time register ***[PMDxDTR]***.

The dead time correction block operates as follows: When ***[PMDxMDCR]***<DTCREN> is set to "1" and one of upper-phase PWM and lower-phase PWM has 0 ON time, the delay time of the other PWM is shortened. When PWM output changes to OFF during the dead time interval, the dead time correction function shortens the delay time of the opposite phase by the remaining dead time interval ("Dead time register setting value" - "ON interval"). That is, when upper-phase PWM output changes to OFF during the dead time interval, the delay time of lower-phase PWM is shortened. When lower-phase PWM output changes to OFF during the dead time interval, the delay time of upper-phase PWM is shortened. The delay time is corrected near 100% duty of upper-phase PWM or near 0% duty of lower-phase PWM, as shown in Figure 3.13.

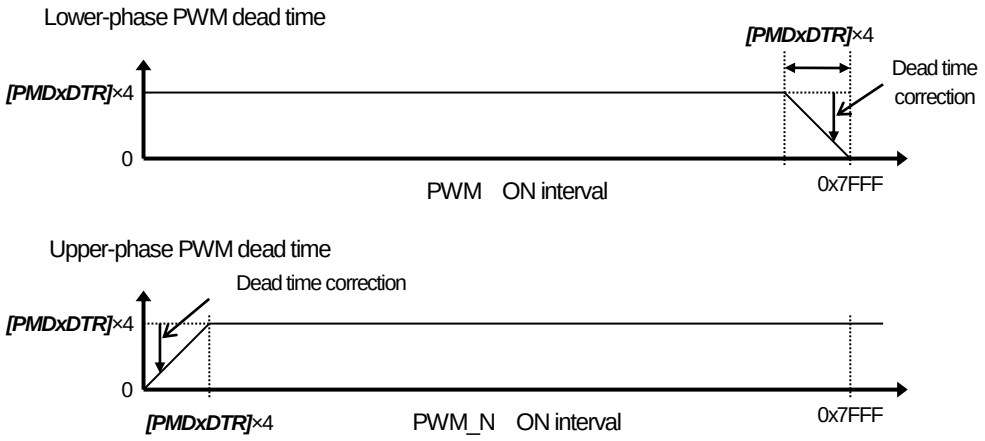

Figure 3.13 Dead time correction

The output polarity change circuit can select high active or low active for upper-phase output (UOx, VOx, and WOx) and lower-phase output (XOx, YOx, and ZOx) independently. The selection is done by PMD output setting register ***[PMDxMDPOT]***<POLH> and <POLL>, respectively.

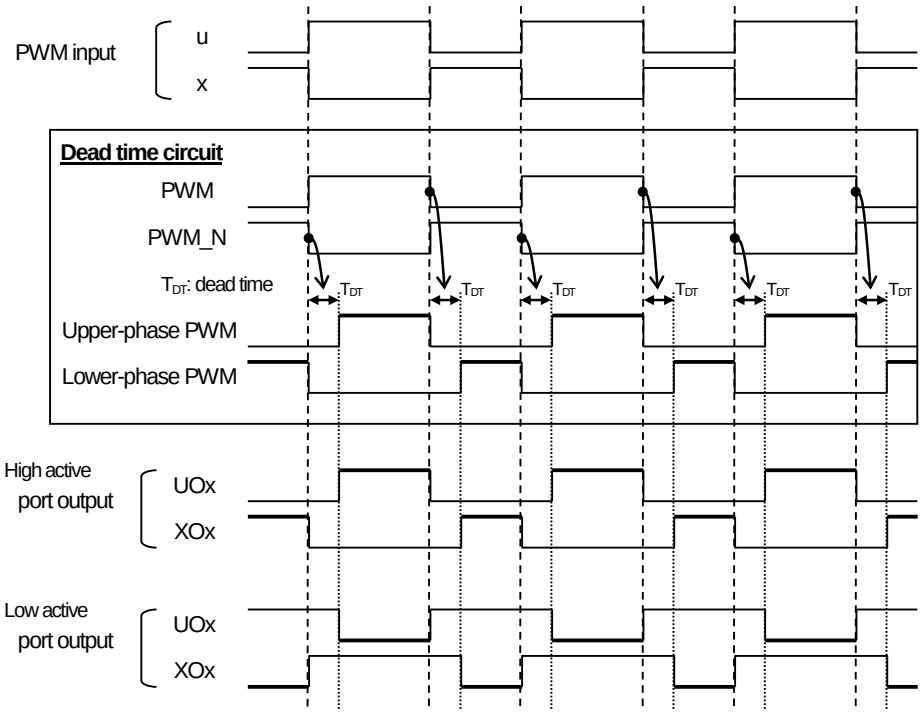

Figure 3.14 Waveform of dead time control circuit

3.6. Synchronous Trigger Generation Circuit

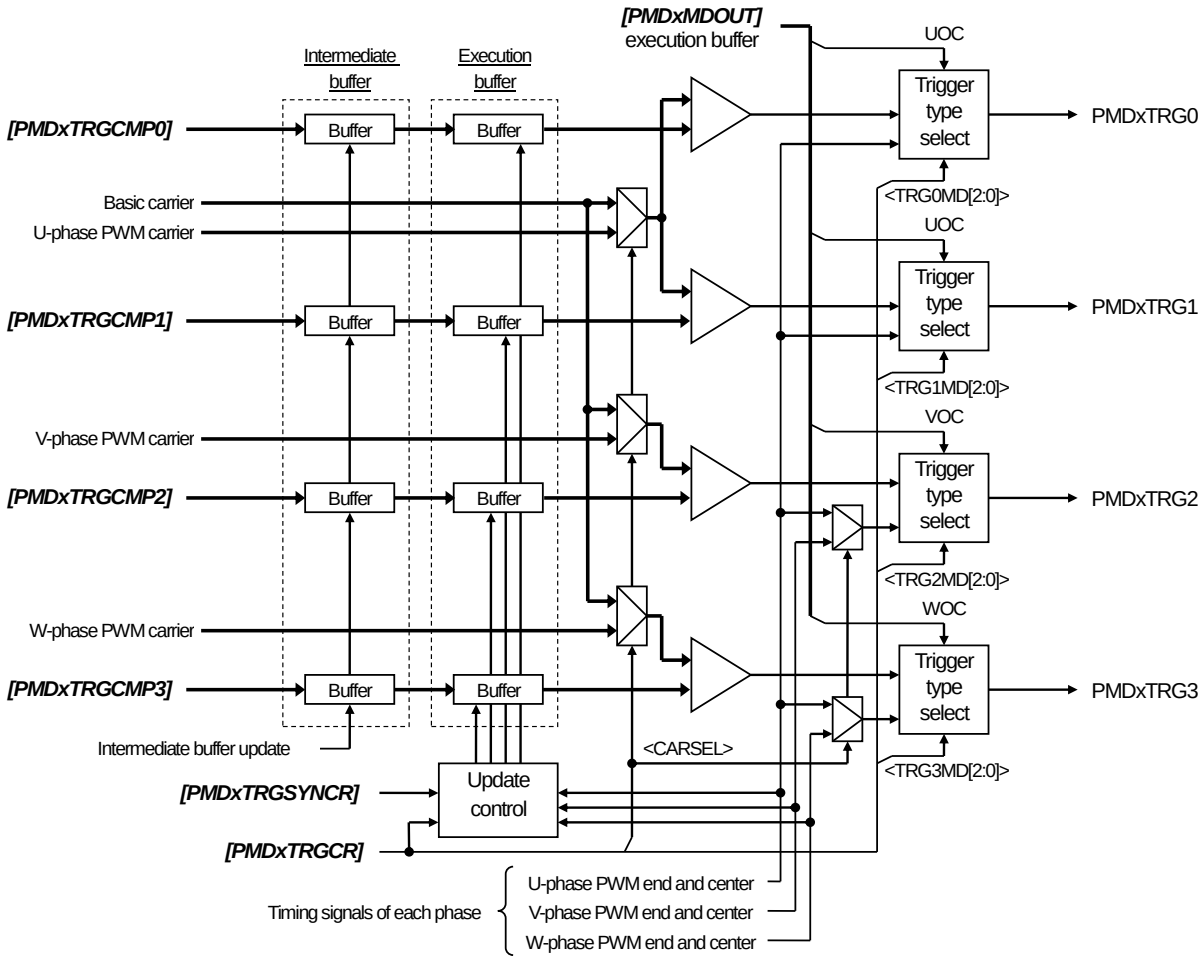

Figure 3.15 Synchronous trigger generation circuit

The synchronous trigger generation circuit generates 4 trigger signals (PMDxTRG0 to PMDxTRG3) which are synchronous with each phase PWM carrier and are used to sample ADC data.

The trigger timing can be selected from the followings:

(1) Coincidence in the first half of a triangular wave carrier (Note1)(Note2)
(2) Coincidence in the second half of a triangular wave carrier (Note1)(Note2)
(3) Coincidence in the first and second halves of a triangular wave carrier (Note1)(Note2)
(4) PWM end of the basic carrier or each phase carrier (Note2)(Note3)
(5) PWM center of the basic carrier or each phase carrier (Note2)(Note3)
(6) PWM center and end of the basic carrier or each phase carrier (Note2)(Note3)

Note1: Coincidence of the basic carrier or each phase carrier and ***[PMDxTRGCMPn]*** value.

Note2: When saw-tooth wave (***[PMDxMDCR]***<UPWMMD[1:0]>/<VPWMMD[1:0]>/<WPWMMD[1:0]> = 00, 10)

- There is no distinction between the first half and the second half.
- The trigger does not occur at the PWM center and it occurs at the PWM end.

Note3: When comparing the basic carrier, the trigger timing is PWM center / end timing of U-phase.

Trigger compare registers are triple-buffer configuration. The execution buffer update timing is shown in the table below. For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Table 3.4 Buffer update timing of Trigger comparison register

[PMDxTRGSYNCR] <TSYNCS[1:0]> Setting	*[PMDxTRGCR]* <TRGnMD[2:0]> Setting	*[PMDxTRGCMPn]* Register Buffer Update Timing
00	000	Immediate update
	001	Update at each phase PWM end (Note1)
	010	Update at each phase PWM center (Note1)(Note2)
	011	Update at each phase PWM end or center (Note1)(Note2)
	1xx	Immediate update
01	xxx	Update at each phase PWM center (Note1)(Note2)
10	xxx	Update at each phase PWM end (Note1)
11	xxx	Update at each phase PWM end or center (Note1)(Note2)

Note1: When comparing the basic carrier, the trigger timing is PWM center / end timing of U-phase.

Note2: When PWM carrier is a saw-tooth wave (***[PMDxMDCR]***<UPWMMD[1:0]>/ <VPWMMD[1:0]>/<WPWMMD[1:0]> = 00 or 10), the update is done at the PWM end.

Note3: xx, xxx: Don’t care

Note4: When ***[PMDxMDEN]***<PWMEN> =0, the immediate update is done regardless of the setting.

When the trigger output is enabled in EMG protection state, ***[PMDxTRGMD]***<EMGTGE> should be set to "1".

3.7. Buffer Operation

The buffer configuration of a register has a single-buffer, double-buffer, and triple-buffer.

[PMDxRATE] register is a double-buffer one. ***[PMDxMDOUT]***, ***[PMDxCMPU]***, ***[PMDxCMPV]***, ***[PMDxCMPW]***, ***[PMDxTRGCMP0]***, ***[PMDxTRGCMP1]***, ***[PMDxTRGCMP2]***, and ***[PMDxTRGCMP3]*** registers, and ***[PMDxMDCR]***<UPWMMD[1:0]>, <VPWMMD[1:0]>, and <WPWMMD[1:0]> have triple-buffer. The other registers are single-buffer ones. The double-buffer structure has a register stage and an execution buffer stage. And the triple-buffer structure has an intermediate buffer stage between the register stage and the execution buffer stage.

The register stage can be read or written.

The intermediate stage can be updated at the timing selected by ***[PMDxMBUFCR]***<BUFCTR[2:0]>. When <BUFCTR[2:0]> =000, the intermediate stage is bypassed.

The update timing of the execution buffer stage can be set per register independently. For the details of the setting, refer to each register description.

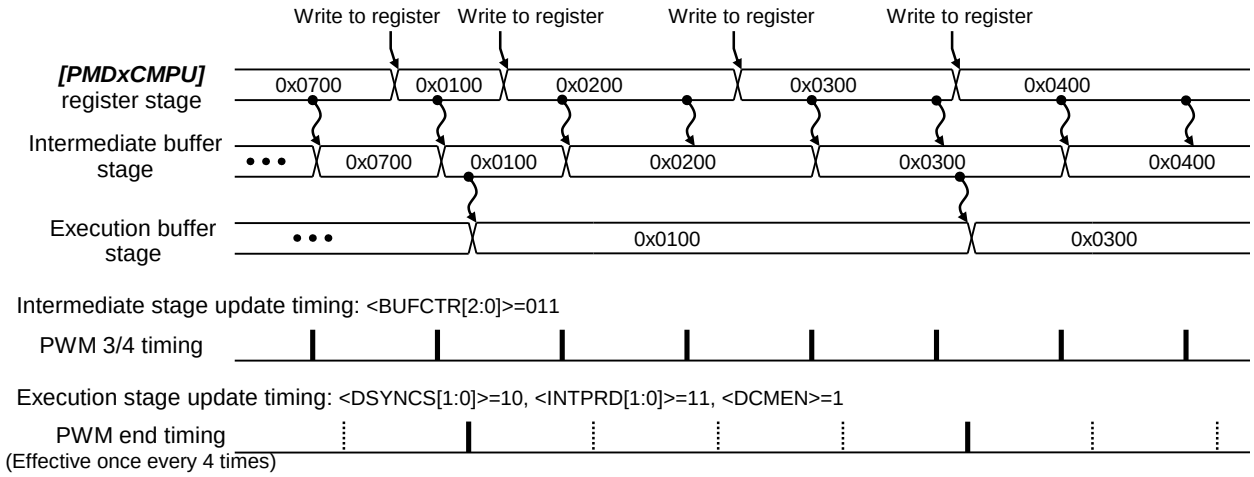

Figure 3.16 Triple-buffer update timing example of *[PMDxCMPU]* register

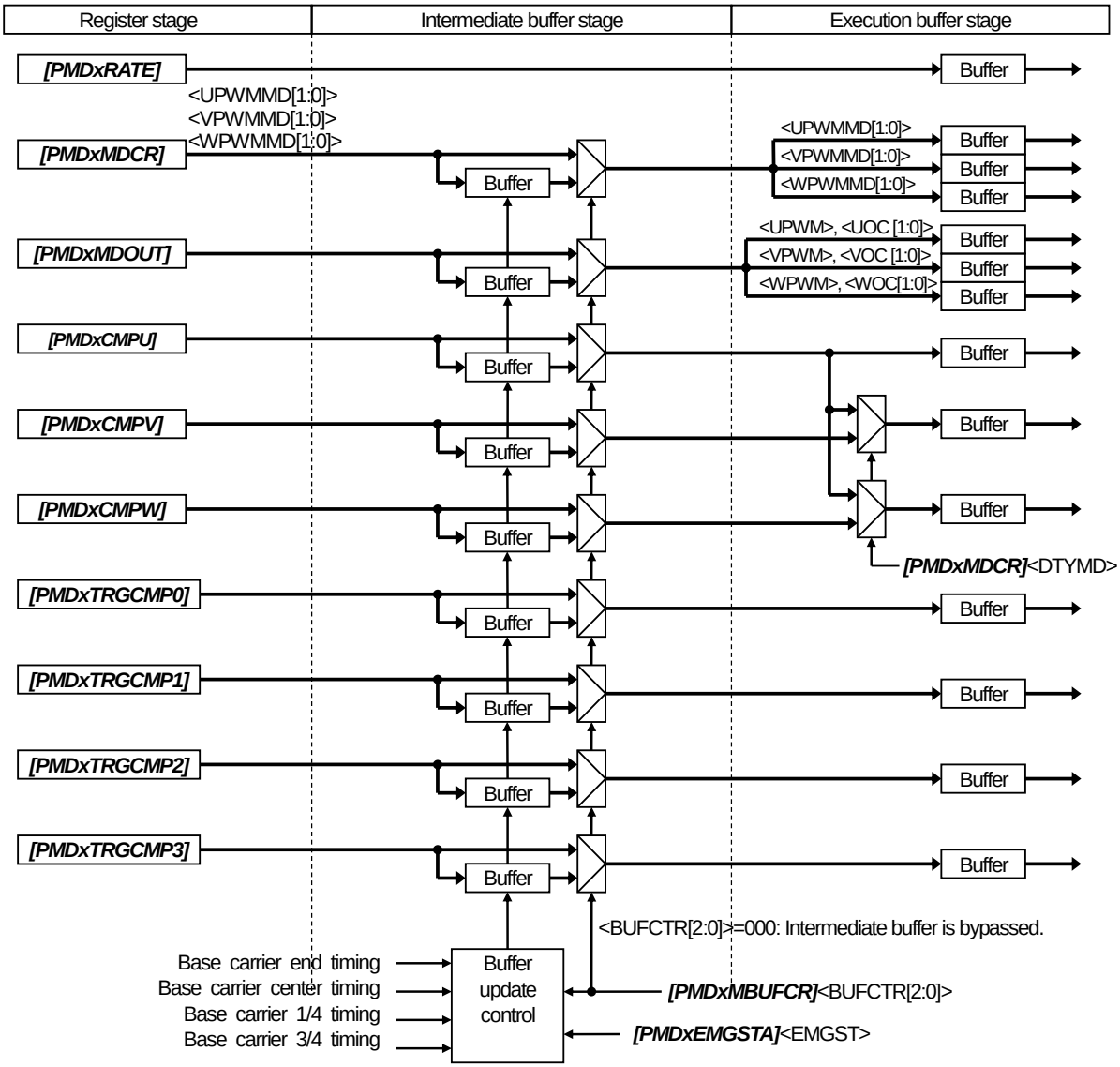

Figure 3.17 Register buffer configuration

3.8. Decimation of Execution Buffer Update Timing and Synchronous Trigger Output Timing

The update of the execution buffer and the trigger output usually occurs once in a PWM period. When the interrupt period is selected to two PWM periods or more, the update timing of the execution buffer and the ADC synchronous trigger output can be decimated.

When ***[PMDxMDCR]***<INTPRD[1:0]> = 10 or 11, the decimation control can be enabled by the setting ***[PMDxMDCR]*** <DCMEN> to "1".

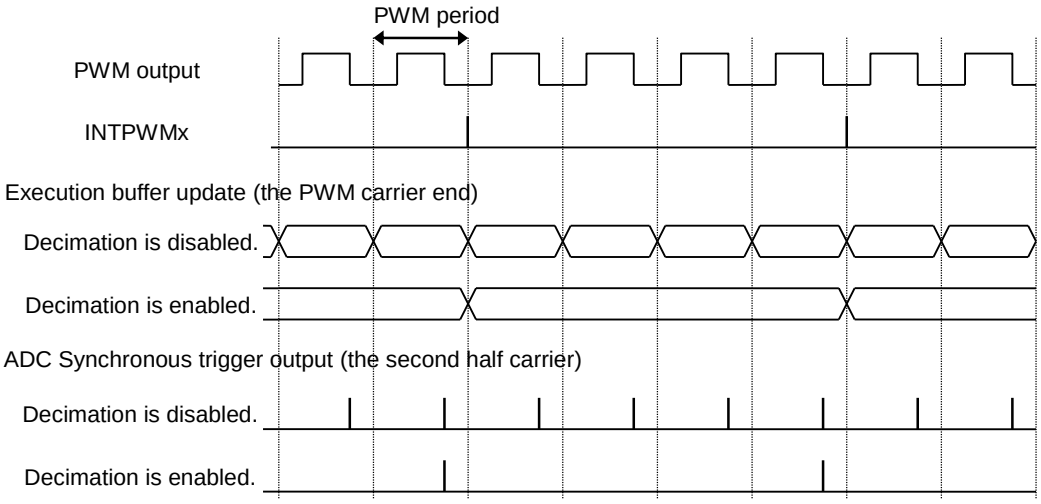

Figure 3.18 Timing example of Decimation control (in the case of <INTPRD[1:0]> =11)

4. Registers

4.1. List of Registers

The control registers and their addresses are shown as follows.

Peripheral Function		Channel/Unit	Base Address		
			TYPE1	TYPE2	TYPE3
Advanced programmable motor control circuit	A-PMD	ch0	0x400F6000	0x400E9000	0x40089000
		ch1	0x400F6100	0x400E9400	0x40089400
		ch2	0x400F6200	0x400E9800	0x40089800
		ch3	0x400F6300	0x400E9C00	0x40089C00

Note: The channel/unit and base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register Name		Address (Base+)
PMD enable register	***[PMDxMDEN]***	0x0000
Port output mode register	***[PMDxPORTMD]***	0x0004
PMD control register	***[PMDxMDCR]***	0x0008
PWM carrier status register	***[PMDxCARSTA]***	0x000C
Basic carrier register	***[PMDxBCARI]***	0x0010
PWM frequency register	***[PMDxRATE]***	0x0014
PWM duty comparison U register	***[PMDxCMPU]***	0x0018
PWM duty comparison V register	***[PMDxCMPV]***	0x001C
PWM duty comparison W register	***[PMDxCMPW]***	0x0020
Reserved	-	0x0024
PMD conduction control register	***[PMDxMDOUT]***	0x0028
PMD output setting register	***[PMDxMDPOT]***	0x002C
EMG release register	***[PMDxEMGREL]***	0x0030
EMG control register	***[PMDxEMGCR]***	0x0034
EMG status register	***[PMDxEMGSTA]***	0x0038
OVV control register	***[PMDxOVVCR]***	0x003C
OVV status register	***[PMDxOVVSTA]***	0x0040
Dead time register	***[PMDxDTR]***	0x0044
Trigger comparison 0 register	***[PMDxTRGCMP0]***	0x0048
Trigger comparison 1 register	***[PMDxTRGCMP1]***	0x004C
Trigger comparison 2 register	***[PMDxTRGCMP2]***	0x0050
Trigger comparison 3 register	***[PMDxTRGCMP3]***	0x0054
Trigger control register	***[PMDxTRGCR]***	0x0058
Trigger output mode setting register	***[PMDxTRGMD]***	0x005C
Reserved	-	0x0060
Trigger update timing setting register	***[PMDxTRGSYNCR]***	0x0064
V-phase phase difference register	***[PMDxVPWMPH]***	0x0068
W-phase phase difference register	***[PMDxWPWMPH]***	0x006C
Intermediate buffer control register	***[PMDxMBUFCR]***	0x0070
Reserved	-	0x0074
Reserved	-	0x0078

4.2. Details of Registers

4.2.1. *[PMDxMDEN]* (PMD enable register)

Bit	Bit Symbol	After Reset	Type	Description
31:1	-	0	R	Read as "0"
0	PWMEN	0	R/W	Wave composition function is enabled or disabled. 0: Disabled. 1: Enabled.

Note1: When the port is set to the function output (PWM output), the port output is disabled (High-impedance) at <PWMEN> =0. For the input/output port setting, refer to "Input/Output Ports" of the reference manual.

Note2: <PWMEN> =1 should be set after initial settings, like an output polarity, other than <PWMEN> are set.

4.2.2. *[PMDxPORTMD]* (Port output mode register)

Bit	Bit Symbol	After Reset	Type	Description
31:2	-	0	R	Read as "0"
1:0	PORTMD[1:0]	00	R/W	Setting of the port control at debug halt 00: Upper-phase High-impedance / Lower-phase High-impedance 01: Upper-phase High-impedance / Lower-phase PMD output 10: Upper-phase PMD output / Lower-phase High-impedance 11: Upper-phase PMD output / Lower-phase PMD output This field sets the port outputs of upper-phase (UOx/VOx/WOx) and lower-phase (XOx/YOx/ZOx) at occurrence of debug halt while the port is set to the function output (PWM output). At occurrence of debug halt while "High-impedance" is selected, the port output is disabled (High-impedance). Otherwise, the output follows PMD output.

Note1: The output is disabled (High-impedance) at ***[PMDxMDEN]***<PWMEN> =0, regardless of <PORTMD[1:0]> setting.

Note2: Depending on the setting of ***[PMDxEMGCR]***<EMGMD[1:0]>, port output control is also performed during EMG protection.

Note3: For the input/output port setting, refer to "Input/Output Ports" of the reference manual.

4.2.3. *[PMDxMDCR]* (PMD control register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0"
15:14	WPWMMD[1:0]	00	R/W	W-phase PWM carrier wave selection (Note1) (Note2) (Note3) (Note4) 00: Saw-tooth wave (Edge PWM) 01: Triangle wave (Center PWM) 10: Reversed saw-tooth wave (Edge PWM) 11: Reversed triangular wave (Center PWM)
13:12	VPWMMD[1:0]	00	R/W	V-phase PWM carrier wave selection (Note1) (Note2) (Note3) (Note4) 00: Saw-tooth wave (Edge PWM) 01: Triangle wave (Center PWM) 10: Reversed saw-tooth wave (Edge PWM) 11: Reversed triangular wave (Center PWM)
11:10	UPWMMD[1:0]	00	R/W	U-phase PWM carrier wave selection (Note1) (Note2) (Note3) (Note4) 00: Saw-tooth wave (Edge PWM) 01: Triangle wave (Center PWM) 10: Reversed saw-tooth wave (Edge PWM) 11: Reversed triangular wave (Center PWM)
9:8	DSYNCS[1:0]	00	R/W	Update timing of the execution buffer in PWM duty comparison register (Note6) (Note8) 00: The timing depends on the interrupt period setting <INTPRD[1:0]> (Refer to Table 3.2.). When the half period interrupt request is selected (<INTPRD[1:0]> =00), the update is done at each phase PWM end and center. Otherwise, at PWM end. 01: Update at each phase PWM center. 10: Update at each phase PWM end. 11: Update at each phase PWM end and center.
7	DTCREN	0	R/W	Dead time correction enable 0: Disabled. 1: Enabled.
6	DCMEN	0	R/W	Decimation control of the execution buffer update and the synchronous trigger output When 2 period interrupt or 4 period interrupt is selected (<INTPRD[1:0]> = 10 or 11), the decimation control is enabled for the update timing of the execution buffer and the synchronous trigger output. 0: Disabled. 1: Enabled. The target buffers are ***[PMDxCMPU]***/***[PMDxCMPV]***/***[PMDxCMPW]***, ***[PMDxTRGCMP0]***/***[PMDxTRGCMP1]***/***[PMDxTRGCMP2]***/ ***[PMDxTRGCMP3]***, ***[PMDxMDOUT]***, and ***[PMDxMDCR]***<UPWMMD[1:0]>/<VPWMMD[1:0]>/<WPWMMD[1:0]>.
5	SYNTMD	0	R/W	Port output mode setting This bit controls the decode circuit output with the combination of ***[PMDxMDOUT]***<UOC[1:0]>/<VOC[1:0]>/<WOC[1:0]>/<UPWM>/ <VPWM>/<WPWM>, and <SYNTMD> (Refer to Table 3.3). The output polarity of the port output can be selected by ***[PMDxMDPOT]***<POLH>/<POLL>.
4	DTYMD	0	R/W	Duty mode selection 0: Common for 3 phases. 1: Independent for each phase. The duty setting is selected between the independent setting (***[PMDxCMPU]***/***[PMDxCMPV]***/***[PMDxCMPW]***) or the common setting for 3 phases (***[PMDxCMPU]***).

Bit	Bit Symbol	After Reset	Type	Description
3	PINT	0	R/W	PWM interrupt request timing selection (Note6) (Note7) 0: Interrupt request is generated at U-phase PWM center. 1: Interrupt request is generated at U-phase PWM end.
2:1	INTPRD[1:0]	00	R/W	PWM interrupt request period selection 00: Request at every PWM half period (Note5) 01: Request at every PWM 1 period 10: Request at every PWM 2 periods 11: Request at every PWM 4 periods The frequency of PWM interrupt request is selected from half PWM period, 1 PWM period, 2 PWM periods, and 4 PWM periods. Execution buffer update timing and trigger output can be decimated out according to interrupt request period selection. (Refer to "3.8. Decimation of Execution Buffer Update Timing and Synchronous Trigger Output Timing".)
0	-	0	R	Read as "0"

Note1: The update can be done while PWM counter is operating owing to the triple-buffer structure.

Note2: The update timing of the execution buffer is selected by ***[PMDxMDPOT]***<PSYNCS[1:0]>.

Note3: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note4: When this field is read, the value of the register stage (the data set through the bus) returns.

Note5: It is valid when the triangular wave carrier is selected (<UPWMMD[1:0]>/<VPWMMD[1:0]>/<WPWMMD[1:0]> = 01, 11).

Note6: When the saw-tooth wave carrier is selected (<UPWMMD[1:0]>/<VPWMMD[1:0]>/<WPWMMD[1:0]> = 00, 10), the update is done at the PWM end, regardless of the setting.

Note7: When the interrupt period is a half period (<INTPRD[1:0]> =00), the update is done at both the PWM end and center.

Note8: When ***[PMDxMDEN]***<PWMEN> =0, the asynchronous update is done regardless of the setting.

4.2.4. *[PMDxCARSTA]* (PWM carrier status register)

Bit	Bit Symbol	After Reset	Type	Description
31:3	-	0	R	Read as "0"
2	PWMWST	0	R	W-phase PWM carrier state 0: First half W-phase PWM period 1: Second half W-phase PWM period
1	PWMVST	0	R	V-phase PWM carrier state 0: First half V-phase PWM period 1: Second half V-phase PWM period
0	PWMUST	0	R	U-phase PWM carrier state 0: First half U-phase PWM period 1: Second half U-phase PWM period

4.2.5. *[PMDxBCARI]* (Basic carrier register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	BCARI[14:0]	0x0000	R	Read of the basic carrier Counter value resolution is 1/fsys (12.5 ns at fsys =80 MHz). The carrier value at PMD disable (***[PMDxMDEN]***<PWMEN> =0) is ***[PMDxRATE]*** /2^{10}.

4.2.6. *[PMDxRATE]* (PWM frequency register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	RATE[14:0]	0x0000	R/W	PWM frequency setting RATE ≥ 0x0010 PWM frequency = fsys x <RATE[14:0]> value / 2^{24} The setting value is calculated with the following formula: (PWM frequency) / fsys x 2^{24}

Note1: When a value less than "0x0010" is set, it is automatically replaced with "0x0010" (the register stores the setting value).

Note2: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note3: ***[PMDxRATE]*** register can be updated while the PWM counter is operating, because it has a double-buffer structure.

Note4: The update timing of the execution buffer is the basic carrier end timing. When, however, ***[PMDxMDEN]***<PWMEN> =0 or ***[PMDxMDPOT]***<PSYNCS[1:0]> =00, the update is done at any time.

Note5: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.7. PWM duty comparison register

4.2.7.1. *[PMDxCMPU]* (PWM duty comparison U register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0"
15:0	CMPU[15:0]	0x0000	R/W	U-phase PWM duty ratio setting 0x0000 to 0x8000 Determines U-phase PWM duty ratio. U-phase PWM carrier is compared with the execution buffer value to output the PWM which has the setting duty ratio.

Note1: For <CMPU[15:0]> ≥ 0x8000, the duty ratio is 100 %.

Note2: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note3: ***[PMDxCMPU]*** register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note4: For the update timing of the execution buffer, refer to "Table 3.2 Update control of the execution buffers in ***[PMDxCMPU]***, ***[PMDxCMPV]***, and ***[PMDxCMPW]***".

Note5: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note6: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.7.2. *[PMDxCMPV]* (PWM duty comparison V register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0"
15:0	CMPV[15:0]	0x0000	R/W	V-phase PWM duty ratio setting 0x0000 to 0x8000 Determines V-phase PWM duty ratio. V-phase PWM carrier is compared with the execution buffer value to output the PWM which has the setting duty ratio.

Note1: For <CMPV[15:0]> ≥ 0x8000, the duty ratio is 100 %.

Note2: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note3: ***[PMDxCMPV]*** register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note4: For the update timing of the execution buffer, refer to "Table 3.2 Update control of the execution buffers in ***[PMDxCMPU]***, ***[PMDxCMPV]***, and ***[PMDxCMPW]***".

Note5: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note6: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.7.3. *[PMDxCMPW]* (PWM duty comparison W register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0"
15:0	CMPW[15:0]	0x0000	R/W	W-phase PWM duty ratio setting 0x0000 to 0x8000 Determines W-phase PWM duty ratio. W-phase PWM carrier is compared with the execution buffer value to output the PWM which has the setting duty ratio.

Note1: For <CMPW[15:0]> ≥ 0x8000, the duty ratio is 100 %.

Note2: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note3: ***[PMDxCMPW]*** register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note4: For the update timing of the execution buffer, refer to "Table 3.2 Update control of the execution buffers in ***[PMDxCMPU]***, ***[PMDxCMPV]***, and ***[PMDxCMPW]***".

Note5: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note6: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.8. PWM carrier phase difference register

4.2.8.1. *[PMDxVPWMPH]* (V-phase phase difference register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	VPWMPH[14:0]	0x0000	R/W	V-phase PWM carrier phase difference setting 0x0000 to 0x7FFF The phase difference from the basic carrier is set.

Note: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

4.2.8.2. *[PMDxWPWMPH]* (W-phase phase difference register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	WPWMPH[14:0]	0x0000	R/W	W-phase PWM carrier phase difference setting 0x0000 to 0x7FFF The phase difference from the basic carrier is set.

Note: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

4.2.9. *[PMDxMDPOT]* (PMD output setting register)

Bit	Bit Symbol	After Reset	Type	Description
31:10	-	0	R	Read as "0"
9:8	-	00	R/W	Write as "00"
7:4	-	0	R	Read as "0"
3	POLH	0	R/W	Selection of the output polarity of the upper-phase outputs (UOx, VOx, and WOx). 0: Low active 1: High active
2	POLL	0	R/W	Selection of the output polarity of the lower-phase outputs (XOx, YOx, and ZOx). 0: Low active 1: High active
1:0	PSYNCS[1:0]	00	R/W	Selection of the update timing of the execution buffer in ***[PMDxMDOUT]*** and ***[PMDxMDCR]***<UPWMMD[1:0]>/<VPWMMD[1:0]>/<WPWMMD[1:0]>. 00: Asynchronous with PWM 01: Each phase PWM center 10: Each phase PWM end 11: Each phase PWM end and center The update timing of the conduction control register execution buffer is selected. (Note2)(Note3)

Note1: This register should be set during ***[PMDxMDEN]***<PWMEN> =0.

Note2: When PMD disable (***[PMDxMDEN]***<PWMEN> =0) or EMG protection state, the update timing is an asynchronous one regardless of the setting.

Note3: When PWM carrier is a saw-tooth wave (***[PMDxMDCR]***<UPWMMD[1:0]>/<VPWMMD[1:0]>/<WPWMMD[1:0]> = 00 or 10), setting except "00" is PWM end update.

4.2.10. *[PMDxMDOUT]* (PMD conduction control register)

Bit	Bit Symbol	After Reset	Type	Description
31:11	-	0	R	Read as "0"
10	WPWM	0	R/W	W-phase PWM output setting 0: H/L output 1: PWM output The decode circuit output is controlled by the combination of this bit, <WOC[1:0]>, <WPWM>, and ***[PMDxMDCR]***<SYNTMD> (Refer to Table 3.3.). The output polarity of the port output can be selected with ***[PMDxMDPOT]***<POLH>/<POLL>.
9	VPWM	0	R/W	V-phase PWM output setting 0: H/L output 1: PWM output The decode circuit output is controlled by the combination of this bit, <VOC[1:0]>, <VPWM>, and ***[PMDxMDCR]***<SYNTMD> (Refer to Table 3.3.). The output polarity of the port output can be selected with ***[PMDxMDPOT]***<POLH>/<POLL>.
8	UPWM	0	R/W	U-phase PWM output setting 0: H/L output 1: PWM output The decode circuit output is controlled by the combination of this bit, <UOC[1:0]>, <UPWM>, and ***[PMDxMDCR]***<SYNTMD> (Refer to Table 3.3.). The output polarity of the port output can be selected with ***[PMDxMDPOT]***<POLH>/<POLL>.
7:6	-	0	R	Read as "0"
5:4	WOC[1:0]	00	R/W	W-phase conduction control setting The decode circuit output is controlled by the combination of this bit, <WOC[1:0]>, <WPWM>, and ***[PMDxMDCR]***<SYNTMD> (Refer to Table 3.3.). The output polarity of the port output can be selected with ***[PMDxMDPOT]***<POLH>/<POLL>. When <WOC[1:0]> =00, W-phase carrier wave is reversed.
3:2	VOC[1:0]	00	R/W	V-phase conduction control setting The decode circuit output is controlled by the combination of this bit, <VOC[1:0]>, <VPWM>, and ***[PMDxMDCR]***<SYNTMD> (Refer to Table 3.3.). The output polarity of the port output can be selected with ***[PMDxMDPOT]***<POLH>/<POLL>. When <VOC[1:0]> =00, V-phase carrier wave is reversed.
1:0	UOC[1:0]	00	R/W	U-phase conduction control setting The decode circuit output is controlled by the combination of this bit, <UOC[1:0]>, <UPWM>, and ***[PMDxMDCR]***<SYNTMD> (Refer to Table 3.3.). The output polarity of the port output can be selected with ***[PMDxMDPOT]***<POLH>/<POLL>. When <UOC[1:0]> =00, U-phase carrier wave is reversed.

Note1: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note2: The conduction control register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note3: The update timing of the execution buffer is selected by ***[PMDxMDPOT]***<PSYNCS[1:0]>.

Note4: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note5: When this register is read, the value of the register stage (the data set through the bus) returns.

4.2.11. *[PMDxEMGCR]* (EMG control register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0"
15:13	-	000	R/W	Write as "000"
12:8	EMGCNT[4:0]	00000	R/W	EMG input detection time (Note1) 00000 to 11111 (When "00000" is set, the noise filter is bypassed.) The noise reduction time is set for detected abnormal input signal. The noise reduction time is calculated with the following formula: <EMGCNT[4:0]> × 16/fsys
7	EMGIPOL	0	R/W	EMGx pin polarity selection (Note1) 0: Low active 1: High active
6	-	0	R	Read as "0"
5	INHEN	1	R/W	PMD enable or disable in Debug halt 0: Disabled. 1: Enabled (Initial state). When debug halt signal is input, this bit selects either to stop PMD, or not.
4:3	EMGMD[1:0]	11	R/W	EMG protection mode selection (Note2) 00: All phase High-impedance 01: All upper-phase ON/All lower-phase High-impedance 10: All upper-phase High-impedance/All lower-phase ON 11: All phase High-impedance Note: ON: PWM output continues. This field sets the port outputs of the upper-phase (UOx, VOx, and WOx) and the lower-phase (XOx, YOx, and ZOx).
2	EMGISEL	0	R/W	EMGx pin input disable 0: Port input is enabled. 1: Port input is disabled. EMGx pin input signal is disabled to input the protection control circuit.
1	EMGRS	0	W	Return from EMG protection state 0: Don't care. 1: Return from the protection state. ***[PMDxMDOUT]*** register should be set to "0x000". Then, ***[PMDxEMGSTA]***<EMGI> becomes "1". When <EMGRS> is set to "1", the device exits EMG protection state. Read as "0".
0	EMGEN	1	R/W	EMG protection control circuit enable or disable setting 0: Disabled. 1: Enabled (Initial state). When EMG protection control circuit is disabled, EMG release register ***[PMDxEMGREL]*** should be set to "0x5A" and "0xA5" in order, then <EMGEN> should be set to "0". (3 instructions should be executed continuously.)

Note1: When <EMGCNT[4:0]> or <EMGIPOL> is changed while EMG protection control circuit is enabled, EMG protection may be activated. Therefore, when these are changed, please return from the EMG protection state by the following procedure.

(1) ***[PMDxEMGSTA]***<EMGI> should be read to confirm its value is "1".

(2) ***[PMDxMDOUT]***<UPWM>, <VPWM>, <WPWM>, <UOC[1:0]>, <VOC[1:0]>, and <WOC[1:0]> should be set to "0" to set all port outputs to inactive state.

(3) ***[PMDxEMGCR]***<EMGRS> should be set to "1" to exit EMG protection**.**

Note2: <EMGMD[1:0]> protection mode setting is prioritized when OVV and EMG occur at the same time.

4.2.12. *[PMDxEMGSTA]* (EMG status register)

Bit	Bit Symbol	After Reset	Type	Description
31:2	-	0	R	Read as "0"
1	EMGI	Undefined	R	EMG input state 0: Active input. 1: Inactive input. When an active signal among the enabled EMG input signals is input, this bit is set to “0”.
0	EMGST	0	R	EMG protection state 0: Normal operation 1: Protection state EMG protection status can be checked by reading this bit.

4.2.13. *[PMDxEMGREL]* (EMG release register)

Bit	Bit Symbol	After Reset	Type	Description
31:8	-	0	R	Read as "0"
7:0	EMGREL[7:0]	0x00	W	EMG/OVV disable code The setting of "0x5A" and "0xA5" in order disables EMG function or OVV function. After the disable code is written, ***[PMDxEMGCR]***<EMGEN> =0 or ***[PMDxOVVCR]***<OVVEN> =0 should be set continuously.

Note: The disable code should be written for EMG function and OVV function separately.

4.2.14. *[PMDxOVVCR]* (OVV control register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0"
15	OVVRSMD	0	R/W	OVV exit operation selection 0: Automatic return from the protection state or return by the setting of <OVVRS> =1. The automatic return timing is synchronous with U-phase PWM carrier after OVV input becomes inactive. 1: Return from the protection state by the setting of <OVVRS> =1.
14:13	-	0	R	Read as "0"
12:8	OVVCNT[4:0]	00000	R/W	OVV input detection time 00001 to 11111 (When "00000" is set, it operates as "00001".) The noise reduction time for OVV input is set. The noise reduction time is calculated with the following formula: <OVVCNT[4:0]> × 16/fsys Please set with OVV disabled state (<OVVEN> =0).
7	OVVIPOL	0	R/W	OVVx pin polarity selection 0: Low active 1: High active
6:5	-	00	R/W	Write as "00"
4:3	OVVMD[1:0]	00	R/W	OVV protection mode selection (Note) 00: No output restrictions. 01: All upper-phase ON/All lower-phase OFF 10: All upper-phase OFF/All lower-phase ON 11: All phase OFF This field sets the upper-phase (UOx, VOx, and WOx) and the lower-phase (XOx, VOx, and ZOx) outputs to ON or OFF when OVV occurs. ON means the fixed active output, and OFF, the fixed inactive output. Active or Inactive is set to ***[PMDxMDPOT]***<POLL> and <POLH>.
2	OVVISEL	0	R/W	OVVx input selection 0: Port input enabled. 1: Port input disabled. OVV signal input to the protection control circuit is disabled to input from the port.
1	OVVRS	0	W	Return from OVV protection state 0: Don't care. 1: Return from the protection state. Read as "0". The return should be done after confirming that ***[PMDxOVVSTA]***<OVVI> becomes "1".
0	OVVEN	0	R/W	OVV protection control circuit enable or disable 0: Disabled. 1: Enabled. When OVV protection control circuit is disabled, EMG release register ***[PMDxEMGREL]*** should be set to "0x5A" and "0xA5" in order, then <OVVEN> should be set to "0". (3 instructions should be executed continuously.)

Note: ***[PMDxEMGCR]***<EMGMD[1:0]> protection mode setting is prioritized when OVV and EMG occur at the same time.

4.2.15. *[PMDxOVVSTA]* (OVV status register)

Bit	Bit Symbol	After Reset	Type	Description
31:2	-	0	R	Read as "0"
1	OVVI	Undefined.	R	OVV input state 0: Active input. 1: Inactive input. When an active signal among the enabled OVV input signals is input, this bit is set to “0”.
0	OVVST	0	R	OVV protection state 0: Normal operation 1: Protection state OVV protection status can be checked by reading this bit.

4.2.16. *[PMDxDTR]* (Dead time register)

Bit	Bit Symbol	After Reset	Type	Description
31:10	-	0	R	Read as "0"
9:0	DTR[9:0]	0x000	R/W	Dead time is set. 0x000 to 0x3FF The dead time is calculated with the following formula: <DTR[9:0]> setting value × 4/fsys

Note: This register should be set during ***[PMDxMDEN]***<PWMEN> =0.

4.2.17. Trigger comparison register

4.2.17.1. *[PMDxTRGCMP0]* (Trigger comparison 0 register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	TRGCMP0[14:0]	0x0000	R/W	Trigger output comparison register Setting range: 0x0000 to 0x7FFF This register value is compared with the basic carrier or U-phase carrier to generate a trigger signal (PMDxTRG0).

Note1: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note2: The trigger comparison register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note3: For the update timing of the execution buffer, refer to "Table 3.4 Buffer update timing of Trigger comparison register".

Note4: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note5: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.17.2. *[PMDxTRGCMP1]* (Trigger comparison 1 register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	TRGCMP1[14:0]	0x0000	R/W	Trigger output comparison register Setting range: 0x0000 to 0x7FFF This register value is compared with the basic carrier or U-phase carrier to generate a trigger signal (PMDxTRG1).

Note1: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note2: The trigger comparison register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note3: For the update timing of the execution buffer, refer to "Table 3.4 Buffer update timing of Trigger comparison register".

Note4: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note5: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.17.3. *[PMDxTRGCMP2]* (Trigger comparison 2 register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	TRGCMP2[14:0]	0x0000	R/W	Trigger output comparison register Setting range: 0x0000 to 0x7FFF This register value is compared with the basic carrier or V-phase carrier to generate a trigger signal (PMDxTRG2).

Note1: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note2: The trigger comparison register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note3: For the update timing of the execution buffer, refer to "Table 3.4 Buffer update timing of Trigger comparison register".

Note4: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note5: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.17.4. *[PMDxTRGCMP3]* (Trigger comparison 3 register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0"
14:0	TRGCMP3[14:0]	0x0000	R/W	Trigger output comparison register Setting range: 0x0000 to 0x7FFF This register value is compared with the basic carrier or W-phase carrier to generate a trigger signal (PMDxTRG3).

Note1: The byte write (upper 8 bits ([15:8]) and lower 8 bits ([7:0]) are written separately) should not be done. When the byte write is done, the operation cannot be guaranteed.

Note2: The trigger comparison register can be updated while the PWM counter is operating, because it has a triple-buffer structure.

Note3: For the update timing of the execution buffer, refer to "Table 3.4 Buffer update timing of Trigger comparison register".

Note4: For the update timing of the intermediate buffer, refer to "3.7. Buffer Operation".

Note5: When this field is read, the value of the register stage (the data set through the bus) returns.

4.2.18. *[PMDxTRGCR]* (Trigger control register)

Bit	Bit Symbol	After Reset	Type	Description
31:17	-	0	R	Read as "0"
16	CARSEL	0	R/W	Comparison carrier selection 0: Comparison with the base carrier ***[PMDxTRGCMP0]*** to ***[PMDxTRGCMP3]*** are compared with the basic carrier. 1: Comparison with each phase carrier ***[PMDxTRGCMP0]*** and ***[PMDxTRGCMP1]*** are compared with U-phase carrier. ***[PMDxTRGCMP2]*** is compared with V-phase carrier. ***[PMDxTRGCMP3]*** is compared with W-phase carrier.
15	TRG3BE	0	R/W	Asynchronous update enables of the execution buffer in ***[PMDxTRGCMP3]*** (Note1) 0: Synchronous update (Note2) 1: Asynchronous update (the update is done immediately after the data write.)
14:12	TRG3MD[2:0]	000	R/W	***[PMDxTRGCMP3]*** mode setting This field selects the coincidence mode of the trigger output. (Note3) 000: Trigger output is disabled. 001: Trigger is output at the coincidence in the first half of the triangular carrier. 010: Trigger is output at the coincidence in the second half of the triangular carrier. 011: Trigger is output at the coincidence in the first and second halves of the triangular carrier. 100: Trigger is output at PWM end timing. 101: Trigger is output at PWM center timing. 110: Trigger is output at PWM end and center timings. 111: Trigger output is disabled.
11	TRG2BE	0	R/W	Asynchronous update enables for the execution buffer in ***[PMDxTRGCMP2]*** (Note1) 0: Synchronous update (Note2) 1: Asynchronous update (the update is done immediately after the data write.)
10:8	TRG2MD[2:0]	000	R/W	***[PMDxTRGCMP2]*** mode setting This field selects the coincidence mode of the trigger output. (Note3) 000: Trigger output is disabled. 001: Trigger is output at the coincidence in the first half of the triangular carrier. 010: Trigger is output at the coincidence in the second half of the triangular carrier. 011: Trigger is output at the coincidence in the first and second halves of the triangular carrier. 100: Trigger is output at PWM end timing. 101: Trigger is output at PWM center timing. 110: Trigger is output at PWM end and center timings. 111: Trigger output is disabled.
7	TRG1BE	0	R/W	Asynchronous update enables for the execution buffer in ***[PMDxTRGCMP1]*** (Note1) 0: Synchronous update (Note2) 1: Asynchronous update (the update is done immediately after the data write.)

Bit	Bit Symbol	After Reset	Type	Description
6:4	TRG1MD[2:0]	000	R/W	***[PMDxTRGCMP1]*** mode setting This field selects the coincidence mode of the trigger output. (Note3) 000: Trigger output is disabled. 001: Trigger is output at the coincidence in the first half of the triangular carrier. 010: Trigger is output at the coincidence in the second half of the triangular carrier. 011: Trigger is output at the coincidence in the first and second halves of the triangular carrier. 100: Trigger is output at PWM end timing. 101: Trigger is output at PWM center timing. 110: Trigger is output at PWM end and center timings. 111: Trigger output is disabled.
3	TRG0BE	0	R/W	Asynchronous update enables for the execution buffer in ***[PMDxTRGCMP0]*** (Note1) 0: Synchronous update (Note2) 1: Asynchronous update (the update is done immediately after the data write.)
2:0	TRG0MD[2:0]	000	R/W	***[PMDxTRGCMP0]*** mode setting This field selects the coincidence mode of the trigger output. (Note3) 000: Trigger output is disabled. 001: Trigger is output at the coincidence in the first half of the triangular carrier. 010: Trigger is output at the coincidence in the second half of the triangular carrier. 011: Trigger is output at the coincidence in the first and second halves of the triangular carrier. 100: Trigger is output at PWM end timing. 101: Trigger is output at PWM center timing. 110: Trigger is output at PWM end and center timings. 111: Trigger output is disabled.

Note1: When ***[PMDxMDEN]***<PWMEN> =0, the asynchronous update is done regardless of the setting.

Note2: For the update timing, refer to "Table 3.4 Buffer update timing of Trigger comparison register".

Note3: When ***[PMDxMDCR]***<UPWMMD[1:0]>/<VPWMMD[1:0]>/<WPWMMD[1:0]> = 00, 10 (Saw-tooth wave);

- There is no distinction between the first half and the second half, regardless of the setting value, "001", "010", or "011".
- Trigger does not occur at the PWM center. Either "100", "101", or "110" is selected, it occurs output at the PWM end.

4.2.19. *[PMDxTRGSYNCR]* (Trigger update timing setting register)

Bit	Bit Symbol	After Reset	Type	Description
31:2	-	0	R	Read as "0"
1:0	TSYNCS[1:0]	00	R/W	Update timing setting for the execution buffer in the trigger comparison register 00: Immediate update, update at each phase PWM end, center and end or center selected by ***[PMDxTRGCR]***<TRGnMD[2:0]> (n= 0 to 3). 01: Update at each phase PWM center 10: Update at each phase PWM end 11: Update at each phase PWM end or center

Note1: For the update timing, refer to "Table 3.4 Buffer update timing of Trigger comparison register".

Note2: When ***[PMDxMDEN]***<PWMEN> =0, the asynchronous update is done regardless of the setting.

4.2.20. *[PMDxTRGMD]* (Trigger output mode setting register)

Bit	Bit Symbol	After Reset	Type	Description
31:2	-	0	R	Read as "0"
1	-	0	R/W	Write as "0"
0	EMGTGE	0	R/W	Output enable setting in EMG protection state 0: Trigger output is disabled during the protection state. 1: Trigger output is enabled during the protection state. This bit selects enable or disable of the trigger output during EMG protection state.

4.2.21. *[PMDxMBUFCR]* (Intermediate buffer control register)

Bit	Bit Symbol	After Reset	Type	Description
31:3	-	0	R	Read as "0"
2:0	BUFCTR[2:0]	000	R/W	Intermediate buffer update control 000: Intermediate buffer is disabled (the buffer is bypassed). 001: PWM period update (U-phase PWM end timing) 010: PWM period update (U-phase PWM center timing) 011: PWM period update (U-phase PWM 3/4 timing) 100: PWM period update (U-phase PWM 1/4 timing) 101: PWM half period update (U-phase PWM end and center timings) 110: PWM half period update (U-phase PWM 1/4 and 3/4 timings) 111: Reserved

Note: When PMD disable (***[PMDxMDEN]***<PWMEN> =0) and in EMG protection state, the update timing is an asynchronous one regardless of the setting.

5. Precaution for Use

- When PMD cooperate with ADC, please refer to "12-bit Analog to Digital Converter" of the reference manual together.

- The byte write of registers is prohibited regardless of whether PWM is operating or stopped.

- ***[PMDxBCARI]*** value may change during PWM operation. Therefore, the byte read of ***[PMDxBCARI]*** should not be done. Read should be done with Word or Half-word unit.

- The following registers have the double-buffer or triple-buffer structure. The data written to these registers is transferred to the subsequent stage buffer at each update timing (depending on the setting).

  – ***[PMDxCMPU]***, ***[PMDxCMPV]***, ***[PMDxCMPW]***
  – ***[PMDxMDOUT]***
  – ***[PMDxRATE]***
  – ***[PMDxMDCR]***<UPWMMD[1:0]>, <VPWMMD[1:0]>, <WPWMMD[1:0]>
  – ***[PMDxTRGCMP0]*** to ***[PMDxTRGCMP3]***

- Be sure to return processing from the EMG protection state before using the PMD (after PORT is set).

- The EMG protection control circuit is enabled after reset. When it is not used, prohibit it with the following procedure.

  (1) Set ***[PMDxEMGREL]*** to "0x5A"
  (2) Set ***[PMDxEMGREL]*** to "0xA5"
  (3) Set ***[PMDxEMGCR]***<EMGEN> to "0"

  Note: These 3 instructions must be executed consecutively.

- When attempting to stop supplying the clock, make sure to check whether the PMD is stopped. Note that when the MCU enters STOP1/STOP2 mode, make sure to check whether the PMD is stopped as well.

6. Revision History

Table 6.1 Revision history

Revision	Date	Description
1.0	2018-01-16	First release
2.0	2018-06-28	- The entire document dead-time→dead time - Related document Arrange documents - 3.1. Clock Supply Modified register name - Figure 3.1 <nPWMMD>→nPWMMD,<nOC>→nOC - Figure 3.5 <UPWMMD><VPWMMD><WPWMMD>→ <UPWMMD><VPWMMD><WPWMMD> Execution buffer - 3.3. Conduction Control Circuit Figure 3.7: <EMGST>→ ***[PMDxEMGSTA]***<EMGST> Deleted "Timing signals of each phase" 2nd line: ***[PMDxMDOUT]*** register → ***[PMDxMDOUT]*** - 3.4.1.EMG Protection Control Circuit 1st term: Deleted ", respectively" 3rd term: title "Return of the EMG"→"Return from the EMG" EMG pin → EMGx pin 4th term: "and "0xA5" in order. then" → "and "0xA5" in order, then" - 3.4.2.OVV Protection Control Circuit 1st term: Deleted ", respectively" 4th term: "and "0xA5" in order. Then" → "and "0xA5" in order, then" - Figure 3.11 output polarity change → output polarity change circuit - 3.6. Synchronous Trigger Generation Circuit Figure 3.14 <UOC>→UOC, <VOC>→VOC, <WOC>→WOC Table 3.4 Note3: x→xxx - 3.7. Buffer Operation 5th line: single buffer → single-buffer 8th line: "If <BUFCTR>=000 is set," → "When <BUFCTR>=000," - 3.8. Decimation of Execution Buffer... Changed in 3rd line: synchronous trigger → ADC synchronous trigger Deleted in 4th line: " is set" - 4.1. List of Registers Table of Base Address: Deleted "Function Name" cell Added TYPE3 column - 4.2.2. Description: Tool break→debug halt - 4.2.3. DCMEN/Description: Deleted "Note: " ***[PMDxCMPn]*** →***[PMDxCMPU]***/***[PMDxCMPV]***/***[PMDxCMPW]*** ***[PMDxTRGCMPn]*** → ***[PMDxTRGCMP0]***/***[PMDxTRGCMP1]***/***[PMDxTRGCMP2]***/***[PMDxTRGCMP3]*** <nPWMMD>→ <UPWMMD>/<VPWMMD>/<WPWMMD> SYNTMD/Description: <nOC>→<UOC>/<VOC>/<WOC> <nPWM>→<UPWM>/<VPWM>/<WPWM> DTYMD/Description: CMPU→***[PMDxCMPU]***, CMPV→***[PMDxCMPV]***, CMPW→***[PMDxCMPW]*** INTPRD/Description 7th line: 2→2 PWM periods Corrected from 8th line Note5,Note6: <UPWMMD><VPWMMD><WPWMMD> → <UPWMMD>/<VPWMMD>/<WPWMMD> - 4.2.5. After Reset: 0→0x0000 Description: 12.5 ns(=1/fsys) at fsys =80 MHz → 1/fsys (12.5 ns at fsys =80 MHz) - 4.2.7.1. Description: set→setting - 4.2.7.2. Description: the V-phase→ V-phase - 4.2.7.3. Description: the W-phase→ W-phase - 4.2.11. EMGCNT/Description: Changed hexadecimal notation to binary notation EMGIPOL/Description: Deleted "Please set with EMG disabled state.... " EMGISEL/Description: protection circuit →protection control circuit

Revision	Date	Description
2.0	2018-06-28	- 4.2.14. OVVCNT/Description: Changed hexadecimal notation to binary notation OVVISEL/Description: protection circuit →protection control circuit - 4.2.18. Note1: Deleted " is set" - 4.2.19. Note1: "For update timing" → "For the update timing" - 5. Precaution for Use 1st term: "with a ADC," → "with ADC," Last term: STOP→STOP1/STOP2
2.1	2020-07-13	- All over document Added bit field to bit symbol - Deleted trademark - Added TXZ+ family - "2.Configuration" Figure 2.1: Added arrow line to dead time circuit - "3.1. Clock Supply" Added clock supply and stop register C for fsys - "3.3.Conduction Control Circuit" Figure 3.7: Changed "Energization control" to "Decode circuit" , and added input and output - "3.4.1.EMG Protection Control Circuit" "return of " → "return from" Return from the EMG protection (4): "exit" → "return from" - "3.4.2.OVV Protection Control Circuit" "return of" → "return from" - "3.4.3.Protection control when using the debug tool" "PMD is stopped by the debug halt" → "CPU is stopped by the debug halt" - "3.5.Dead time Control Circuit" Added "(refer to Figure 3.11)" "dead time correction circuit" → "dead time correction block" Moved "The output polarity change ... <POLL>, respectively." to end Added "Figure 3.14 Waveform of dead time control circuit" - "3.7. Buffer Operation" Added "The register stage can be read or written." - "4.2.Details of Registers" "4.2.2." Revised the expression of Note2 "4.2.3." <SYNTMD>: Revised the expression of Description "4.2.10." <WPWM> to <UPWM>, <WOC[1:0]> to <UOC[1:0]>: Revised the expression of Description - "5.Precaution for Use" 5th item: "release processing" → "return processing" - "RESTRICTIONS ON PRODUCT USE" Updated, Added URL
2.2	2021-10-15	1. Outlines Contents revised
2.3	2022-06-01	- Table 3.4 Changed the error - "4.2.19." Change the description of TSYNCS[1:0]

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