32-bit RISC Microcontroller

TXZ Family

Reference Manual
Interval Sensor Detection Circuit (ISD-A)

Revision 1.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related Documents

Document name
Clock Control and Operation Mode
Exception
Power Supply and Reset Operation
Product Information
Input/Output Ports

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ISD	Interval Sensor Detection Circuit

1. Outlines

Interval sensor detection circuit (ISD) generates the control timing to operate intermittently an external device such as a sensor. It also detects the level of an input signal from an external device to generate an interrupt.
This interrupt is used to release the low power consumption mode.

The list of the functions of ISD is shown in the following table.

Function category	Function	Description
External circuit control	Reference clock	Reference clock (fisdclk) Low speed clock (32.768 kHz) or the clock that Timer trigger for Clock source (ISDxCLKTRG) is divided by 1, 2, 4, or 8.
	Control timing output	Control timing output (ISDxOUT): 1 output - Active level: Selectable from High and Low. - Active interval: Selectable from among 2 to 256 times of Reference clock cycle. - Active cycle: Selectable from among 1 to 256 times of Active interval.
	Level detection input	Level detection input (ISDxIN0 to 3): 4 inputs - An interrupt (INTISDx) is generated when change of an input level is detected. (The interrupt can release low power consumption mode.) - Detection level patterns of the input signal: One of followings can be selected per input signal. "Low level" "High level" "(Previous) Low level to (Current) High level" "(Previous) High level to (Current) Low level" "Current level is different from Previous one" - Detection timing of the input level: Any timing can be set during the active interval of the control timing output. The input level is stored in a buffer.
	Link operation	Multiple units can be linked and they can operate in the same timing. - Master: Supply slaves with the timing signals of Control timing output/Level detection input. - Slave: Operate at the timing controlled by Master.

2. Configuration

The circuit configuration of the interval sensor detection is shown in the following figure.

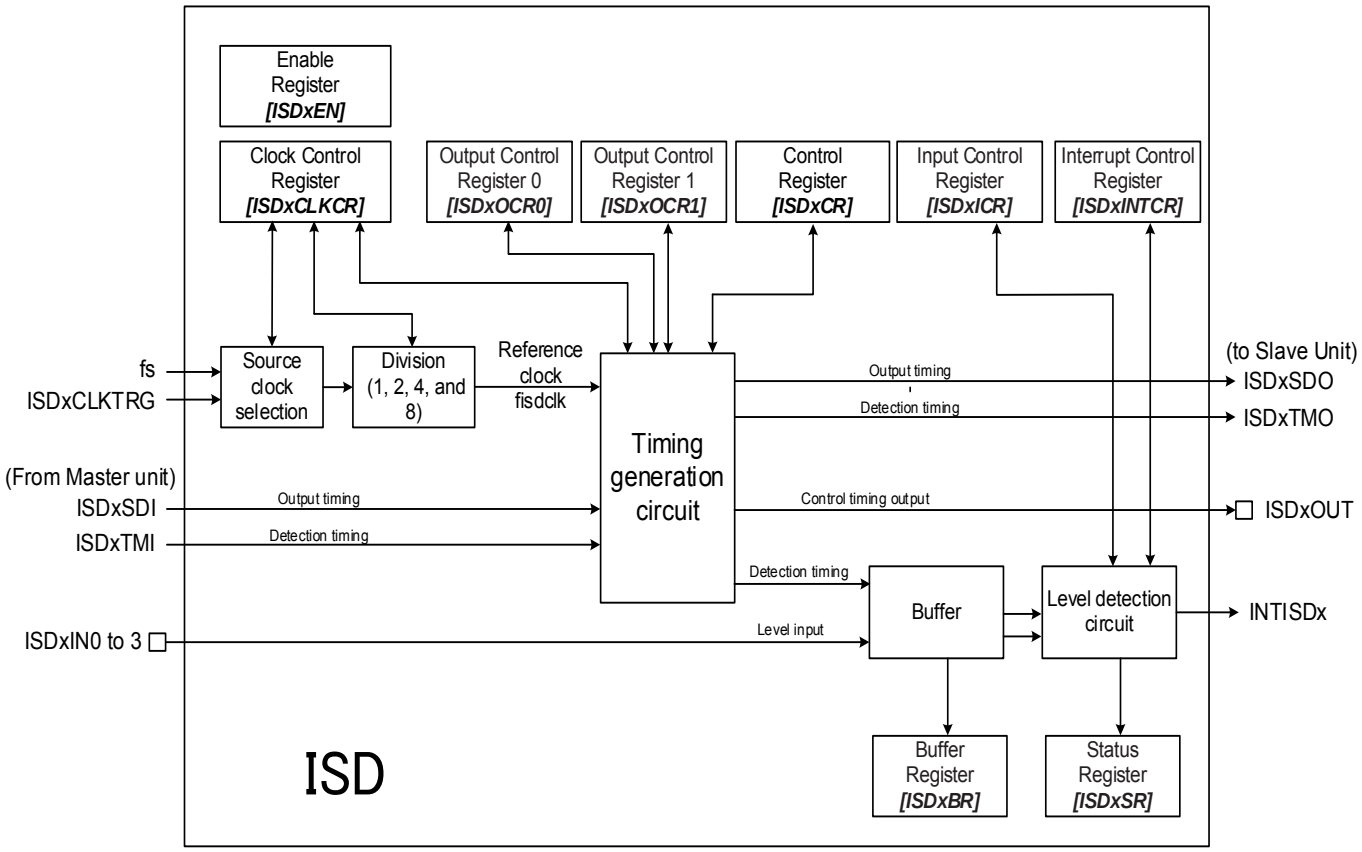

Figure 2.1 Block diagram of Interval sensor detection circuit

Table 2.1 Connection specification

No.	Symbol	Signal name	I/O	Reference manual
1	f_s	Low speed clock (32.768 kHz)	Input	Clock Control and Operation Mode
2	ISDxCLKTRG	Timer trigger for Clock source	input	Product Information
3	ISDxOUT	Control timing output	Output	Product Information, Input/Output Ports
4	ISDxIN0 to 3	Level detection input 0 to 3	Input	Product Information Input/Output Ports
5	INTISDx	ISD interrupt	Output	Exception
6	ISDxSDO	Output timing connection to Slave unit	Output	Product Information
7	ISDxTMO	Detection timing connection to Slave unit	Output	Product Information
8	ISDxSDI	Output timing connection from Master unit	Input	Product Information
9	ISDxTMI	Detection timing connection from Master unit	Input	Product Information

3. Function and Operation

3.1. Clock Supply

When ISD is used, setting of system supply stop register of fsys / fc is unnecessary.
For the source clock, see Table 3.1.

Table 3.1 Source clock

Source clock	Supply setting
Low speed clock (fs)	Supply the low speed clock (fs). For details, refer to "Clock Control and Operation Mode" of the reference manual.
Timer trigger (ISDxCLKTRG)	Please set the clock supply according to the function of the connection destination. Refer to "Product Information" of the reference manual for details of connection destination.

3.2. Basic Operation

ISDxOUT pin outputs frequently a control timing signal at Active cycle T1 to operate intermittently an external device such as a sensor. And, the signal level of the level detection input (ISDxIN0 to 3) is acquired at Detection timing T2 in Active interval T0. If the signal level pattern is the same as the set detection pattern, an interrupt (INTISDx) is generated. The interrupt is used to return from the low power consumption mode or to execute input signal procedure. The acquired signal level is stored in a buffer, which is used as "Previous" level value.

Figure 3.1 shows examples of the control timing output and the level detection input timing.

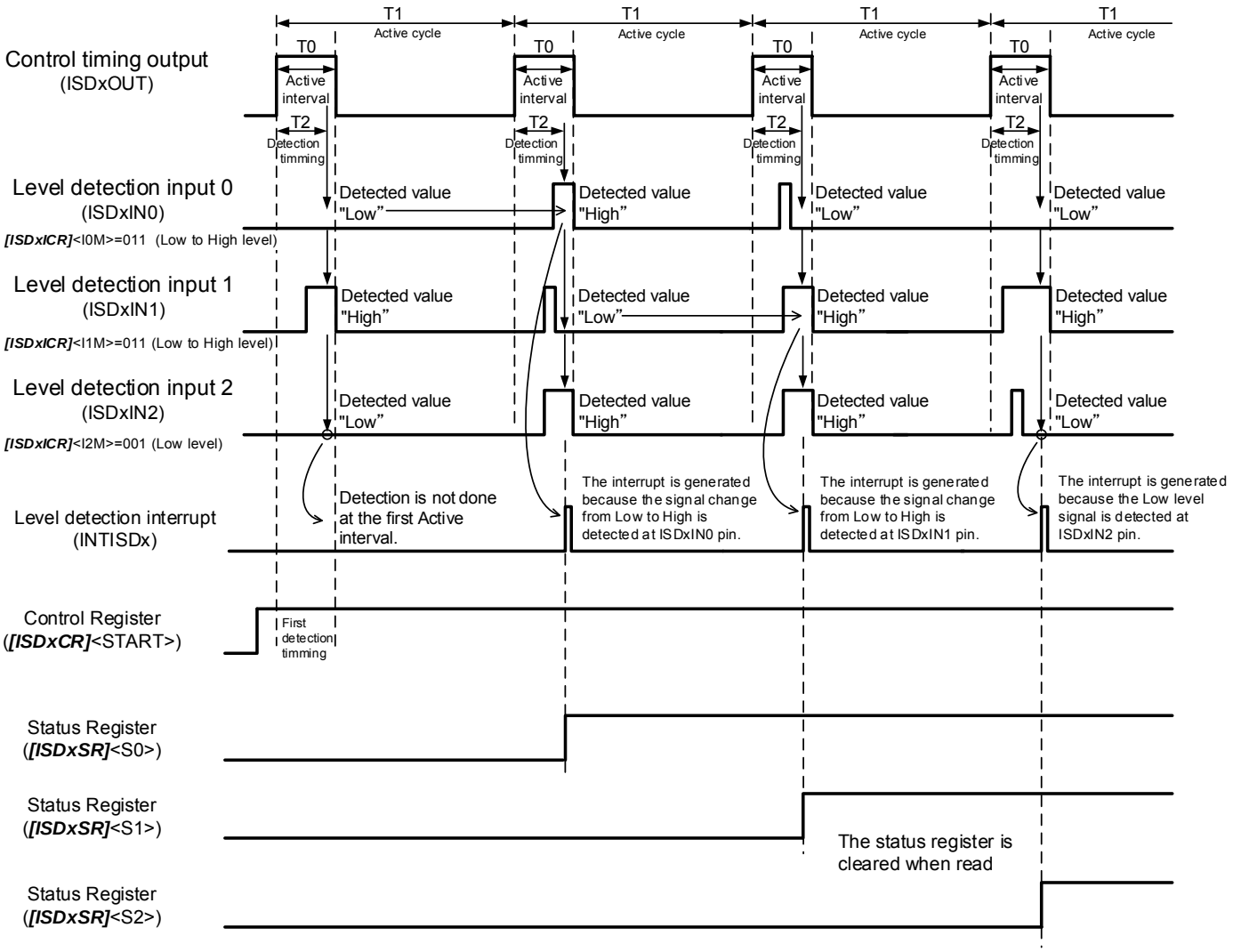

Figure 3.1 Example of Sensor operation timing

3.3. ISD Setting

3.3.1. Reference Clock and Link Operation Settings

The source clock of the reference clock, the division ratio of the reference clock, and the link operation (Master or Slave) are set in ***[ISDxCLKCR]***<SC>, <DIV>, and <MS>, respectively. ***[ISDxCLKCR]*** should be set during ***[ISDxEN]***<EN> = 0.

The frequency of the input signal to ISDxCLKTRG should be 100 kHz or less.

For the details of the timer which is connected to ISDxCLKTRG, refer to "Product Information" in Reference manual. When the low speed clock (fs) is used, fs clock should be set to "Enabled". For the details, refer to "Clock Control and Operation Mode" in Reference manual.

3.3.2. Enable Setting

After ***[ISDxCLKCR]*** is set, ***[ISDxEN]***<EN> should be set to "1" to enable ISD operation. The settings of the registers except ***[ISDxCLKCR]*** should be done after ***[ISDxEN]***<EN> = 1 is set.

If ***[ISDxEN]***<EN> is changed from "1" (Enabled) to "0" (Disabled), the change setting should be done after ***[ISDxCR]***<START> = 0 (signal transfer stop) is confirmed.

3.3.3. Interrupt setting

[ISDxINTCR]<INTEN> sets the enable or disable of an interrupt generation. ISD interrupt (INTISDx) is generated when the level change between a previous level and a current level of the level detection input matches the preset detection pattern.

The status is cleared by reading the Input detection status register ***[ISDxSR]***<S0> to <S3>. And the interrupt is also cleared by it. So ***[ISDxSR]***<S0> to <S3> should be read to clear the generated interrupt.

3.3.4. Setting of Control Timing Output

The control timing output (ISDxOUT) controls the power supply and the operation of an external device such as a sensor. ***[ISDxOCR0]***<OP> sets the active level of the output. ***[ISDxOCR1]***<T0[7:0]> sets the active interval T0 and <T1[7:0]> sets the active cycle time T1. The start of the active interval T0 or the active cycle time T1 is the rise of ISDxOUT signal (the fall if the active level is set to "0").

In the link operation mode, Master unit's settings of the active interval T0 and the active cycle time T0 are valid, and Slave unit's settings are invalid. The active level set in each unit is, however, valid regardless of Master or Slave setting.

When ISDxOUT is used, the setting of the control register of the assigned port is necessary. For the details, refer to "Input/Output Ports" in Reference manual.

3.3.5. Setting of Level Detection Input

In order to detect the level change of the signals input to the level detection pins (ISDxIN0 to 3) from an external device such as a sensor, the detection timing T2 should be set to ***[ISDxOCR1]***<T2[7:0]> and the detection pattern of each pin should be set to ***[ISDxICR]***<I3M>, <I2M>, <I1M>, or <I0M>.

When the pattern of the signal level acquired at Detection timing T2 is the same as the set detection pattern, an interrupt (INTISDx) can be generated as well as the detection status changes. The signal level at Detection timing T2 is stored in a buffer and is used as "Previous" level value.

The start of the detection timing T2 is the rise of ISDxOUT output signal (the fall when the active level is set to "0").

The detection timing T2 should be set to the timing where the input signal becomes stable during the active interval T0.

In the link operation mode, Master unit's setting of the detection timing T2 is valid, and Slave unit's setting is invalid.

When ISDxIN0 to 3 are used, the setting of each control register of the assigned port is necessary. For the details, refer to "Input/Output Ports" in Reference manual.

ISDxIN0 to 3 input signals should not be unstable. To prevent from the unstable state, a suitable setting should be done to the ports or the external devices.

3.3.6. Start of Operation

When ***[ISDxCR]***<START> is set to "1", the control timing (ISDxOUT) is output, the level detection signal is input, and the level detection starts. The operation status is known by reading ***[ISDxCR]***<START>.

In the first active period T0 after setting <START> to "1", only the signal level buffer acquisition is performed and the level detection operation is not performed.

3.4. Buffer Register

The acquired level input from the level detection input pin (ISDxIN0 to 3) at the detection timing T2 set by ***[ISDxOCR1]***<T2[7:0]> is stored in a buffer. The stored level is used as "Previous" detection value of the detection pattern.

The level of the buffer of the pin (ISDxIN0 to 3) is known by reading ***[ISDxBR]***<B0> to <B3>, respectively.

3.5. Input Detection Status

When the level change of a level detection input matches the preset detection pattern, the corresponding ***[ISDxSR]***<S0> to <S3> is set to "1". The detection status of each input pin (ISDxIN0 to 3) is known by reading <S0> to <S3>, respectively. <S0> to <S3> is cleared after it is read. The interrupt is cleared as well as the status is cleared.

It takes 3 cycles of the source clock (fs or ISDxCLKTRG) to clear it after its read. If a level change is detected before the clear, the status is updated to reflect the change. And, if an interrupt is enabled, the interrupt can be generated at the detection.

3.6. Link Operation

When multiple ISD units are integrated and those units are connected with the link output timing/detection timing, the link operation can execute in the same timing. ***[ISDxCLKCR]***<MS> sets the unit to Master or Slave. Master's settings of ***[ISDxCLKCR]***<DIV>, <SC>, ***[ISDxOCR1]***<T2[7:0]>, <T1[7:0]>, and <T0[7:0]> are valid and Slave's settings follow them, which enables Master and Slave link operation. The active level of ISDxOUT in each unit is, however, valid regardless of Master or Slave setting.

The connections of Master unit and Slave unit depend on a product. For the details, refer to "Product Information" in Reference manual.

Figure 3.2 shows an example of the link operation. Unit A is Master, and Unit B and Unit C are Slaves in the figure.

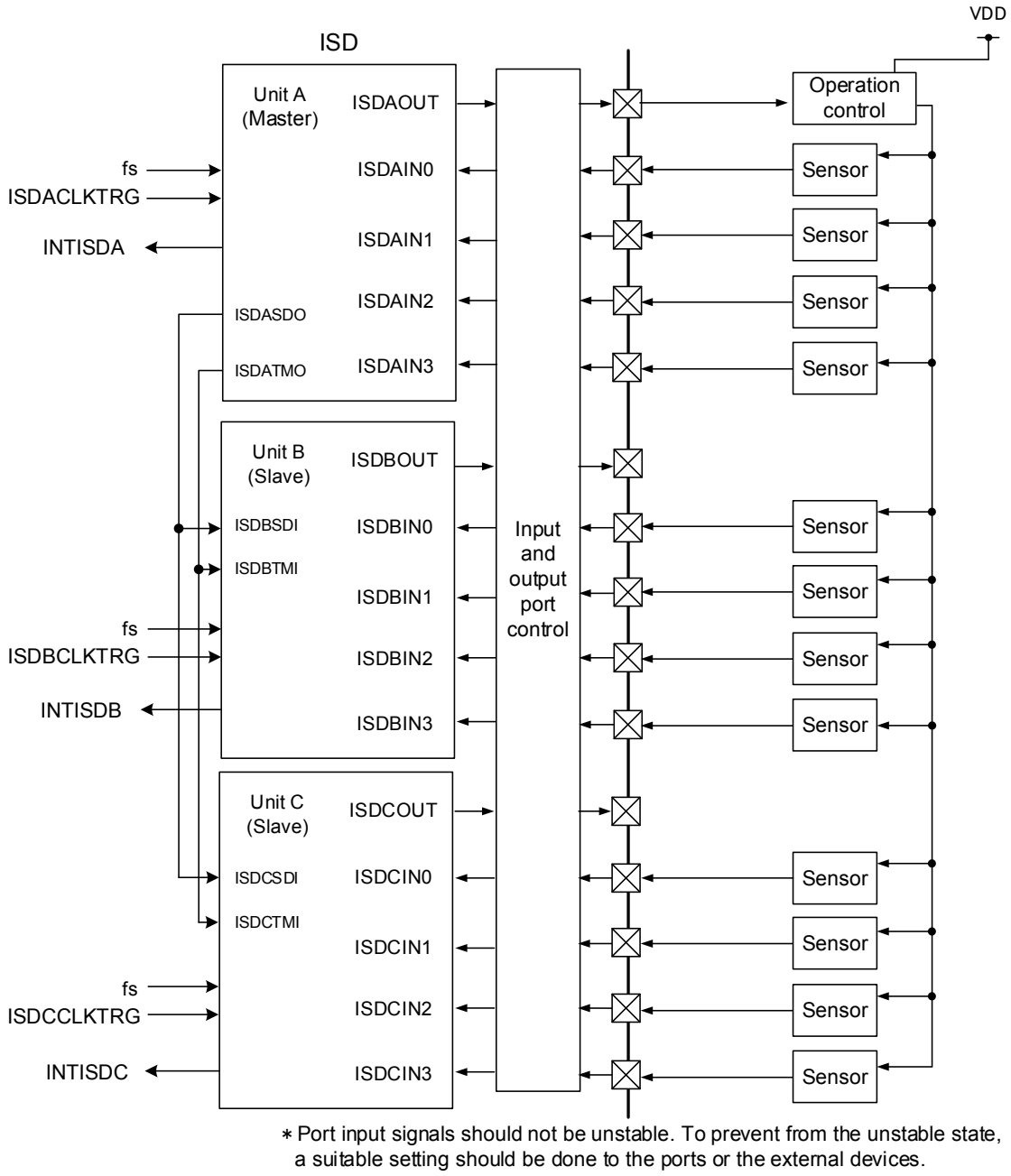

Figure 3.2 Example of ISD link operation

4. Registers

4.1. List of Registers

The control registers and their addresses are shown in the following tables.

Peripheral function		Channel/Unit	Base address (Base)	
			TYPE1	TYPE2
Interval sensor detection circuit	ISD	Unit A	0x400FB800	0x400F0000
		Unit B	0x400FB900	0x400F0100
		Unit C	0x400FBA00	0x400F0200

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Base address (Base+)
Enable Register	***[ISDxEN]***	0x0000
Clock Control Register	***[ISDxCLKCR]***	0x0004
Output Control Register 0	***[ISDxOCR0]***	0x0008
Output Control Register 1	***[ISDxOCR1]***	0x000C
Input Control Register	***[ISDxICR]***	0x0010
Control Register	***[ISDxCR]***	0x0014
Buffer Register	***[ISDxBR]***	0x0018
Status Register	***[ISDxSR]***	0x001C
Interrupt Control Register	***[ISDxINTCR]***	0x0020

4.2. Details of Registers

4.2.1. *[ISDxEN]* (Enable Register)

Bit	Bit Symbol	After Reset	Type	Description
31:1	-	0	R	Read as “0”.
0	EN	0	R/W	Operation of Interval sensor detection circuit 0: Disabled. (Note1) 1: Enabled. This bit controls enable or disable of ISD operation. When ISD is used, this bit should be set to “Enabled” at first. When ISD operation is set to “Disabled” after it is set to “Enabled”, each register setting is held.

Note1: Before ***[ISDxEN]***<EN> is cleared to “0”, ***[ISDxCR]***<START> = “0” should be checked.
Note2: The registers except ***[ISDxCLKCR]*** should be set during ***[ISDxEN]***<EN> = 1.

4.2.2. *[ISDxCLKCR]* (Clock Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:4	-	0	R	Read as “0”.
3:2	DIV	00	R/W	Reference clock selection (Note2) 00: No dividing 01: Divide by 2 10: Divide by 4 11: Divide by 8 This field sets a division ratio of the source clock which is selected by <SC>. The reference clock (fisdclk) of Master operation is generated.
1	SC	0	R/W	Source clock selection (Note2) 0: Low speed clock (fs) 1: Timer trigger for Clock source (ISDxCLKTRG) (Note3) The source clock for the reference clock is selected.
0	MS	0	R/W	Link operation setting 0: Master operation (Single operation) 1: Slave operation (Linked operation)

Note1: Only ***[ISDxCLKCR]*** register should be set during ***[ISDxEN]***<EN> = 0.
The ISD related registers except ***[ISDxEN]*** and ***[ISDxCLKCR]*** should be set during ***[ISDxEN]***<EN> = 1.
Note2: During Slave operation, the settings of <DIV> and <SC> are invalid, and the settings in Master unit are valid.
Note3: The frequency of ISDxCLKTRG input should be 100 kHz or less.
If the source of ISDxCLKTRG stops due to Low power consumption mode, the ISD operation also stops.

4.2.3. *[ISDxOCR0]* (Output Control Register 0)

Bit	Bit Symbol	After Reset	Type	Description
31:1	-	0	R	Read as “0”.
0	OP	0	R/W	ISDxOUT output active level 0: Low level 1: High level This bit sets an active level of the signal output from ISDxOUT pin.

Note1: ***[ISDxOCR0]***<OP> should be set during ***[ISDxEN]***<EN> = 1 and ***[ISDxCR]***<START> = 0.
Note2: The setting of ***[ISDxOCR0]***<OP> is valid regardless of Master or Slave operation.

4.2.4. *[ISDxOCR1]* (Output Control Register 1)

Bit	Bit Symbol	After Reset	Type	Description
31:24	-	0	R	Read as “0”.
23:16	T2[7:0]	0x00	R/W	Detection timing T2 of the input signal (Note1) 0x00 to 0xFF: Detection timing T2 T2 = (<T2> + 1)/fisdclk This field sets detection timing of the signal which inputs on ISDxIN0 to 3 pins.
15:8	T1[7:0]	0x00	R/W	Active cycle T1 for the control timing output 0x00 to 0xFF: Active cycle T1 (Note2) T1 = (<T0> + 1) x (<T1> + 1)/fisdclk This field sets active cycle of the signal which outputs from ISDxOUT pin.
7:0	T0[7:0]	0x01	R/W	Active interval T0 for the control timing output (Note1) 0x00: Setting prohibited 0x01 to 0xFF: Active interval T0 T0 = (<T0> + 1)/fisdclk This field sets active interval of the signal which outputs from ISDxOUT pin.

Note1: The T0 setting value should be T0 ≥ T2.
Note2: When <T1> = 0 is set, the output is always active. In case of always active output, setting of reference clock: no dividing (***[ISDxCLKCR]***<DIV> = 00) is prohibited. Please select other than no dividing.
Note3: T0, T1, and T2 are based on the rise of the ISDxOUT output signal (falling when ***[ISDxOCR0]*** <OP> = 0).
Note4: During Slave operation, the settings follow Master unit ones.
Note5: ***[ISDxOCR1]*** should be set during ***[ISDxEN]***<EN> = 1 and ***[ISDxCR]***<START> = 0.

4.2.5. *[ISDxICR]* (Input Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as “0”.
14:12	I3M	000	R/W	Detection pattern of ISDINx3 000: No detection. 001: Low level 010: High level 011: Previous input signal is Low → Current one is High. 100: Previous input signal is High → Current one is Low. 101: Current signal level is different from Previous one. 110 to 111: Reserved.
11	-	0	R	Read as “0”.
10:8	I2M	000	R/W	Detection pattern of ISDINx2 000: No detection. 001: Low level 010: High level 011: Previous input signal is Low → Current one is High. 100: Previous input signal is High → Current one is Low. 101: Current signal level is different from Previous one. 110 to 111: Reserved.
7	-	0	R	Read as “0”.
6:4	I1M	000	R/W	Detection pattern of ISDINx1 000: No detection. 001: Low level 010: High level 011: Previous input signal is Low → Current one is High. 100: Previous input signal is High → Current one is Low. 101: Current signal level is different from Previous one. 110 to 111: Reserved.
3	-	0	R	Read as “0”.
2:0	I0M	000	R/W	Detection pattern of ISDINx0 000: No detection. 001: Low level 010: High level 011: Previous input signal is Low → Current one is High. 100: Previous input signal is High → Current one is Low. 101: Current signal level is different from Previous one. 110 to 111: Reserved.

Note: ***[ISDxICR]*** should be set during ***[ISDxEN]***<EN> = 1 and ***[ISDxCR]***<START> = 0.

4.2.6. *[ISDxCR]* (Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:1	-	0	R	Read as “0”.
0	START	0	R	Operating condition monitor 0: Stop of operation (Note1) 1: Operating/Start of operation
			W	Control timing output operation and detection operation stop / start 0: Operation stop (Note1) 1: Start operation (Note2)(Note3)

Note1: When “Stop of operation” (= 0) is set, <START> becomes “0” after the current ISDxOUT active interval elapses. If the operation should start again, it should be checked that the current state is “Stop of operation” (= 0).
Note2: ***[ISDxCR]***<START> should be set during ***[ISDxEN]***<EN> = 1.
Note3: Detection is not done at the first Active interval after <START> = 1 is set.

4.2.7. *[ISDxBR]* (Buffer Register)

Bit	Bit Symbol	After Reset	Type	Description
31:4	-	0	R	Read as “0”.
3	B3	0	R	ISDxIN3 buffer level 0: Low level 1: High level
2	B2	0	R	ISDxIN2 buffer level 0: Low level 1: High level
1	B1	0	R	ISDxIN1 buffer level 0: Low level 1: High level
0	B0	0	R	ISDxIN0 buffer level 0: Low level 1: High level

Note: This register shows the signal level which is acquired into the buffer at the detection timing T2.

4.2.8. *[ISDxSR]* (Status Register)

Bit	Bit Symbol	After Reset	Type	Description
31:4	-	0	R	Read as “0”.
3	S3	0	R	ISDxIN3 detection state 0: Not detected. 1: Detected (The detection pattern matches).
2	S2	0	R	ISDxIN2 detection state 0: Not detected. 1: Detected (The detection pattern matches).
1	S1	0	R	ISDxIN1 detection state 0: Not detected. 1: Detected (The detection pattern matches).
0	S0	0	R	ISDxIN0 detection state 0: Not detected. 1: Detected (The detection pattern matches).

Note1: The bit becomes “1” when the level change of the level detection input matches the detection pattern set in ***[ISDxICR]***.
Note2: ***[ISDxSR]*** is cleared when it is read. At the same time, the interrupt is cleared.
Note3: ***[ISDxSR]*** should not be polled. It should be read and checked in the interrupt routine.
Note4: ***[ISDxSR]*** should not be accessed for 3 cycles of the source clock after it is read.

4.2.9. *[ISDxINTCR]* (Interrupt Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:1	-	0	R	Read as “0”.
0	INTEN	0	R/W	Interrupt enable/disable 0: Disabled. 1: Enabled. This bit sets enable or disable of ISD interrupt (INTISDx) generation.

Note: ***[ISDxINTCR]***<INTEN> should be set during ***[ISDxEN]***<EN> = 1 and ***[ISDxCR]***<START> = 0.

5. Revision History

Table 5.1 Revision history

Revision	Date	Description
1.0	2018-01-23	First release
1.1	2018-04-03	3.6. Link Operation Corrected: Figure 3.2 Unit A "ISD interrupt" -> "INTISDA" Unit B "ISD interrupt" -> "INTISDB" Unit C "ISD interrupt" -> "INTISDC" In addition, the signal name was corrected according to the unit name. 4.2.1. ***[ISDxEN]*** to 4.2.9. ***[ISDxINTCR]*** Corrected: Symbol column of Table. "Symbol"->"Bit Symbol"

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