32-bit RISC Microcontroller

TXZ Family

Reference Manual
Remote Control Signal Preprocessor (RMC-B)

Revision 1.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Related Document

Document name
Clock Control and Operation Mode
Exception
Product Information

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

RMC	Remote Control Signal Preprocessor
MAX	Maximum

1. Outlines

Remote control signal preprocessor (RMC) receives a remote control signal of which carrier is removed. The following table shows the list of the functions.

Function Classification	Function	Operation
Reception of a remote control signal	Sampling clock	The sampling clock can be selected from either Low speed clock (32.768 kHz) or Timer trigger for Clock source (TBxOUT).
	Noise filter	Noise canceling time can be adjusted (15 stages).
	Leader detection	Leader can be detected by the settings of a leader cycle and a Low width. - Leader-less remote control signal can be received in the leader wait state. - Remote control signal which begins with only a Low width leader can be received. - Phase-type remote control signal with a fixed cycle can be received.
	Repeat code detection	A leader and a repeat code can be distinguished and detected. - The cycles of the leader and the repeat code are set, respectively, then they are distinguished from each other.
	Data reception	Maximum of 72 bits can be received. - Two kinds of data bit 0/1 judgment are possible. Judgment by setting a threshold value Judgment by Falling edge interrupt
	Interrupt	Interrupt (INTRMCx) can be generated by the following factors. They can be set to enable or disable. - Leader detection - Repeat code detection - Low width detection - Maximum data bit cycle detection - Falling edge detection
	Trigger output	The trigger signal is generated when a leader or a repeat code is detected. - The reception interval of the leader or the repeat code can be measured by the combination of the trigger output and a timer capture function.

2. Block Diagram

The block diagram of RMC is shown in the following figure.

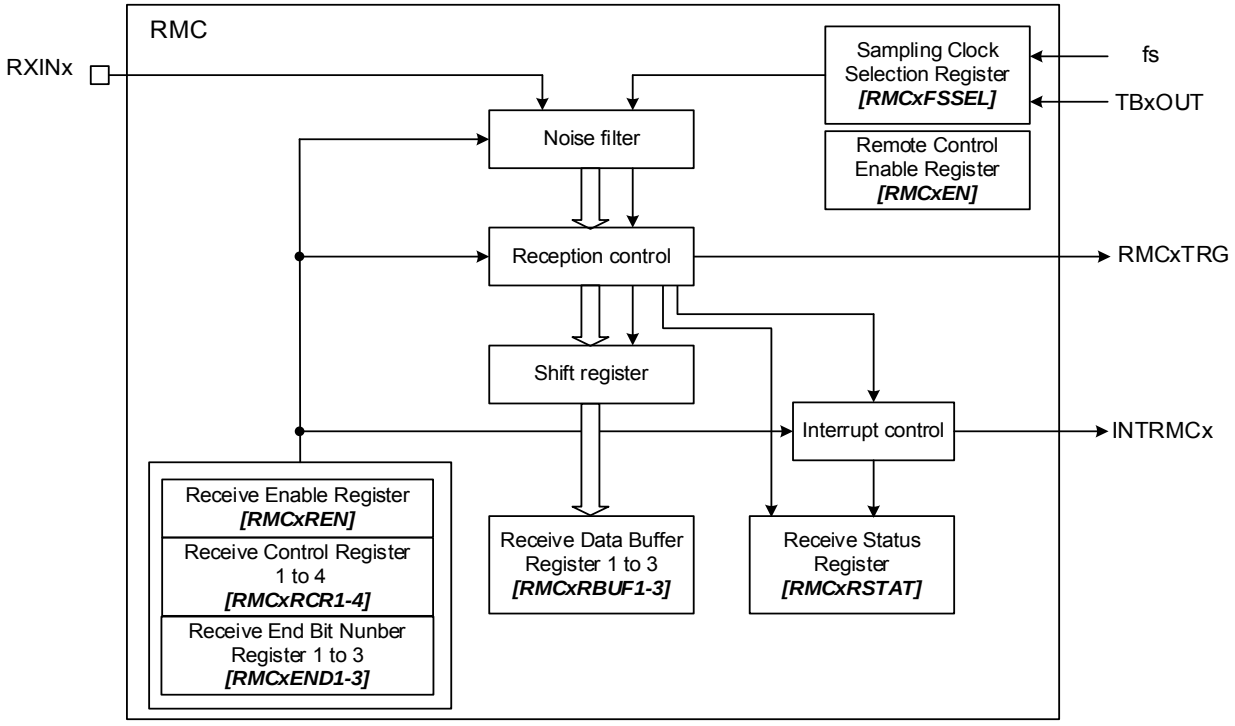

Figure 2.1 RMC block diagram

Table 2.1 List of signals

No.	Symbol	Signal name	I/O	Related reference manual
1	RXINx	Remote control signal	Input	Product Information
2	fs	Low speed clock	Input	Clock Control and Operation Mode
3	TBxOUT	Timer trigger for Clock source	Input	Product Information
4	INTRMCx	Remote control interrupt	Output	Exception
5	RMCxTRG	Trigger output	Output	Product Information

3. Function and Operation

3.1. Clock Supply

When RMC is used, setting of system supply stop register of fsys / fc is unnecessary.
For the source clock, see Table 3.1.

Table 3.1 Source clock

Source clock	Supply setting
Low speed clock (fs)	Supply the low speed clock (fs). For details, refer to "Clock Control and Operation Mode" of the reference manual.
Timer trigger (TBxOUT)	Please set the clock supply according to the function of the connection destination. Refer to "Product Information" of the reference manual for details of connection destination.

3.2. Reception of Remote Control Signal

3.2.1. Sampling Clock

A remote control signal is sampled by 32.768kHz low speed clock (fs) or a Timer trigger (TBxOUT). ***[RMCxFSSEL]***<RMCCLK> selects the sampling clock. When the sampling clock is changed by ***[RMCxFSSEL]*** <RMCCLK>, it should be checked that the remote control operation stops (is disabled; ***[RMCxREN]***<RMCREN> = 0). And ***[RMCxFSSEL]***<RMCCLK> should be set before setting any other registers which relate to the signal reception of the remote controller.

For the timer connected to TBxOUT, refer to "Product Information" in reference manual. When Low speed clock (fs) is used, fs clock should be enabled. For the details, refer to "Clock Control and Operation Mode" in reference manual.

The frequency of the input signal to TBxOUT should be in the range of 30 to 34 kHz.

3.2.2. Basic Operation

The noise of a signal input from RXINx is reduced by the noise filter circuit. And its output signal is input to the reception control circuit.

When the reception control circuit detects a leader, ***[RMCxRSTAT]***<RMCRLDR> is set. And when it detects a repeat code, ***[RMCxRSTAT]***<RMCRRP> is set. If ***[RMCxRCR2]***<RMCLIEN> = 1 has been set, Leader detection interrupt is generated and ***[RMCxRSTAT]***<RMCRLIF> is set. If ***[RMCxRCR2]***<RMCRPIEN> = 1 has been set, repeat code interrupt is generated and ***[RMCxRSTAT]***<RMCRRPIF> is set.

The 0/1 judgment of the data bit is done one by one after the leader or repeat code detection, and the result is stored in the shift register. 72-bit results at maximum can be stored in the shift register.

If ***[RMCxRCR2]***<RMCEDIEN> = 1 has been set, falling edge interrupt is generated at every falling edge of a data bit, and ***[RMCxRSTAT]***<RMCEDIF> is set.

Reception operation completes when the maximum data bit cycle or the Low width becomes each set value, respectively. Then, the data in the shift register is transmitted to ***[RMCxRBUF1]***, ***[RMCxRBUF2]***, and ***[RMCxRBUF3]*** registers, and an interrupt is generated. If ***[RMCxEND1]***< RMCEND1>, ***[RMCxEND2]*** <RMCEND2>, and ***[RMCxEND3]***<RMCEND3> have been set, the interrupt is generated only when the received bit count matches the value set in those registers.

Unless a reception end signal is received, data reception continues even though 73-bit or more data are received. The content of the data buffer is not guaranteed.

To check the status of RMC at the reception completion, Receive Status Register ***[RMCxRSTAT]*** should be read.

After the reception completion, RMC waits for the next leader or repeat code.

When only the data bit signal is set as the remote control signal, a leader or a repeat code is not detected and RMC treats the received signal as data from the beginning.

If the current reception completes before the previous reception data is read, the reception data is replaced by the latest one.

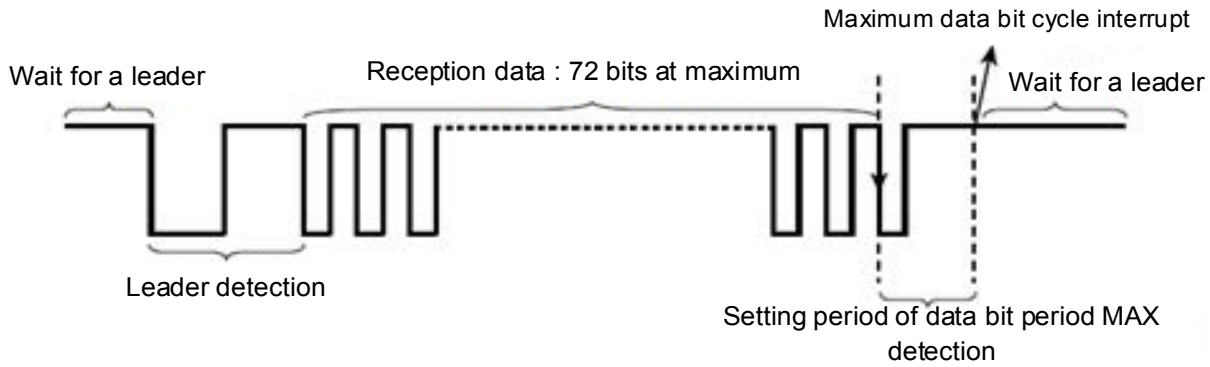

Figure 3.1 Data reception completes by detecting the maximum data bit cycle

3.2.3. Preparation

Before starting data reception, the setting for the reception of a remote control signal should be done to Receive Control Registers (***[RMCxRCR1]***, ***[RMCxRCR2]***, ***[RMCxRCR3]***, and ***[RMCxRCR4]***).

3.2.3.1. Setting of Noise Canceling Time

A noise canceling time should be set to ***[RMCxRCR4]***<RMCNC[3:0]>.

A remote control signal is sampled at the rising edge of the sampling clock. The noise canceling is applied to the sampled signal. RMC monitors the sampled signal. If the signal is "High", RMC recognizes the signal change to "Low" after RMC detects the "Low" width of the cycles specified in <RMCNC>. If the signal is "Low", RMC recognizes the signal change to "High" after RMC detects the "High" width of the cycles specified in <RMCNC>.

The following figure shows the operation when the noise cancelation setting of <RMCNC[3:0]> = 0011 (3 cycles) is done. The noise cancelation signal changes from "High" to "Low" after monitoring the "Low" width of 3 cycles in the sampled signal, and from "Low" to "High" after monitoring the "High" width of 3 cycles.

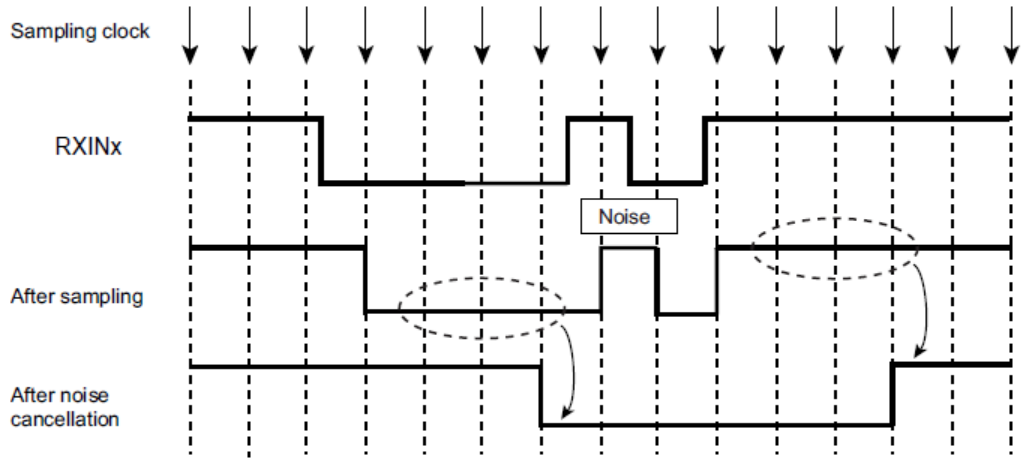

Figure 3.2 Noise cancel (In the case of *[RMCxRCR4]*<RMCNC[3:0]> = 0011 (3 cycles))

3.2.3.2. Setting for Leader Detection

In order to detect a leader, the leader cycle and the Low width should be set to <RMCLCMIN[7:0]>, <RMCLCMAX[7:0]>, <RMCLLMIN[7:0]>, and <RMCLLMAX[7:0]> in ***[RMCxRCR1]***.

Leader detection interrupt can be generated by setting ***[RMCxRCR2]***<RMCLIEN>.
When a leader is detected, ***[RMCxRSTAT]***<RMCRLDR> is set regardless of the setting of the interrupt.

When a leader-less remote control signal is used, <RMCLMAX[7:0]> should be set to "0x00".
Leader detection interrupt cannot be generated for the leader-less remote control signal.

When ***[RMCxRCR2]***<RMCLD> is set, the remote control signal with and without a leader can be received. For the details, refer to Section "3.2.7 Reception of Leader-less Remote Control Signal during Leader Wait State". The remote signal which starts with a Low width only leader should be reversed by setting ***[RMCxRCR4]***<RMCPO> = 1. For the details, refer to Section "3.2.8 Reception of Remote Control Signal Which Starts with Low width only Leader".

Set the ***[RMCxRCR1]*** register in the relation of "Table 3.2 Leader and formula of related registers".

3.2.3.3. Setting for Repeat Code Detection and Judgment

A repeat code can be detected and distinguished from a leader when a repeat code cycle is set to ***[RMCxRCR3]*** <RMCRCMAX><RMCRCMIN> and ***[RMCxRCR3]***<RMCRP> is set to "1".
The Low width value is in ***[RMCxRCR1]***<RMCLLMIN[7:0]><RMCLLMAX[7:0]> which is the same value for the leader detection.

In order to generate Repeat code detection interrupt, ***[RMCxRCR2]***<RMCRPIEN> should be set.
When a repeat code is detected, ***[RMCxRSTAT]***<RMCRRP> is set regardless of the setting of the interrupt.
If the detection periods for a leader and a repeat code overlap, both Leader detection interrupt and Repeat code detection interrupt may be generated.

After a repeat code is detected, the same data bit 0/1 judgment and reception completion as the leader detection are applied. After the reception data bit count should be checked in ***[RMCxRSTAT]***<RMCRNUM[6:0]>, an appropriate procedure should be done for the remote control signal with the repeat code.

Set the ***[RMCxRCR1]*** and ***[RMCxRCR3]*** registers in the relation of "Table 3.2 Leader and formula of related registers".

Table 3.2 Leader and formula of related registers

Repeat code distinction	Leader or Repeat code	Formula
Disable ***[RMCxRCR3]*** <RMCRP> = 0	Low width + High width	***[RMCxRCR1]***<RMCLCMAX[7:0]> > ***[RMCxRCR1]***<RMCLCMIN[7:0]> ***[RMCxRCR1]***<RMCLCMIN[7:0]> > ***[RMCxRCR1]***<RMCLLMAX[7:0]> ***[RMCxRCR1]***<RMCLLMAX[7:0]> > ***[RMCxRCR1]***<RMCLLMIN[7:0]> ***[RMCxRCR3]***<RMCRCMAX[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMIN[7:0]> = Don't care
	High width only or Low width only (Note)	***[RMCxRCR1]***<RMCLCMAX[7:0]> > ***[RMCxRCR1]***<RMCLCMIN[7:0]> ***[RMCxRCR1]***<RMCLLMAX[7:0]> = 0x00 ***[RMCxRCR1]***<RMCLLMIN[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMAX[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMIN[7:0]> = Don't care
	No leader and no repeat code	***[RMCxRCR1]***<RMCLCMAX[7:0]> = 0x00 ***[RMCxRCR1]***<RMCLCMIN[7:0]> = Don't care ***[RMCxRCR1]***<RMCLLMAX[7:0]> = Don't care ***[RMCxRCR1]***<RMCLLMIN[[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMAX[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMIN[7:0]> = Don't care
Enable ***[RMCxRCR3]*** <RMCRP>=1	Low width + High width	***[RMCxRCR1***<RMCLCMAX[7:0]> > ***[RMCxRCR1]***<RMCLCMIN[7:0]> ***[RMCxRCR1]***<RMCLLMAX[7:0]> > ***[RMCxRCR1]***<RMCLLMIN[7:0]> ***[RMCxRCR3]***<RMCRCMAX[7:0]> > ***[RMCxRCR3]***<RMCRCMIN[7:0]> ***[RMCxRCR3]***<RMCRCMIN[7:0]> > ***[RMCxRCR1]***<RMCLLMAX[7:0]>
	High width only or Low width only (Note)	***[RMCxRCR1]***<RMCLCMAX[7:0]> > ***[RMCxRCR1]***<RMCLCMIN[7:0]> ***[RMCxRCR1]***<RMCLCMIN[7:0]> > ***[RMCxRCR3]***<RMCRCMAX[7:0]> ***[RMCxRCR1]***<RMCLLMAX[7:0]> = 0x00 ***[RMCxRCR1]***<RMCLLMIN[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMAX[7:0]> > ***[RMCxRCR3]***<RMCRCMIN[7:0]> ***[RMCxRCR3]***<RMCRCMIN[7:0]> > 0x00
	No leader and no repeat code	***[RMCxRCR1]***<RMCLCMAX[7:0]> = 0x00 ***[RMCxRCR1]***<RMCLCMIN[7:0]> = Don't care ***[RMCxRCR1]***<RMCLLMAX[7:0]> = Don't care ***[RMCxRCR1]***<RMCLLMIN[[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMAX[7:0]> = Don't care ***[RMCxRCR3]***<RMCRCMIN[7:0]> = Don't care

Note: For "Low width only", ***[RMCxRCR4]***<RMCPO> = 1 should be set.

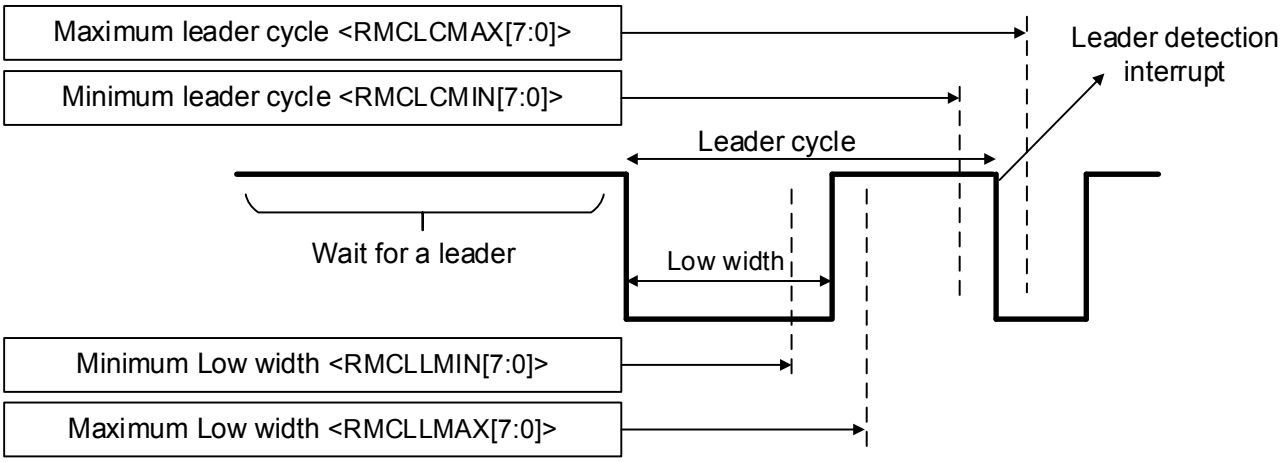

Figure 3.3 Leader waveform and *[RMCxRCR1]*

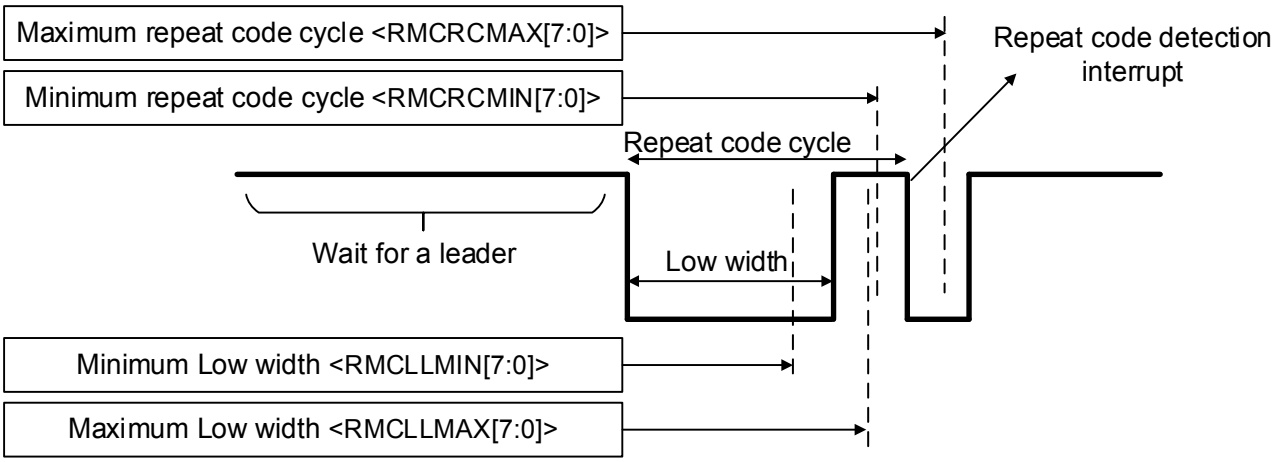

Figure 3.4 Repeat code waveform and registers *[RMCxRCR1]* and *[RMCxRCR3]*

3.2.3.4. Setting for 0/1 Judgment of Data Bit

The 0/1 judgment of a data bit for the cycle-type is done by measuring the length of the interval between two adjacent falling edges. A threshold value is set to ***[RMCxRCR3]***<RMCDATL[6:0]> for the 0/1 judgment. The period of the threshold value or more means "1", and less than the threshold value, "0".

The 0/1 judgment of a data bit for the phase-type remote control signal is described in Section "3.2.9 Reception of Phase-type Remote Control Signal with Fixed Cycle".

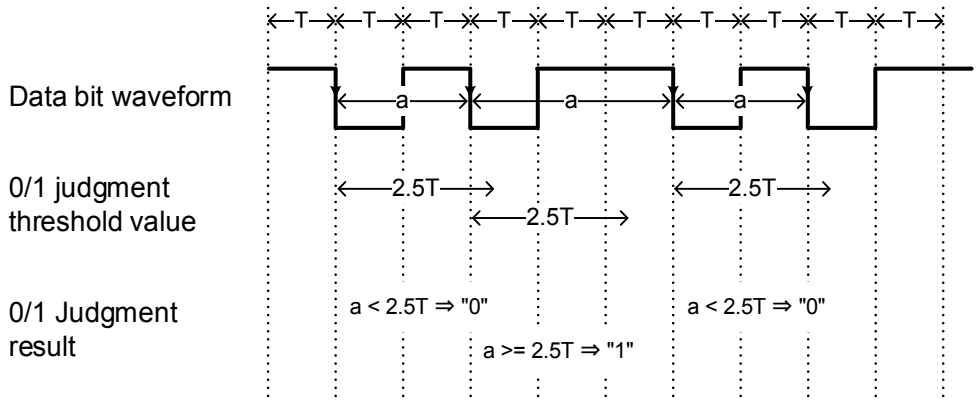

Figure 3.5 0/1 judgment of a data bit (Threshold value: 2.5T)

3.2.3.5. Precaution for Reception Operation

The remote controller is in Data reception state after a leader code or a repeat code is received. If another leader code or repeat code is received before data, the code is treated as data. When a leader code is received, the next frame should be transferred after the last data is transferred and the Low level time interval set in ***[RMCxRCR1]*** <RMCLLMAX> elapses. And, when a repeat code is received, the next frame should be transferred after the repeat code finishes (is detected) and the High level time interval set in ***[RMCxRCR1]***<RMCLLMAX> elapses, too.
When the data polarity is reversed (in ***[RMxCRCR4]***<RMCPO>), the next frame should be transferred after the High level time interval set in ***[RMCxRCR1]***<RMCLLMIN> elapses.

3.2.3.6. Setting for Reception Completion

In order to complete the reception, a maximum data bit cycle detection or a Low width detection should be set to ***[RMCxRCR2]***. If both factors are set, the earlier detected factor completes the reception. Be sure to do the setting of the reception completion.

(1) Reception completion by detecting a maximum data bit cycle

The maximum data bit cycle should be set to ***[RMCxRCR2]***<RMCDMAX[7:0]>. When the interval between two adjacent falling edges of the data bit is equal to or larger than the set value in <RMCDMAX[7:0]>, the maximum data bit cycle is detected. Then the reception completes and RMC waits for the next leader/repeat code.

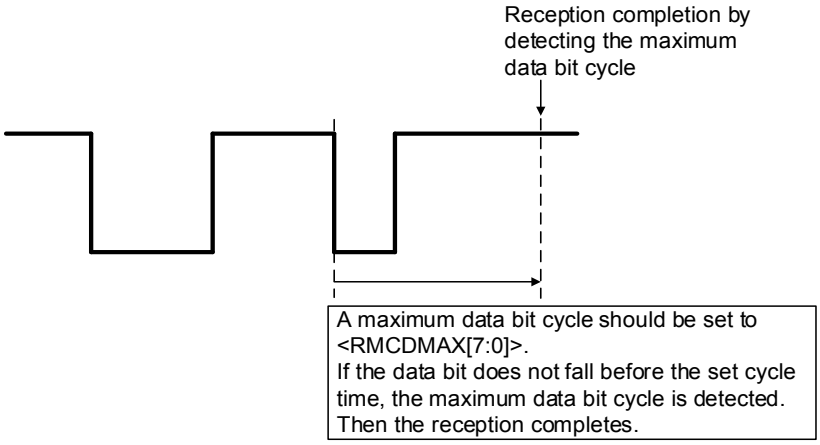

Figure 3.6 Reception completion by detecting a maximum data bit cycle

(2) Reception completion by detecting Low width

The Low width should be set to ***[RMCxRCR2]***<RMCLL[7:0]>. When the data bit falls and stays in Low for the set time value or more, the Low width is detected. Then the reception completes and RMC waits for the next leader/repeat code.

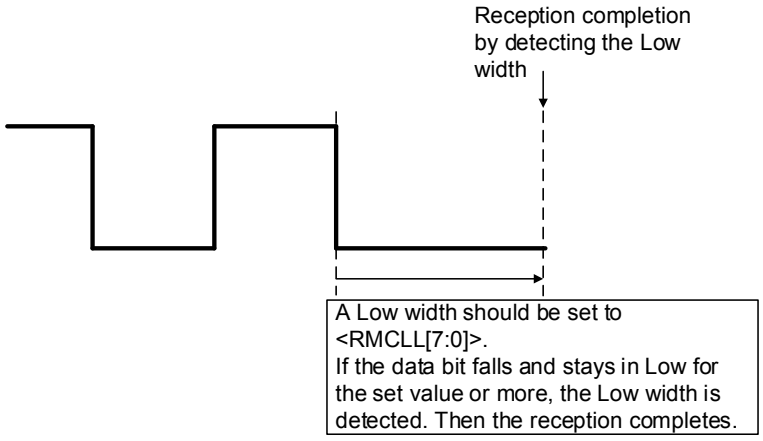

Figure 3.7 Reception completion by detecting Low width

(3) Interrupt generation at the reception completion

An interrupt is generated when the reception completes with the detection of the maximum data bit cycle or the Low width.

If ***[RMCxEND1]***<RMCEND1>, ***[RMCxEND2]***<RMCEND2>, ***[RMCxEND3]***<RMCEND3> are set, the interrupt can be generated only when the bit count at the reception completion matches one of those set values. When the interrupt is generated by the detection of the maximum data bit cycle, ***[RMCxRSTAT]***<RMCDMAXIF> is set to "1", and when the interrupt is generated by the detection of the Low width, ***[RMCxRSTAT]***<RMCLOIF> is set to "1".

3.2.4. Reception Enable

After ***[RMCxRCR1]***, ***[RMCxRCR2]***, ***[RMCxRCR3]***, and ***[RMCxRCR4]*** registers are set, ***[RMCxREN]*** <RMCREN> should be set to the reception enable. Then RMC is in the reception wait state. When it detects a remote control signal, it starts data reception.

Note: If ***[RMCxRCR1]***, ***[RMCxRCR2]***, ***[RMCxRCR3]***, or ***[RMCxRCR4]*** register is updated during the reception, the reception data may not be correct. When the setting is updated during the reception enable, the update should be done carefully.

3.2.5. Reception Stop

The reception is stopped by clearing the ***[RMCxREN]***<RMCREN> to "0" (reception disable).
Clearing this bit during reception stops the reception immediately and the data which has been received till then is discarded.

3.2.6. Interrupt

RMC has 5 interrupt factors. The factors are gathered to one signal which is output as a remote control interrupt signal (INTRMCx). Receive Status Register (***[RMCxRSTAT]***) shows the factor which generates the interrupt.

Table 3.3 Interrupt factor and register

Interrupt factor	Interrupt enable or disable setting	Status flag
	Receive Control Register 2 (***[RMCxRCR2]***)	Receive Status Register (***[RMCxRSTAT]***)
Leader detection interrupt	<RMCLIEN>	<RMCRLIF>
Repeat code detection interrupt	<RMCRPIEN>	<RMCRRPIF>
Falling edge interrupt	<RMCEDIEN>	<RMCEDIF>
Maximum data bit cycle interrupt	-	<RMCDMAXIF>
Low width detection interrupt	-	<RMCLOIF>

3.2.6.1. Leader Detection Interrupt

This interrupt is generated when a leader is detected.
The enable or disable of the interrupt is selected by Receive Control Register (***[RMCxRCR2]***<RMCLIEN>). The status of the interrupt generation is shown in Receive Status Register (***[RMCxRSTAT]***<RMCRLIF>).

3.2.6.2. Repeat Code Detection Interrupt

This interrupt is generated when a repeat code is detected.
The enable or disable of the interrupt is selected by Receive Control Register (***[RMCxRCR2]***<RMCRPIEN>). The status of the interrupt generation is shown in Receive Status Register (***[RMCxRSTAT]***<RMCRRPIF>).

3.2.6.3. Falling Edge Interrupt

This interrupt is generated at every fall edge of a data bit.
The enable or disable of the interrupt is selected by Receive Control Register (***[RMCxRCR2]***<RMCEDIEN>). The status of the interrupt generation is shown in Receive Status Register (***[RMCxRSTAT]***<RMCEDIF>).

3.2.6.4. Maximum Data Bit Cycle Interrupt

This interrupt is generated when the interval between the adjacent falling edges of a data bit is equal to or more than the set value of the maximum data bit cycle in Receive Control Register 2 (***[RMCxRCR2]*** <RMCDMAX[7**:**0]>).
If Receive End Bit Number Registers (***[RMCxEND1][RMCxEND2][RMCxEND3]***) are set, the interrupt can be generated only when the bit count at the reception completion matches one of those set values.
The status of the interrupt generation is shown in Receive Status Register (***[RMCxRSTAT]***<RMCDMAXIF>).

3.2.6.5. Low Width Detection Interrupt

This interrupt is generated when the Low width after the falling edge of a data bit is equal to or more than the set value of the Low width in Receive Control Register 2 (***[RMCxRCR2]***<RMCLL[7:0]>).
If Receive End Bit Number Registers (***[RMCxEND1][RMCxEND2][RMCxEND3]***) are set, the interrupt can be generated only when the bit count at the reception completion matches one of those set values.
The status of the interrupt generation is shown in Receive Status Register (***[RMCxRSTAT]***<RMCLOIF>).

Figure 3.8 shows the waveform of the remote control signals and the interrupt generation timings.

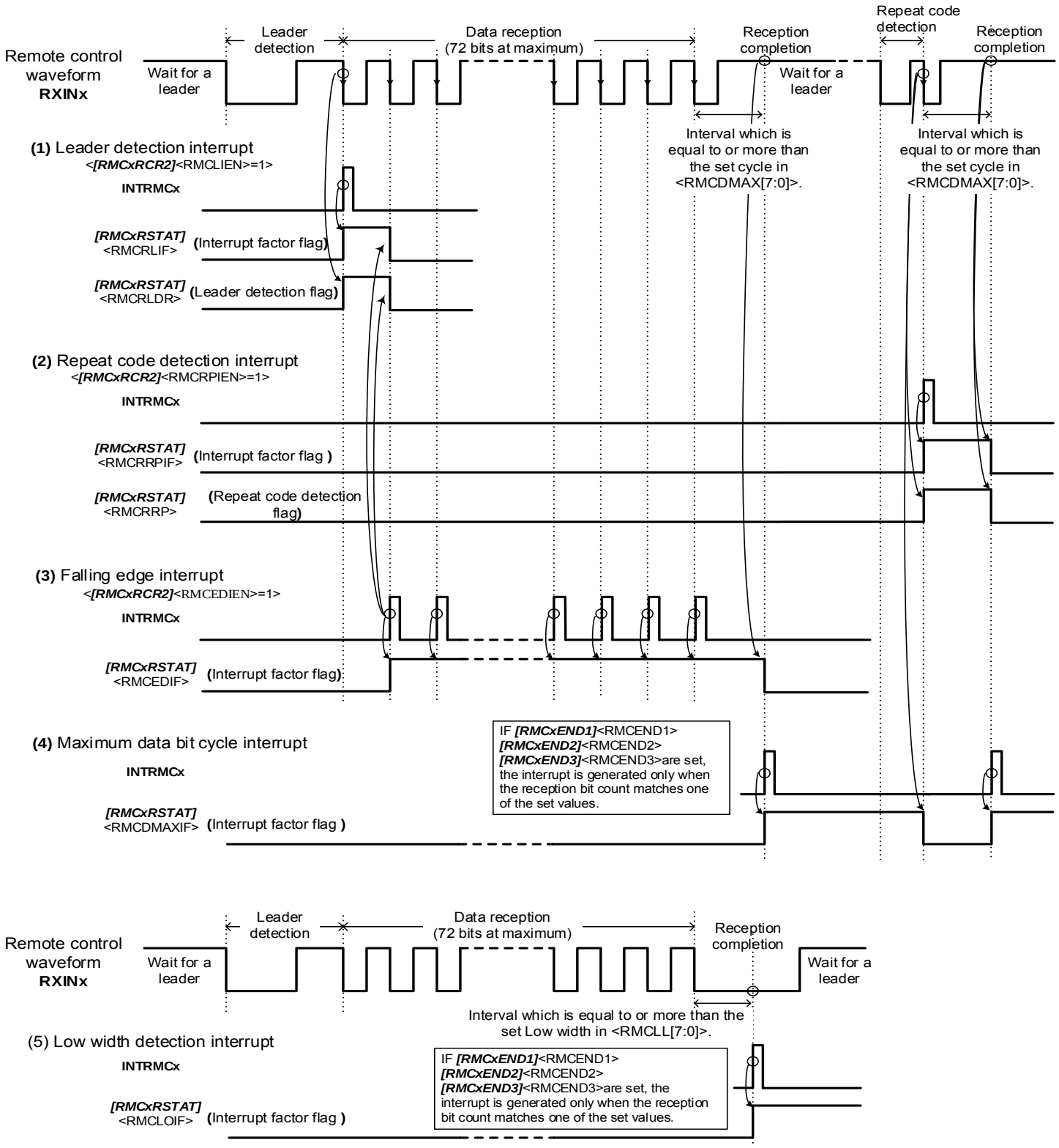

Figure 3.8 Remote control waveform and interrupt generation timing

3.2.7. Reception of Leader-less Remote Control Signal during Leader Wait State

Setting ***[RMCxRCR2]*** <RMCLD> enables RMC to receive both remote control signals with and without a leader.

By setting ***[RMCxRCR2]***<RMCLD>=1, RMC starts receiving data if the signal of which Low width is shorter than the set Low width in the ***[RMCxRCR1]***<RMCLLMIN[7:0]>. RMC keeps receiving data until the final data bit is received.

When this setting is used, the settings of 0/1 judgment of a data bit, error detection, reception completion are the same for both signals with and without a leader. So, the remote signals which can be received may be limited.

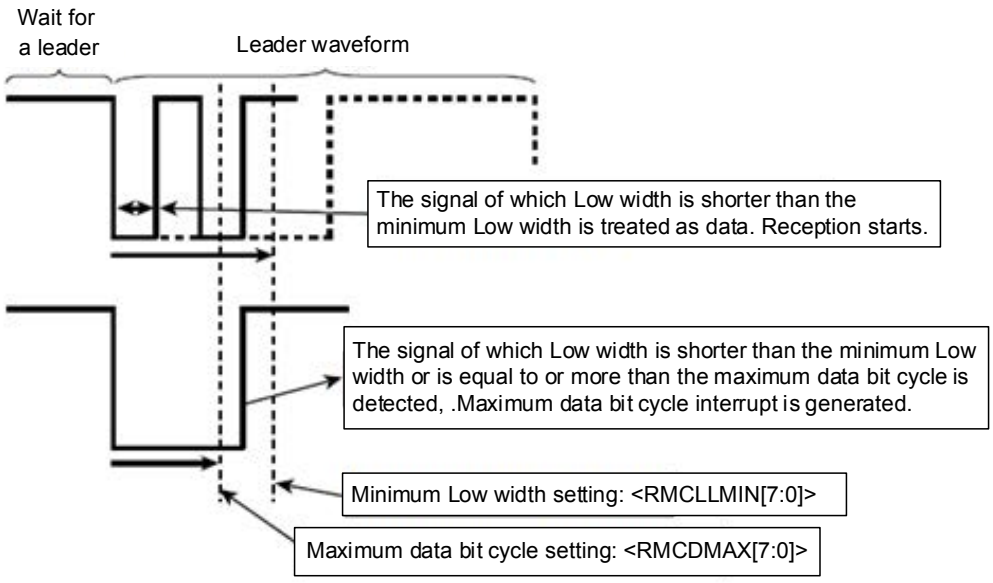

Figure 3.9 Leader-less remote control signal during the leader wait state (In the case of *[RMCxRCR2]*<RMCLD> = 1)

3.2.8. Reception of Remote Control Signal Which Starts with Low width only Leader

"Low width only leader" is the leader which is just a Low signal, as shown in Figure 3.10. The value of a data bit is judged with the rising edge cycle and the remote control signal ends at High. The remote control reception circuit detects a data bit with falling edges. So, ***[RMCxRCR4]***<RMCPO> = 1 should be set because the reverse of the input signal is necessary to handle the remote control signal with a Low width only leader.

For the leader detection, only Low width (High width) should be set: ***[RMCxRCR1]***<RMCLLMAX[7:0]> = 0x00, and <RMCLCMAX[7:0]> > <RMCLCMIN[7:0]> are set. <RMCLLMIN[7:0]> is "Don't care", in this case.

The threshold value for 0/1 judgment of data should be set to ***[RMCxRCR3]***<RMCDATL[6:0]>.

To complete the reception, Low width should be set to ***[RMCxRCR2]***<RMCLL[7:0]>.

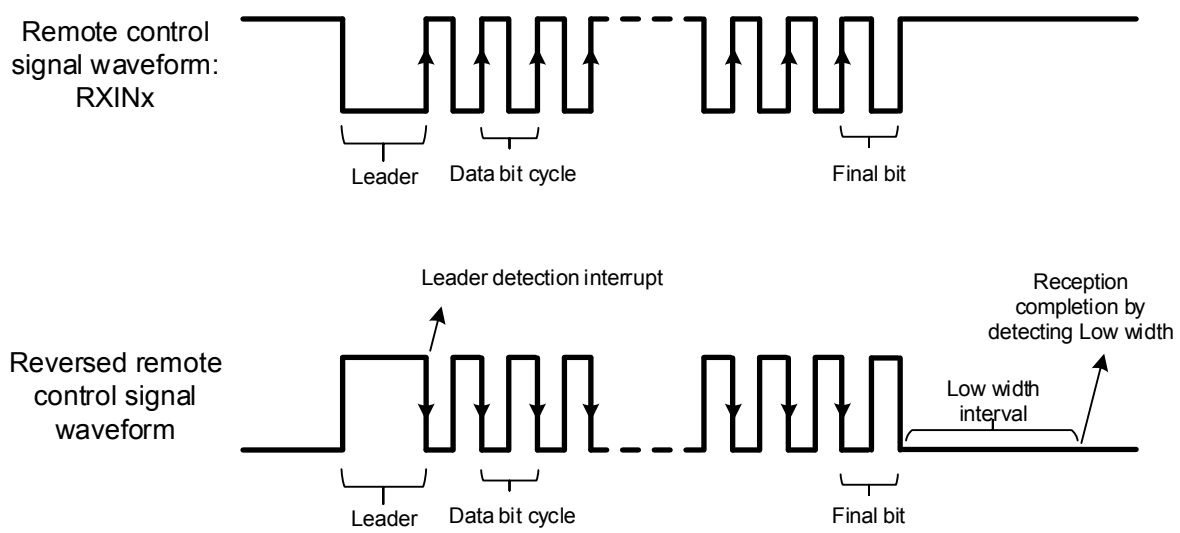

Figure 3.10 Reception of the remote control signal which starts with Low width only leader

3.2.9. Reception of Phase-type Remote Control Signal with Fixed Cycle

Setting ***[RMCxRCR2]***<RMCPHM> = 1 enables the reception of the phase-type remote control signal with a fixed cycle. This phase-type signal has 3 kinds of data change pattern. Two threshold values should be set to ***[RMCxRCR3]***<RMCDATL[6:0]> and <RMCDATH[6:0]>, respectively and the pattern judgment is done using these threshold values. The converted reception data can be stored to ***[RMCxRBUF1]***, ***[RMCxRBUF2]***, and ***[RMCxRBUF3]***.

Two threshold value should be set to define 3 kinds of data change pattern as shown in Figure 3.11. The patterns have 1T, 1.5T, and 2T cycles (T is a fixed cycle value), respectively. The threshold values are set as the following table.

Table 3.4 Threshold value and pattern judgment

	Judgment	Threshold value	Setting register
Threshold value 1	Pattern 1 and Pattern 2	1T to 1.5T	***[RMCxRCR3]***<RMCDATL[6:0]>
Threshold value 2	Pattern 2 and Pattern 3	1.5T to 2T	***[RMCxRCR3]***<RMCDATH[6:0]>

In the discrimination of the stationary fixed-phase remote control signal, three patterns of data change and the data of the immediately preceding period of the judgment pattern are necessary. The phase-type signal should start with data "11".

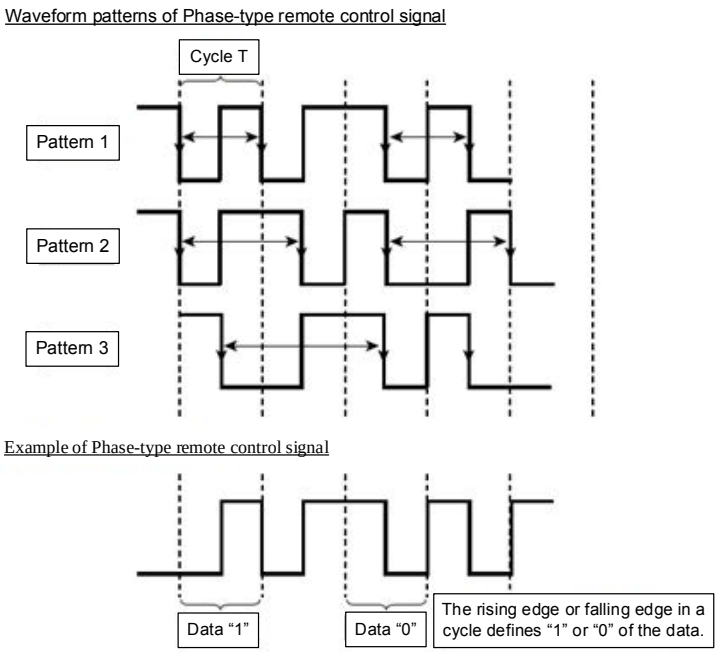

Figure 3.11 Phase-type waveform pattern and a data example

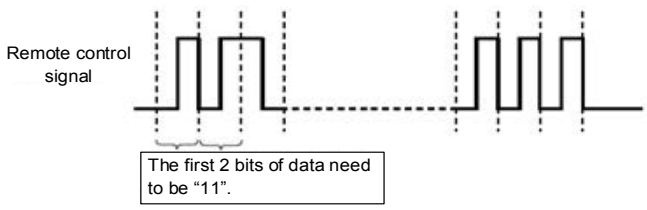

Figure 3.12 Example of a phase-type remote control waveform

3.3. Trigger Output at Detection of Leader or Repeat Code

When a leader or a repeat code is detected, a trigger signal (RMCxTRG) is issued.
The trigger signal can be used for capture function, and the reception interval of the leader or the repeat code can be measured.

Regardless of the setting of Leader or Repeat code detection interrupt (***[RMCxRCR2]***<RMCLIEN> or <RMCRPIEN>), the trigger signal (RMCxTRG) is issued when a leader or a repeat code is detected (***[RMCxRSTAT]***<RMCRLDR> or <RMCRRP> is set to "1").

When the repeat code is not distinguished (***[RMCxRCR3]***<RMCRP> = 0), the trigger signal is issued at the detection of the leader only. When the repeat code is detected (***[RMCxRCR3]***<RMCRP> = 1), the trigger signal is issued at the detection of either the leader or the repeat code. The trigger signal cannot be issued at the detection of the repeat code only.

For the timers which can use the trigger signal, refer to "Product Information" in reference manual.

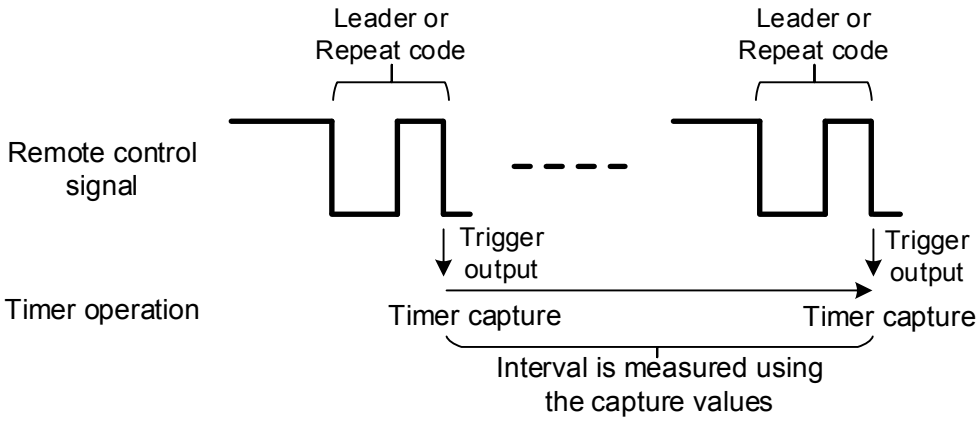

Figure 3.13 Reception interval measured by a timer capture function

4. Registers

4.1. List of Registers

The control registers of RMC and their addresses are shown in the following tables.

Table 4.1 List of registers and their addresses

Peripheral function		Channel/Unit	Base address	
			TYPE 1	TYPE 2
Remote Control Signal Preprocessor	RMC	ch 0	0x400E7000	0x400E8100
		ch 1	0x400E7100	0x400E8200

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Address (Base+)
Remote Control Enable Register	***[RMCxEN]***	0x0000
Receive Enable Register	***[RMCxREN]***	0x0004
Receive Data Buffer Register 1	***[RMCxRBUF1]***	0x0008
Receive Data Buffer Register 2	***[RMCxRBUF2]***	0x000C
Receive Data Buffer Register 3	***[RMCxRBUF3]***	0x0010
Receive Control Register 1	***[RMCxRCR1]***	0x0014
Receive Control Register 2	***[RMCxRCR2]***	0x0018
Receive Control Register 3	***[RMCxRCR3]***	0x001C
Receive Control Register 4	***[RMCxRCR4]***	0x0020
Receive Status Register	***[RMCxRSTAT]***	0x0024
Receive End Bit Number Register 1	***[RMCxEND1]***	0x0028
Receive End Bit Number Register 2	***[RMCxEND2]***	0x002C
Receive End Bit Number Register 3	***[RMCxEND3]***	0x0030
Sampling Clock Selection Register	***[RMCxFSSEL]***	0x0034

4.2. Details of Registers

4.2.1. *[RMCxEN]* (Remote Control Enable Register)

Bit	Bit Symbol	After Reset	Type	Description
31:2	-	0	R	Read as "0".
1	-	0	R/W	Write as "1".
0	RMCEN	0	R/W	Operation of RMC 0: Disabled. 1: Enabled. This bit controls the operation of RMC. When RMC is used, this bit should be set to "Enabled" first. When the operation is disabled after it is enabled, the settings in the registers are held.

4.2.2. *[RMCxREN]* (Receive Enable Register)

Bit	Bit Symbol	After Reset	Type	Description
31:1		0	R	Read as "0".
0	RMCREN	0	R/W	Reception enable 0: Disabled. 1: Enabled. This bit controls the reception operation. When this bit is set to "1", RMC is in the reception wait state.

Note: ***[RMCxREN]***<RMCREN> should be set to "1" after ***[RMCxRCR1] [RMCxRCR2] [RMCxRCR3] [RMCxRCR4]*** are set.

4.2.3. *[RMCxRBUF1]* (Receive Data Buffer Register 1)

Bit	Bit Symbol	After Reset	Type	Description
31:0	RMCRBUF[31:0]	0x00000000	R	Reception data (bit 31 to 0) Received 4-Byte data (bit 31 to 0) can be read.

4.2.4. *[RMCxRBUF2]* (Receive Data Buffer Register 2)

Bit	Bit Symbol	After Reset	Type	Description
31:0	RMCRBUF[63:32]	0x00000000	R	Reception data (bit 63 to 32) Received 4-Byte data (bit 63 to 32) can be read.

4.2.5. *[RMCxRBUF3]* (Receive Data Buffer Register 3)

Bit	Bit Symbol	After Reset	Type	Description
31:8	-	0	R	Read as "0".
7:0	RMCRBUF[71:64]	0x00	R	Reception data (bit 71 to 64) Received 1 Byte data (bit 71 to 64) can be read.

Note1: The first bit of received data is stored in MSB of the buffer register, and the last bit, in LSB (bit 0). If the remote control signal in LSB-first format is received, data of the reversed significant bit is stored in the registers.

Note2: Data of more than 73 bits can be received before the waveform of the reception completion is input. In this case, the data in the reception data buffers are not guaranteed.

4.2.6. *[RMCxRCR1]* (Receive Control Register 1)

Bit	Bit Symbol	After Reset	Type	Description
31:24	RMCLCMAX[7:0]	0x00	R/W	Maximum value of the cycle for the leader detection Calculation formula for the maximum value: <RMCLCMAX> × 4/fs (Note1)
23:16	RMCLCMIN[7:0]	0x00	R/W	Minimum value of the cycle for the leader detection Calculation formula for the minimum value: <RMCLCMIN> × 4/fs (Note1)
15:8	RMCLLMAX[7:0]	0x00	R/W	Maximum value of the Low width for the leader detection Calculation formula for the maximum value: <RMCLLMAX> × 4/fs (Note1)
7:0	RMCLLMIN[7:0]	0x00	R/W	Minimum value of the Low width for the leader detection Calculation formula for the minimum value: <RMCLLMIN> × 4/fs (Note1) When ***[RMCxRCR2]***<RMCLD> = 1, Low width of the value less than the set one is treated as a data bit.

Note1: In the formula, the sampling clock is the fs clock. If TBxOUT is selected, fs should be replaced by the frequency of TBxOUT.

Note2: The setting of the cycle for the leader detection should follow the relation formulas in Table 3.2.

4.2.7. *[RMCxRCR2]* (Receive Control Register 2)

Bit	Bit Symbol	After Reset	Type	Description
31	RMCLIEN	0	R/W	Leader detection interrupt enable 0: Interrupt is not generated. 1: Interrupt is generated.
30	RMCEDIEN	0	R/W	Remote control input falling edge interrupt enable 0: Interrupt is not generated. 1: Interrupt is generated.
29	RMCRPIEN	0	R/W	Repeat code detection interrupt enable 0: Interrupt is not generated. 1: Interrupt is generated.
28:26	-	0	R	Read as "0".
25	RMCLD	0	R/W	Reception of the signal with and without a leader 0: Disabled. 1: Enabled.
24	RMCPHM	0	R/W	Enable of the phase-type remote control signal 0: Cycle-type remote control signal is received. 1: Phase-type remote control signal with a fixed cycle is received.
23:16	-	0	R	Read as "0".
15:8	RMCLL[7:0]	0xFF	R/W	Low width detection setting 0x00 to 0xFE: The reception completes and the interrupt is generated at <RMCLL> × 1/fs [s]. (Note1) (Note2) 0xFF: Low Width is not detected.
7:0	RMCDMAX[7:0]	0xFF	R/W	Maximum data bit cycle detection setting 0x00 to 0xFE: The reception completes and the interrupt is generated at <RMCDMAX> × 1/fs [s]. (Note1) (Note2) 0xFF: Data bit cycle MAX is not detected.

Note1: In the formula, the sampling clock is the fs clock. If TBxOUT is selected, fs should be replaced by the frequency of TBxOUT.

Note2: If ***[RMCxEND1]***<RMCEND1>***[RMCxEND2]***<RMCEND2>***[RMCxEND3]***<RMCEND3> are set, the interrupt is generated only when the reception bit count matches one of the set values.

4.2.8. *[RMCxRCR3]* (Receive Control Register 3)

Bit	Bit Symbol	After Reset	Type	Description
31:24	RMCRCMAX[7:0]	0x00	R/W	Maximum value of the cycle for the repeat code detection (Note1) Calculation formula for the maximum value: <RMCRCMAX> × 4/fs [s]
23:16	RMCRCMIN[7:0]	0x00	R/W	Minimum value of the cycle for the repeat code detection (Note1) Calculation formula for the minimum value: <RMCRCMIN> × 4/fs [s]
15	RMCRP	0	R/W	Repeat code distinction setting 0: Disabled. 1: Enabled.
14:8	RMCDATH[6:0]	0x00	R/W	An upper threshold value setting to judge one of 3 kinds of data bit (Note2) Calculation formula for the threshold value: <RMCDATH> × 1/fs [s] (Note3) A threshold value should be set to a value between 1.5T and 2T to judge one of 3 kinds of data bit in the phase-type remote control signal. (Note4)
7	-	0	R	Read as "0".
6:0	RMCDATL[6:0]	0x00	R/W	A threshold value for 0/1 judgment of a data bit, or a lower threshold value setting to judge one of 3 kinds of data bit Calculation formula for the threshold value: <RMCDATL> × 1/fs [s] (Note3) The upper threshold value should be set for 0/1 judgment of a data bit, or the upper threshold value should be set to a value between 1T and 1.5T to judge one of 3 kinds of data bit in the phase-type remote control signal. (Note5)

Note1: Please follow the relational expression "Table 3.2 Leader and formula of related registers" for setting the repeat code detection period.

Note2: <RMCDATH[6:0]> is enabled only when ***[RMCxRCR2]***<RMCPHM> = 1.

Note3: In the formula, the sampling clock is the fs clock. If TBxOUT is selected, fs should be replaced by the frequency of TBxOUT.

Note4: If the measurement result of the data bit is equal to or larger than the threshold value, the data is judged as "10". If, less than the threshold, "01".

Note5: In 0/1 judgment of a data bit, if the data bit is equal or larger than the threshold value, the data is judged as "1", and if, less than the threshold value, "0".

In the judgment of 3 kinds of data bit in the phase-type remote control signal, if the data bit is equal to or larger than the threshold value, the data is judged as "01". If, less than the threshold, "00".

4.2.9. *[RMCxRCR4]* (Receive Control Register 4)

Bit	Bit Symbol	After Reset	Type	Description
31:8	-	0	R	Read as "0".
7	RMCPO	0	R/W	Selection of the reverse of a remote control signal 0: Unreversed. 1: Reversed.
6:4	-	0	R	Read as "0".
3:0	RMCNC[3:0]	0x0	R/W	Setting of the noise canceling time 0x0: No noise cancelation 0x1 to 0xF: Noise cancelation enable Calculation formula for the noise canceling time: <RMCNC> × 1/fs [s] (Note)

Note: In the formula, the sampling clock is the fs clock. If TBxOUT is selected, fs should be replaced by the frequency of TBxOUT.

4.2.10. *[RMCxRSTAT]* (Receive Status Register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0".
15	RMCRLIF	0	R	Interrupt factor flag 0: Leader detection interrupt has not been generated. 1: Leader detection interrupt has been generated.
14	RMCLOIF	0	R	Interrupt factor flag 0: Low width detection interrupt has not been generated. 1: Low width detection interrupt has been generated.
13	RMCDMAXIF	0	R	Interrupt factor flag 0: Maximum data bit cycle interrupt has not been generated. 1: Maximum data bit cycle interrupt has been generated.
12	RMCEDIF	0	R	Interrupt factor flag 0: Falling edge interrupt has not been generated. 1: Falling edge interrupt has been generated.
11	RMCRRPIF	0	R	Interrupt factor flag 0: Repeat code detection interrupt has not been generated. 1: Repeat code detection interrupt has been generated.
10:9	-	0	R	Read as "0".
8	RMCRRP	0	R	Repeat code detection 0: No repeat code is detected. 1: A repeat code is detected.
7	RMCRLDR	0	R	Leader detection 0: No leader is detected. 1: A leader is detected.
6:0	RMCRNUM[6:0]	0x00	R	Received data bit count of the remote control signal 0x00: No data bits (only a leader or a repeat code) 0x01 to 0x48: 1 to 72-bit reception 0x49 to 0xFF: More than 72 bits This field shows the received count of data bits of the remote control signal. (Note2)

Note1: The fields except <RMCRNUM[6:0]> are updated (set or cleared) by each interrupt factor generation, the leader detection, the repeat code detection, and the reception completion, respectively.

Note2: <RMCRNUM[6:0]> is updated after the reception completion. The received data bit count cannot be monitored during the reception.

4.2.11. *[RMCxEND1]* (Receive End Bit Number Register 1)

The following is an example of ***[RMCxEND1]***, ***[RMCxEND2]***, ***[RMCxEND3]*** have the same configuration.

Bit	Bit Symbol	After Reset	Type	Description
31:7	-	0	R	Read as "0".
6:0	RMCEND1[6:0]	0x00	R/W	Reception bit count setting 1 to generate an interrupt after the reception completion. 0x00: An interrupt is not generated by this count factor. (Note1) 0x01 to 0x48: The reception count to generate the interrupt (1 to 72 bits) (Note2) 0x49 to 0x7F: Inhibited.

Note1: If all of <RMCEND1>, <RMCEND2>, <RMCEND3> are set to "0x00", an interrupt (the maximum data bit cycle detection and the Low width detection) is generated regardless of the reception bit count.

Note2: An interrupt is generated only when the reception bit count matches one of ***[RMCxEND1], [RMCxEND2],[RMCxEND3]*** at the reception completion. If the register values do not match the count, no interrupt is generated. ***[RMCxEND1]***,***[RMCxEND2]***,***[RMCxEND3]*** can be set to different values, respectively.

4.2.12. *[RMCxFSSEL]* (Sampling Clock Selection Register)

Bit	Bit Symbol	After Reset	Type	Description
31:1	-	0	R	Read as "0".
0	RMCCLK	0	R/W	Sampling clock selection 0: Low speed clock (32.768 kHz) 1: Timer trigger (TBxOUT) The sampling clock for the remote control signal is selected. For the timers to be connected to TBxOUT, refer to "Product Information" in reference manual. The frequency of the input signal to TBxOUT should be in the range of 30 to 34 kHz.

Note1: When the sampling clock is changed by ***[RMCxFSSEL]***, the RMC should be stopped (disabled) by ***[RMCxEN]***<RMCEN>. Then, the circuit is started up (enabled), and the setting of this register should be done before the other related registers are set.

Note2: The RMC can be stopped (disabled) by ***[RMCxEN]***<RMCEN>. Then the circuit is started up (enabled) again. When the sampling clock is changed, it should be checked that the RMC is stopped (disabled). Then, the setting of ***[RMCxFSSEL]***<RMCCLK> should be done before the other related registers are set.

5. Precaution

The timer trigger (TBxOUT) for Clock source cannot be selected as the sampling clock in some products. For the details, refer to "Product Information" in reference manual.

6. Revision History

Table 6.1 Revision history

Revision	Date	Description
1.0	2018-01-25	First release
1.1	2018-07-30	-Conventions Modified explanation of trademark 1.Outlines Corrected the contents of the table. ("Remote control interrupt (INTRMCx) " -> "Interrupt (INTRMCx) ")

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