# 32-bit RISC Microcontroller

# TXZ Family

## Reference Manual
## External Bus Interface
## (EBIF-A)

## Revision 1.2

**2018-11**

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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# Preface

**Related document**

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| Product Information |
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## Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123- Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the “0b” when the number of bit can be distinctly understood from a sentence.
- “_N” is added to the end of signal names to indicate low active signals.
- It is called “assert” that a signal moves to its active level, “deassert” to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- “n” substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, “x” means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, “x” means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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## Terms and Abbreviation

Some of abbreviations used in this document are as follows:

| | |
|---|---|
| ALE | Address Latch Enable |
| CS | Chip Select |
| EBIF | External Bus Interface |
| SRAM | Static RAM |

# 1. Outlines

External bus interface (EBIF) is interface to connect to memory and I/Os external of MCU. These features are shown in the following table.

| Function classification | Function | Operation explanation |
|---|---|---|
| Connection specification | Support Devices | NOR Flash memory, SRAM, Peripheral I/O, etc. |
| | Mode | Separate bus mode, Multiplexed bus mode |
| | Data bus width | Either an 8-bit or 16-bit width can be set for each channel. |
| Memory allocation | Address access area | Supports up to 64MB memory area<br>0x60000000 to 0x63FFFFFF (Max. 16MB for each CS) |
| | CS control | 4 channels (ECS0_N pin, ECS1_N pin, ECS2_N pin, ECS3_N pin) |
| External bus control | Clock output | This function can output clock synchronizing with bus cycles. |
| | Internal wait function | A wait can be inserted up to 15 cycles for each channel. |
| | External wait function | In addition to the internal wait function, the wait cycle can be extended by EWAIT_N pin. |
| | | Active "Low" or active "High" is selectable. |
| | ALE assert time setting function | An assert time can be selected from 1, 2, 3, or 5 cycles for each channel. |
| | Setup cycle insertion function | Read or Write setup cycle can be inserted for each channel. |
| | Recovery cycle insertion function | In consecutive external bus cycles, a dummy cycle up to 8 clocks can be inserted and this dummy cycle can be specified for each channel. |
| | | Address/ data hold cycle insertion at ECSn_N pin, ERD_N pin, EWR_N pin |
| | Bus expansion function | Internal wait, ALE assert time, Setup cycle and Recovery cycle can be expanded double or quadruple. (Used in common in all channels) |

# 2. Configuration

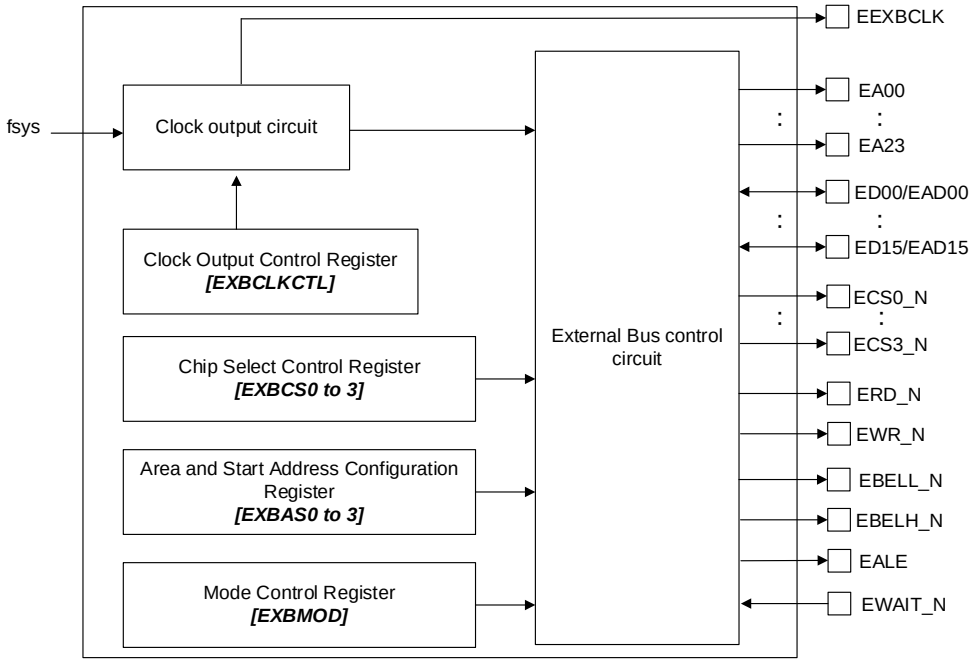


**Figure 2.1 EBIF Block Diagram**

**Table 2.1 List of Signals**

| No | Signal name | | I/O | Related Reference manual |
|---|---|---|---|---|
| 1 | fsys | System clock | Input | Clock Control and Operation Mode |
| 2 | EEXBCLK | Clock output pin | Output | Product Information, Input/Output Ports |
| 3 | EA00 to EA23 | Address bus output pins | Output | Product Information, Input/Output Ports |
| 4 | ED00 to ED15 | Data bus input/output pins (Separate bus mode) | I/O | Product Information, Input/Output Ports |
| | EAD00 to EAD15 | Address/Data bus input/output pins (Multiplexed bus mode) | I/O | Product Information, Input/Output Ports |
| 5 | ERD_N | Read strobe output pin | Output | Product Information, Input/Output Ports |
| 6 | EWR_N | Write strobe output pin | Output | Product Information, Input/Output Ports |
| 7 | ECS0_N to ECS3_N | Chip select output pins | Output | Product Information, Input/Output Ports |
| 8 | EBELL_N | Lower Byte enable output pin | Output | Product Information, Input/Output Ports |
| 9 | EBELH_N | Upper Byte enable output pin | Output | Product Information, Input/Output Ports |
| 10 | EALE | Address latch enable output pin | Output | Product Information, Input/Output Ports |
| 11 | EWAIT_N | Wait input pin | Input | Product Information, Input/Output Ports |

# 3. Function and Operation

## 3.1. Clock supply

When using EBIF, set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB***]), and fc supply stop register (***[CGFCEN]***).
An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

## 3.2. Data format

This section describes the relationship between internal registers of MCU and external bus interfaces.

### 3.2.1. Word access

- **16-bit bus width**

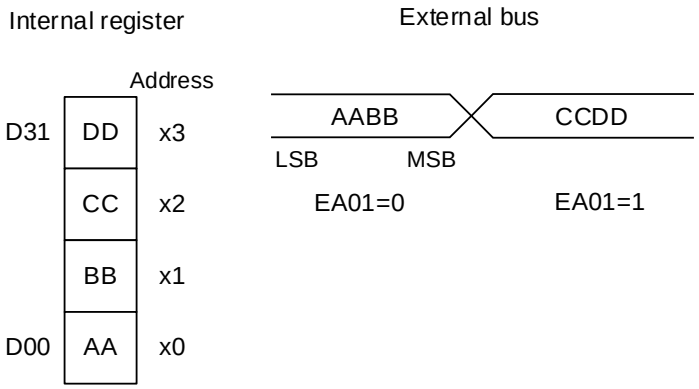


**Figure 3.1 Word access (16-bit bus width)**

- **8-bit bus width**

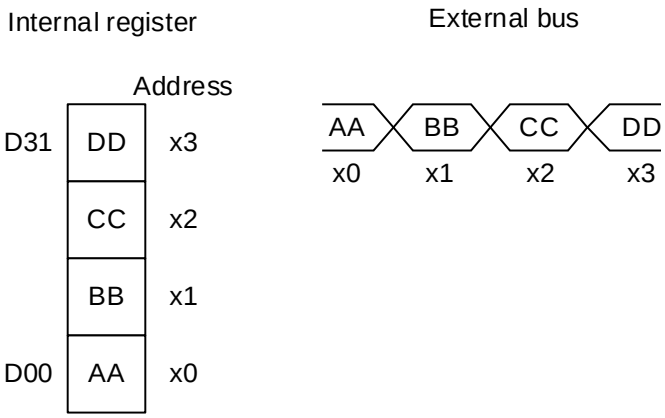


**Figure 3.2 Word access (8-bit bus width)**

### 3.2.2. Half word access

- **16-bit bus width**

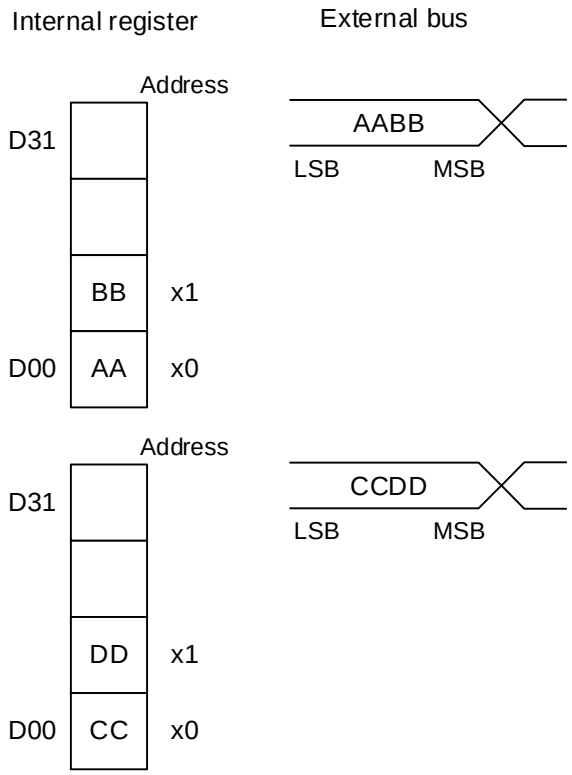


**Figure 3.3 Half word access (16-bit bus width)**)

- **8-bit bus width**

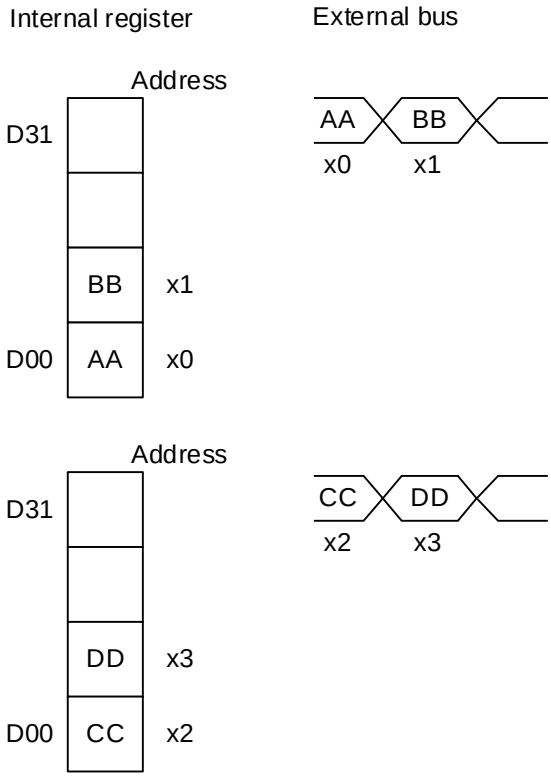


**Figure 3.4 Half word access (8-bit bus width)**

### 3.2.3. Byte access

- **16-bit bus width**

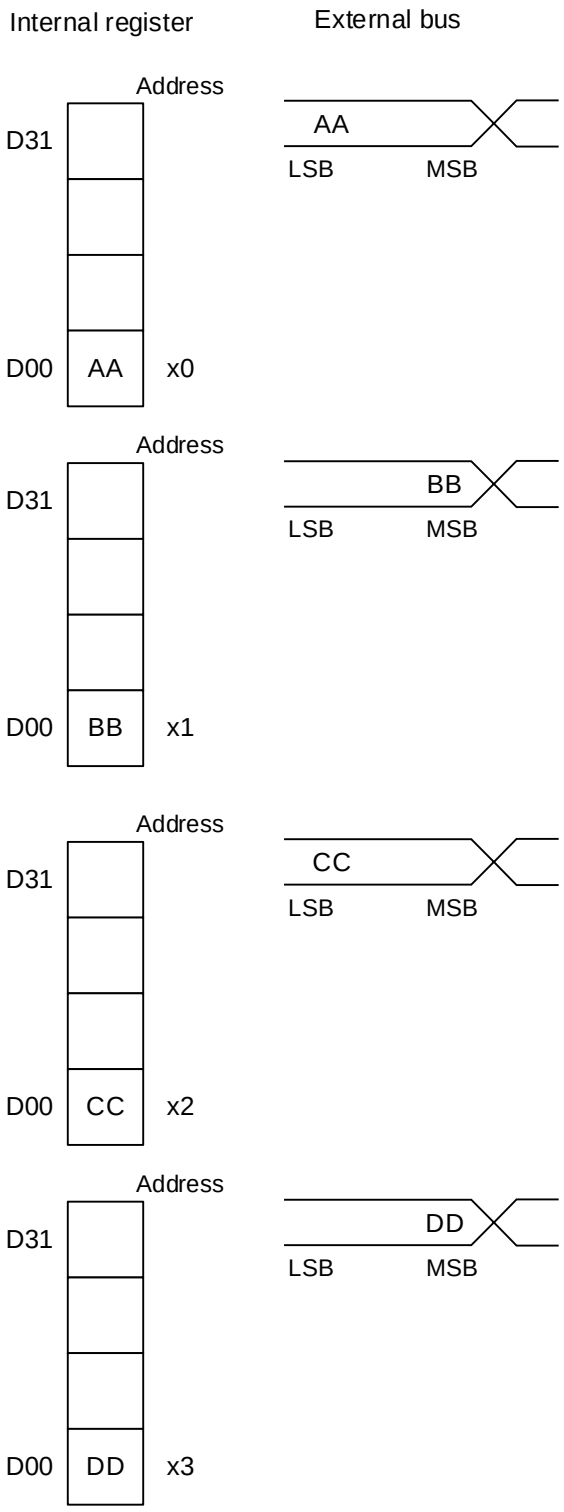


**Figure 3.5 Byte access (16-bit bus width)**

- **8-bit bus width**

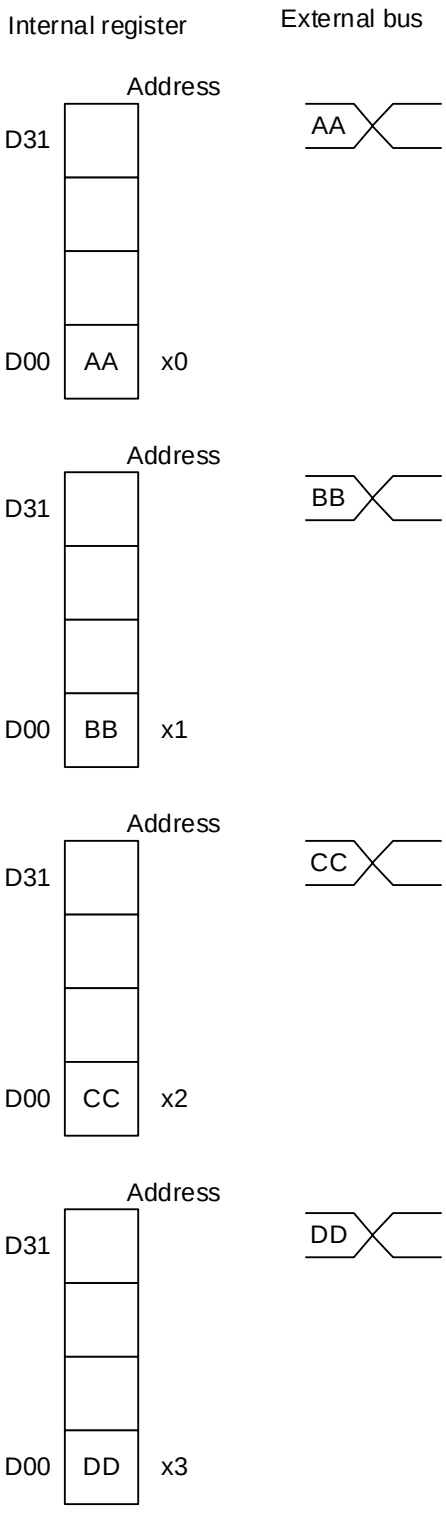


**Figure 3.6 Byte access (8-bit bus width)**

## 3.3. Clock Output Circuit

The external bus operation is synchronous with the bus clock. When the clock output function is not used, the system clock fsys is used as the bus clock. And when the clock output function is used, the bus clock should be one of the divided clocks of the system clock fsys (the dividing ratio is 2, 4, and 8).

### 3.3.1. Setting of Clock Output

The settings of the clock output should be done in Clock output control register ***[EXBCLKCTL]*** and the port register of EEXBCLK pin. For the details of the port register setting, refer to “Input/Output Ports” in Reference manual.

#### 3.3.1.1. Frequency of Clock Output

***[EXBCLKCTL]***<CLKDIV> use for setting of Clock Output.

**Table 3.1 Clock Output**

| <CLKDIV[1:0]> | 01 | 10 | 11 |
|---|---|---|---|
| Dividing ratio / fsys[MHz] | 2 | 4 | 8 |
| 160 | (80.0) | (40.0) | 20.0 |
| 140 | (70.0) | (35.0) | 17.5 |
| 120 | (60.0) | 30.0 | 15.0 |
| 100 | (50.0) | 25.0 | 12.5 |
| 80 | (40.0) | 20.0 | 10.0 |
| 60 | 30.0 | 15.0 | 7.5 |
| 40 | 20.0 | 10.0 | 5.0 |

Note: Output Clock frequency should be set under 30MHz. Do not set combination of fsys and a dividing ratio as the gray cell of Table 3.1.

#### 3.3.1.2. How to Set Clock Output Function

The Clock Output function is set as follows. A setup is performed while the external bus cycle has not occurred.

- Frequency setting and enable output

  1. Set a dividing ratio by ***[EXBCLKCTL]***<CLKDIV>
  2. Set "1" to ***[EXBCLKCTL]***<CLKEN>.
  3. Set the function of EEXBCLK pin in the corresponding port register.

- Changing a dividing ratio

  1. Disable EEXBCLK output by output control register.
  2. Set "0" to ***[EXBCLKCTL]***<CLKEN>.
  3. Change a dividing ratio by ***[EXBCLKCTL]***<CLKDIV>.
  4. Set "1" to ***[EXBCLKCTL]***<CLKEN>.
  5. Enable EEXBCLK output by output control register.

  Note: A clock waveform may be disturbed when EEXBCLK output is enabled/disabled.

# 3.4. External Bus Control Circuit

## 3.4.1. Setting of Address pins and Data pins

The EBIF has separate bus mode and multiplexed bus modes.

***[EXBMOD]*** is used for setting of External Bus. ***[EXBMOD]***<EXBSEL> is set to "1", the separate bus mode is selected, ***[EXBMOD]***<EXBSEL> is set to "0", the multiplexed bus mode is selected.

Table 3.2 shows the address pins and the data pins used in each mode. For the information about the connection to an external device, refer to “Product Information” and "Input/Output Ports" in Reference manual.

**Table 3.2 Bus Mode, Address and Data Pins**

| Separate bus mode *[EXBMOD]*<EXBSEL>=1 | Multiplexed bus mode *[EXBMOD]*<EXBSEL>=0 |
|---|---|
| EA00 to EA07 | - |
| EA08 to EA15 | - |
| EA16 to EA23 | EA16 to EA23 |
| ED00 to ED15 | EAD00 to EAD15 |

When access is changed from the external area to internal area, the address buses maintain the address output of the previous external area and the data buses become high impedance.

### 3.4.2. Separate Bus Mode

This section describes various bus timings. The timing diagrams shown below assumes that the address buses are EA23 through EA00 and the data buses are ED15 through ED00. Bus cycle (tsys) becomes one cycle of fsys when the Clock Output function is not used.

It becomes one cycle of Clock Output specified with ***[EXBCLKCTL]***<CLKDIV> when the Clock Output function is used.

#### 3.4.2.1. Basic Bus Operation

External bus cycle is basically 3 clocks. Figure 3.7 shows a read bus timing and Figure 3.8 shows a write bus timing. When access is changed from the external area to internal area, the address buses maintain the address output of the previous external area in these figures.

Additionally, data buses are in a state of high impedance and control signals such as ERD_N pin and EWR_N pin do not become active.

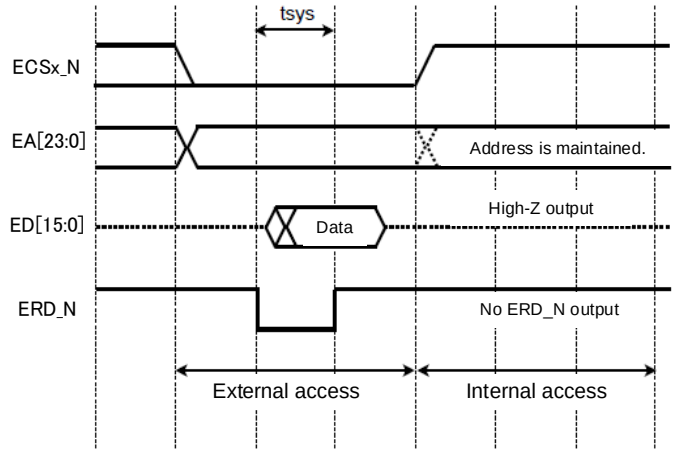


**Figure 3.7 Read Operation Timing**

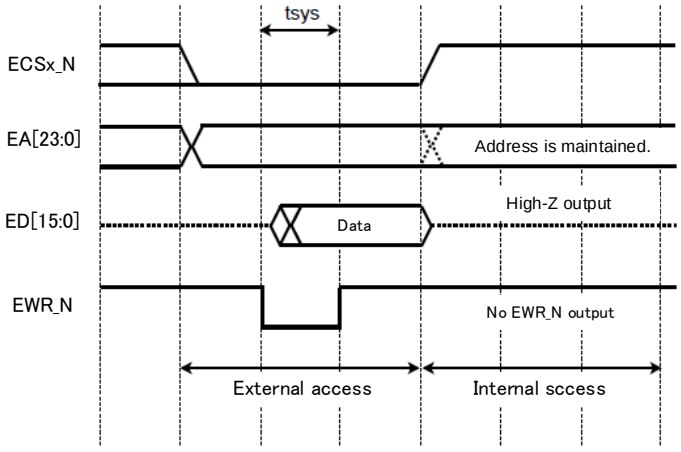


**Figure 3.8 Write Operation Timing**

### 3.4.2.2. Wait Insertion

A wait cycle can be inserted for each channel. The following waits can be inserted.

- An internal wait of up to 15 clocks (automatic insertion)
- An external wait by WAIT signal

#### (1) Internal Wait

To use the internal wait function, set "0" to ***[EXBCSn]***<WAIT>. The setting of the number of waits can be set using ***[EXBCSn]***<CSIW>.

Figure 3.9 and Figure 3.10 show the read timing diagrams in which internal waits have been inserted.

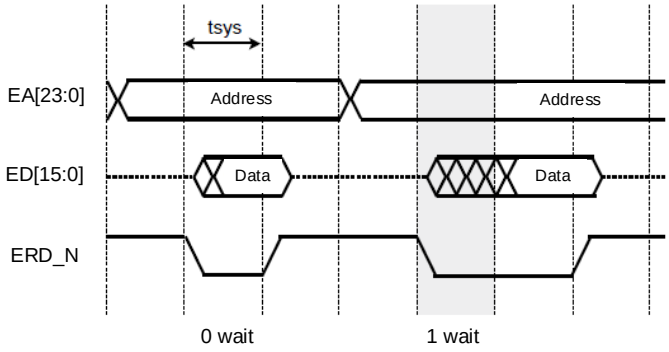


**Figure 3.9 Read Operation Timing (0 wait, Internal 1 wait)**

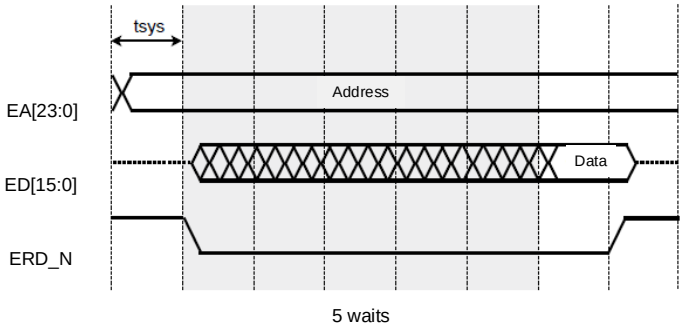


**Figure 3.10 Read Operation Timing (Internal 5 waits)**

Figure 3.11 and Figure 3.12 show the read/write operation timing diagrams in which internal 0 and 2 waits have been inserted.

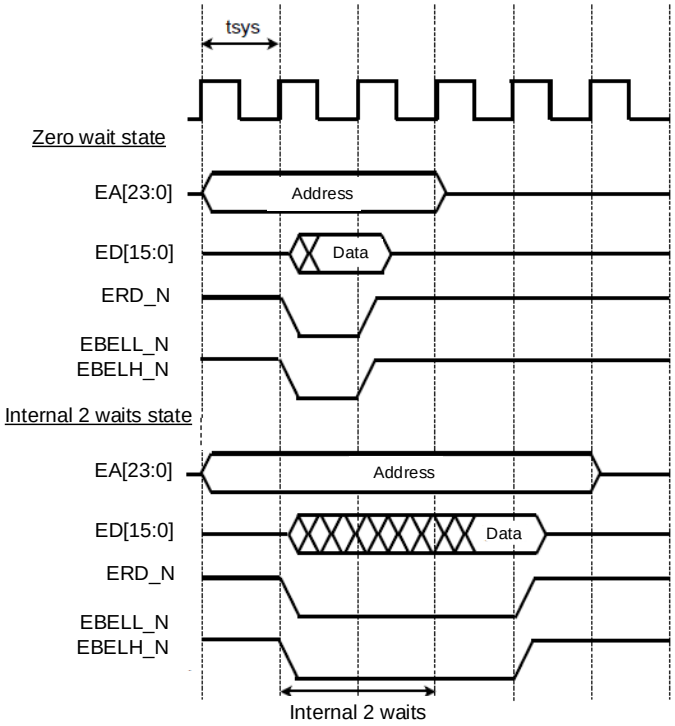


**Figure 3.11 Read operation timing (Internal wait)**

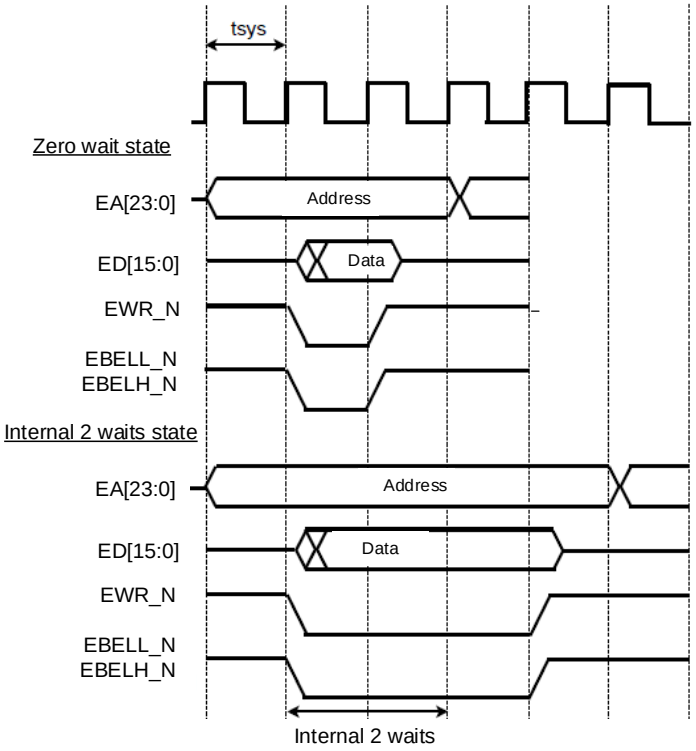


**Figure 3.12 Write operation timing (Internal wait)**

### (2) External Wait

To use the external wait function, set "1" to ***[EXBCSn]***<WAIT>. The external wait function is used combined with WAIT signal and internal wait function.

When an external wait is set, a WAIT signal is sampled on bus cycle clock after the internal wait defined by ***[EXBCSn]***<CSIW> has elapsed. As long as the signal is enabled, a wait cycle is inserted. When external wait function is used, set "3 or more internal waits.

Active "Low" or "High" of WAIT is determined by ***[EXBCSn]***<WSEL>. Input a WAIT signal at least 2 cycles before starting sampling.

Figure 3.13 and Figure 3.14 show wait timing diagrams in which an external wait is inserted. In this case, WAIT signal is set as active "Low".

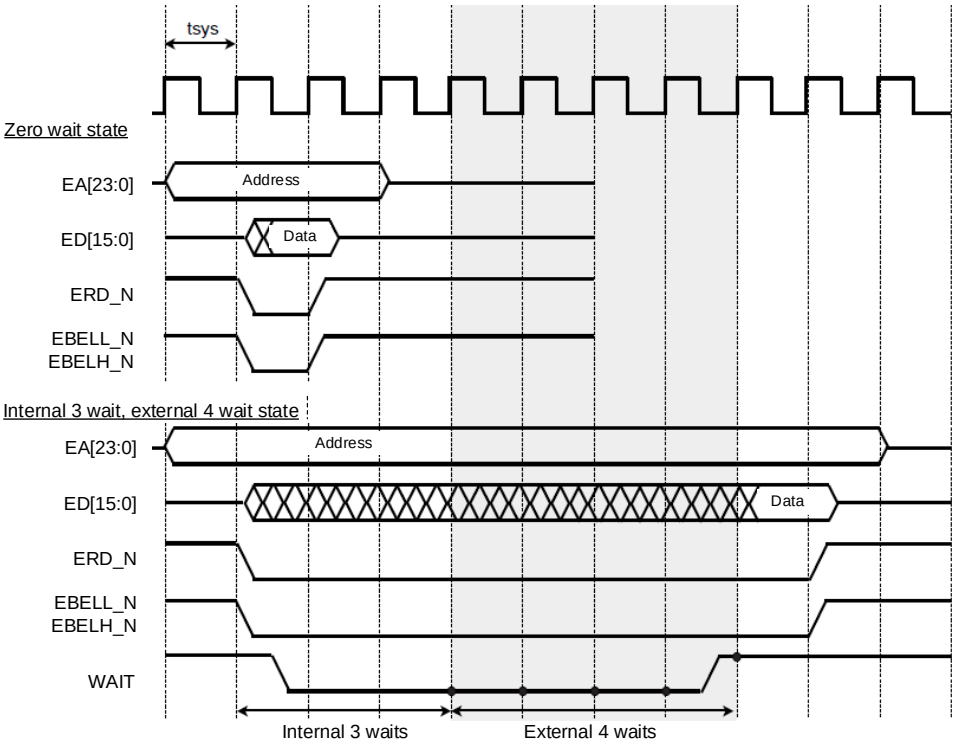


**Figure 3.13 Read operation timing (External wait)**

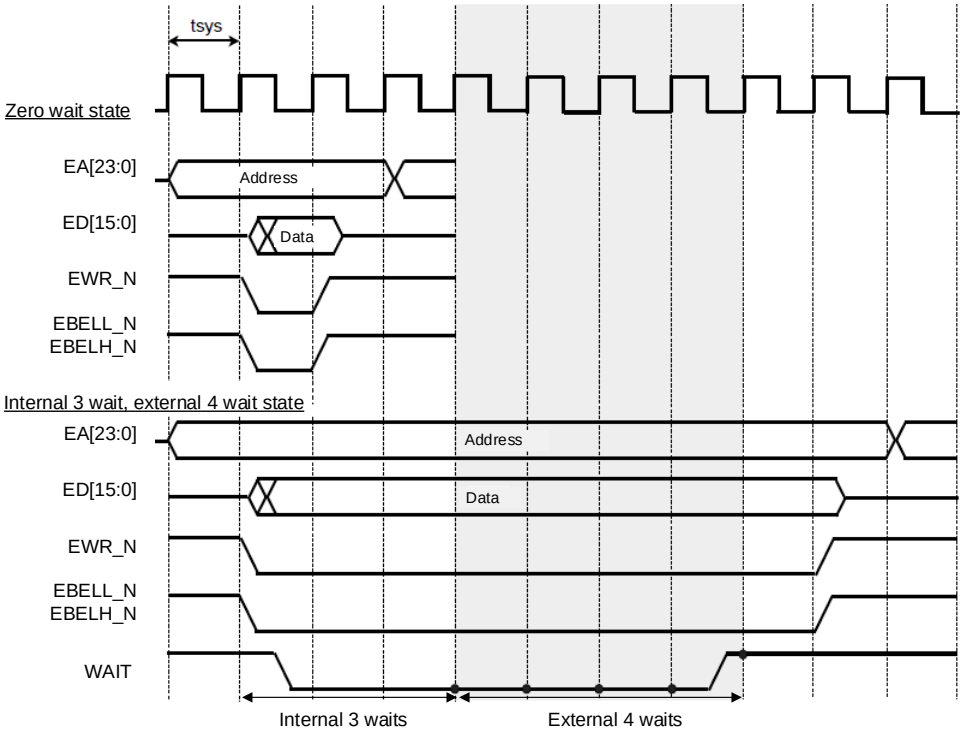


**Figure 3.14 Write operation timing (External wait)**

### 3.4.2.3. Read and Write Recovery Time

When access to external areas occurs consecutively, a dummy cycle can be inserted as recovery time.

A dummy cycle can be inserted in both a read and write cycle. The dummy cycle insertion can be set by ***[EXBCSn]***<WRR> (write recovery cycle) and ***[EXBCSn]***<RDR> (read recovery cycle). As for the number of dummy cycle, 0 through 6 and 8 system clocks can be specified for each channel. Figure 3.15 shows the timing of recovery time insertion.

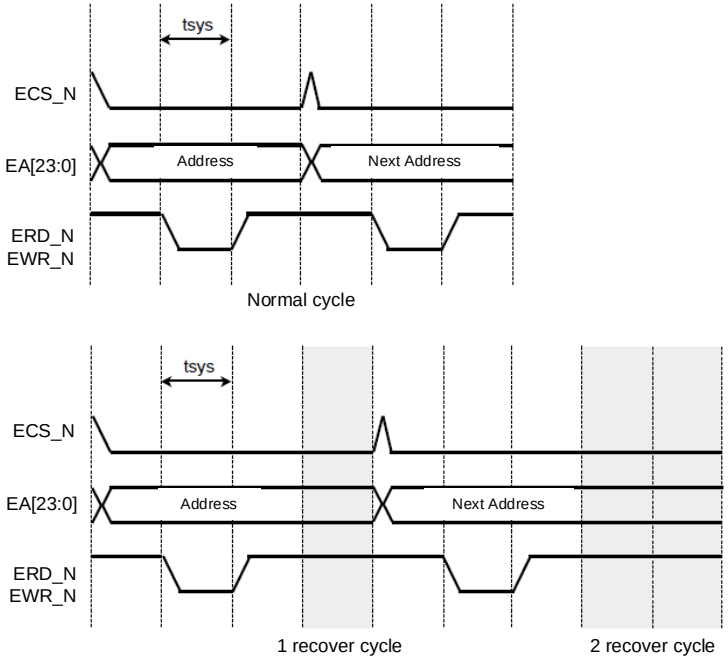


**Figure 3.15 Timing of recovery time insertion**

### 3.4.2.4. Chip Select Recovery Time

When access to external areas occurs consecutively, a dummy cycle can be inserted as recovery time.

The dummy cycle insertion can be set by ***[EXBCSn]***<CSR>. As for the number of dummy cycles, 0, 1, 2, 4 system clocks can be specified for each channel. Figure 3.16 shows the timing of recovery time insertion.

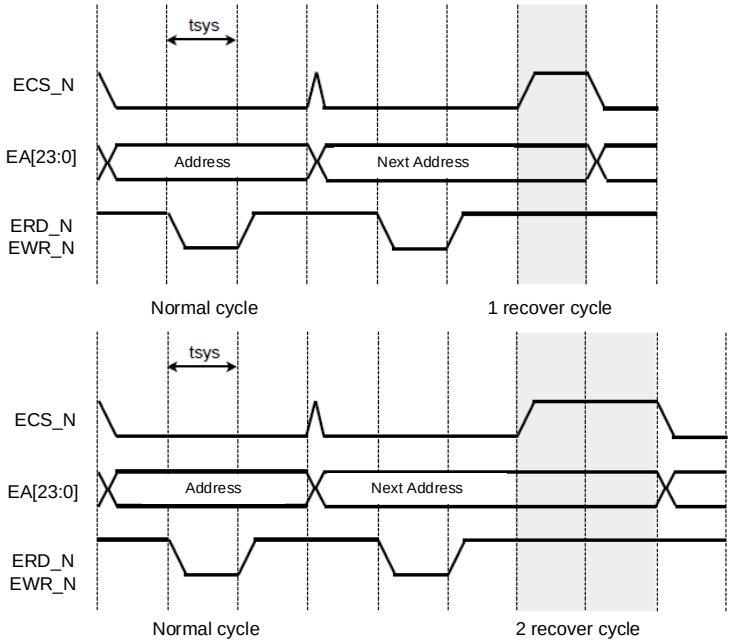


**Figure 3.16 Timing of chip select recovery time insertion**

### 3.4.2.5. Read and Write Setup Cycle

A read and a write setup cycle can be inserted for each channel. The following cycle can be inserted.

- Internal read and write setup cycles up to 4 clocks.(automatic insertion)

The setting of the number of setup cycles can be set using ***[EXBCSn]***<WRS> and <RDS>.
Figure 3.17 shows the timing diagrams in which read or write setup cycles have been inserted.

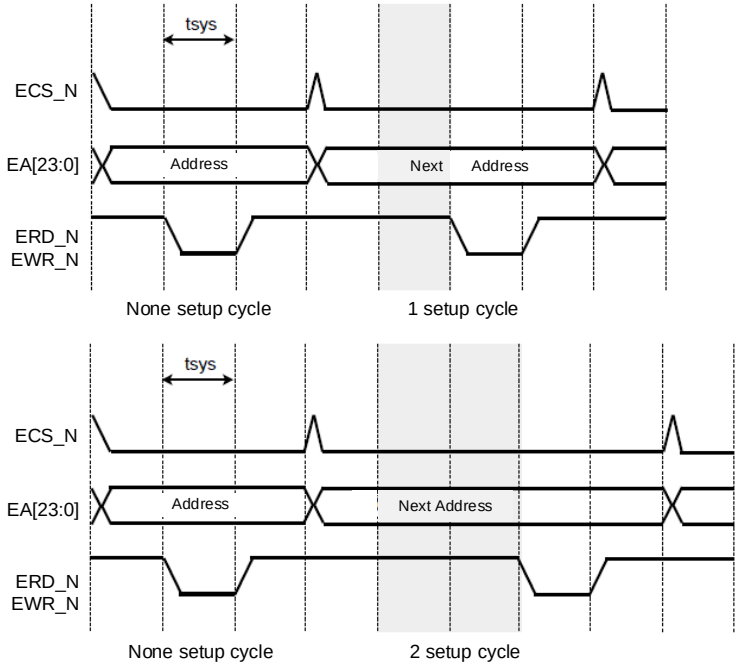


**Figure 3.17 Timing of read and write setup time insertion**

### 3.4.3. Multiplexed Bus Mode

This section describes various bus timings. The timing diagram shown below assumes that the address buses are EA23 through EA16 and address/data buses are EAD15 through EAD00. Bus cycle (tsys) becomes one cycle of fsys when the Clock Output function is not used.

It becomes one cycle of Clock Output specified with ***[EXBCLKCTL]***<CLKDIV> when the Clock Output function is used.

#### 3.4.3.1. Basic Bus Operation

External bus cycle is basically 4 clocks. Figure 3.18 shows a read bus timing and Figure 3.19 shows a write bus timing. When access is changed from the external area to internal area, the address buses maintain the address output of the previous external area and the EALE does not output latch pulses as shown in these figures.

Additionally, data buses are in a state of high impedance and control signals such as ERD_N pin and EWR_N pin do not become active.

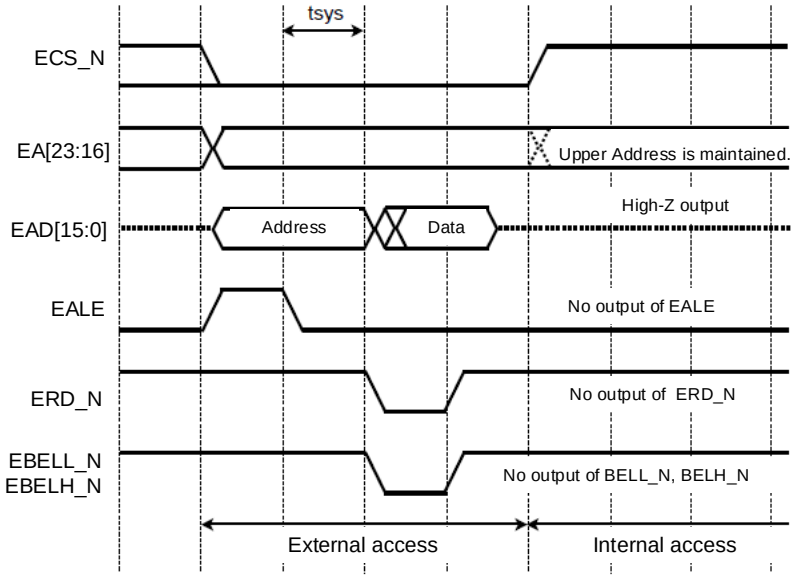


**Figure 3.18 Read operation timing**

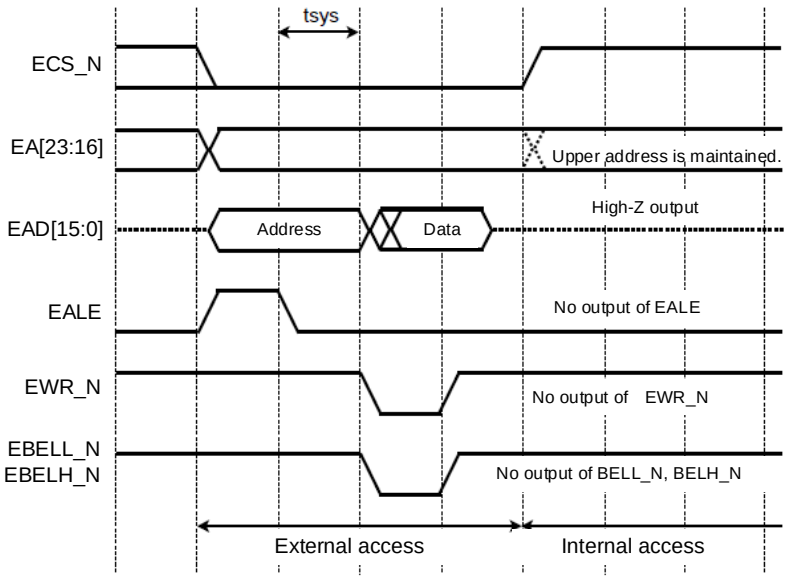


**Figure 3.19 Write operation timing**

### 3.4.3.2. Wait Insertion

A wait cycle can be inserted for each channel. The following waits can be inserted.

- An internal wait of up to 15 clocks (automatic insertion).
- An external wait by WAIT signal

#### (1) Internal Wait

To use the internal wait function, set "0" to ***[EXBCSn]***<WAIT>. The setting of the number of waits can be set using ***[EXBCSn]***<CSIW>.

Figure 3.20 and Figure 3.21 show the read and write timing diagrams in which internal non wait and 2 waits have been inserted for multiplexed bus.

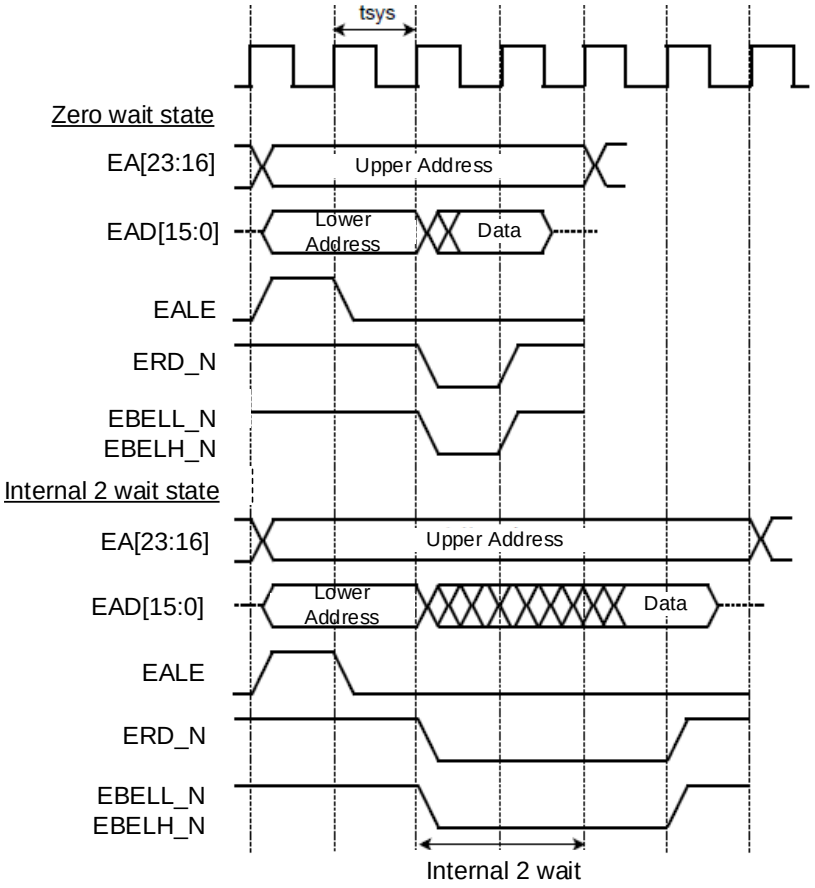


**Figure 3.20 Read operation timing (0 wait, Internal 2 wait)**

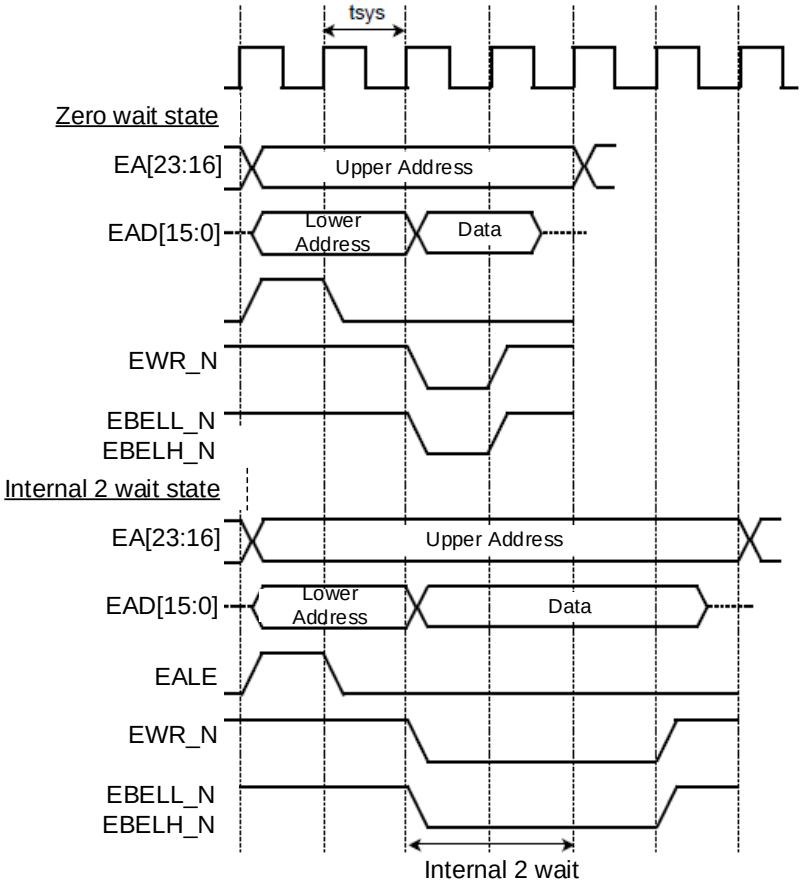


**Figure 3.21 Write operation timing (0 wait, Internal 2 wait)**

### (2) External Wait

To use the external wait function, set "1" to ***[EXBCSn]***<WAIT>. The external wait function is used combining with WAIT signal and internal wait function.

When an external wait is set, a WAIT signal is sampled on bus cycle clock after the internal wait defined by ***[EXBCSn]***<CSIW> has elapsed. As long as the signal is enabled, wait cycle is inserted. When the external wait function is used, set "3" or more internal waits.

Active "Low" or "High" of WAIT is determined by ***[EXBCSn]***<WSEL>. Input a WAIT signal at least 2 cycles before starting sampling.

Figure 3.22 and Figure 3.23 show timing diagrams in which external waits have been inserted. In this case, the WAIT signal is set as active "Low".

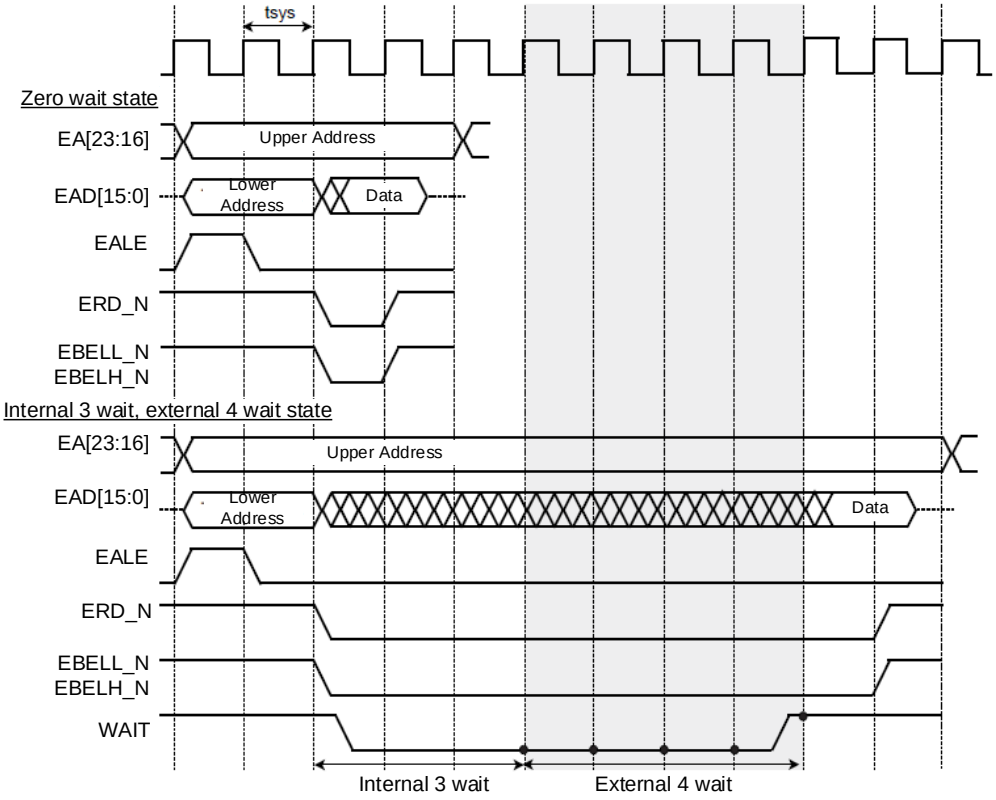


**Figure 3.22 Read operation timing (External wait)**

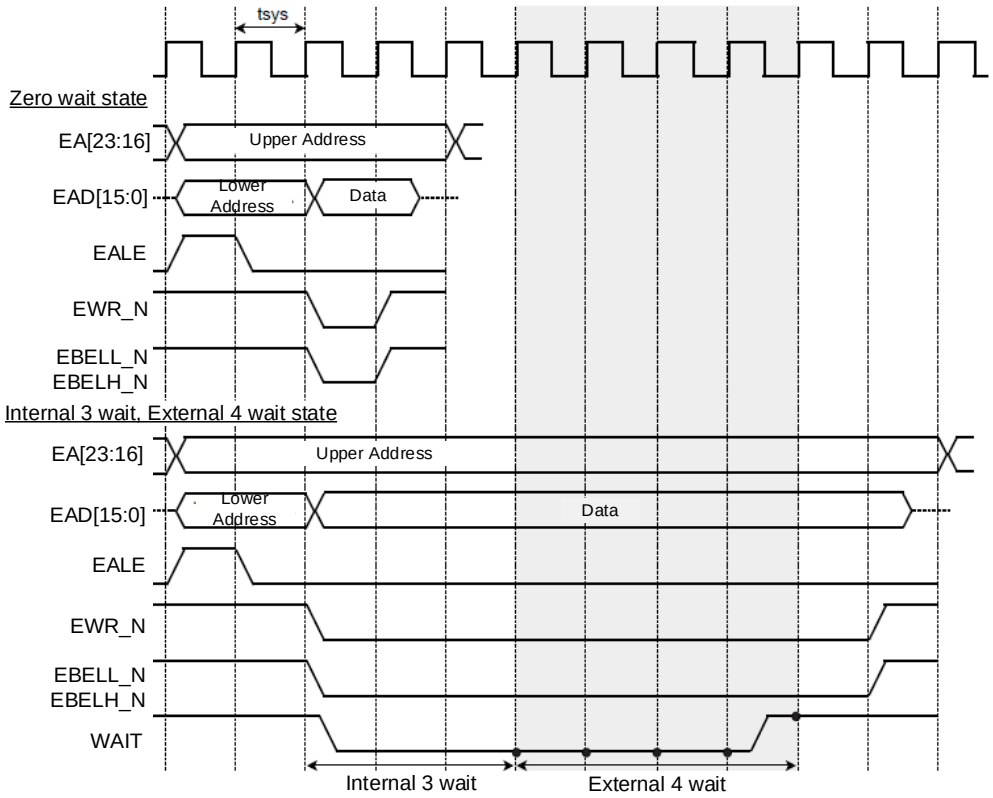


**Figure 3.23 Write operation timing (External wait)**

### 3.4.3.3. ALE Assert Time

An ALE assert time can be selected from 1, 2, 3 or 5 clocks of system clock by setting of ***[EXBCSn]***<ALEW>. In the default setting, ERD_N or EWR_N signal is asserted after 2 system clocks after the address is generated.

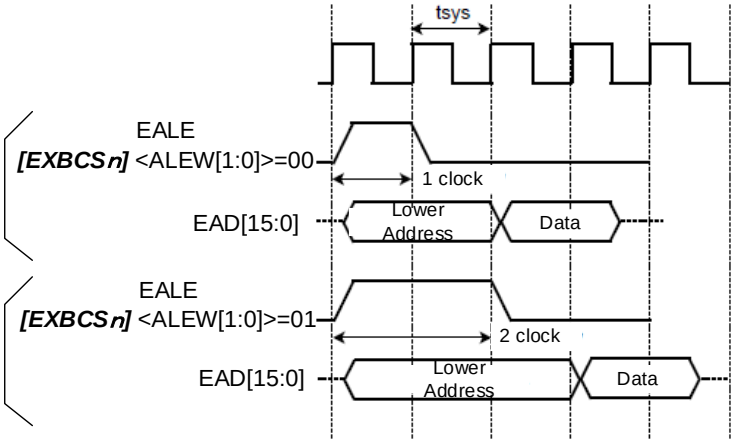


**Figure 3.24 ALE asserted time**

Figure 3.25 shows the timing when the ALE assert time is 1 clock and 2 clocks.

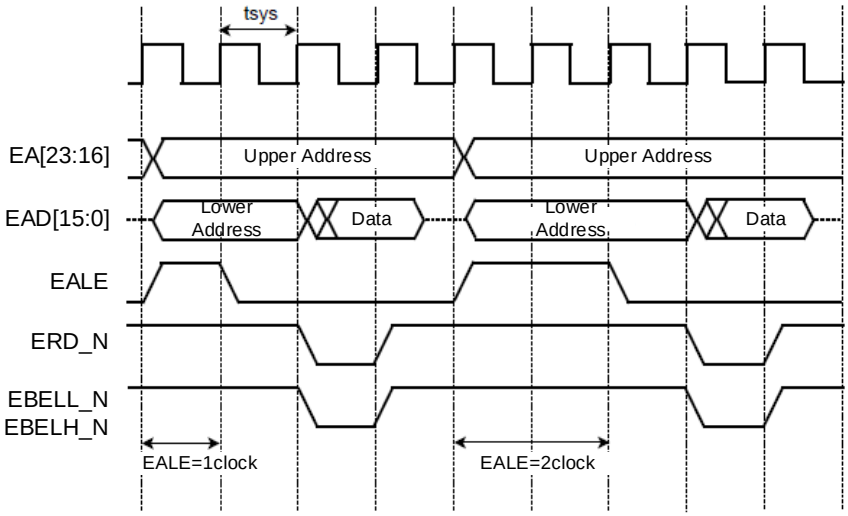


**Figure 3.25 Read Operation Timing (When the EALE is 1 Clock or 2 Clocks)**

### 3.4.3.4. Read and Write Recovery Time

When access to external areas occurs consecutively, a dummy cycle can be inserted as recovery time.

A dummy cycle can be inserted in both a read and a write cycle. The dummy cycle insertion can be set by ***[EXBCSn]***<WRR> (write recovery cycle) and <RDR> (read recovery cycle). As for the number of dummy cycles, 0 through 6 and 8 system clocks can be specified for each channel. Figure 3.26 shows the timing of recovery time insertion.

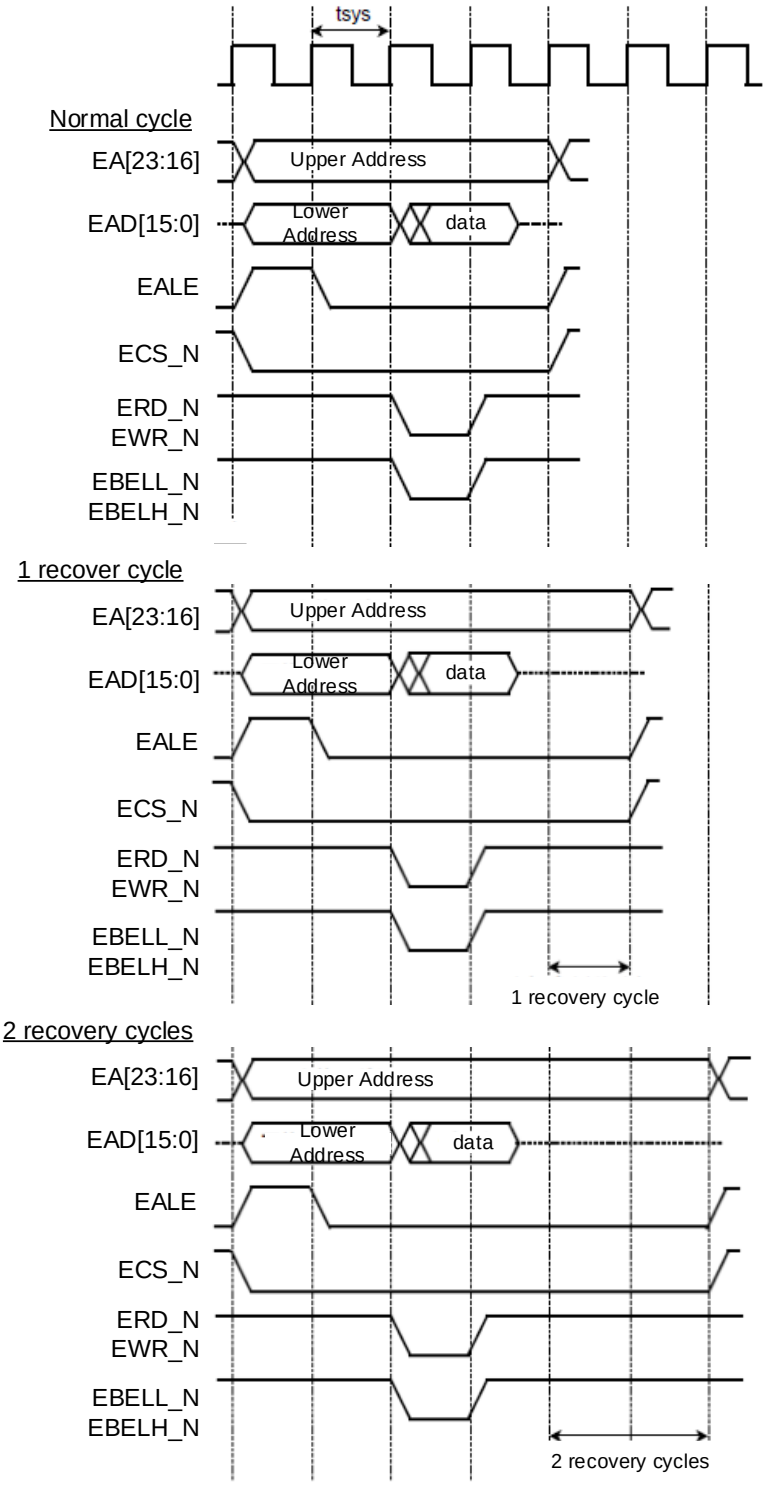


**Figure 3.26 Timing of Recovery Time Insertion**

### 3.4.3.5. Chip Select Recovery Time

When access to external areas occurs consecutively, a dummy cycle can be inserted as recovery time.

The dummy cycle insertion can be set by ***[EXBCSn]***<CSR>. As for the number of dummy cycles, 0, 1, 2, 4 system clocks can be specified for each channel. Figure 3.27 shows the timing of recovery time insertion.

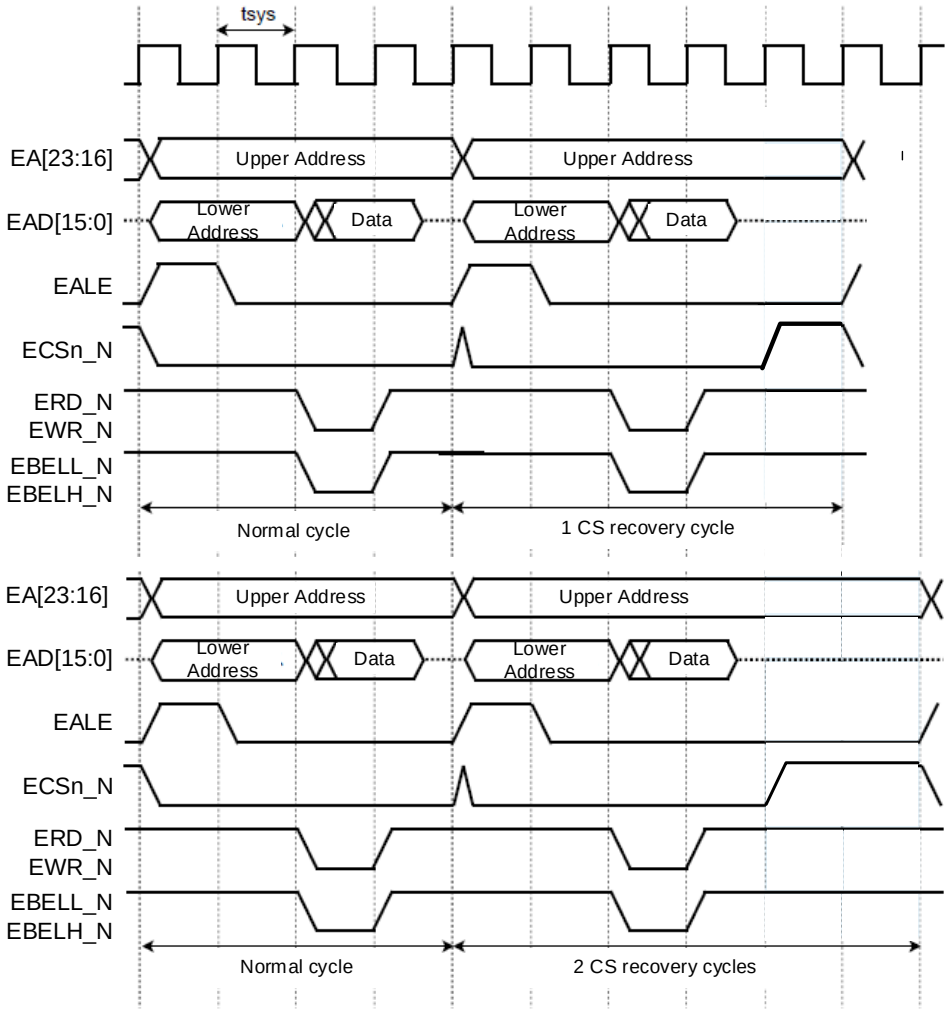


**Figure 3.27 Timing of recovery Time insertion (When the EALE is 1 Clock)**

### 3.4.3.6. Read and Write Setup Cycle

A read and a write setup cycle can be inserted for each channel. The following cycle can be inserted.

- Internal read and write setup cycle up to 4 clocks.(automatic insertion)

The setting of the number of setup cycles can be set using ***[EXBCSn]***<WRS> and <RDS>.
Figure 3.28 shows the timing diagrams in which read or write setup cycle has been inserted.

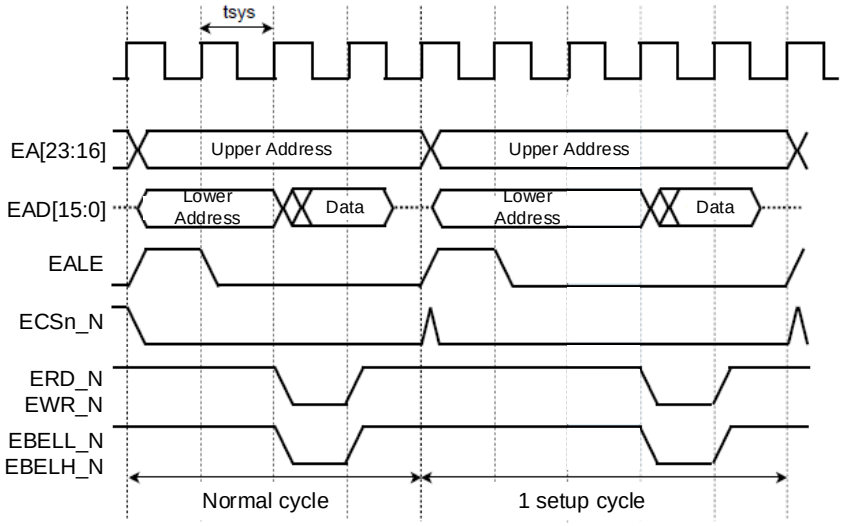


**Figure 3.28 Timing of read or write setup time insertion**

# 4. Registers

## 4.1. List of Registers

The control registers and their addresses are shown as follows.

| Function | | Channel/Unit | Base address | |
|---|---|---|---|---|
| | | | TYPE 1 | TYPE 2 |
| External Bus Interface | EBIF | - | 0x4005C000 | 0x40076000 |

Note: The channel/unit and base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

| Register Name | | Address (Base+) |
|---|---|---|
| Mode Control Register | ***[EXBMOD]*** | 0x0000 |
| Area and Start Address Configuration Register 0 | ***[EXBAS0]*** | 0x0010 |
| Area and Start Address Configuration Register 1 | ***[EXBAS1]*** | 0x0014 |
| Area and Start Address Configuration Register 2 | ***[EXBAS2]*** | 0x0018 |
| Area and Start Address Configuration Register 3 | ***[EXBAS3]*** | 0x001C |
| Chip Select Control Register 0 | ***[EXBCS0]*** | 0x0040 |
| Chip Select Control Register 1 | ***[EXBCS1]*** | 0x0044 |
| Chip Select Control Register 2 | ***[EXBCS2]*** | 0x0048 |
| Chip Select Control Register 3 | ***[EXBCS3]*** | 0x004C |
| Clock Output Control Register | ***[EXBCLKCTL]*** | 0x0060 |

Note: Reading/writing registers are allowed only in the unit of word (32-bit).

## 4.2. Details of Registers

### 4.2.1. *[EXBMOD]* (Mode Control Register)

| Bit | Bit Symbol | After Reset | Type | Function |
|---|---|---|---|---|
| 31:3 | - | 0 | R | Read as “0” |
| 2:1 | EXBWAIT[1:0] | 00 | R/W | Bus cycle wait extension<br>00: No extension<br>01: Double<br>10: Quadruple<br>11: Prohibited<br><br>These bits are used to set the setup, wait and recovery of the bus cycle to be double or quadruple.<br><br>For example, in case of the read setup cycle is set as 2 cycles at the time of <EXBWAIT>=00 setup. When a setting change to <EXBWAIT>=01(Double), it will be extended to 4 cycles. Also when a setting change to <EXBWAIT>=10(Quadruple), it will be extended to 8 cycles.<br>Extended cycles are the read / write setup, chip select / read / write recovery and ALE assert time / internal wait cycle set by the ***[EXBCSn]*** register, and <EXBWAIT> (2 times / 4 times) setting value. |
| 0 | EXBSEL | 0 | R/W | Select external bus mode (Note)<br>0: Multiplexed bus mode<br>1: Separate bus mode |

Note: Do not change the setting of external bus mode in operating the external bus access.

### 4.2.2. *[EXBAS0] [EXBAS1] [EXBAS2] [EXBAS3]*(Area and Start Address Configuration Register n)

| Bit | Bit Symbol | After Reset | Type | Function |
|---|---|---|---|---|
| 31:16 | SA[15:0] | 0x0000 | R/W | Start address of Chip select (Note)<br><br>Set the start address of address EA31 to EA16(<SA[15]> to <SA[0]>). Table 4.1shows the start address settings for each area size. |
| 15:8 | - | 0 | R | Read as “0” |
| 7:0 | EXAR[7:0] | 0x00 | R/W | Chip select (ECSn_N) address area size.<br>00000000: 16M byte<br>00000001: 8M byte<br>00000010: 4M byte<br>00000011: 2M byte<br>00000100: 1M byte<br>00000101: 512K byte<br>00000110: 256K byte<br>00000111: 128K byte<br>00001000: 64K byte<br>Other than the above settings: Prohibited |

Note: When accessing the external bus address area, if the address area to be accessed is mapped to multiple chip select address area, activate the chip select signal according to the priority order below;

High priority >> ECS0_N > ECS1_N > ECS2_N > ECS3_N >> Low priority

**Table 4.1 <SA[15:0]> Start address setting**

| Address area size of chip selection | <SA[15:0]> | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 16M byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8M byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4M byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | 0 | 0 | 0 | 0 | 0 | 0 |
| 2M byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | 0 | 0 | 0 | 0 | 0 |
| 1M byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | 0 | 0 | 0 | 0 |
| 512K byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | x | 0 | 0 | 0 |
| 256K byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | 0 | 0 |
| 128K byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | 0 |
| 64K byte | 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | x |

x : Optional

### 4.2.3. *[EXBCS0] [EXBCS1] [EXBCS2] [EXBCS3]* (Chip Select Control Register n)

| Bit | Bit Symbol | After Reset | Type | Function |
|---|---|---|---|---|
| 31:30 | CSR[1:0] | 01 | R/W | Chip select (ECSn_N) Recovery cycle<br>00: None<br>01: 1 cycle<br>10: 2 cycles<br>11: 4 cycles |
| 29:27 | WRR[2:0] | 001 | R/W | Write (EWR_N) Recovery cycle<br>000: None<br>001: 1 cycle<br>010: 2 cycles<br>011: 3 cycles,<br>100: 4 cycles<br>101: 5 cycles<br>110: 6 cycles<br>111: 8 cycles |
| 26:24 | RDR[2:0] | 001 | R/W | Read (ERD_N) Recovery cycle<br>000: None<br>001: 1 cycle<br>010: 2 cycles<br>011: 3 cycles,<br>100: 4 cycles<br>101: 5 cycles<br>110: 6 cycles<br>111: 8 cycles |
| 23:22 | - | 0 | R | Read as “0” |
| 21:20 | ALEW[1:0] | 01 | R/W | ALE wait time for multiplex bus mode<br>00: No Wait<br>01: 1 cycles<br>10: 2 cycles<br>11: 4 cycles |
| 19:18 | WRS[1:0] | 01 | R/W | Write (EWR_N) Setup cycle<br>00: None<br>01: 1 cycle<br>10: 2 cycles<br>11: 4 cycles |
| 17:16 | RDS[1:0] | 01 | R/W | Read (ERD_N) Setup cycle<br>00: None<br>01: 1 cycle<br>10: 2 cycles<br>11: 4 cycles |
| 15:14 | - | 0 | R | Read as “0” |
| 13 | WSEL | 0 | R/W | Wait signal active level selection<br>0: Active "Low"<br>1: Active "High" |
| 12 | WAIT | 0 | R/W | Wait insertion function selection<br>0: Internal wait<br>1: External wait |

| Bit | Bit Symbol | After Reset | Type | Function |
|---|---|---|---|---|
| 11:8 | CSIW[3:0] | 0010 | R/W | Selection of number of waits<br>0000: 0 waits<br>0001: 1 wait<br>0010: 2 waits<br>0011: 3 waits<br>0100: 4 waits<br>0101: 5 waits<br>0110: 6 waits<br>0111: 7 waits<br>1000: 8 waits<br>1001: 9 waits<br>1010: 10 waits<br>1011: 11waits<br>1100: 12 waits<br>1101: 13 waits<br>1110: 14 waits<br>1111: 15 waits<br><br>When <WAIT> is "0", fixed number of wait is specified.<br>When <WAIT> is "1", the number of internal waits in external wait function are specified. When an external wait is used, specify at least 3 waits. |
| 7:3 | - | 0 | R | Read as “0” |
| 2:1 | CSW[2:1] | 01 | R/W | Data bus width<br>00: 8-bit<br>01: 16-bit<br>Other than the above settings: Prohibited |
| 0 | CSW0 | 0 | R/W | CS enable control<br>0: Disable<br>1: Enable |

### 4.2.4. *[EXBCLKCTL]* (Clock Output Control Register)

| Bit | Bit Symbol | After Reset | Type | Function |
|---|---|---|---|---|
| 31:3 | - | 0 | R | Read as “0” |
| 2:1 | CLKDIV[1:0] | 00 | R/W | Clock dividing ratio setting for Clock Output (Note1)(Note2)<br>00: Reserved<br>01: fsys/2<br>10: fsys/4<br>11: fsys/8 |
| 0 | CLKEN | 0 | R/W | Clock output control (Note3)<br>0: Disabled<br>1: Enabled |

Note1: Setting of <CLKDIV> should be done under <CLKEN>=0.

Note2: Output Clock frequency should be set under 30MHz.

Note3: A clock waveform may be disturbed when clock output is enabled/disabled

# 5. Usage example

## 5.1. Connection Example of external 16-bit SRAM and NOR-Flash in Asynchronous Separate bus mode

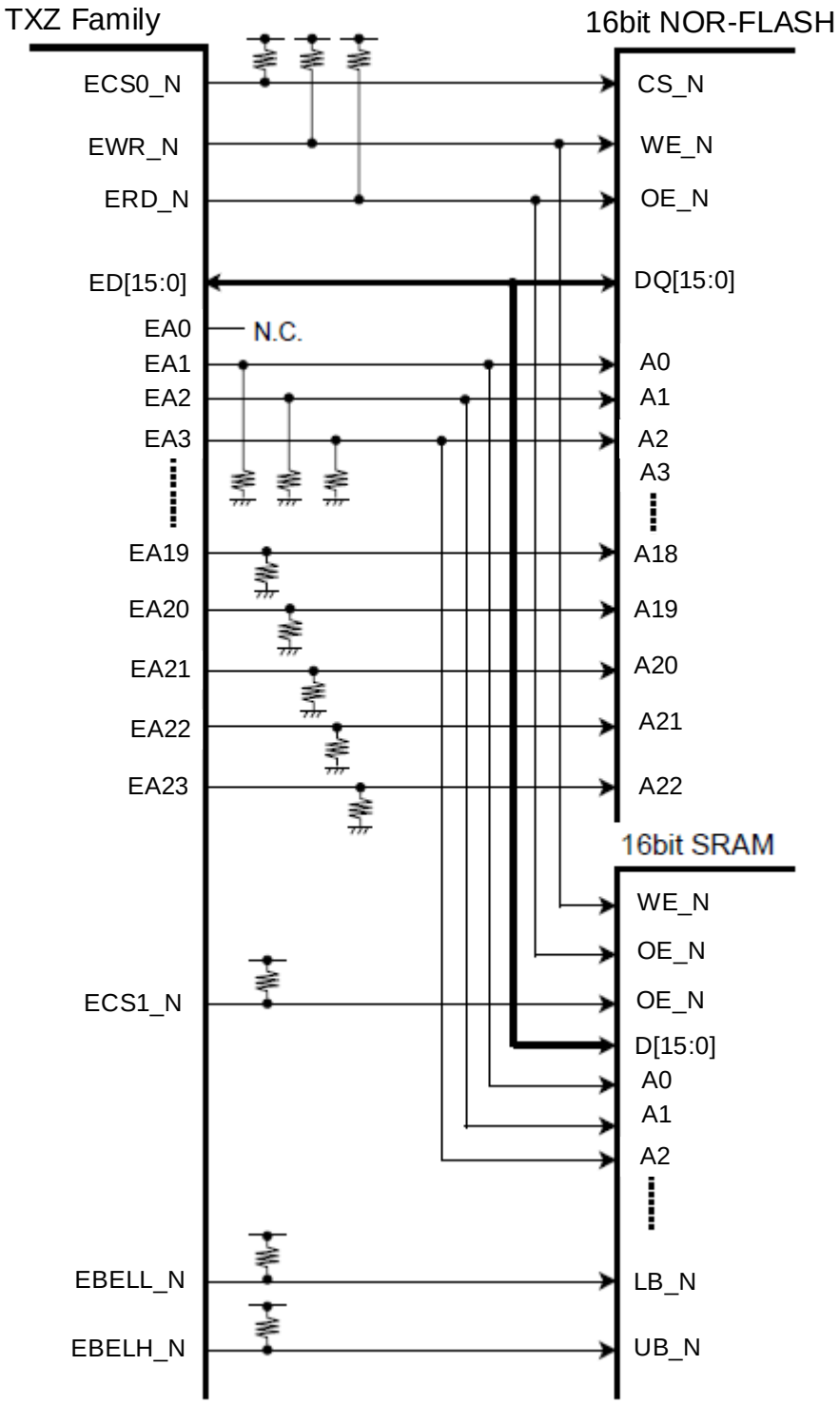


**Figure 5.1 Connection Example of external 16-bit SRAM and NOR-Flash (Asynchronous separate bus)**

## 5.2. Connection Example of External 16-bit SRAM and NOR-Flash in Synchronous multiplexed bus mode

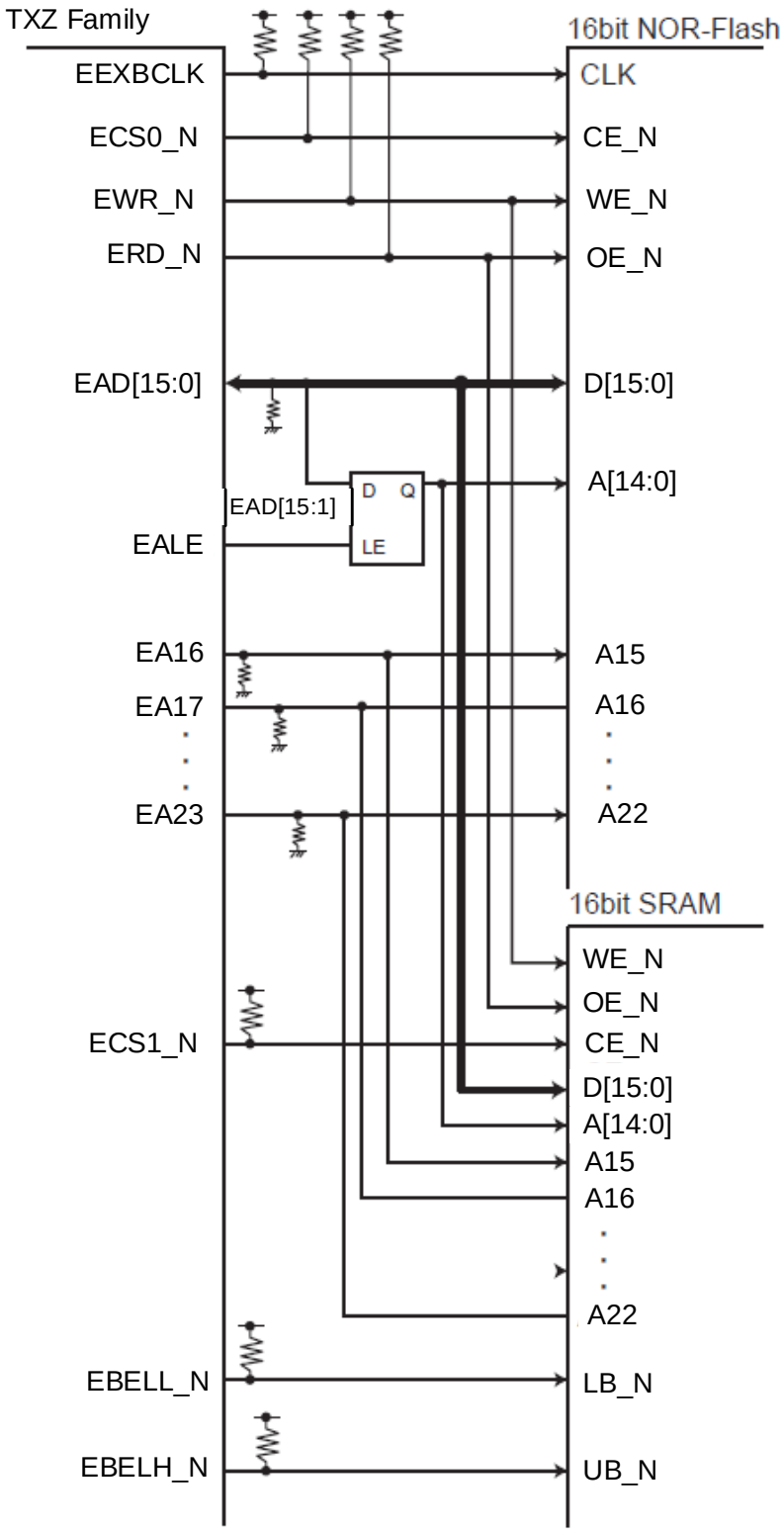


**Figure 5.2 Connection Example of external 16-bit SRAM and NOR-Flash (Synchronous multiplexed bus)**

# 6. Revision History

**Table 6.1 Revision history**

| Revision | Date | Description |
|---|---|---|
| 1.0 | 2018-01-30 | First release |
| 1.1 | 2018-06-26 | - 2. Configuration<br>Modified signal name of EBELL_N/EBELH_N.<br>- 3.4.2.2 Wait Insertion<br>Modified explanation of 1st paragraph<br>-3.4.2.5 Read and Write Setup Cycle<br>Modified explanation of 1st paragraph<br>Modified ***[EXBCSn]***<RDS> to <RDS> in 3rd line<br>- 3.4.3.2 Wait Insertion<br>Modified explanation of 1st paragraph<br>- 3.4.3.4 Read and Write Recovery Time<br>Modified ***[EXBCSn]***<RDS> to <RDR> in 3rd line<br>- 3.4.3.6 Read and Write Setup Cycle<br>Modified explanation of 1st paragraph<br>Modified ***[EXBCSn]***<RDS> to <RDS> in 3rd line<br>-4.2.4 ***[EXBLKCTL]***<br>Modified explanation of Note3, EEXBCKL to clock output.<br>- 5.1 Connection Example of external 16-bit SRAM and NOR-Flash in Asynchronous Separate mode<br>Modified Non-synchronous to Asynchronous |
| 1.2 | 2018-11-12 | - Conventions<br>Modified description of trademark<br>- 4.2.3 ***[EXBCS0][EXBCS1][EXBCS2][EXBCS3]***<br>Corrected parameter of <ALEW[1:0]><br>- 5.1 Connection Example of external 16-bit SRAM and NOR-Flash in Asynchronous Separate bus mode<br>Changed title<br>- 5.2 Connection Example of External 16-bit SRAM and NOR-Flash in Synchronous multiplexed bus mode<br>Changed title |

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