32-bit RISC Microcontroller

TXZ Family

Reference Manual
Consumer Electronics Control Circuit (CEC-A)

Revision 1.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

CEC	Consumer Electronics Control
EOM	End Of Message

1. Outline

The brief outline of CEC Control Circuit (CEC) function is shown as follows.

Function Classification	Function	Operation
HDMI standard	-	Compliant with Version 1.3a.
Reception control	Sampling clock	Selected from the followings: - fs (Low speed clock) - CECxCLKTRG (Timer trigger for Clock source)
	Noise reduction	Noise canceling time is adjustable. -"High" detection time Sampling clock selected from 1 to 4 consecutive observations. -"Low" detection time Sampling clock selected from 1 to 4 consecutive observations.
	Data reception	Data reception per Byte - Flexible data sampling point - Data reception is available even when a Destination address does not match.
	Error detection	- Cycle error (Max/Min) - ACK collision - Waveform error
Transmission control	Data transmission	Data transmission per Byte - Triggered by auto-detection of bus free state
	Waveform adjustment	Transmission waveform adjustment - The timing of a rising edge and the cycle time are adjustable.
	Error detection	- Arbitration lost - ACK response error
Interrupt	Transmission interrupt	- Start transmission - Transmission end - Arbitration lost - ACK Error - Underrun
	Reception interrupt	- Reception completed - Start bit - Max cycle error - Min cycle error - ACK collision - Overrun - Waveform error

2. Configuration

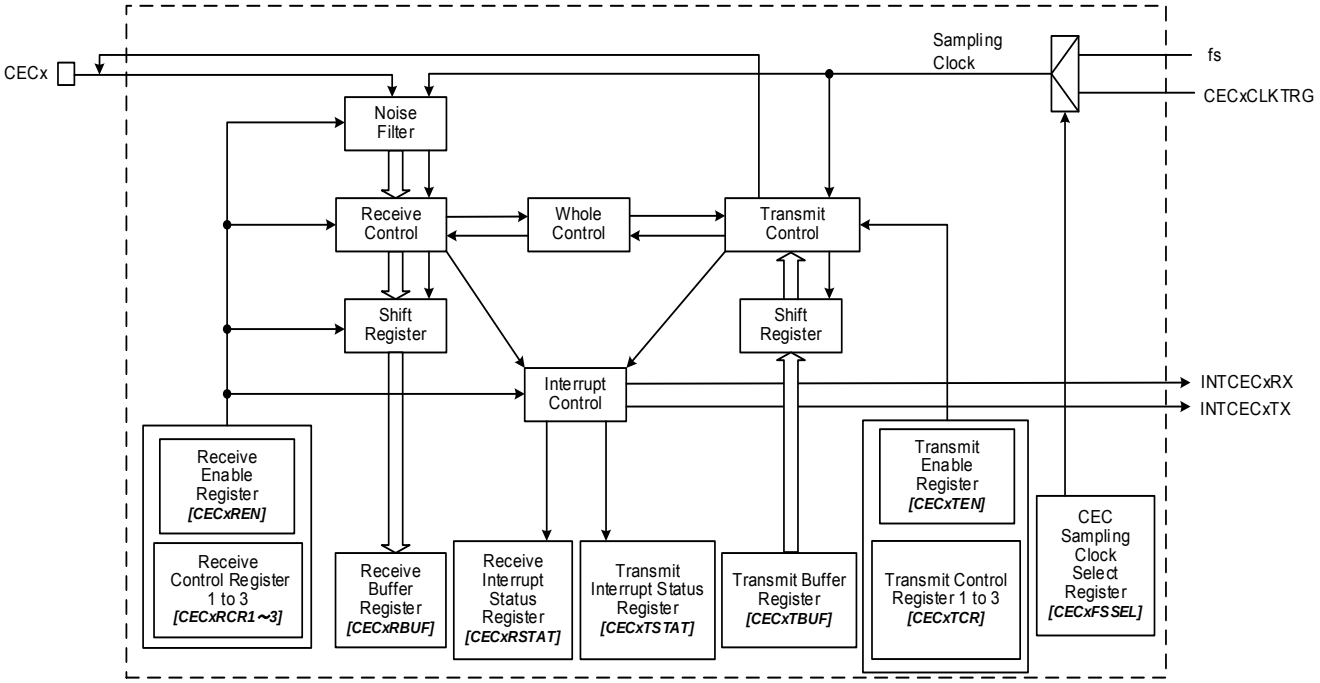

Figure 2.1 CEC block diagram

Table 2.1 List of signals

No.	Signal name	Description	I/O	Reference manual
1	CECx	CECx data input and output pin	I/O	Product Information
2	fs	Low speed clock	Input	Clock Control and Operation Mode
3	CECxCLKTRG	Timer trigger for Clock source	Input	Product Information
4	INTCECxRX	CEC ch x reception interrupt	Output	Exception
5	INTCECxTX	CEC ch x transmission interrupt	Output	Exception

3. Function and Operations

3.1. Clock Supply

When CEC is used, setting of system supply stop register of fsys / fc is unnecessary.
For the source clock, see Table 3.1.

Table 3.1 Source clock

Source clock	Supply setting
Low speed clock (fs)	Supply the low speed clock (fs). For details, refer to "Clock Control and Operation Mode" of the reference manual..
Timer trigger (CECxCLKTRG)	Please set the clock supply according to the function of the connection destination. Refer to "Product Information" of the reference manual for details of connection destination.

3.2. Sampling Clock

The sampling clock for CEC signal can be selected from 32.768kHz low speed clock (fs) and the timer trigger for the clock source (CECxCLKTRG).

The setting of the sampling clock should be done in ***[CECxFSSEL]***.

Before the sampling clock is changed, the stop state of the data transfer should be confirmed in ***[CECxREN]*** <CECREN> and ***[CECxTEN]***<CECTEN>. Then ***[CECxFSSEL]*** should be set. It should be set before the settings of the other registers related to CEC are done.

For the timer which is connected to the timer trigger for the clock source (CECxCLKTRG), refer to "Product Information" in Reference manual.

3.3. Reception

3.3.1. Basic Operation

When a start bit is detected, a start bit interruption generates. By generating start bit interruption, ***[CECxRSTAT]*** <CECRISTA> is set. The start bit interrupt is generated when the ***[CECxRCR3]*** <CECRSTAEN> is set to "1".
If one byte data, EOM bit and ACK bit are received, the received data is stored in ***[CECxRBUF]*** register, and a received interruption generates. By generating the received interruption, ***[CECxRSTAT]***<CECRIEND> is set.
In the ***[CECxRBUF]*** register, 8 bit data, EOM bit and ACK bit are stored. The ACK bit is not generated in the CEC circuit internally. This bit is generated from observations of CEC signal same as other data.
After one data block is received, receiving operation continues until detecting that the last block of data with EOM bit is set to "1". Detecting the end of last block, CEC becomes the start bit waiting mode.
Detecting an error during data reception causes an error interrupt, and CEC waits for the next start bit.
The received data is discarded.

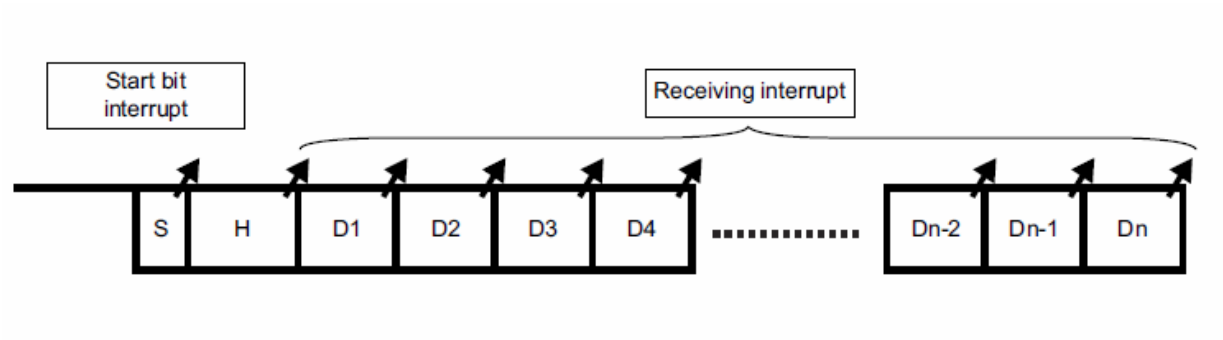

Figure 3.1 Basic operation of CEC (Reception)

3.3.2. Start or Stop of Counter Operation and Preparation of Reception

Before receiving data, reception settings to the Logical Address Register (***[CECxADD]***), the Receive Control Register 1 (***[CECxRCR1]***), the Receive Control Register 2 (***[CECxRCR2]***) and the Receive Control Register 3 (***[CECxRCR3]***) are required.

3.3.2.1. Logical Address Configuration

Configure logical address assigned to this product to the ***[CECxADD]*** register. Multiple addresses can be set simultaneously since every bit in this register corresponds with each address.

Note: A broadcast message is received regardless of the ***[CECxADD]*** register setting, ACK response with logic "1" is made. By allocating a logical address of a device to 15, logical "0" is sent as an ACK response to the broadcast message.

3.3.2.2. Noise Cancellation Time

The noise cancellation time is configurable with the <CECHNC[1:0]> and <CECLNC[2:0]> bits of the ***[CECxRCR1]*** register. It is considered as noise if "High" or "Low" of the same number as the specified value are not sampled. You can configure the time to detect "High" and "Low" respectively.

Note: Use ***[CECxRCR1]***<CECLNC[2:0]> in the same settings used for ***[CECxTCR]***<CECDTRS>.

The noise cancelation is done to the CEC signal which is sampled by the sampling clock. A CEC line is monitored at each rising edge of a sampling clock. In the case that the CEC line is changed from "High" to "Low", the change is fully recognized if "Low" levels of the same number as specified in the <CECLNC[2:0]> bit are monitored. In the case that the CEC line is changed from "Low" to "High", the change is fully recognized if "High" of the same number as specified in the <CECHNC[1:0]> bit are sampled.

Figure 3.2 shows the operation of the case that a noise canceling is done at <CECHNC[1:0]> = 10 (3 samplings) and <CECLNC[2:0]> = 011 (4 samplings). Using the noise canceling, the result signal output is shifted from "1" to "0" after "0" is sampled four times continuously in the sampled signal and is shifted from "0" to "1" after "1" is sampled three times continuously.

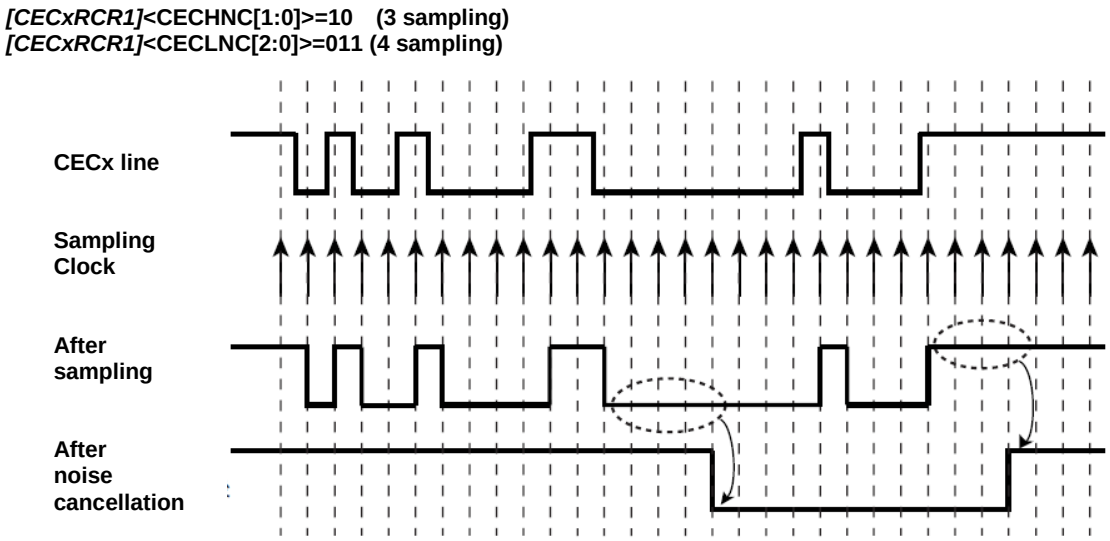

Figure 3.2 Noise cancelation

3.3.2.3. Cycle Error

Configure ***[CECxRCR1]***<CECMIN> and <CECMAX> bits to detect a cycle error.

A cycle error can be detected from each sampling clock cycle between the ranges -4/fs to +3/fs by the unit of 1/fs from the minimum value (67/fs, approx. 2.045ms) or the maximum value (90/fs approx. 2.747ms).

Detecting an error during data reception causes an error interrupt, and CEC waits for the next start bit. The received data is discarded.

3.3.2.4. Point of Determining Data

Configure the ***[CECxRCR1]***<CECDAT> bit for the point of determining the data as "0" or "1".
Base time is 34/fs (approx.1.038ms) from the start point and also configurable ±6/fs by the unit (2/fs).

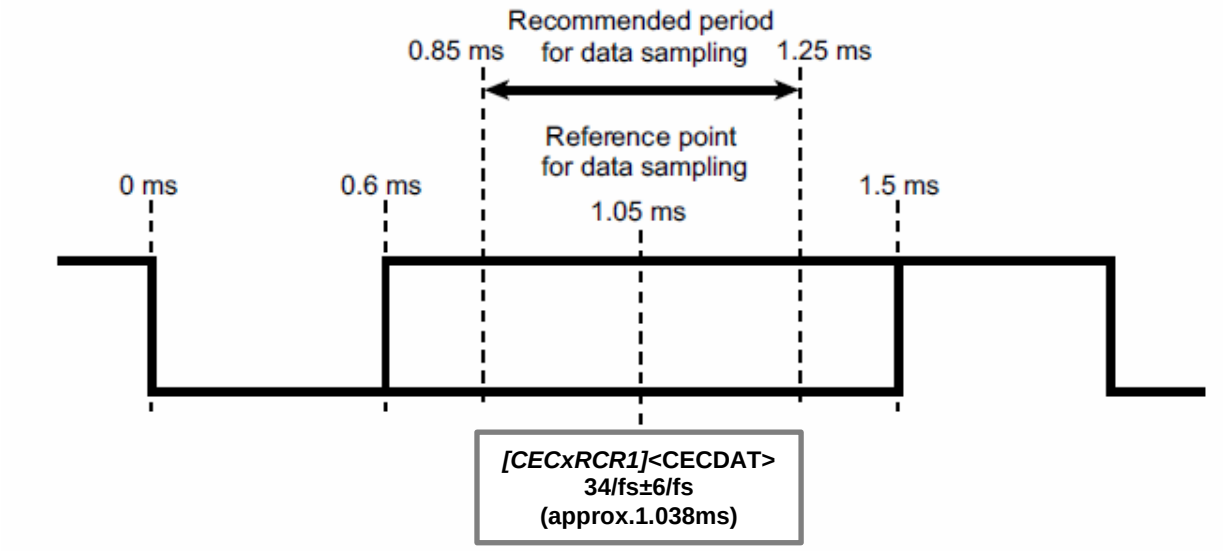

Figure 3.3 Data sampling timing recommended by the standard

3.3.2.5. ACK Response

For data blocks, when the destination address matches the address set in the ***[CECxADD]*** register, it is possible to arbitrarily enable / disable the ACK response of logic "0" with ***[CECxRCR1]*** <CECACKDIS>.

Logical "0" is sent to the header block as an ACK response regardless of the bit setting of <CECACKDIS>.

The following lists the ACK responses.

"Yes" indicates that CEC outputs "0" as a response to the ACK signal from a transmission device (ACK bit: logical "0"). "No" indicates that CEC does not output "0" as a response to the ACK signal from a transmission device (ACK bit: logical "1").

Table 3.2 ACK response operation

Register setting		Header block address		Data block address	
		Conformity	Discrepancy	Conformity	Discrepancy
[CECxRCR1] <CECACKDIS>	0 (Responding logical "0")	Yes	No	Yes	No
	1 (Not responding logical "0")			No	No

The following describes the ACK response timing.
When the falling edge of the ACK bit from the initiator is detected, this IP outputs "Low" for approximately 1.526 ms. The start time of detecting "Low" is specified with ***[CECxRCR1]***<CECLNC> that sets the noise canceling time.

Note: Use ***[CECxRCR1]***<CECLNC> in the same settings used for ***[CECxTCR]***<CECDTRS>.

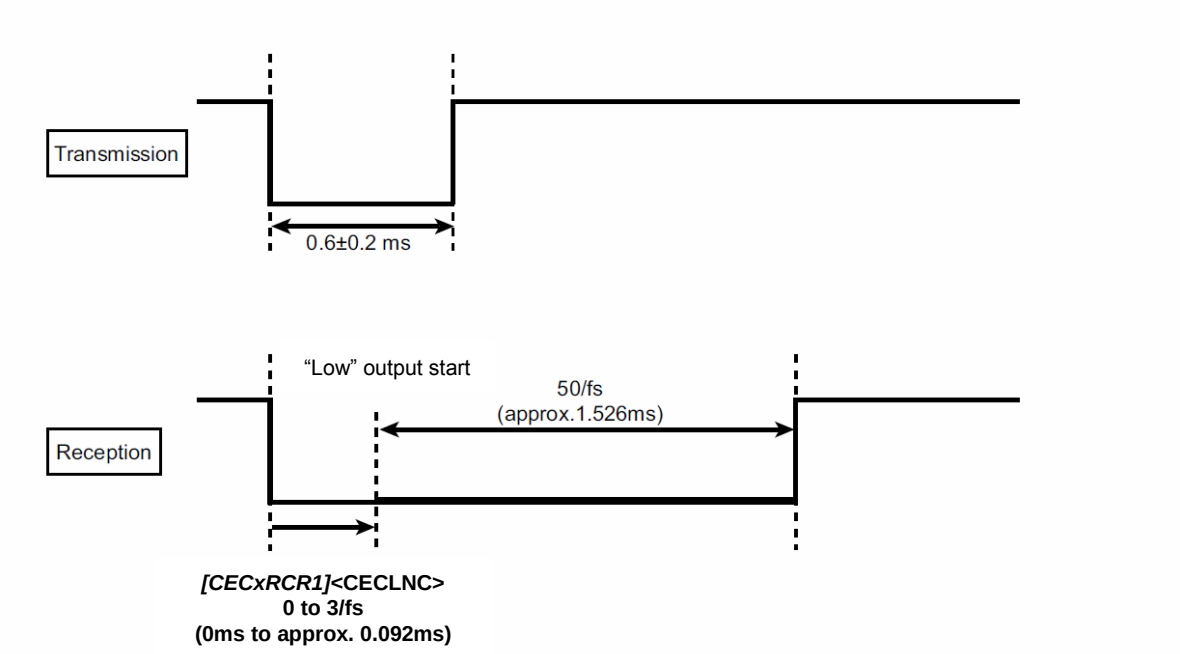

Figure 3.4 ACK response timing

3.3.2.6. Receive Error Interrupt Suspend

Configure the ***[CECxRCR1]***<CECRIHLD> to specify whether a receive error interrupt (maximum cycle error, buffer overrun and waveform error) is suspended or not. Setting "1" generates no interrupts at the error detection.
If data continues to the ACK bit, an ACK response is executed by reversed logic. If the subsequent bits are interrupted, it is determined as a timeout, based on the setting in ***[CECxRCR1]***<CECTOUT>.
After the ACK response or the timeout determination, an interrupt is generated.

3.3.2.7. Cycles to Identify Timeout

Configure the ***[CECxRCR1]***<CECTOUT> to specify the time to determine a timeout.
This setting is used when the setting of a receive error interrupt suspension (***[CECxRCR1]***<CECRIHLD>) is "1".

3.3.2.8. Data Reception at Logical Address Discrepancy

It can be set to receive even when ***[CECxRCR1]*** <CECOTH> does not match the destination address with the address set in the ***[CECxADD]*** register.

In this case, data reception is normally performed and an interrupt is generated by detecting an error.
An ACK response is, however, not performed on, neither the header block nor the data block.

Note 1: A broadcast message is received regardless of the ***[CECxRCR1]***<CECOTH> setting.
Note 2: If an initiator sends a new message beginning with the start bit without having sent the last block with EOM = 1, the ACK bit is determined as a maximum cycle error, so that an interrupt is generated. Subsequent reception is normally performed.

3.3.2.9. Start Bit Detection

Set the condition of the start bit detection with the ***[CECxRCR2]*** register. Rising timing and cycle can be set individually.

[CECxRCR2]<CECSWAV0> is to specify the fastest start bit rising timing. ***[CECxRCR2]***<CECSWAV1> is to specify the latest start bit rising timing (the time period 1 in the Figure 3.5 shown below).

[CECxRCR2]<CECSWAV2> is to specify the minimum cycle of a start bit. ***[CECxRCR2]***<CECSWAV3> is to specify the maximum cycle of a start bit (the time period 2 in the Figure 3.5 shown below).

If a rising edge in the period 1 and a falling edge in the period 2 are detected, the start bit is considered to be valid.

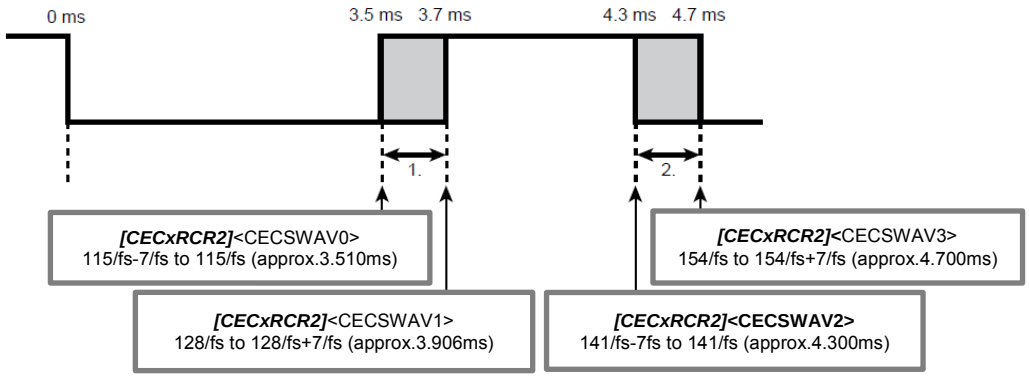

Figure 3.5 Minimum and maximum permissible values on the standard (Start bit)

3.3.2.10. Waveform Error Detection

To detect an error when a received waveform is out of the defined tolerance range, configure the ***[CECxRCR3]*** register.

An error is detected when ***[CECxRCR3]***<CECWAVEN> is enabled. The detection period can be adjusted with ***[CECxRCR3]*** <CECWAV0>, <CECWAV1>, <CECWAV2>, and <CECWAV3>.

A waveform error interrupt is generated when a rise of the signal occurs in the interval of 1 or 2 in Figure 3.6 or when no rises of the signal occur until the timing of 3 in the same figure.

1. A period between the beginning of a bit and the earliest logical "1" rising timing
2. A period between the latest logical "1" rising timing and the earliest logical "0" rising timing.
3. The latest logical "0" rising timing.

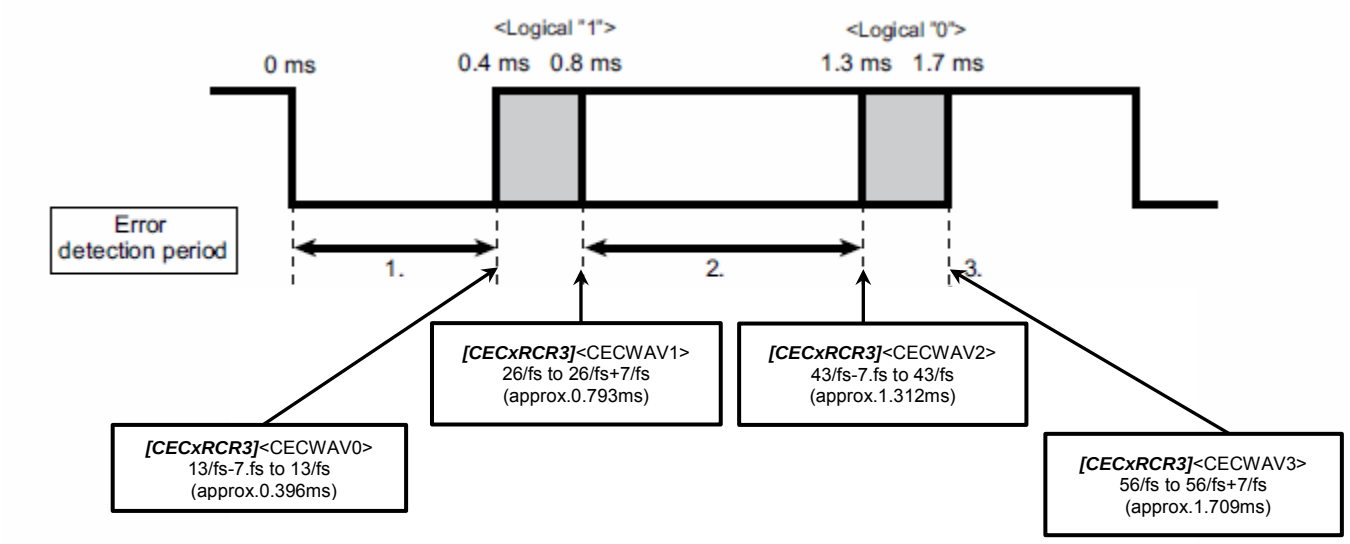

Figure 3.6 Minimum and maximum permissible values on the standard (Data bit)

3.3.3. Enabling Reception

After configuring the ***[CECxADD***], ***[CECxRCR1]***, ***[CECxRCR2]***, and ***[CECxRCR3]*** is ready for reception by enabling the ***[CECxREN]***<CECREN>. Detecting a start bit initiates the reception.

Note: Changing the configuration of the ***[CECxADD]***, ***[CECxRCR1]***, ***[CECxRCR2]***, and ***[CECxRCR3]*** during reception may harm the proper reception. Before the change of the registers shown below, set ***[CECxREN]***<CECREN> to disable the reception and read the ***[CECxREN]***<CECREN> and ***[CECxTEN]*** <CECTRANS> to ensure that the operation is stopped.

Table 3.3 Reception setting registers

Register name	Bit symbol	Setting item
[CECxADD]	<CECADD[15:0]>	Logical address
[CECxRCR1]	<CECHNC><CECLNC>	Noise cancellation time
	<CECMIN><CECMAX>	Time to identify cycle error
	<CECOTH>	Data reception at logical address discrepancy
[CECxRCR2]	<CECSWAV0><CECSWAV1> <CECSWAV2><CECSWAV3>	Start bit detection
[CECxRCR3] (<CECWAVEN>=1)	<CECWAV0><CECWAV1> <CECWAV2><CECWAV3>	Waveform confirmation setting

3.3.4. Reception Error Detection

If an error is detected during data reception, an interrupt occurs to stop reception, and CEC waits for the next start bit. The received data in which an error occurred is discarded.

For a maximum cycle error, receive buffer overrun and waveform error, it is possible to suspend a receive error interrupt and continue reception. At this time, an ACK response can be sent as reverse logic.

CEC provides a factor bit in ***[CECxRSTAT]*** to check an interrupt factor. This factor bit corresponds to each interrupt.

3.3.5. Details of Reception Error

3.3.5.1. Cycle error

A period between the falling edges of the two sequential bits is measured during reception. If the period does not comply with the specified minimum or maximum value, a cycle error interrupt is generated.

A setting of maximum cycle or minimum cycle time is specified by ***[CECxRCR1]***<CECMIN> and <CECMAX>. The maximum value is 90/fs (approx.2.747ms) and minimum value is 67/fs (approx. 2.045ms). They can be specified between the ranges -4/fs to +3/fs by the unit of 1/fs to detect cycle errors.
If a cycle error interrupt occurs, ***[CECxRSTAT]***<CECRIMIN> or <CECRIMAX> is set.
If a minimum cycle error occurs, CEC signal becomes "Low" for approx. 3.63 ms.

Note 1: When minimum cycle error is detected, "Low" is output after "Low" detection noise cancellation time.
Note 2: If an initiator sends a new message beginning with the start bit without having sent the last block with EOM = 1, the ACK bit is determined as a maximum cycle error, so that an interrupt is generated. Subsequent reception is normally performed. For detailed information, refer to "5. Precautions".

3.3.5.2. ACK Collision

At an ACK response, detecting "Low" after the specified period to output generates an ACK collision interrupt or minimum cycle error interrupt.

The ACK collision interrupt sets the ***[CECxRSTAT]***<CECRIACK>. The minimum cycle error interrupt sets ***[CECxRSTAT]***<CECRIMIN>.

The following describes the period and method of detection.

Detection starts approx. 0.3 ms after the end of the period of outputting "Low" and ends approx. 2.0 ms from the starting point (the falling edge) of the ACK bit.

After 0.3 ms has elapsed from the end of the period of outputting "Low", CEC checks if the CEC line is "0" or not. If it is "Low", an ACK collision interrupt is generated. If it is "High" and "Low" is detected during the detection period, the minimum cycle error interrupt is generated. The minimum cycle error causes CEC to output "Low" for approx. 3.63 ms.

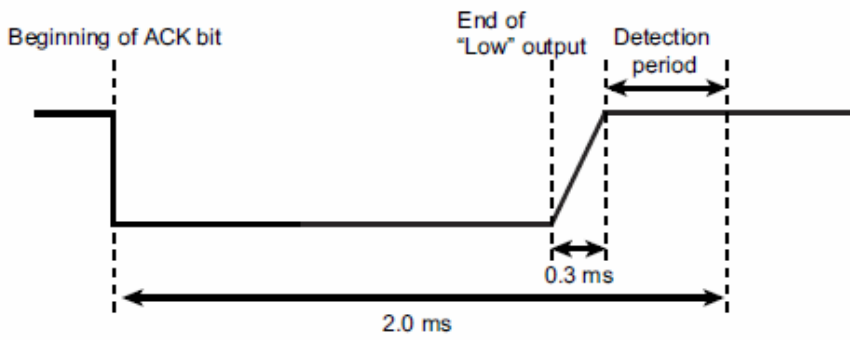

Figure 3.7 ACK collision detection

3.3.5.3. Receive Buffer Overrun

A receive buffer overrun interrupt is generated when the next data reception is completed before reading the data stored in the receive buffer.
The interrupt sets ***[CECxRSTAT]***<CECRIOR>.

3.3.5.4. Waveform Error

A waveform error occurs when waveform error detection is enabled in ***[CECxRCR3]***.
If a waveform did not comply with the standard, a waveform error occurs to generate an interrupt.

If a waveform interrupt occurs, ***[CECxRSTAT]***<CECRIWAV> is set.

3.3.5.5. Suspending Receive Error Interrupt

For a maximum cycle error, a buffer overrun and a waveform error, it is possible to suspend without generating an interrupt when an error is detected. This can be set in ***[CECxRCR1]***<CECRIHLD>. When the setting is enabled, a timeout setting is also required with ***[CECxRCR1]***<CECTOUT>.

When this interrupt suspension is enabled, if CEC keeps receiving the next bit and the entire reception including the ACK bit is completed, CEC generates an interrupt after a reversed ACK response is executed. At this time, ***[CECxRSTAT]***<CECRIEND> indicating the reception completion and the suspended error flag are set.

If the reception of the next bit is interrupted, CEC starts to measure the timeout period, and an interrupt is generated after the timeout. At this time, only the suspended error flag is set in ***[CECxRSTAT]***.

The timeout is measured from the end of the last bit received in the same manner as a wait time when the bus becomes free in transmission.

The information that the interrupts are suspended is held until "1" as EOM bit indicating reception completion is received or the timeout occurs. Thus, an interrupt is generated in each reception of a byte of data if multiple bytes are received while interrupts are suspended. A flag indicating reception completion and the suspended interrupt flag are set in ***[CECxRSTAT]***.

Note 1: If a minimum cycle error occurs at the subsequent reception while interrupts are suspended, a minimum cycle error interrupt is immediately generated and CEC signal becomes "Low" for approx.3.63 ms. A suspended interrupts and the minimum cycle error flag are set to ***[CECxRSTAT]***.

Note 2: If an interrupt other than a minimum cycle error interrupt is generated at subsequent reception while interrupts are suspended, CEC continues reception until the ACK response or the timeout. All the flags of the detected interrupts are set to ***[CECxRSTAT]***.

3.3.6. Stopping Reception

Writing "0" to the ***[CECxREN]***<CECREN> disables data reception. If the data reception is disabled during data reception, receiving operation immediately stops and the received data is discarded.

Note: If the reception is disabled while "Low" is sent as a signal of minimum cycle error, the "Low" output is stopped as well.

3.4. Transmission

3.4.1. Basic Operation

In the transmission setting, the CEC firstly confirms the bus free wait status; it checks whether a CEC falling edge signal does not exist in the specified bit cycles, and then sends a start bit. The confirmation of bus free wait is performed all the time. At setting the transmission, once bus free wait condition is satisfied, a transmission will start immediately.
After transmitting a start bit, CEC transmits one byte data and EOM data stored in the transmit buffer to the shift register. When the transmission of the first bit of the one byte data begins, transmission interrupt is generated, and ***[CECxTSTAT]***<CECTISTA> is set. After transmission interrupt generation, next one byte data is set to the transmit data buffer.

One byte data transmission completes in the order of transmission of 8 bits data, EOM bit, ACK bit transmission and ACK bit response.

Data transmission continues until EOM is set to "1".

If EOM is set to "1", the end of transmission interrupt occurs after confirmation of data, EOM, ACK bit transmission and ACK bit response. When transmission completion interrupt occurs, ***[CECxTSTAT]*** <CECTIEND> is set.

Transmission interrupt ends a series of transmission process, and ***[CECxTEN]***<CECTEN> is cleared.
If an error is generated in transmission, an error interrupt is generated to stop transmission.
Even if reception is enabled, no reception is executed in transmission.

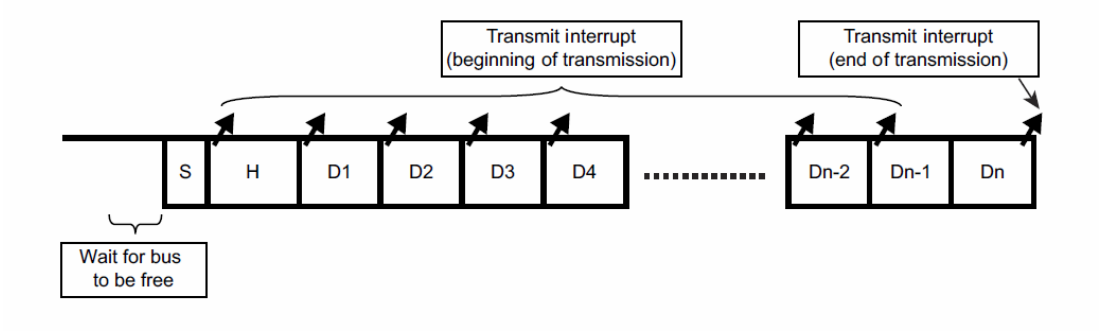

Figure 3.8 Basic operation of CEC (Transmission)

3.4.2. Pre-configuration

Before transmitting data, set the transmit control register ***[CECxTCR]*** and transmit buffer register ***[CECxTBUF]***.

3.4.2.1. Bus Free Wait Time

Specify a bus free wait time in ***[CECxTCR]***<CECFREE>. It can be specified in a range from 1 to 16-bit cycle.

Confirmation of the bus free wait time is started after one bit cycle of falling edge in the final bit. If the signal stays high for the specified number of bit cycles, transmission starts.

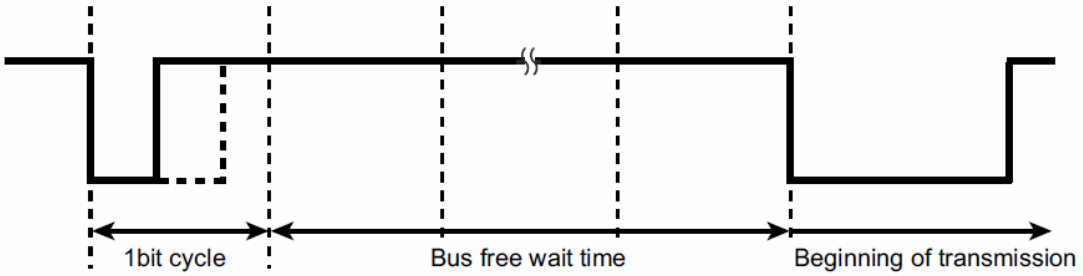

Figure 3.9 Bus free wait time

3.4.2.2. Transmitting Broadcast Message

To transmit a broadcast message, set ***[CECxTCR]***<CECBRD>=1. If this bit is set, a logical "0" response during an ACK cycle results in an error; if this bit is not set, a logical "1" response during an ACK cycle results in an error.

3.4.2.3. Adjusting Transmission Waveform

Both a start bit and data bit are capable of adjusting a rising timing and cycle. With ***[CECxTCR]***<CECSTRS>, <CECSPRD>, <CECDTRS>, and <CECDPRD>, the timing can be specified between the earliest rising/cycle timing in the standard and typical values.

Note: Use ***[CECxTCR]***<CECDTRS> as the same settings as ***[CECxRCR1]***<CECLNC>.

The following figures show how the waveforms differ depending on the configurations of the start bit, logical "0" and logical "1".

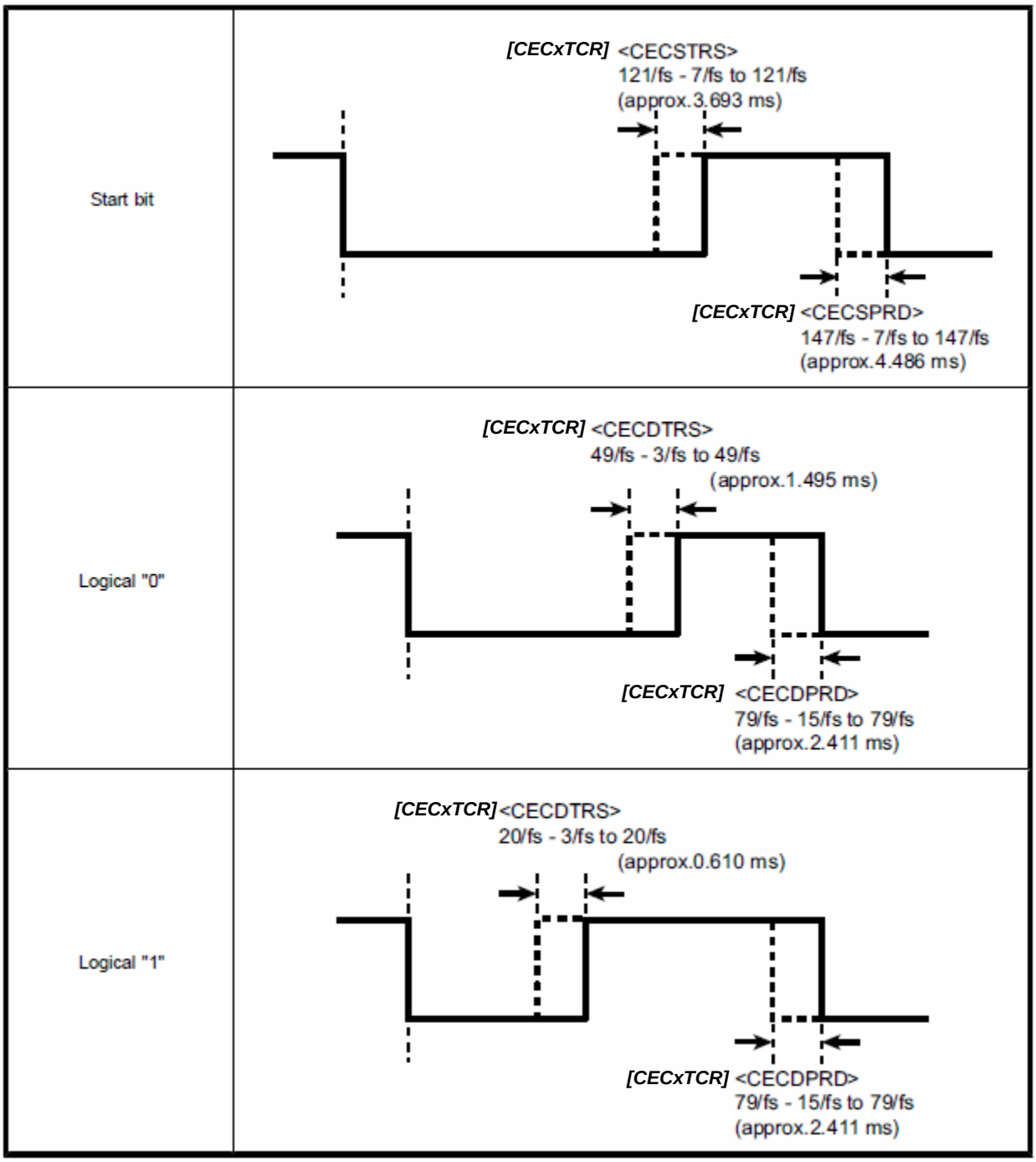

Figure 3.10 Transmission waveform adjustment

3.4.2.4. Preparing Transmission Data

Set a byte of transmission data and EOM data to ***[CECxTBUF]*** register.

3.4.3. Transmission Error Detection

Error detection in transmission generates an interrupt to stop transmission. This clears ***[CECxTEN]*** <CECTEN>.

[CECxTSTAT] register has bits corresponding to each interrupt to identify an error factor. You can identify the interrupt factor by checking these bits.

Note: If transmission is stopped by an error, an improper waveform may be output to CEC. This is because output is stopped immediately after an error occurs.

3.4.4. Details of Transmission Error

3.4.4.1. Arbitration Lost

An arbitration lost error occurs when CEC detects "Low" during the start bit transmission or data transmission, or when CEC signal becomes "Low" after an ACK response is sent.

When an arbitration lost error occurs, ***[CECxTSTAT]***<CECTIAL> is set.

The following figures show an arbitration lost detection periods.

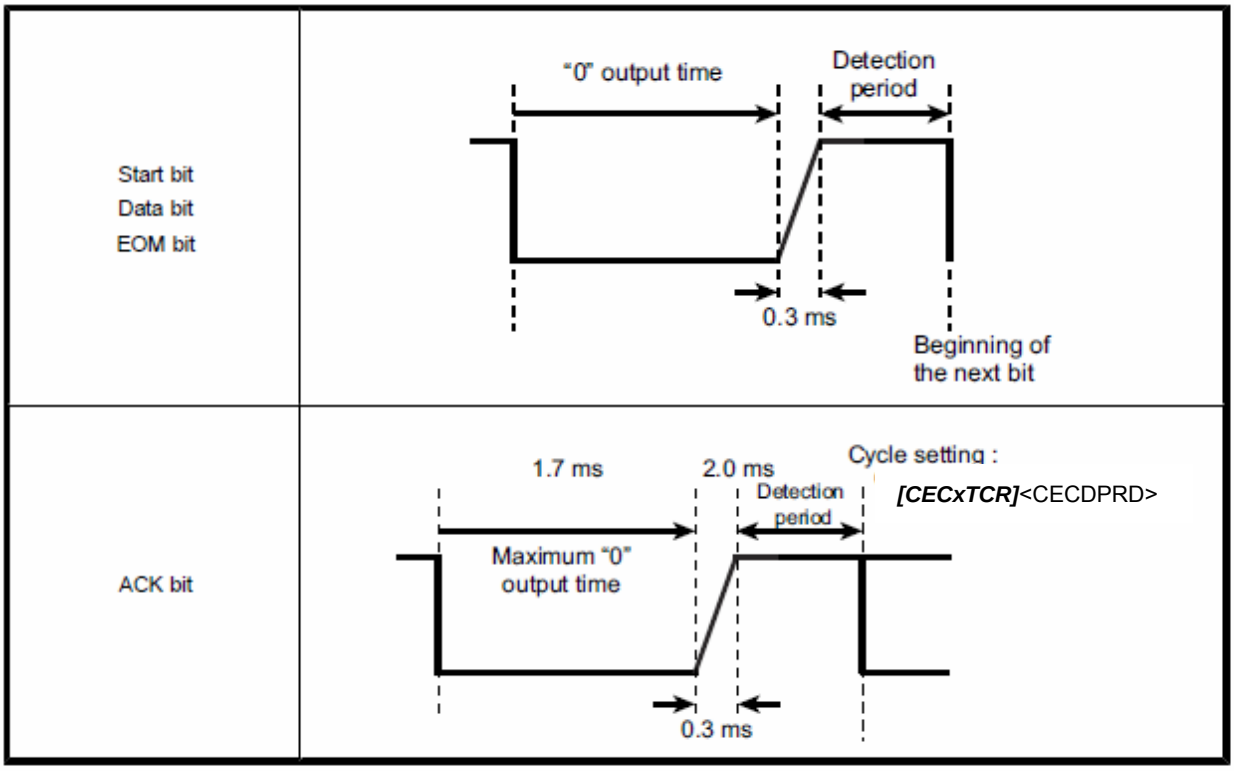

Figure 3.11 Arbitration lost detection period

3.4.4.2. ACK Error

An ACK error interrupt occurs when an ACK response does not conform to the configuration specified in ***[CECxTCR]***<CECBRD>.

When an ACK error interrupt occurs, ***[CECxTSTAT]***<CECTIACK> is set.

The ACK error is set as follows:

Table 3.4 ACK response confirmation

Configuration	description
<CECBRD> = 0 Broadcast transmission?: No	ACK error when ACK response is logical "1"
<CECBRD> = 1 Broadcast transmission?: Yes	ACK error when ACK response is logical "0"

3.4.4.3. Transmit Buffer Underrun

When the data in the transmit buffer is transmitted to the shift-register, an interrupt is generated. Then 1-Byte data is transmitted. If data is not set in the transmit buffer until the next 1-Byte data transmission, a transmit buffer underrun error is generated.

When the underrun error occurs, ***[CECxTSTAT]***<CECTIUR> is set.

3.4.4.4. Order of ACK Error and Transmit Buffer Underrun

If interrupt factors of the ACK error and transmit buffer underrun are detected at the end of transmission of a byte of data, the transmit buffer underrun has priority.
The transmit buffer underrun interrupt occurs first and then the ACK error interrupt occurs.

3.4.5. Stopping Transmission

To stop transmission, send data in which EOM bit is "1". This generates a transmit completion interrupt.
Note that proper operation is not ensured if the start bit of transmission is set to "0" during transmission.

3.4.6. Retransmission

Transmission is stopped by error detection. To retry the transmission, configure the condition and data of starting the transmission.

3.5. Software Reset

The entire CEC function can be initialized by software.

Setting "1" to the ***[CECxRESET]***<CECRESET> causes the following operations.

- Reception: Immediately stops. The received data is discarded.
- Transmission: Immediately stops including CEC signal output.
- Register: All the registers are initialized except ***[CECxEN]***.

Note that if software reset is performed in transmission, a CEC signal waveform may not comply with the standard.

4. Registers

The registers of CEC are described in this chapter.

4.1. List of Registers

The control registers and address for CEC are as follows.

Peripheral function		Channel/Unit	Base address	
			TYPE 1	TYPE 2
Consumer Electronics Control Circuit	CEC	ch0	0x400E6000	0x400E8000

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Base address (Base +)
CEC Enable Register	***[CECxEN]***	0x0000
Logical Address Register	***[CECxADD]***	0x0004
Software Reset Register	***[CECxRESET]***	0x0008
Receive Enable Register	***[CECxREN]***	0x000C
Receive Buffer Register	***[CECxRBUF]***	0x0010
Receive Control Register 1	***[CECxRCR1]***	0x0014
Receive Control Register 2	***[CECxRCR2]***	0x0018
Receive Control Register 3	***[CECxRCR3]***	0x001C
Transmit Enable Register	***[CECxTEN]***	0x0020
Transmit Buffer Register	***[CECxTBUF]***	0x0024
Transmit Control Register	***[CECxTCR]***	0x0028
Receive Interrupt Status Register	***[CECxRSTAT]***	0x002C
Transmit Interrupt Status Register	***[CECxTSTAT]***	0x0030
CEC Sampling Clock Select Register	***[CECxFSSEL]***	0x0034

4.2. Details of Registers

4.2.1. *[CECxEN]* (CEC Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:3	-	0	R	Read as "0".
2	-	0	R/W	Write as "0".
1	-	0	R/W	Write as "1".
0	CECEN	0	R/W	CEC operation 0: Disabled 1: Enabled Specifies the CEC operation. Enable CEC before using. When the CEC operation is disabled, no clocks are supplied to the CEC module except for the ***[CECxEN]*** register. Thus power consumption can be reduced. When CEC is disabled after it was enabled, each register setting is retained.

4.2.2. *[CECxADD]* (Logical Address Register)

Bit	Bit Symbol	After Reset	Type	Function
31:16	-	0	R	Read as "0".
15:0	CECADD[15:0]	0x0000	R/W	Logical address 15 to 0 Specifies the logical address assigned to CEC. Multiple addresses can be set simultaneously since each bit corresponds with each address.

Note: A broadcast message is received regardless of the register setting. By allocating a logical address of a device to 15, logical "0" is sent as an ACK response to the broadcast message.

4.2.3. *[CECxRESET]* (Software Reset Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	CECRESET	0	W	Software reset 0: Disabled 1: Enabled Stops all the CEC operation and initializes the register. Read as "0".

4.2.4. *[CECxREN]* (Receive Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	CECREN	0	W	Reception control 0: Disabled 1: Enabled Controls the reception operation of CEC. By writing to this bit, enable / disable reception setting. Writing "1" puts it in the reception wait state.
			R	Reception control monitor 0: Stop. 1: Operating. The status of the reception circuit can be monitored by reading this bit. If this bit is read after the setting is done, it can be checked that the setting has been reflected.

Note1: Enable<CECREN> bit after setting the ***[CECxRCR1]***, ***[CECxRCR2]***, and ***[CECxRCR3].***

Note2: There is a time lag to reflect the setting of the <CECREN>bit to the circuit. Make sure that the register is under suspension when you try to change settings or to enable disabled-settings.

4.2.5. *[CECxRBUF]* (Receive Buffer Register)

Bit	Bit Symbol	After Reset	Type	Function
31:10	-	0	R	Read as "0".
9	CECACK	0	R	ACK bit Reads the received ACK bit.
8	CECEOM	0	R	EOM bit Reads the received EOM bit.
7:0	CECRBUF[7:0]	0x00	R	Received data Reads one byte of data received. The bit 7 is the MSB.

Note: Read this register before completion of next data reception. When the next data reception is completed, the buffer is overwritten.

4.2.6. *[CECxRCR1]* (Receive Control Register 1)

Bit	Bit Symbol	After Reset	Type	Function
31:25	-	0	R	Read as "0".
24	CECACKDIS	0	R/W	Logical "0" as ACK response 0: Response 1: Not response Specifies if logical "0" is sent or not as an ACK response to the data block when destination address matches with the address set in the logical address register. (Logical "0" is sent to the header block as an ACK response regardless of the bit setting when detecting the corresponded addresses.)
23:22	-	0	R	Read as "0".
21:20	CECHNC[1:0]	0	R/W	The number of "High" samplings for noise cancellation. (Note1) 00: None (one time of fs clock is observed.) 01: 1/fs (two consecutive fs clocks are observed.) 10: 2/fs (three consecutive fs clocks are observed.) 11: 3/fs (four consecutive fs clocks are observed.) Specifies the time of the noise cancellation for each 1/fs when detecting "High". If the specified number of "High" levels are not observed, the signal is considered as noise.
19	-	0	R	Read as "0".
18:16	CECLNC[2:0]	000	R/W	The number of "Low" samplings for noise cancellation. (Note1) (Note2) 000: None (one time of fs clock observed.) 001: 1/fs (two consecutive fs clocks observed) 010: 2/fs (three consecutive fs clocks observed) 011: 3/fs (four consecutive fs clocks observed.) 100: - (Reserved) 101: - (Reserved) 110: - (Reserved) 111: - (Reserved) Specifies the time of the noise cancellation for each 1/fs when detecting "Low". It is considered as noise if "Low" levels of the same number as the specified cycles are not sampled.
15	-	0	R	Read as "0".
14:12	CECMIN[2:0]	000	R/W	Time to identify as minimum cycle error 000: 67/fs(approx.2.045 ms) 001: 67/fs + 1/fs 010: 67/fs + 2/fs 011: 67/fs + 3/fs 100: 67/fs - 1/fs 101: 67/fs - 2/fs 110: 67/fs - 3/fs 111: 67/fs - 4/fs Specifies the minimum time to identify a valid bit. Base time is 67/fs (approx.2.045 ms). Enables to specify it between the ranges -4/fs to +3/fs by the unit of 1/fs. An interrupt is generated and "Low" is output to CEC for approx. 3.63 ms when one bit cycle is shorter than the specified time.
11	-	0	R	Read as "0".

10:8	CECMAX[2:0]	000	R/W	Time to identify as maximum cycle error 000: 90/fs (approx. 2.747 ms) 001: 90/fs + 1/fs 010: 90/fs + 2/fs 011: 90/fs + 3/fs 100: 90/fs - 1/fs 101: 90/fs - 2/fs 110: 90/fs - 3/fs 111: 90/fs - 4/fs Specifies the maximum time to identify as a valid bit. Base time is 90/fs (approx. 2.747 ms). Enables to specify it between the ranges -4/fs to +3/fs by the unit of 1/fs. An interrupt is generated when one bit cycle is longer than the specified time.
7	-	0	R	Read as "0".
6:4	CECDAT[2:0]	000	R/W	Point of determining the data as 0 or 1.(Note1) 000: 34/fs(Approx. 1.038 ms) 001: 34/fs + 2/fs 010: 34/fs + 4/fs 011: 34/fs + 6/fs 100: 34/fs - 2/fs 101: 34/fs - 4/fs 110: 34/fs - 6/fs 111: Reserved Specifies the point of determining the data as logical "0" or logical "1". Base time is 34/fs (approx.1.038 ms). Enables to specify it within ±6/fs by the unit of 2/fs.
3:2	CECTOUT[1:0]	00	R/W	Cycle to identify timeout 00: 1-bit cycle 01: 2-bit cycle 10: 3-bit cycle 11: Reserved Specifies the time to determine a timeout. Enables to specify it between 1 bit and 3 bits for each bit cycle. This setting is used to detect a timeout when the <CECRIHLD> bit is valid.
1	CECRIHLD	0	R/W	Error interrupt suspend 0: Not suspended 1: Suspended Specifies whether to suspend a receive error interrupt (maximum cycle error, buffer overrun and waveform error). Setting "1" generates no interrupt at the error detection. If data continues to an ACK bit, an ACK response is executed by reversed logic. If the subsequent bits are interrupted, it is determined as a timeout, based on the setting in <CECTOUT>. After the ACK response or the timeout determination, an interrupt is generated.
0	CECOTH	0	R/W	Data reception at logical address discrepancy (Note3) 0: Not received. 1: Received. Specifies whether to receive data when the destination address does not matches with the address set in the ***[CECxADD]*** register.

Note1: The settings in <CECHNC>, <CECLNC> and <CECDAT> are also used in receiving an ACK response at transmission.

Note2: <CECLNC> must be used under the same setting as ***[CECxTCR]***<CECDTRS>.

Note3: A broadcast message is received regardless of the <CECOTH> register setting.

Note4: Changing the configurations during transmission or reception may harm its proper operation. Before the change, set the ***[CECxREN]***<CECREN> bit to disable the reception and read the <CECREN> bit and the ***[CECxTEN]***<CECTRANS> bit to ensure that the operation is stopped.

4.2.7. *[CECxRCR2]* (Receive Control Register 2)

Bit	Bit Symbol	After Reset	Type	Function
31:15	-	0	R	Read as "0".
14:12	CECSWAV3[2:0]	000	R/W	Maximum cycles to detect a start bit. 000: 154/fs (approx. 4.700 ms) 001: 154/fs + 1/fs 010: 154/fs + 2/fs 011: 154/fs + 3/fs 100: 154/fs + 4/fs 101: 154/fs + 5/fs 110: 154/fs + 6/fs 111: 154/fs + 7/fs
11	-	0	R	Read as "0".
10:8	CECSWAV2[2:0]	000	R/W	Minimum cycles to detect a start bit. 000: 141/fs(approx. 4.303 ms) 001: 141/fs + 1/fs 010: 141/fs + 2/fs 011: 141/fs + 3/fs 100: 141/fs + 4/fs 101: 141/fs + 5/fs 110: 141/fs + 6/fs 111: 141/fs + 7/fs
7	-	0	R	Read as "0".
6:4	CECSWAV1[2:0]	000	R/W	Maximum time of start bit rising timing. 000: 128/fs(approx. 3.906 ms) 001: 128/fs + 1/fs 010: 128/fs + 2/fs 011: 128/fs + 3/fs 100: 128/fs + 4/fs 101: 128/fs + 5/fs 110: 128/fs + 6/fs 111: 128/fs + 7/fs
3	-	0	R	Read as "0".
2:0	CECSWAV0[2:0]	000	R/W	Minimum time of start bit rising timing. 000: 115/fs(approx. 3.510 ms) 001: 115/fs + 1/fs 010: 115/fs + 2/fs 011: 115/fs + 3/fs 100: 115/fs + 4/fs 101: 115/fs + 5/fs 110: 115/fs + 6/fs 111: 115/fs + 7/fs

Note: Changing the configurations during reception may harm its proper operation. Before the change, set ***[CECxREN]***<CECREN> to disable the reception and read the <CECREN> bit to ensure that the operation is stopped.

4.2.8. *[CECxRCR3]* (Receive Control Register 3)

Bit	Bit Symbol	After Reset	Type	Function
31:23	-	0	R	Read as "0".
22:20	CECWAV3[2:0]	000	R/W	Waveform confirmation setting 3 (Note1) 000: 56/fs(approx. 1.709 ms) 001: 56/fs + 1/fs 010: 56/fs + 2/fs 011: 56/fs + 3/fs 100: 56/fs + 4/fs 101: 56/fs + 5/fs 110: 56/fs + 6/fs 111: 56/fs + 7/fs
19	-	0	R	Read as "0".
18:16	CECWAV2[2:0]	000	R/W	Waveform confirmation setting 2 (Note2) 000: 43/fs(approx. 1.312 ms) 001: 43/fs + 1/fs 010: 43/fs + 2/fs 011: 43/fs + 3/fs 100: 43/fs + 4/fs 101: 43/fs + 5/fs 110: 43/fs + 6/fs 111: 43/fs + 7/fs
15	-	0	R	Read as "0".
14:12	CECWAV1[2:0]	000	R/W	Waveform confirmation setting 1 (Note3) 000: 26/fs(approx. 0.793 ms) 001: 26/fs + 1/fs 010: 26/fs + 2/fs 011: 26/fs + 3/fs 100: 26/fs + 4/fs 101: 26/fs + 5/fs 110: 26/fs + 6/fs 111: 26/fs + 7/fs
11	-	0	R	Read as "0".
10:8	CECWAV0[2:0]	000	R/W	Waveform confirmation setting 0 (Note4) 000: 13/fs(approx. 0.396 ms) 001: 13/fs + 1/fs 010: 13/fs + 2/fs 011: 13/fs + 3/fs 100: 13/fs + 4/fs 101: 13/fs + 5/fs 110: 13/fs + 6/fs 111: 13/fs + 7/fs
7:2	-	0	R	Read as "0".
1	CECRSTAEN	0	R/W	Start bit interrupt detection 0: Disable 1: Enable Detects a reception of start bit and generates interrupt.
0	CECWAVEN	0	R/W	Waveform error detection 0: Disable 1: Enable Detects a received waveform does not comply with the standard to generate a waveform error interrupt. If enabled, an error is detected according to the setting of <CECWAV0>, <CECWAV1>, <CECWAV2>, and <CEC WAV3>.

Note1: <CECWAV3>: This setting is enabled when the <CECWAVEN> bit is set to "1".
By setting these bits, an error is detected if rising edge of the received waveform comes later than that of proper logical "0". The received waveform is considered to be an error if a rising edge is not detected from the start point of the bit to the value specified in <CECWAV3>.

Note2: <CECWAV2>: This setting is enabled when the <CECWAVEN> bit is set to "1".

Note3: <CECWAV1>: By setting these bits, an error is detected if rising edge of the received waveform comes faster than logical "0" and later than that of proper logical "1". If a rising edge is detected during <CECWAV2> bit and <CECWAV1> bit setting, an error occurs.

Note4: <CECWAV0>: This setting is enabled when the <CECWAVEN> bit is set to "1". By setting these bits, an error is detected if rising edge of the received waveform comes faster than that of proper logical "1". The received waveform is considered to be an error if a rising edge is not detected from a start point of the bit to the value specified in <CECWAV0>.

Note5: Changing the configurations during reception may harm its proper operation. Before the change, set ***[CECxREN]***<CECREN> to disable the reception and read the <CECREN> bit to ensure that the operation is stopped.

4.2.9. *[CECxTEN]* (Transmit Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:2	-	0	R	Read as "0".
1	CECTRANS	0	R	Transmission state 0: Not in progress 1: In progress Indicates whether the transmission is in progress or not. It indicates "1" upon starting the transmission of the start bit. It indicates "0" if transmission is completed or an error interrupt is generated.
0	CECTEN	0.	W	Transmission control 0: Disable 1: Enable Controls the CEC transmission. Writing this bit enables or disables the transmission. Writing "1" to this bit initiates the transmission. This bit is automatically cleared by a transmit completion interrupt or an error interrupt.
			R	Transmission control monitor 0: Stop 1: Operating By reading this bit, it is possible to monitor the state of the transmit circuit. It can be checked by reading after the setup whether the setup has been reflected or not.

Note1: Set <CECTEN> after ***[CECxTBUF]*** and ***[CECxTCR]*** registers.

Note2: Make sure that it is stopped before changing various settings or setting permission again after prohibiting it.

4.2.10. *[CECxTBUF]* (Transmit Buffer Register)

Bit	Bit Symbol	After Reset	Type	Function
31:9	-	0	R	Read as "0".
8	CECTEOM	0	R/W	EOM bit Specifies the EOM bit to transmit.
7:0	CECTBUF[7:0]	0x00	R/W	Transmitted data Specifies a byte of data to transmit. The bit 7 is the MSB.

4.2.11. *[CECxTCR]* (Transmit Control Register)

Bit	Bit Symbol	After Reset	Type	Function
31:23	-	0	R	Read as "0".
22:20	CECSTRS[2:0]	000	R/W	Rising timing of a start bit 000: 121/fs 001: 121/fs - 1/fs 010: 121/fs - 2/fs 011: 121/fs - 3/fs 100: 121/fs - 4/fs 101: 121/fs - 5/fs 110: 121/fs - 6/fs 111: 121/fs - 7/fs
19	-	0	R	Read as "0".
18:16	CECSPRD[2:0]	000	R/W	Start bit cycle 000: 147/fs 001: 147/fs - 1/fs 010: 147/fs - 2/fs 011: 147/fs - 3/fs 100: 147/fs - 4/fs 101: 147/fs - 5/fs 110: 147/fs - 6/fs 111: 147/fs - 7/fs
15	-	0	R	Read as "0".
14:12	CECDTRS[2:0]	000	R/W	Rising timing of a data bit. (Note) logical "0" / logical "1" 000: 49/fs / 20/fs 001: 49/fs - 1/fs / 20/fs - 1/fs 010: 49/fs - 2/fs / 20/fs - 2/fs 011: 49/fs - 3/fs / 20/fs - 3/fs 100: Reserved / Reserved 101: Reserved / Reserved 110: Reserved / Reserved 111: Reserved / Reserved

11:8	CECDPRD[2:0]	0000	R/W	Data bit cycle 0000: 79/fs 0001: 79/fs - 1/fs 0010: 79/fs - 2/fs 0011: 79/fs - 3/fs 0100: 79/fs - 4/fs 0101: 79/fs - 5/fs 0110: 79/fs - 6/fs 0111: 79/fs - 7/fs 1000: 79/fs - 8/fs 1001: 79/fs - 9/fs 1010: 79/fs - 10/fs 1011: 79/fs - 11/fs 1100: 79/fs - 12/fs 1101: 79/fs - 13/fs 1110: 79/fs - 14/fs 1111: 79/fs - 15/fs
7:5	-	0	R	Read as "0".
4	CECBRD	0	R/W	Broadcast transmission 0: Not broadcast transmission 1: Broadcast transmission Set this bit to "1" when transmitting a broadcast message.
3:0	CECFREE[3:0]	0000	R/W	Time of bus to be free 0000: 1bit cycle 0001: 2bit cycle 0010: 3bit cycle 0011: 4bit cycle 0100: 5bit cycle 0101: 6bit cycle 0110: 7bit cycle 0111: 8bit cycle 1000: 9bit cycle 1001: 10bit cycle 1010: 11bit cycle 1011: 12bit cycle 1100: 13bit cycle 1101: 14bit cycle 1110: 15bit cycle 1111: 16bit cycle Specifies time of a bus to be free that checked before transmission. Start transmission after checking the CEC line kept inactive during the specified cycles.

Note: <CECDTRS> must be used under the same setting as ***[CECxRCR1]***<CECLNC>.

4.2.12. *[CECxRSTAT]* (Receive Interrupt Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:7	-	0	R	Read as "0".
6	CECRIWAV	0	R	Interrupt flag 0: No wave form error 1: Wave form error Indicates that waveform error is detected. The error occurs when waveform error detection is enabled in ***[CECxRCR3]***<CECWAVEN>.
5	CECRIOR	0	R	Interrupt flag 0: No receive buffer overrun 1: Receive buffer overrun Indicates the receive buffer receives next data before reading the data that had already been set.
4	CECRIACK	0	R	Interrupt flag 0: No ACK collision 1: ACK collision Indicates "0" is detected after the specified time to output ACK bit "0".
3	CECRIMIN	0	R	Interrupt flag 0: No minimum cycle error 1:Minimum cycle error Indicates one bit cycle is shorter than the minimum cycle error detection time specified in ***[CECxRCR1]***<CECMIN>.
2	CECRIMAX	0	R	Interrupt flag 0: No maximum cycle error 1: Maximum cycle error Indicates one bit cycle is longer than the maximum cycle error detection time specified in ***[CECxRCR1]***<CECMAX>.
1	CECRISTA	0	R	Interrupt flag 0: No start bit detection 1: Start bit detection Indicates a start bit is detected.
0	CECRIEND	0	R	Interrupt flag 0: Not one byte data reception completed 1: Completion of one byte data reception Indicates one byte of data reception is completed.

4.2.13. *[CECxTSTAT]* (Transmit Interrupt Status Register)

Bit	Bit Symbol	After Reset	Type	Function
31:5	-	0	R	Read as "0".
4	CECTIUR	0	R	Interrupt flag 0: No transmit buffer underrun 1: Transmit buffer underrun Indicates next data has not set to the transmission buffer within a one byte of data transmission.
3	CECTIACK	0	R	Interrupt flag 0: No ACK error detection 1: ACK error detection Indicates one of the following conditions occurs. - When logical "0" is not detected in transmission to the specific address. - When logical "1" is not detected in transmission of a broadcast message.
2	CECTIAL	0	R	Interrupt flag 0: No arbitration lost 1: Arbitration lost occurs Indicates "Low" is detected while outputting "High".
1	CECTIEND	0	R	Interrupt flag 0: No data transmission completion 1: data transmission is completed Indicates data transmission including the EOM bit is completed.
0	CECTISTA	0	R	Interrupt flag 0: No start transmission 1: Start transmission Indicates one byte of data transmission is started.

4.2.14. *[CECxFSSEL]* (CEC Sampling Clock Select Register)

Bit	Bit Symbol	After Reset	Type	Function
31:1	-	0	R	Read as "0".
0	CECCLK	0	R/W	CEC sampling clock 0: Low speed clock (fs) 1: CECxCLKTRG Sets the sampling clock for CEC function. It is possible to select either the low speed clock (fs) or the clock source timer trigger (CECxCLKTRG). For the information of CECxCLKTRG used for sampling clock, refer to "Product Information" of reference manual. The timer output range that can set CECxCLKTRG is 30 kHz to 34 kHz.

Note: Before the sampling clock is changed, the stop state of the data transfer should be confirmed. Then ***[CECxFSSEL]*** should be set before the settings of the other registers related to CEC are done.
And when the sampling clock is changed after the software reset done by ***[CECxRESET]***, ***[CECxFSSEL]*** should be set before the settings of the other registers related to CEC are done.

5. Precautions

While data reception at the logical address discrepancy is enabled (***[CECxRCR1]***<CECOTH> = 1), if the transmitter sends a new message from a start bit without having sent the data in the block of EOM = 1, it is regarded as occurrence of a maximum cycle error of the ACK bit and its corresponding interrupt is generated. After that, the reception operation is performed in the usual way.

6. Revision History

Table 6.1 Revision history

Revision	Date	Description
1.0	2018-01-29	First release
1.1	2018-07-30	-Conventions Modified explanation of trademark 3.3.2.5. ACK Response Description correction: "For data blocks, when the destination address matches the address set in the ***[CECxADD]*** register, it is possible to arbitrarily enable / disable the ACK response of logic "0" with ***[CECxRCR1]*** <CECACKDIS>."

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