Outlines

This application note explains the operation of the sample programs of Startup and System files. It is reference material when developing products using M3H Group (2) with each function. This document helps the user check operation of the product and develop its program.
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1. Preface

This sample program executes the initial settings when an application program is used. The watchdog timer and the system clock can be set properly. This sample program assumes that the watchdog timer is set to "disable" immediately after a reset. For the details, refer to “Clock control and operation mode” and “Clock selective watchdog timer” in Reference manual.

2. Reference Document

- Datasheet
  TMPM3H group (2) datasheet Rev2.0 (Japanese edition)
- Reference manual
  Clock Control and operation mode (CG-M3H(2)-D) Rev2.0 (Japanese edition)
  Clock Selective Watchdog Timer (SIWDT-A) Rev2.1 (Japanese edition)

3. Function to Use

<table>
<thead>
<tr>
<th>IP</th>
<th>channel</th>
<th>port</th>
<th>Function / operation mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog timer</td>
<td>-</td>
<td>-</td>
<td>Watchdog timer disable</td>
</tr>
<tr>
<td>Clock control</td>
<td>-</td>
<td>-</td>
<td>External oscillation input and PLL enable</td>
</tr>
</tbody>
</table>

4. Target Device

The target devices of application note are as follows.

<table>
<thead>
<tr>
<th>Target Device</th>
<th>TMPM3HQFDFG</th>
<th>TMPM3HQFZFG</th>
<th>TMPM3HQFYFG</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMPM3HPFDFG</td>
<td>TMPM3HPFZFG</td>
<td>TMPM3HPFYFG</td>
<td></td>
</tr>
<tr>
<td>TMPM3HNFDFG</td>
<td>TMPM3HNFZFG</td>
<td>TMPM3HNFYFG</td>
<td></td>
</tr>
<tr>
<td>TMPM3HNFDDFG</td>
<td>TMPM3HNFZDFG</td>
<td>TMPM3HNFYDFG</td>
<td></td>
</tr>
<tr>
<td>TMPM3HMFDFG</td>
<td>TMPM3HMFZFG</td>
<td>TMPM3HMFYFG</td>
<td></td>
</tr>
</tbody>
</table>

* This sample program operates on the evaluation board of TMPM3HQFDFG. If other function than the TMPM3HQ one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly. The BSP related file is dedicated to the evaluation board (TMPM3HQ). If other function than the TMPM3HQ one is checked, the BSP related file should be changed properly.
5. Operation confirmation condition

<table>
<thead>
<tr>
<th>Used microcontroller</th>
<th>TMPM3HQFDFG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Used board</td>
<td>TMPM3HQFDFG Evaluation Board (Product of Sensyst)</td>
</tr>
<tr>
<td>Unified development environment</td>
<td>IAR Embedded Workbench for ARM 8.11.2.13606</td>
</tr>
<tr>
<td>Unified development environment</td>
<td>μVision MDK Version 5.24.2.0</td>
</tr>
<tr>
<td>Sample program</td>
<td>V1100</td>
</tr>
</tbody>
</table>

Evaluation board (TMPM3HQFDFG Evaluation Board) (Top view)

For purchasing the board, refer to the following homepage. ([http://www.chip1stop.com/](http://www.chip1stop.com/))
6. Function

The settings of the watchdog timer and CG are executed. After reset, it is run from the startup and proceeds to main processing. The following files are described in this application note.

- startup_TMPM3HQ.s
- system_TMPM3Hy.c

6.1. Watchdog Timer Setting

Set the watchdog timer. This sample program does not use this function (Disabled). The control register is set to disable code.

6.2. Clock Generator Setting

This sample program switches the system clock between an external clock ($f_{EHOSC}$) and an internal one ($f_{IHOSC1}$). And it also performs clock division to other IP and switching of multiplication ratio of PLL.
7. Start-up and System File

This sample program is used for the operation of TMPM3HQ.

7.1. Operation

This sample program executes the settings of each clock, the watchdog timer, the system core clock, and the PLL.
After the settings are done, the main procedure of an application program executes.

7.2. Watchdog Timer Setting

In the sample program, the watchdog timer is set to disable.
When setting to enable, switching can be done by macro change of "system_TMPM3Hy.c".
SIWD_SETUP (1U) should be changed to 0, then the watchdog timer is set to enable.
When this sample program is used in the Enable setting, the watchdog timer starts with the initial setting value and the reset is asserted after the watchdog operation is detected.

7.3. Clock Setting

An external oscillation or an internal oscillation are selected by switching.
An external oscillation has been selected in the sample program.

CLOCK_SETUP (1U)
When switch to internal oscillation, change to "0 U".

The system clock should be set.
SYSCR_Val (0x00000000UL)
This sample program executes to set the initial values.
The prescaler clock and the system clock operate with the setting of fc.
After the warming-up register and the oscillation register are set, the PLL register should be set.
7.4. PLL Setting

The clock multiplying circuit outputs \( f_{PLL} \) clock (maximum 80 MHz) which is generated by multiplying suitably the output clock \( f_{osc} \) frequency (6 MHz to 12 MHz) of the high speed oscillator. In this sample program, the external clock frequency is supposed to be 12 MHz.

This sample program operates with the \( f_{PLL} \) setting.

This sample program supports the input frequency 6/8/10/12 MHz.

The suitably multiplied frequencies are as follows.

\[
\text{External input frequency} \times \left( \frac{\text{Multiplying value}}{\text{Dividing value}} \right) = \text{Operating frequency}
\]

<table>
<thead>
<tr>
<th>Input Frequency</th>
<th>Multiplied Value</th>
<th>Operating Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 MHz</td>
<td>6.00 MHz</td>
<td>79.97 MHz</td>
</tr>
<tr>
<td>8 MHz</td>
<td>8.00 MHz</td>
<td>80 MHz</td>
</tr>
<tr>
<td>10 MHz</td>
<td>10.00 MHz</td>
<td>80 MHz</td>
</tr>
<tr>
<td>12 MHz</td>
<td>12.00 MHz</td>
<td>80 MHz</td>
</tr>
<tr>
<td>6 MHz</td>
<td>6.00 MHz</td>
<td>39.98 MHz</td>
</tr>
<tr>
<td>8 MHz</td>
<td>8.00 MHz</td>
<td>40 MHz</td>
</tr>
<tr>
<td>10 MHz</td>
<td>10.00 MHz</td>
<td>40 MHz</td>
</tr>
<tr>
<td>12 MHz</td>
<td>12.00 MHz</td>
<td>39.94 MHz</td>
</tr>
</tbody>
</table>

In this sample program, the PLL setting value has been selected to 12 MHz and the multiplying ratio has been set to 6.656.

```c
#define PLL0SEL_Ready          CG_12M_MUL_6_656_FPLL
```

If PLL0SEL_Ready is changed to the setting value in system_TMPM3Hy.c, the PLL setting value can be changed.

```c
CG_6M_MUL_13_328_FPLL      6 MHz selection and the multiplying rate 13.328 (fc=79.97MHz)
CG_8M_MUL_10_FPLL          8 MHz selection and the multiplying rate 10 (fc=80MHz)
CG_10M_MUL_8_FPLL          10 MHz selection and the multiplying rate 8 (fc=80MHz)
CG_12M_MUL_6_656_FPLL      12 MHz selection and the multiplying rate 6.656 (fc=79.88MHz)
CG_6M_MUL_6_664_FPLL       6 MHz selection and the multiplying rate 6.664 (fc=39.98MHz)
CG_8M_MUL_5_FPLL           8 MHz selection and the multiplying rate 5 (fc=40MHz)
CG_10M_MUL_4_FPLL          10 MHz selection and the multiplying rate 4 (fc=40MHz)
CG_12M_MUL_3_328_FPLL      12 MHz selection and the multiplying rate 3.328 (fc=39.94MHz)
```

7.5. Clock Frequency Switching

The system clock can be divided by the clock gear in [CGSYSCR].

```c
SYSCR_Val               (0x00000000UL)
```

The clock selection and the system clock gear selection can be done if the setting value above is changed.

The sample program operates with the fc setting.

The input of the core clock is the clock divided by SYSCR.

The system core clock is used for the sample program (CGRST, I2C, and others).
8. Precaution

When using the sample program with CPU other than TMPM3HQ, please check operation sufficiently.

9. Revision History

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>2018-05-18</td>
<td>-</td>
<td>First release</td>
</tr>
</tbody>
</table>
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