

CMOS Digital Integrated Circuit Silicon Monolithic

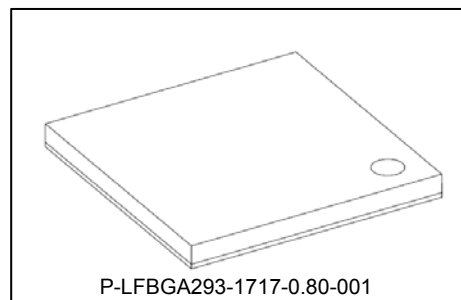
TC90195AXBG

Video signal Processing

Overview

TC90195AXBG is a video signal processing LSI for the HD input and output.

This device receives an analog video signal (CVBS) or a digital video signal (LVTTL/LVDS), executes the video signal processing (scaling function, image synthesis, and picture improvement feature), and outputs a digital signal (LVTTL/LVDS).



0.66g (Typ.)

Application

This device is used for the equipment implementing a panel which displays a multiple image systems including a car navigation system, a display audio system, and other display equipment.

Features

- Analog video signal (CVBS) input
 - 1 channel of 10-bit ADC: 2 inputs
 - Pre-filter (LPF)
 - 2D comb filter for Y and C separation
 - Multi-color system decoder
- Digital video signal input
 - LVTTL: 1 channel
Maximum 85 MHz. YUV = 4:2:2 or RGB = 4:4:4
 - LVDS (Single 2channels or Dual 1channel)
Maximum 100 MHz. YUV = 4:4:4/4:2:2 or RGB = 4:4:4
- Scaling function
 - Up- scaling and down-scaling
 - Horizontal aberration correction
 - Trapezoidal correction
 - Non-linear extension
- Built-in frame memory
 - Overlay processing (an externally superimposed signal input, Chroma key processing, and rectangle region setting by a register)
 - Frame rate conversion
 - 3D-IP conversion (simple field superimposition)
- YUV picture improvement feature
 - Edge correction (HVD enhancer, sharpness, and CTI)
 - Static and dynamic YC-gamma correction
 - Color management
 - TINT adjustment
 - Contrast and brightness adjustment
 - Color gain and color offset adjustment
- RGB adjustment feature
 - Offset and gain adjustment
 - Gamma correction
 - Dither processing
- OSD superimposition
 - Font OSD display
 - Line drawing
- Digital signal output format
 - LVTTL: 1 channel
Maximum 80MHz(SDR mode), 75MHz(DDR mode)
YUV = 4:2:2 or RGB = 4:4:4
T-con pulse output (at RGB 18-bit output)
 - LVDS (Single 2 channels or Dual 1 channel)
Maximum 100 MHz. YUV = 4:4:4/4:2:2 or RGB = 4:4:4
- PWM output (2 pins)
- Built-in PLL (built-in SSCG function)
- I²C BUS control
- Operating temperature: -40 °C to 85 °C
- Power supply voltage: 1.2 V and 3.3 V

1. Block Diagram

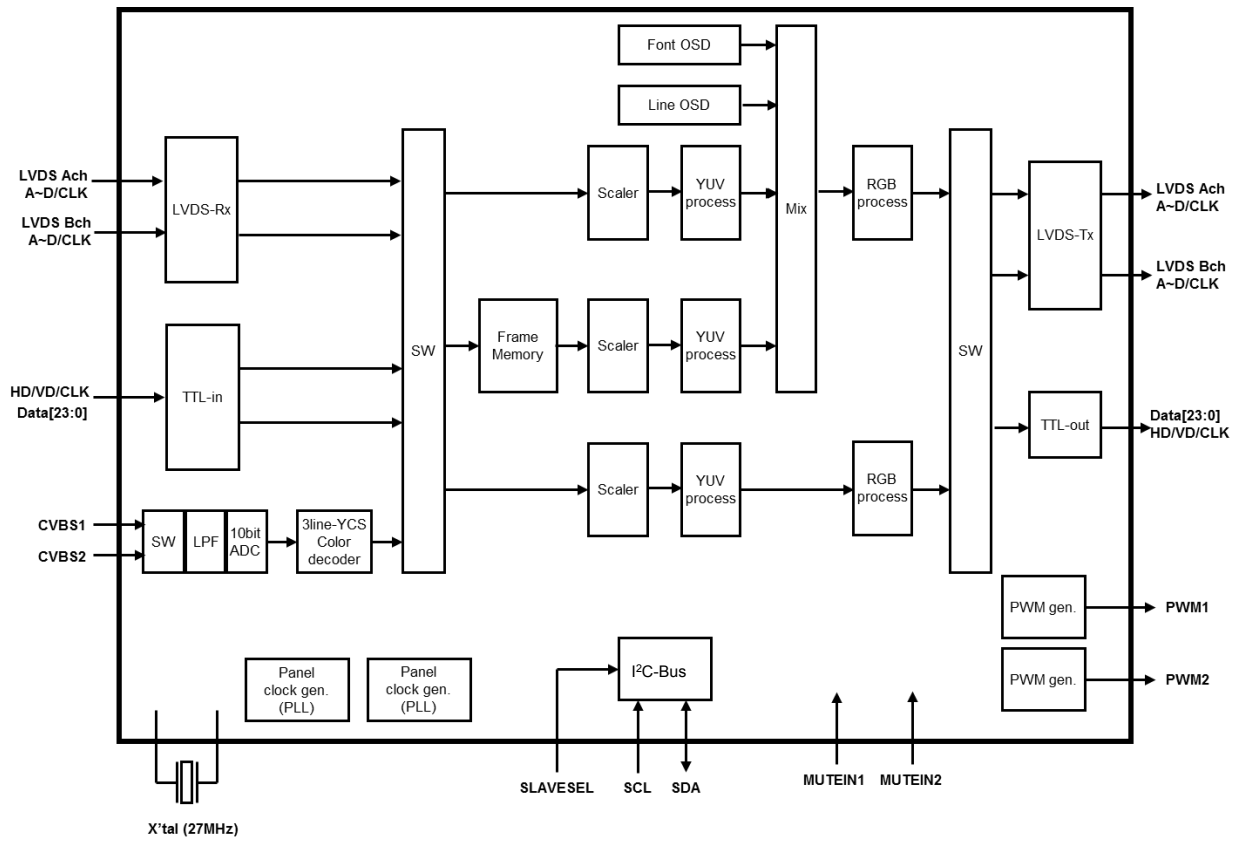


Figure 1.1 Block diagram

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

The absolute maximum ratings are the rated values which must not be exceeded during operation, even for an instant. Exceeding the maximum rating may result in destruction, degradation or other damages of the device.

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Core power supply (1.2 V)	VDD12	-0.3	—	VSS + 1.8	V
Standard I/O power supply (3.3 V)	VDD33	-0.3	—	VSS + 3.9	V
ADC power supply (1.2 V)	AVDD12	-0.3	—	VSS + 1.8	V
ADC power supply (3.3 V)	AVDD33	-0.3	—	VSS + 3.9	V
LVDS-Rx power supply (1.2 V)	RVDD12	-0.3	—	VSS + 1.8	V
LVDS-Rx power supply (3.3 V)	RVDD33	-0.3	—	VSS + 3.9	V
LVDS-Tx power supply (1.2 V)	TVDD12	-0.3	—	VSS + 1.8	V
LVDS-Tx power supply (3.3 V)	TVDD33	-0.3	—	VSS + 3.9	V
X'tal power supply (3.3 V)	XVDD33	-0.3	—	VSS + 3.9	V
PLL power supply (1.2 V)	PVDD12	-0.3	—	VSS + 1.8	V
DC input voltage (3.3 V)	VIN33	-0.3	—	VDD33 + 0.3	V
DC output voltage (3.3 V)	VOOUT33	-0.3	—	VDD33 + 0.3	V
DC input current	IIN	—	—	±10	mA
Operating ambient temperature	Ta	-40	—	85	°C
Storage temperature	Tstg	-40	—	125	°C

2.2. Operating Conditions

Table 2.2 Operating conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Core power supply (1.2 V)	VDD12	1.1	1.2	1.3	V
Standard I/O power supply (3.3 V)	VDD33	3.0	3.3	3.6	V
ADC power supply (1.2 V)	AVDD12	1.1	1.2	1.3	V
ADC power supply (3.3 V)	AVDD33	3.0	3.3	3.6	V
LVDS-Rx power supply (1.2 V)	RVDD12	1.1	1.2	1.3	V
LVDS-Rx power supply (3.3 V)	RVDD33	3.0	3.3	3.6	V
LVDS-Tx power supply (1.2 V)	TVDD12	1.1	1.2	1.3	V
LVDS-Tx power supply (3.3 V)	TVDD33	3.0	3.3	3.6	V
XTAL power supply (3.3 V)	XVDD33	3.0	3.3	3.6	V
PLL power supply (1.2 V)	PVDD12	1.1	1.2	1.3	V

2.3. Consumption current

Table 2.3 Consumption current

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Current of Core (1.2V)	IDD12	-	200	400	mA	PLL1/PLL2=75MHz, 1dot-crosshatch processing (Notes.1)
Current of Standard I/O (3.3 V)	IDD33	-	65	90	mA	At 75MHz output / RGB SDR clock mode / 1dot cross hatch pattern (Notes.2)
		-	55	70	mA	At 75MHz output / 8bit YUV DDR clock mode (Notes.2)
Current of ADC (1.2 V)	AIDD12	-	12	25	mA	—
Current of ADC (3.3V)	AIDD33	-	15	25	mA	—
Current of LVDS-Rx (1.2V)	RIDD12	-	75	90	mA	When Dual mode
Current of LVDS-Rx (3.3V)	RIDD33	-	60	100	mA	When Dual mode
Current of LVDS-Tx (1.2V)	TIDD12	-	10	20	mA	When Dual mode
Current of LVDS-Tx (3.3V)	TIDD33	-	100	120	mA	When Dual mode
Current of XTAL (3.3V)	XIDD33	-	5	10	mA	—
Current of PLL (1.2V)	PIDD12	-	10	15	mA	—

Notes1: The consumption current of Core (IDD12) is depends on operating frequency and using circuit block at this IC.

Notes2: The consumption current of Standard IO power is depends on the load capacity at output pin. When the load capacity is large value, the consumption current of IDD33 may exceed the above described maximum value.

2.4. 3.3V system I/O

Table 2.4 DC characteristic (3.3V system I/O)

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Input voltage	V _{IH}	VDD33 × 0.8	-	VDD33	V	I/O input terminal of 3.3V system
	V _{IL}	DVSS	-	VDD33 × 0.2		I/O input terminal of 3.3V system
Input current	I _{IH}	-10	-	10	μA	I/O input terminal of 3.3V system
	I _{IL}	-10	-	10		I/O input terminal of 3.3V system
Output voltage	V _{OH}	VDD33-0.6	-	VDD33	V	I/O output terminal of 3.3V system when load current 4mA
		VDD33-0.6	-	VDD33		I/O output terminal of 3.3V system when load current 8mA
	V _{OL}	DVSS	-	0.4		I/O output terminal of 3.3V system when load current 4mA
		DVSS	-	0.4		I/O output terminal of 3.3V system when load current 8mA

2.5. LVDS input

Table 2.5 DC characteristic (LVDS input)

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Input voltage	V _{IN}	0.2	-	2.4	V	-
Absolute input differential voltage	V _{id}	100	-	600	mV	-

2.6. LVDS output

Table 2.6 DC characteristic (LVDS output)

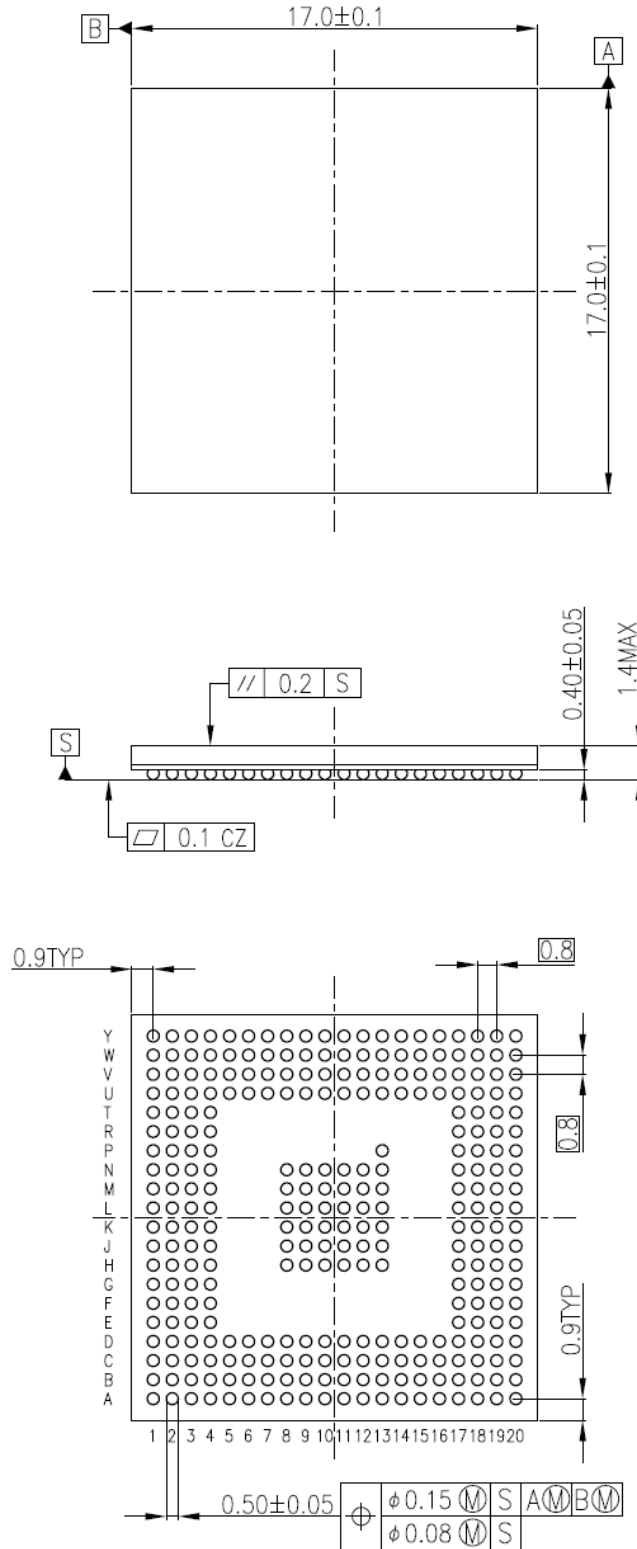
Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Output voltage	V _{OH}	-	-	1600	mV	R _{LOAD} =100Ω±1%
	V _{OL}	900	-	—	mV	R _{LOAD} =100Ω±1%
Absolute differential output voltage	V _{OD}	250	-	450	mV	R _{LOAD} =100Ω±1%
Output offset voltage	V _{OS}	1075	-	1325	mV	R _{LOAD} =100Ω±1%

3. Package Information

3.1. Package Diagram

P-LFBGA293-1717-0.80-001

Unit: mm



Weight: 0.66 g (Typical)

Figure 3.1 Package diagram

4. Revision History

Table 4.1 Revision history

Revision	Date	Description
1.00	2018-05-07	First edition

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