CMOS Digital Integrated Circuit Silicon Monolithic

TMPM4K Group(1)

LQFP64 10x10mm 0.5mm pitch
LQFP64 14x14mm 0.8mm pitch
LQFP48 7x7mm 0.5mm pitch
LQFP44 10x10mm 0.8mm pitch
LQFP32 7x7mm 0.8mm pitch

General Description

- Arm® Cortex®-M4 processor with FPU, Operation frequency: 1 to 80 MHz.
  Operation voltage: 2.7 to 5.5 V
- Code flash: 64 to 256 KB.
- Package: 32-pin to 64-pin. 5 types of packages are available.
- Hardware IPs such as A-VE+, 12-bit ADC, and A-PMD are provided for implementation of vector control and PFC control

Applications

Motors, major appliances using motors, and industrial equipment.

Features

- Arm Cortex-M4 processor with FPU
  - Operation frequency: 1 to 80 MHz
  - Memory Protection Unit (MPU)
- Low-power consumption mode
  - Operation voltage: 2.7 to 5.5 V
  - Low-power consumption operation: IDLE, STOP1
- Operation temperature: -40 to +105°C
- Internal memory
  - Code flash: 64 to 256 KB, rewritable up to 10,000 times
  - RAM: 18KB, with parity
- Clock
  - External high speed oscillator: 6 MHz to 12 MHz(Ceramic, Crystal)
  - External high speed clock input: 1 to 10 MHz
  - Internal high speed oscillator (IHOSC1): 10 MHz, user trimming function
  - PLL: 80 MHz output(System clock), 120 MHz output(for ADC)
- Oscillation frequency detector (OFD): Abnormal system clock detection
- Voltage Detection (LVD): 8 level, Generate interrupts and reset outputs
- Interruption
  - External: 6 to 11 factors, with DNF
  - internal: 66 to 76 factors
- I/O ports: 22 to 52
  - 5V-tolerant, open-drain, pull-up/-down
- On-chip debug (JTAG/SW), NBDIF(RAM monitor)
- Trigger Selector (TRGSEL)
  - Expand Trigger request for DMA controller, Timer, others
- DMA controller (DMAC)
  - DMA requests: 20 to 32 factors, internal/external triggers
- CRC Calculation Circuit (CRC): 1 channel, CRC32, CRC16
- Asynchronous Serial Interface (UART): 2 to 4 channels
  - 5Mbps(Max),FIFO(Send 8-stage, Receive 8-stage)
- Serial Peripheral Interface (TSPI): 1 to 4 channels
  - SIO mode,20Mbps(MAX),FIFO(Send 16bitx8,Receive: 16bitx8)
- I²C Interface (I²C): 0 to 1 channels
  - Multi Master
- 12-bit Analog to Digital Converter (ADC): 6 to 13 channel inputs
  - Conversion time: 0.5µs at f_{ADCLK}=120MHz
  - Self-diagnosis support function
- Operational amplifier(OPAMP): 1 to 3 channels
  - Gain selectable
- Advanced programmable motor control circuit (A-PMD): 1 to 2 channels
  - 3-phase complementary PWM output, Synchronized with 12-bit ADC
  - PFC control: support 3-phase interleaved PFC
  - Emergency stop function by external inputs (EMG pin, OVV pin)
- Advanced vector engine plus (A-VE+): 1 channel
  - Vector control coprocessor cooperates with ADC/A-PMD
  - 1-shunt current detection area can be enlarged
  - Dead time compensation control, non-interference control
- Advanced Encoder input circuit (A-ENC): 1 channel
  - Encoder/sensor (3 types)/Timer /Phase counter mode
- 32-bit Timer Event Counter (T32A)
  - 6 channels as 32-bit Timers, 12 channels as 16-bit Timers
  - Interval Timer, event counter, input capture, phase difference input, PPG output, Sync Start, Trigger start
- Watchdog Timer (SIWDT): 1 channel
  - Clock system other than the system clock can be selected
  - Clear window, interrupts and reset output

Start of commercial production
2018-07

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, Please contact your sales representative.

Table 1 Products Lists

Built-in Functions		TMPM4K4FYAUG TMPM4K4FWAUG TMPM4K4FUAUG TMPM4K4FSAUG	TMPM4K4FYAFG TMPM4K4FWAFG TMPM4K4FUAFG TMPM4K4FSAFG	TMPM4K2FYADUG TMPM4K2FWADUG TMPM4K2FUADUG TMPM4K2FSADUG	TMPM4K1FYAUG TMPM4K1FWAUG TMPM4K1FUAUG TMPM4K1FSAUG	TMPM4K0FSADUG
Memory	Code Flash (KB)	256 128 96 64	256 128 96 64	256 128 96 64	256 128 96 64	64
	RAM (KB)	18	18	18	18	18
I/O port	PORT (pin)	52	52	38	34	22
External interrupt	INT (pin)	11	11	10	9	6
DMA	DMAC (ch)	32	32	26	24	20
Timer function	T32A (ch)	6	6	6	6	6
Serial communication function	UART (ch)	4	4	3	2	2
	I^2C (ch)	1	1	1	1	0
	TSPI (SIO) (ch)	4	4	2	2	1
Analog function	12-bit ADC (AIN ch)	13	13	11	10	6
	OPAMP (ch)	3	3	3	3	1
Motor control peripherals	A-VE+ (ch)	1	1	1	1	1
	A-PMD (ch)	2	2	2	1	1
	A-ENC (ch)	1	1	1	1	1
Other peripherals	CRC (ch)	1	1	1	1	1
	RAMP (ch)	1	1	1	1	1
System function	LVD (ch)	1	1	1	1	1
	WDT (ch)	1	1	1	1	1
	OFD (ch)	1	1	1	1	1
	POR (ch)	1	1	1	1	1
Debug interface	Debug	JTAG/SW TRACE(4bits) NBDIF	JTAG/SW TRACE(4bits) NBDIF	JTAG/SW	JTAG/SW	JTAG/SW(Note)
Package	Package type	LQFP64 (10 mm x 10 mm, 0.5 mm pitch)	LQFP64 (14 mm x 14 mm, 0.8 mm pitch)	LQFP48 (7 mm x 7 mm, 0.5 mm pitch)	LQFP44 (10 mm x 10 mm, 0.8 mm pitch)	LQFP32 (7 mm x 7 mm, 0.8 mm pitch)
	Package name	P-LQFP64-1010 -0.50-003	P-LQFP64-1414 -0.80-002	P-LQFP48-0707 -0.50-002	P-LQFP44-1010 -0.80-003	P-LQFP32-0707 -0.80-002

Note: JTAG can use 4 pins (TMS,TCK,TDO,TDI).

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Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine plus
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High speed Oscillator
Fm	I^2C Fast Mode
IHOSC	Internal High speed Oscillator
INT	Interrupt
I^2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
POR	Power On Reset Circuit
RAMP	RAM parity
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Block Diagram

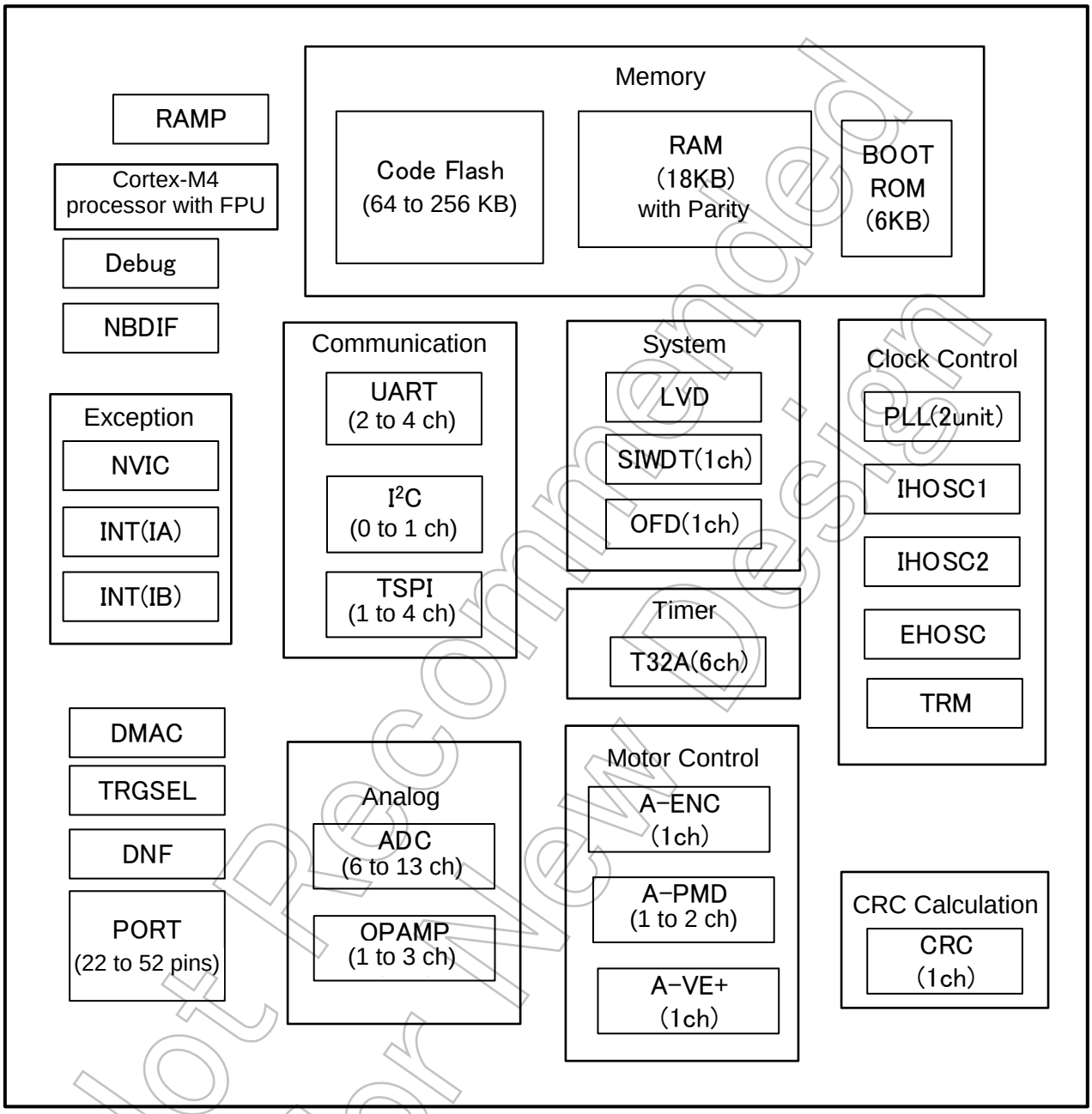
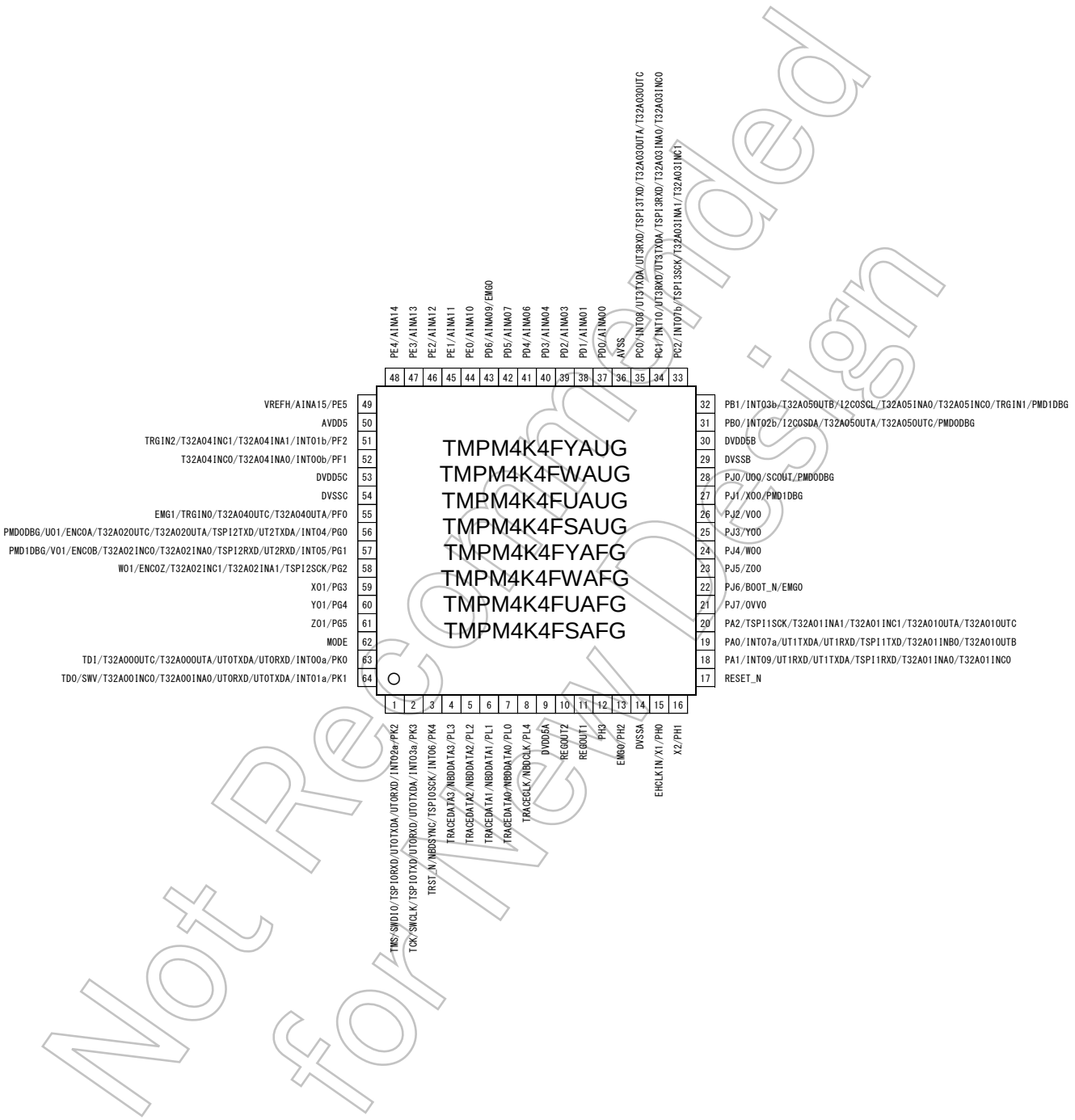


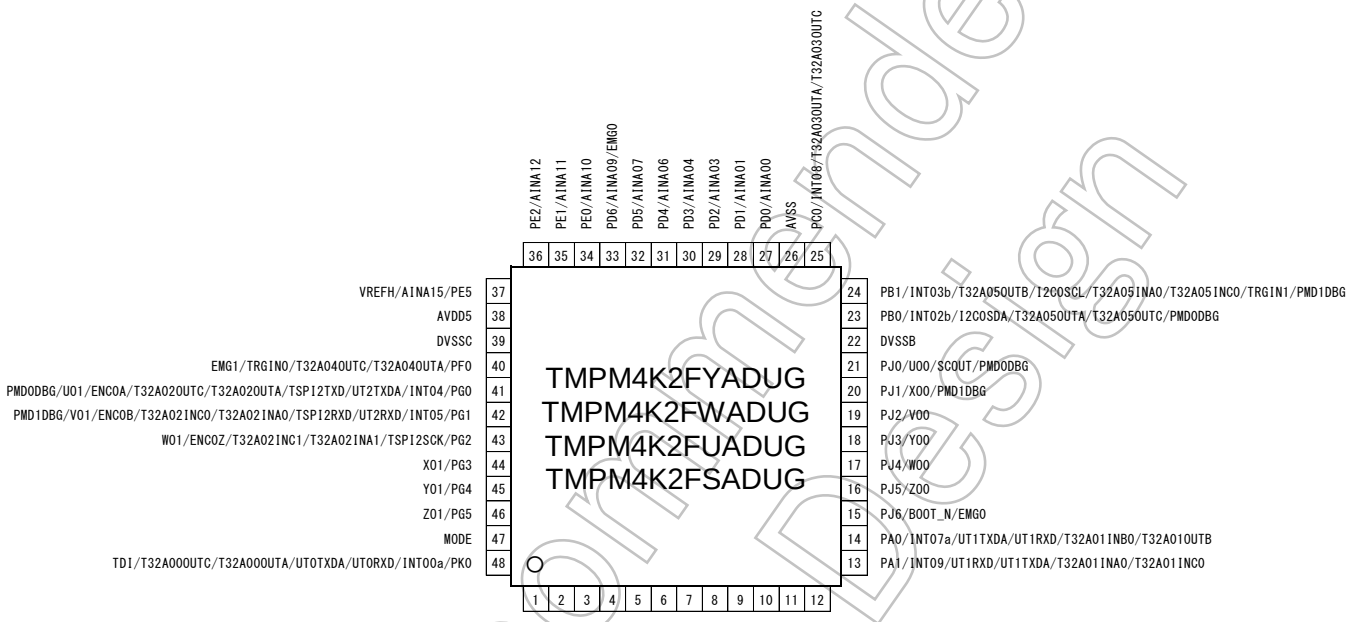
Figure 1.1 Block diagram of the TMPM4K Group(1)

2. Pin Assignment

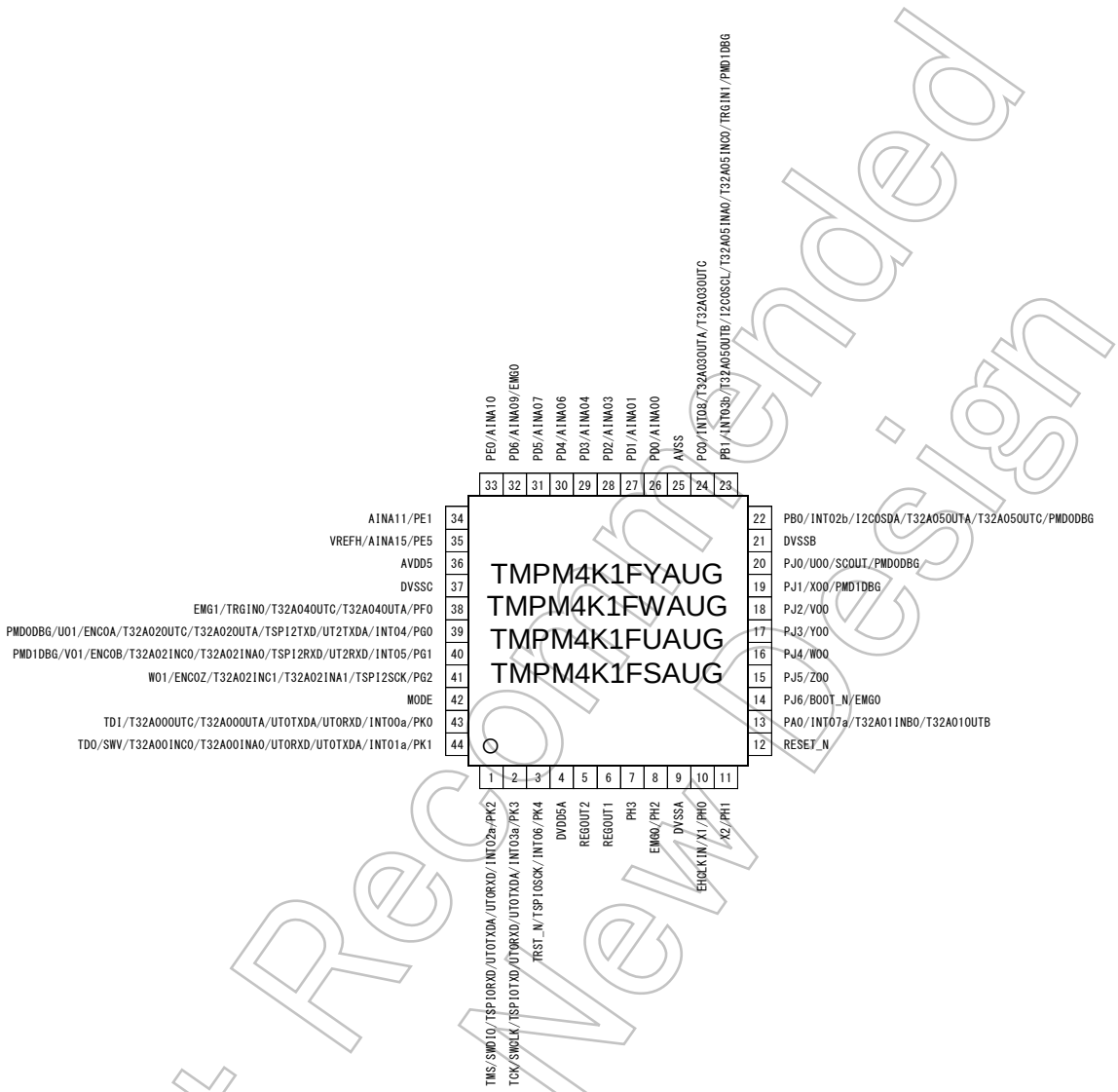
2.1. LQFP64



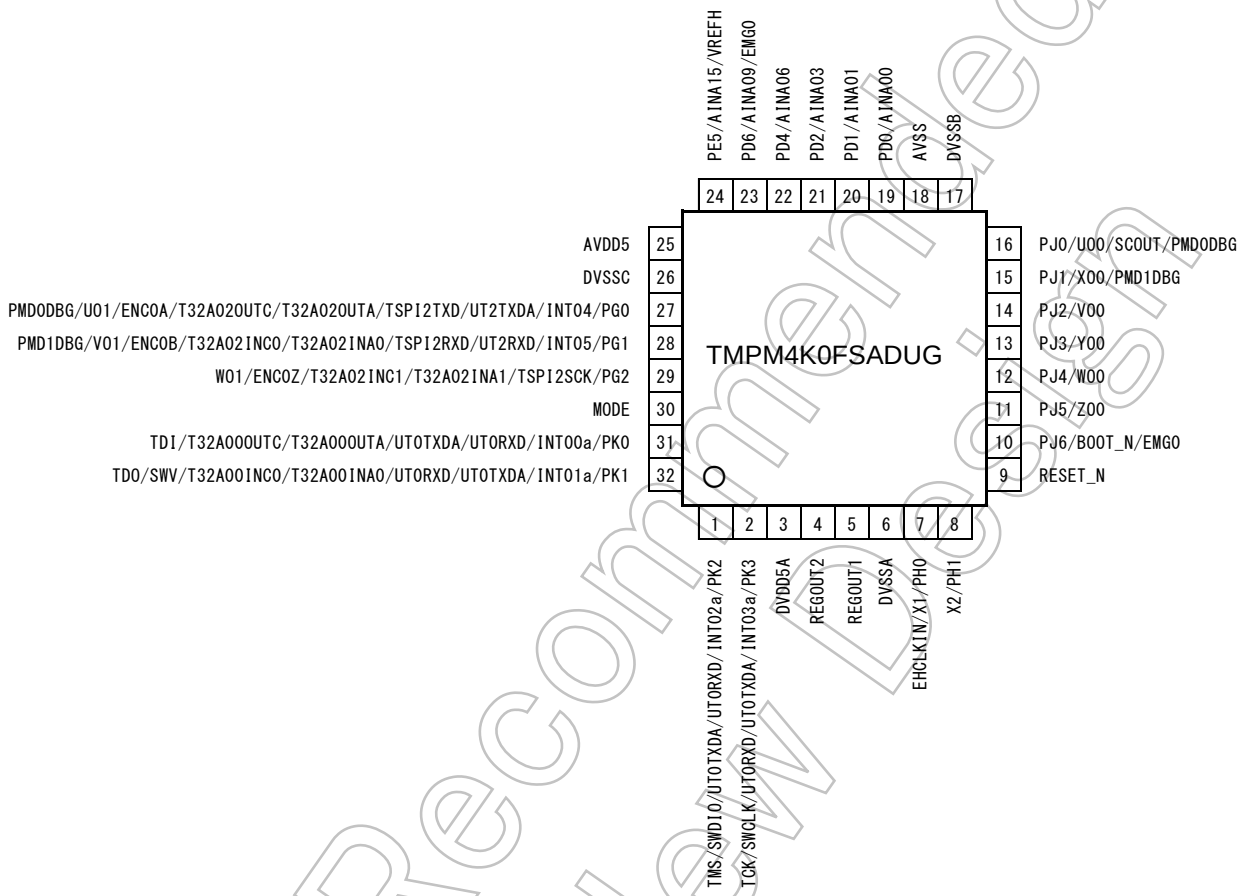
2.2. LQFP48



2.3. LQFP44



2.4. LQFP32



3. Memory Map

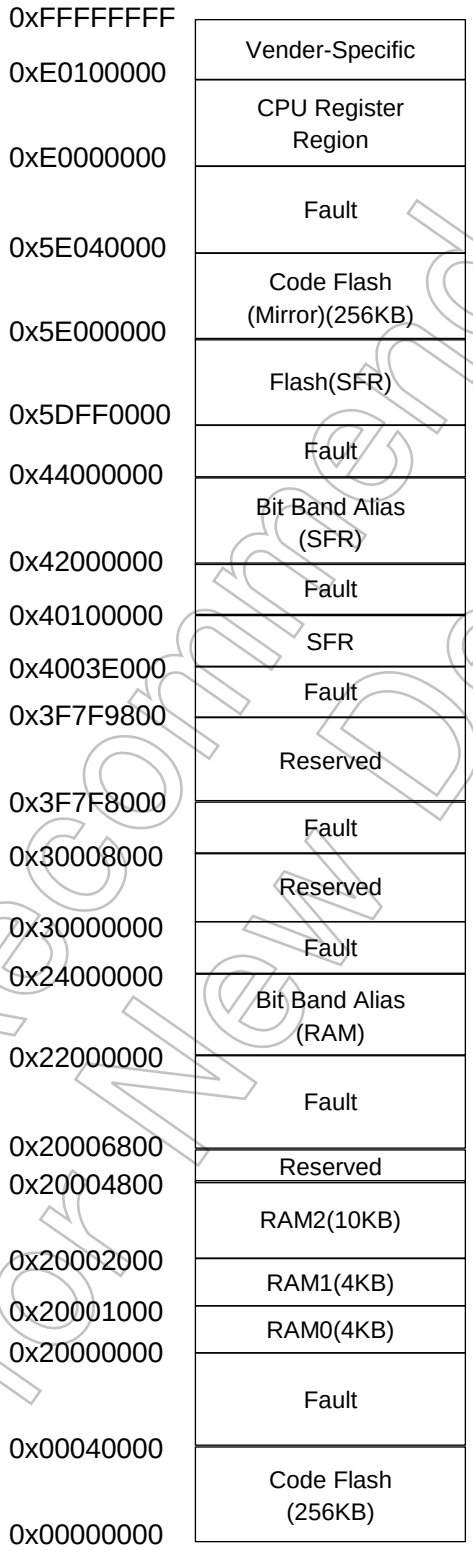


Figure 3.1 Example of the TMPM4KxFYA

Note: Fault, Reserved: Please do not access their region.

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM4K4FYAUG TMPM4K4FYAFG TMPM4K2FYADUG TMPM4K1FYAUG	TMPM4K4FWAUG TMPM4K4FWAFG TMPM4K2FWADUG TMPM4K1FWAUG	TMPM4K4FUAUG TMPM4K4FUAFG TMPM4K2FUADUG TMPM4K1FUAUG	TMPM4K4FSAUG TMPM4K4FSAFG TMPM4K2FSADUG TMPM4K1FSAUG TMPM4K0FSADUG
Peripheral region	Code Flash (Mirror)	Size	256 KB	128 KB	96 KB	64 KB
		START	0x5E000000	0x5E000000	0x5E000000	0x5E000000
		END	0x5E03FFFF	0x5E01FFFF	0x5E017FFF	0x5E00FFFF
SRAM region	RAM	Size	18KB			
		START	0x20000000			
		END	0x200047FF			
Code Region	Code Flash	Size	256KB	128KB	96KB	64KB
		START	0x00000000	0x00000000	0x00000000	0x00000000
		END	0x0003FFFF	0x0001FFFF	0x00017FFF	0x0000FFFF

4. Pin Description

4.1. Functional Pin Name and Functions

4.1.1. Function Pins of Peripheral

Table 4.1 Pin names and functions of peripheral pins

Peripheral function	Pin name	Input or Output	Function
Clock control and operation mode (CG)	SCOUT	Output	Output pin for the system clock
Interrupt control (IA/IB)	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: typ. 30 ns).
32-bit Timer event counter (T32A)	T32AxINA0	Input	16-bit timer A input capture input pin 0
	T32AxINA1	Input	16-bit timer A input capture input pin 1
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxINB1	Input	16-bit timer B input capture input pin 1
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer input capture input pin 0
	T32AxINC1	Input	32-bit timer input capture input pin 1
	T32AxOUTC	Output	32-bit timer output pin
Serial peripheral interface (TSPI)	TSPIxRXD	Input	Data input pin
	TSPIxTXD	Output	Data output pin
	TSPIxSCK	I/O	Clock input/output pin
Asynchronous serial communication circuit (UART)	UTxRXD	Input	Data input pin
	UTxTXDA	Output	Data output pin A
I^2C interface (I^2C)	I2CxSDA	I/O	Data input/output pin
	I2CxSCL	I/O	Clock input/output pin
Advanced Programmable Motor control circuit (A-PMD)	EMGx	Input	Emergency state detection input pin
	OVVx	Input	Overvoltage detection input pin
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
	PMDxDBG	Output	Debug output pin for motor control
Advanced Encoder input circuit (A-ENC)	ENCxA	Input	Encoder input pin A
	ENCxB	Input	Encoder input pin B
	ENCxZ	Input	Encoder input pin Z

Peripheral function	Pin name	Input or Output	Function
Analog to Digital Converter (ADC)	AINAx	Input	Analog input pin
Trigger input (TRGSEL)	TRGINx	Input	External trigger input pin

Note: "x" means channel number or unit number or interrupt number.

4.1.2. Debug Pins

Table 4.2 Debug pin names and their function

Debug PORT	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
	TRST_N	Input	JTAG test reset input pin
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin
TRACE	TRACECLK	Output	Trace clock output pin
	TRACEDATA0	Output	Trace data output pin 0
	TRACEDATA1	Output	Trace data output pin 1
	TRACEDATA2	Output	Trace data output pin 2
	TRACEDATA3	Output	Trace data output pin 3
NBDIF	NBDSYNC	Input	Non-break debug synchronous input pin
	NBDCLK	Input	Non-break debug clock input pin
	NBDDATA0	I/O	Non-break debug data output pin 0
	NBDDATA1	I/O	Non-break debug data output pin 1
	NBDDATA2	I/O	Non-break debug data output pin 2
	NBDDATA3	I/O	Non-break debug data output pin 3

4.1.3. Control Pins

Table 4.3 Control pin names and their function

	Pin name	Input or Output	Function
Control Pin	X1	Input	High speed oscillator connection pin
	X2	Output	High speed oscillator connection pin
	EHCLKIN	Input	External Clock signal input pin
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled on the rising edge of the RESET_N input. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single boot mode. If it is "High", the MCU enters single chip mode. For details, refer to "Flash Memory" of Reference Manual.
	RESET_N	Input	Reset signal input pin
	MODE	Input	Mode Pin This pin must be fixed to "Low" level.

4.1.4. Power Supply Pins

Table 4.4 Power supply pin names and their function

	Pin name	Function
Power Supply	DVDD5A (Note1) DVDD5B (Note1) DVDD5C (Note1)	Power supply pin for digital DVDD5A/B/C supplies the power to the following pins: PA to PC, PF to PL, MODE, RESET_N, BOOT_N A power supply is supplied to an oscillating circuit from a built-in regulator. X1, X2
	DVSSA (Note2) DVSSB (Note2) DVSSC (Note2)	GND pin for digital
	REGOUT1 (Note3)	Capacitor for a regulator connection pin (Note4)
	REGOUT2 (Note3)	Capacitor for a regulator connection pin (Note4)
	AVDD5	Power supply pin and reference power pin (VREFH) for analog are combination pins. AVDD5 supplies the power to the following pins: PD, PE
	AVSS	GND pin for analog, reference GND pin for analog

Note1: Apply the voltage to DVDD5A, DVDD5B, and DVDD5C at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA, DVSSB, and DVSSC at the same potential except the case that the pins are not provided.

Note3: For REGOUT1 and REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B, or DVDD5C; or DVSSA, DVSSB, or DVSSC.

Note4: For the capacitor value, refer to the "Electrical Characteristics".

Note5: Apply same voltage to DVDD5 and AVDD5.

4.1.5. Capacitors between power supply pins

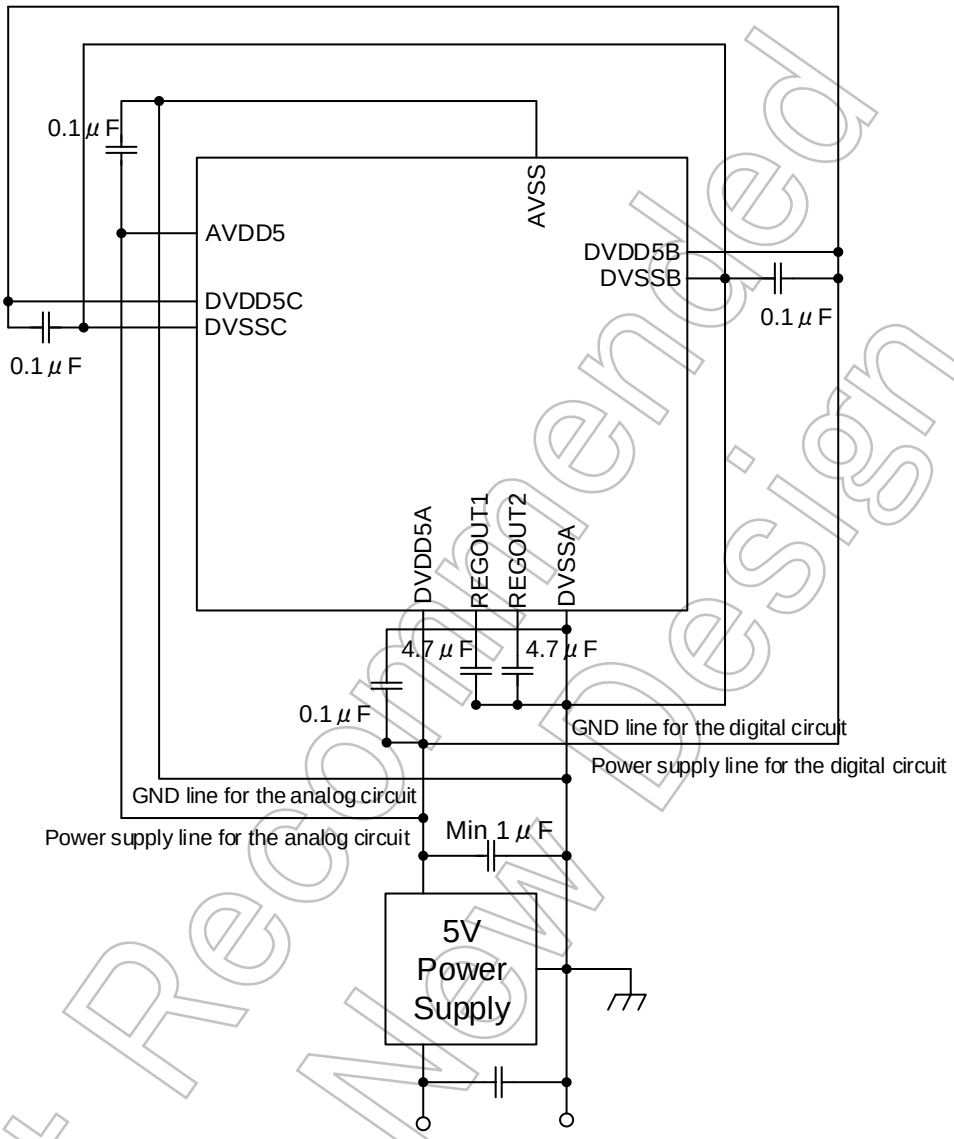


Figure 4.1 Capacitors for power supply pins connection circuit

Note1: Insert a ceramic capacitor of 1 µF or more near the output terminal of the 5V power supply.

Note2: Insert the bypass capacitor (about 0.01 to 0.1 µF) between the power supply and GND near each MCU power supply pin.

Note3: Insert the power supply stabilizing ceramic capacitor (4.7 µF) of the same capacity into the capacitor connection pin for the internal regulator (REGOUT1, REGOUT2). The capacitor should be placed near DVSSB pin.

Note4: In order to suppress noise mixing from the digital power supply to the analog circuit, separate the analog power supply line and the digital power supply line near the 5V power supply output.

Note5: In order to suppress noise mixing from the peripheral circuit to the analog circuit, when inserting a filter circuit or pull-up / down resistor to the input / output terminal of the analog power supply system, connect the components that make up these circuits to the analog power supply line.

Note6: In order to suppress high frequency noise received from the loop circuit by the power supply line, the GND line and the capacitor, do not separate the power supply line and the GND line from each other.

4.2. Functional Pin and Ports Assignment (Pin Number)

Following table shows a terminal number of the port assignment and each product which were seen from the functional pin.

"-" means that it does not have a pin or there is no assignment of a function.

Table 4.5 Signal connection List(1/6)

Function	Combination functional pin name	Port Name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
UART ch 0	UT0RXD	PK0	63	48	43	31
		PK1	64	1	44	32
		PK2	1	2	1	1
		PK3	2	3	2	2
	UT0TXDA	PK1	64	1	44	32
		PK0	63	48	43	31
		PK3	2	3	2	2
		PK2	1	2	1	1
UART ch 1	UT1RXD	PA1	18	13	-	-
		PA0	19	14		
	UT1TXDA	PA0	19	14		
		PA1	18	13		
UART ch 2	UT2RXD	PG1	57	42	40	28
	UT2TXDA	PG0	56	41	39	27
UART ch 3	UT3RXD	PC1	34	-	-	-
		PC0	35			
	UT3TXDA	PC0	35			
		PC1	34			
I^2C ch 0	I2C0SDA	PB0	31	23	22	-
	I2C0SCL	PB1	32	24	23	
TSPI ch 0	TSPI0RXD	PK2	1	2	1	-
	TSPI0TXD	PK3	2	3	2	
	TSPI0SCK	PK4	3	4	3	
TSPI ch 1	TSPI1RXD	PA1	18	-	-	-
	TSPI1TXD	PA0	19			
	TSPI1SCK	PA2	20			
TSPI ch 2	TSPI2RXD	PG1	57	42	40	28
	TSPI2TXD	PG0	56	41	39	27
	TSPI2SCK	PG2	58	43	41	29
TSPI ch 3	TSPI3RXD	PC1	34	-	-	-
	TSPI3TXD	PC0	35			
	TSPI3SCK	PC2	33			

Table 4.6 Signal connection List(2/6)

Function	Combination functional pin name	Port Name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
T32A ch 0	T32A00INA0	PK1	64	1	44	32
	T32A00OUTA	PK0	63	48	43	31
	T32A00INC0	PK1	64	1	44	32
	T32A00OUTC	PK0	63	48	43	31
T32A ch 1	T32A01INA0	PA1	18	13	-	-
	T32A01INA1	PA2	20	-	-	-
	T32A01OUTA	PA2	20	-	-	-
	T32A01INB0	PA0	19	14	13	-
	T32A01OUTB	PA0	19	14	13	-
	T32A01INC0	PA1	18	13	-	-
	T32A01INC1	PA2	20	-	-	-
	T32A01OUTC	PA2	20	-	-	-
T32A ch 2	T32A02INA0	PG1	57	42	40	28
	T32A02INA1	PG2	58	43	41	29
	T32A02OUTA	PG0	56	41	39	27
	T32A02INC0	PG1	57	42	40	28
	T32A02INC1	PG2	58	43	41	29
	T32A02OUTC	PG0	56	41	39	27
T32A ch 3	T32A03INA0	PC1	34	-	-	-
	T32A03INA1	PC2	33	-	-	-
	T32A03OUTA	PC0	35	25	24	-
	T32A03INC0	PC1	34	-	-	-
	T32A03INC1	PC2	33	-	-	-
	T32A03OUTC	PC0	35	25	24	-
T32A ch 4	T32A04INA0	PF1	52	-	-	-
	T32A04INA1	PF2	51	-	-	-
	T32A04OUTA	PF0	55	40	38	-
	T32A04INC0	PF1	52	-	-	-
	T32A04INC1	PF2	51	-	-	-
	T32A04OUTC	PF0	55	40	38	-
T32A ch 5	T32A05INA0	PB1	32	24	23	-
	T32A05OUTA	PB0	31	23	22	-
	T32A05OUTB	PB1	32	24	23	-
	T32A05INC0	PB1	32	24	23	-
	T32A05OUTC	PB0	31	23	22	-

Table 4.7 Signal connection List(3/6)

Function	Combination functional pin name	Port Name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
12-bit ADC unit A	AINA00	PD0	37	27	26	19
	AINA01	PD1	38	28	27	20
	AINA03	PD2	39	29	28	21
	AINA04	PD3	40	30	29	-
	AINA06	PD4	41	31	30	22
	AINA07	PD5	42	32	31	-
	AINA09	PD6	43	33	32	23
	AINA10	PE0	44	34	33	-
	AINA11	PE1	45	35	34	-
	AINA12	PE2	46	36	-	-
	AINA13	PE3	47	-	-	-
	AINA14	PE4	48	-	-	-
	AINA15	PE5	49	37	35	24
INT	INT00a	PK0	63	48	43	31
	INT00b	PF1	52	-	-	-
	INT01a	PK1	64	1	44	32
	INT01b	PF2	51	-	-	-
	INT02a	PK2	1	2	1	1
	INT02b	PB0	31	23	22	-
	INT03a	PK3	2	3	2	2
	INT03b	PB1	32	24	23	-
	INT04	PG0	56	41	39	27
	INT05	PG1	57	42	40	28
	INT06	PK4	3	4	3	-
	INT07a	PA0	19	14	13	-
	INT07b	PC2	33	-	-	-
	INT08	PC0	35	25	24	-
	INT09	PA1	18	13	-	-
	INT10	PC1	34	-	-	-

Table 4.8 Signal connection List(4/6)

Function	Combination functional pin name	Port Name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
A-PMD ch 0	EMG0	PJ6	22	15	14	10
		PD6	43	33	32	23
		PH2	13	8	8	-
	OVV0	PJ7	21	-	-	-
	UO0	PJ0	28	21	20	16
	VO0	PJ2	26	19	18	14
	WO0	PJ4	24	17	16	12
	XO0	PJ1	27	20	19	15
	YO0	PJ3	25	18	17	13
	ZO0	PJ5	23	16	15	11
	PMD0DBG	PB0	31	23	22	-
		PG0	56	41	39	27
		PJ0	28	21	20	16
A-PMD ch 1	EMG1	PF0	55	40	38	-
	UO1	PG0	56	41	39	27
	VO1	PG1	57	42	40	28
	WO1	PG2	58	43	41	29
	XO1	PG3	59	44	-	-
	YO1	PG4	60	45	-	-
	ZO1	PG5	61	46	-	-
	PMD1DBG	PB1	32	24	23	-
		PJ1	27	20	19	15
		PG1	57	42	40	28
A-ENC ch 0	ENC0A	PG0	56	41	39	27
	ENC0B	PG1	57	42	40	28
	ENC0Z	PG2	58	43	41	29

Table 4.9 Signal connection List(5/6)

Function	Combination functional pin name	Port Name	M4K4 (LQFP64)	M4K22 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
TRGSEL	TRGIN0	PF0	55	40	38	-
	TRGIN1	PB1	32	24	23	-
	TRGIN2	PF2	51	-	-	-
JTAG/SW	TMS	PK2	1	2	1	1
	TCK	PK3	2	3	2	2
	TDO	PK1	64	1	44	32
	TDI	PK0	63	48	43	31
	TRST_N	PK4	3	4	3	-
	SWDIO	PK2	1	2	1	1
	SWCLK	PK3	2	3	2	2
	SWV	PK1	64	1	44	32
TRACE	TRACECLK	PL4	8	-	-	-
	TRACEDATA0	PL0	7			
	TRACEDATA1	PL1	6			
	TRACEDATA2	PL2	5			
	TRACEDATA3	PL3	4			
NBDIF	NBDSYNC	PK4	3	-	-	-
	NBDCLK	PL4	8			
	NBDDATA0	PL0	7			
	NBDDATA1	PL1	6			
	NBDDATA2	PL2	5			
	NBDDATA3	PL3	4			

Table 4.10 Signal connection List(6/6)

Function	Pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)	M4K0 (LQFP32)
Input/output port	PH3		12	-	7	-
Control pin	X1	PH0	15	10	10	7
	X2	PH1	16	11	11	8
	EHCLKIN	PH0	15	10	10	7
	SCOUT	PJ0	28	21	20	16
	BOOT_N	PJ6	22	15	14	10
	RESET_N		17	12	12	9
	MODE		62	47	42	30
Power supply pin	AVDD5		50	38	36	25
	AVSS		36	26	25	18
	DVDD5A		9	5	4	3
	DVDD5B		30	-	-	-
	DVDD5C		53	-	-	-
	DVSSA		14	9	9	6
	DVSSB		29	22	21	17
	DVSSC		54	39	37	26
	REGOUT1		11	7	6	5
	REGOUT2		10	6	5	4

4.3. Ports

The symbols of each table of the port have the following meanings.

- Input/Output: Input or/and Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/Output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  Yes: Support
  No: Non support

- 5V_T: 5V-tolerant
  Yes: Support
  N/A: Not available

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- State Under Reset: Port state under Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

- State After Reset: Port state after Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

4.3.1. Port Specification Table

Table 4.11 Pin numbers, and specifications of Port A,B,C,D,E,F,G

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PA0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB0	Input/Output	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PB1	Input/Output	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PC0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD3	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD4	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD5	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD6	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE3	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE4	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE5	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG3	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG4	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG5	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Table 4.12 Pin numbers, and specifications of Port H, J, K, L

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PH0	Input	PD	N/A	N/A	SMT	Hi-z	Hi-z
PH1	Input	PD	N/A	N/A	SMT	Hi-z	Hi-z
PH2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH3	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ3	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ4	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ5	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ6	Input/Output	PU/PD (Note1)	YES	N/A	SMT	PU	Hi-z
PJ7	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK0	Input/Output	PU/PD	YES	N/A	SMT	PU (Note2)	PU (Note2)
PK1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z (Note2)	Hi-z Note2
PK2	Input/Output	PU/PD	YES	N/A	SMT	PU (Note2)	PU (Note2)
PK3	Input/Output	PU/PD	YES	N/A	SMT	PD (Note2)	PD (Note2)
PK4	Input/Output	PU/PD	YES	N/A	SMT	PU (Note2)	PU (Note2)
PL0	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL1	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL2	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL3	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL4	Input/Output	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Note1: Combination with BOOT_N. When RESET_N=0, Pull-up resistor is enabled. When RESET_N=1, the pin state is Hi-z with internal reset.

Note2: It is assigned to a debugging pin in the state of the initial stage. (PK0: TDI, PK1: TDO/SWV, PK2: TMS/SWDIO, PK3: TCK/SWCLK, PK4: TRST_N)
When receiving the command from TOOL, PK1: TDO/SWV becomes output.

5. Functional Description and Operation Description

5.1. Reference Manuals

For more information on product of TMPM4K Group(1), please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM4K Group(1)

Reference Manual	IP Symbol	Category
Input/Output Ports (TMPM4K Group(1))	PORT-M4K(1)	System
Memory Map (TMPM4K Group(1))	MMAP-M4K(1)	System
Exception (TMPM4K Group(1))	EXCEPT-M4K(1)	System
Clock Control and Operation Mode (TMPM4K Group(1))	CG-M4K(1)-A	System
Product Information (TMPM4K Group(1))	PINFO-M4K(1)	System
Power supply and Reset operation (TMPM4K Group(1))	RESET-M4K(1)	System
Flash Memory	FLASH256-B	Peripheral
Trimming Circuit	TRM-A	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-B	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
Non-break debug Interface	NBDIF-A	Peripheral
DMA Controller	DMAC-B	Peripheral
Asynchronous Serial Communication Circuit	UART-C	Peripheral
Serial Peripheral Interface	TSPI-B	Peripheral
I^2C Interface	I2C-B	Peripheral
12-bit Analog to Digital Converter	ADC-B	Peripheral
OPAMP	OPAMP-A	Peripheral
Advanced Programmable Motor Control Circuit	A-PMD-A	Peripheral
Advanced Encoder Input Circuit	A-ENC-A	Peripheral
Advanced Vector Engine Plus	A-VE+-B	Peripheral
32-bit Timer Event Counter	T32A-B	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
CRC Calculation Circuit	CRC-A	Peripheral
RAM Parity	RAMP-A	Peripheral

5.2. Processor Core

The TMPM4K Group(1) incorporates a high-performance 32-bit processor core (Arm Cortex-M4 processor with FPU).

For the operation of the processor core, refer to the Arm documentation set for "Cortex-M series processors". This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M4 processor with FPU revision used in the TMPM4K Group(1) is shown as below:

For details of the CPU core and the architecture, refer to the documentation of the Arm in the following URL:

http://infocenter.arm.com/help/index.jsp

Table 5.2 Core revision

Group name	Core revision
TMPM4K Group(1)	r0p1

5.2.2. Configurable Options

In the Cortex-M4 processor with FPU, some blocks can be selected to implement. The following table shows the configurations of the TMPM4K Group(1).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/Serial wire
Bit band	Available
Sequential control of AHB	Not available

5.3. Clock Control and Operation Mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The outline of the clock/mode control circuit is as follows:

- Internal high speed oscillator: 10MHz
- Selectable from the external high speed oscillator or internal high speed oscillator.
- PLL (Clock Multiplication Circuit)

For System clock, Capable of 80 MHz output by changing the multiplication ratio according to the frequency of the high speed oscillation circuit.

For ADC Clock, Capable of 120 MHz output by changing the multiplication ratio according to the AD conversion speed and the frequency of the high speed oscillation circuit.

- Clock gear:

The high speed clock can be divided by 1/1, 1/2, 1/4, 1/8, or 1/16 and the clock is used as the system clock (fsys).

- Low-power consumption mode:

  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enable or disable operation in the IDLE mode.

  STOP1: The system clock is stopped in this mode.

5.4. Flash Memory (256KB/128KB/96KB/64KB)

The cord flash stores instruction code, and CPU reads instruction code and executes.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

5.5. Oscillator

External High Speed Oscillator (EHOSC):

Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.

Internal High Speed Oscillator 1 (IHOSC1):

The oscillation frequency is 10MHz. Use clock source for System clock.

Internal High Speed Oscillator 2 (IHOSC2):

The oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

	M4K4	M4K2	M4K1	M4K0
EHOSC	✓	✓	✓	✓
IHOSC1	✓	✓	✓	✓
IHOSC2	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust oscillation frequency of the internal high speed oscillator 1 (IHOSC1).

Table 5.5 Built-in TRM

	M4K4	M4K2	M4K1	M4K0
TRM	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detector (OFD) is a function that detects an abnormal state of the clock. It measures the external high speed oscillation (f_{EHOSC}) or high speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.

The upper limit and the lower limit of detection frequency ranges can be specified respectively.

Table 5.6 Built-in OFD

	M4K4	M4K2	M4K1	M4K0
OFD	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from eight kinds. LVD is set to enable from the Reset state at the Power on.

Table 5.7 Built-in LVD

	M4K4	M4K2	M4K1	M4K0
LVD	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter circuit(DNF)

The digital noise filter circuit can eliminate the noise of input signals from external interrupt pins at the certain range. The noise of the High level / Low level input of the external interrupt signal INTx is removed.

Table 5.8 Number of External Interrupt (Built-in DNF)

DNF	M4K4	M4K2	M4K1	M4K0
Number of External Interrupt	11	10	9	6

5.10. Debug Interface (DEBUG)

TMPM4K Group(1) contain Interface for connecting debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the Debug tool and used for program development. And also it contains the trace clock(TRACECLK), data output (TRACEDATA0to3) and the NBDIF(NBDSYNC, NBDCLK, NBDDATA0 to 3) to reduce the Debug Process.

TMPM4K Group(1) products support serial wire debug ports, JTAG debug ports, trace outputs, and NBDIF.

Table 5.9 Built-in Debug Interface

Debug Pin (Signal Name)	PORT	M4K4	M4K2	M4K1	M4K0
TMS/SWDIO	PK2	✓	✓	✓	✓
TCK/SWCLK	PK3	✓	✓	✓	✓
TDO/SWV	PK1	✓	✓	✓	✓
TDI	PK0	✓	✓	✓	✓
TRST_N	PK4	✓	✓	✓	-
TRACECLK	PL4	✓	-	-	-
TRACEDATA0	PL0	✓	-	-	-
TRACEDATA1	PL1	✓	-	-	-
TRACEDATA2	PL2	✓	-	-	-
TRACEDATA3	PL3	✓	-	-	-
NBDSYNC	PK4	✓	-	-	-
NBDCLK	PL4	✓	-	-	-
NBDDATA0	PL0	✓	-	-	-
NBDDATA1	PL1	✓	-	-	-
NBDDATA2	PL2	✓	-	-	-
NBDDATA3	PL3	✓	-	-	-

Note: ✓: Available, -: N/A

5.10.1. Non-Break Debug Interface (NBDIF)

Connecting debug tools supporting NBDIF can provide RAM monitor function.
NBDIF support vary depending on the product. Please refer to "Table 5.9 Built-in Debug Interface".

5.11. DMA Controller (DMAC)

The DMAC is the peripheral function to move the data between peripheral functions and the memory, or between memories. These operations are performed separately from the CPU control; thus, the CPU load can greatly be reduced by using the DMA.

DMAC has the 32 channels DMA requests per unit.

Table 5.10 Built-in DMAC

DMAC	M4K4	M4K2	M4K1	M4K0
Unit A	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.12. Asynchronous Serial Communication Circuit (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first / LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8-stage at transmission; and on 8-stage at reception.

Table 5.11 Built-in UART

UART	M4K4	M4K2	M4K1	M4K0
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	-	-
Channel 2	✓	✓	✓	✓
Channel 3	✓	-	-	-

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

5.13. Serial Peripheral Interface (TSPI)

The TSPI supports SIO bus type which does not use a CS signal at communications and enables to perform serial communication between other devices at high speed.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There is an 8-stage 16-bit FIFO for reception and transmission, each. The TSPI supports the master and slave communications.

Table 5.12 Built-in TSPI

TSPI(SIO)	M4K4	M4K2	M4K1	M4K0
Channel 0	✓	✓	✓	-
Channel 1	✓	-	-	-
Channel 2	✓	✓	✓	✓
Channel 3	✓	-	-	-

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

5.14. I^2C Interface (I^2C)

I^2C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports Standard mode (Max 100kbps), Fast mode (Max 400kbps).

Table 5.13 Built-in I^2C

I^2C	M4K4	M4K2	M4K1	M4K0
Channel 0	✓	✓	✓	-

Note: ✓: Available, -: N/A

5.15. 12-bit Analog to Digital Converter (ADC)

The ADC is a successive-approximation analog-to-digital converter. The combination of a conversion result register and analog input can be programmed in each startup trigger of AD conversion. A startup trigger for analog-to-digital conversion can be selected from software or peripheral functions (A-PMD trigger outputs, timer/event counter outputs, port inputs).

The monitor function of conversion result is also available and it can generate an interrupt request when the compare conditions are matched.

This ADC incorporates a selector to connect VREFH/VREFL with reference power supply. Controlling by software can support self-diagnosis function.

Table 5.14 Built-in ADC

ADC	M4K4	M4K2	M4K1	M4K0
Unit A	✓	✓	✓	✓
Analog Inputs Pin count	13	11	10	6

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

5.16. Operational amplifier(OPAMP)

This MCU incorporates an OPAMP to amplify weak analog signals inputting to the ADC. The input gain is selectable.

Table 5.15 Built-in OPAMP

OPAMP	M4K4	M4K2	M4K1	M4K0
Unit A	✓	✓	✓	✓
Unit B	✓	✓	✓	-
Unit C	✓	✓	✓	-

Note: ✓: Available, -: N/A

5.17. Advanced Programmable Motor Control Circuit (A-PMD)

The advanced programmable motor control circuit (A-PMD) enables users to control brushless DC motors easily. It incorporates the three-phase pulse modulation circuit and dead-time circuit, and easily generates waveforms for motor control by operating with the ADC in a coordinated fashion.

It also provides the over-voltage detection input and abnormal detection input to support safety measures.

Furthermore, 3-phase interleaved PFC control for power-factor improvement can be provided.

Table 5.16 Built-in A-PMD

A-PMD	M4K4	M4K2	M4K1	M4K0
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	- (Note3)	- (Note3)

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

Note3: This product cannot be used for 3 phase motor drive, but some pins are assigned.

5.18. Advanced Encoder Input Circuit (A-ENC)

The advanced encoder input circuit (A-ENC) supports an incremental encoder to acquire the motor position easily. The noise canceller is installed in the input pins, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC provides six operation modes: encoder mode, sensor modes (3 kinds), timer mode, and phase counter mode.

Table 5.17 Built-in A-ENC

A-ENC	M4K4	M4K2	M4K1	M4K0
Channel 0	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.19. Advanced Vector Engine Plus (A-VE+)

The advanced vector engine plus executes vector control by hardware. In this vector operation, the ADC and A-PMD operate in a coordinated fashion without software involvement.

Also, it provides 1-shunt current detection area enlargement process, dead time compensation control, and non-interfere control.

Table 5.18 Built-in A-VE+

A-VE+	M4K4	M4K2	M4K1	M4K0
Channel 0	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.20. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter respectively. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A have an interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.19 Built-in T32A

T32A	M4K4	M4K2	M4K1	M4K0
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓
Channel 5	✓	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2 Pin Assignment".

5.21. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys/4), internal oscillator 1 (f_{IHOSC1}), or internal oscillator 2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, change of a register can be forbidden until reset starts by setting to protected mode.(the count-clear function is possible)

Table 5.20 Built-in SIWDT

	M4K4	M4K2	M4K1	M4K0
SIWDT	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.22. CRC Calculation Circuit (CRC)

This product has the Hardware calculation circuit for CRC32 and CRC16.

It can be used for detecting a memory and communication data error.

Table 5.21 Built-in CRC

	M4K4	M4K2	M4K1	M4K0
CRC	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.23. RAM Parity (RAMP)

A RAM parity function generates and (8-bit unit) stores even parity data at the time of the writing to RAM, and performs a parity judging at the time of reading from RAM.

An interrupt is generated when it becomes an error by judgment. The Status and Address which the error generated are known.

A parity error is detectable in real time, since parity generating/ judgment is hardware.

Table 5.22 Built-in RAMP

	M4K4	M4K2	M4K1	M4K0
RAMP	✓	✓	✓	✓

Note: ✓: Available, -: N/A

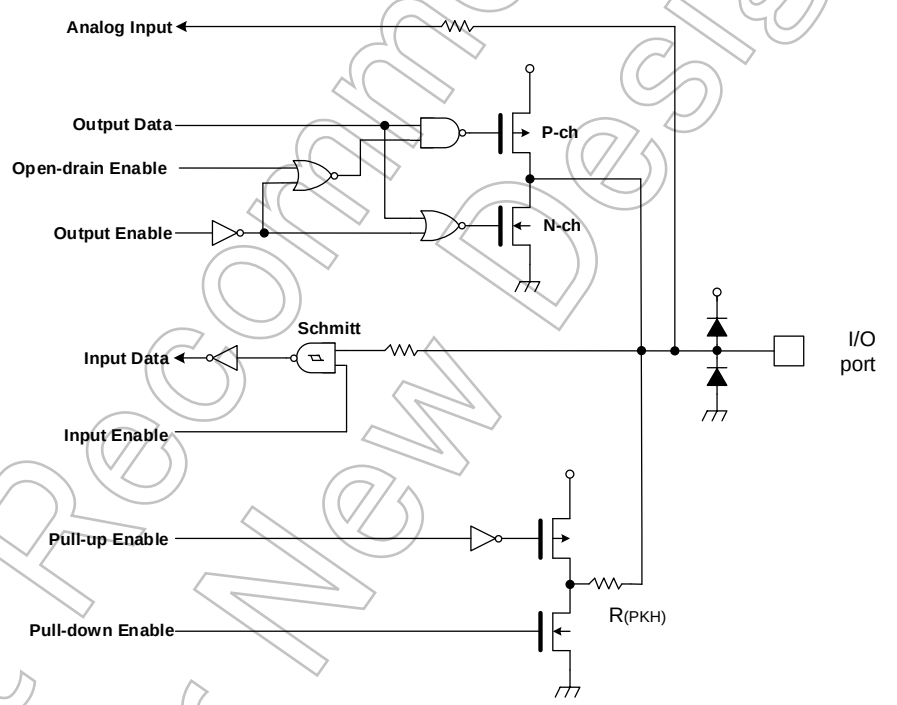
6. Equivalent Circuit

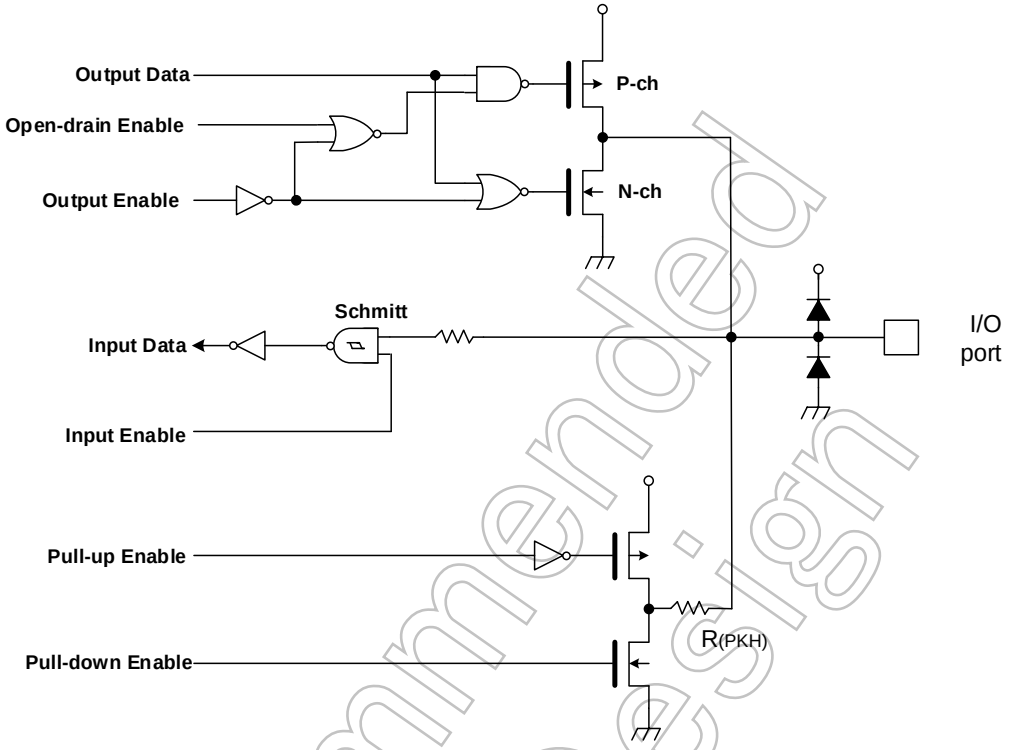
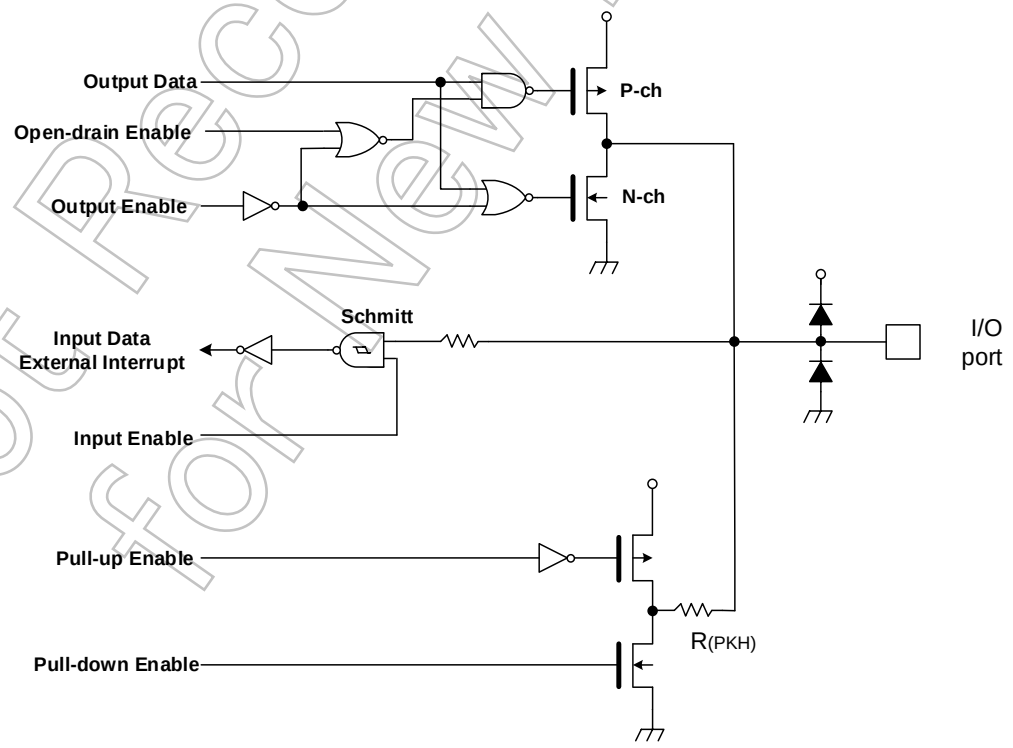
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCXX] series.
The input protection resistance ranges from several tens of Ω to several hundred Ω. Feedback resistor and Damping resistor are shown with a typical value.

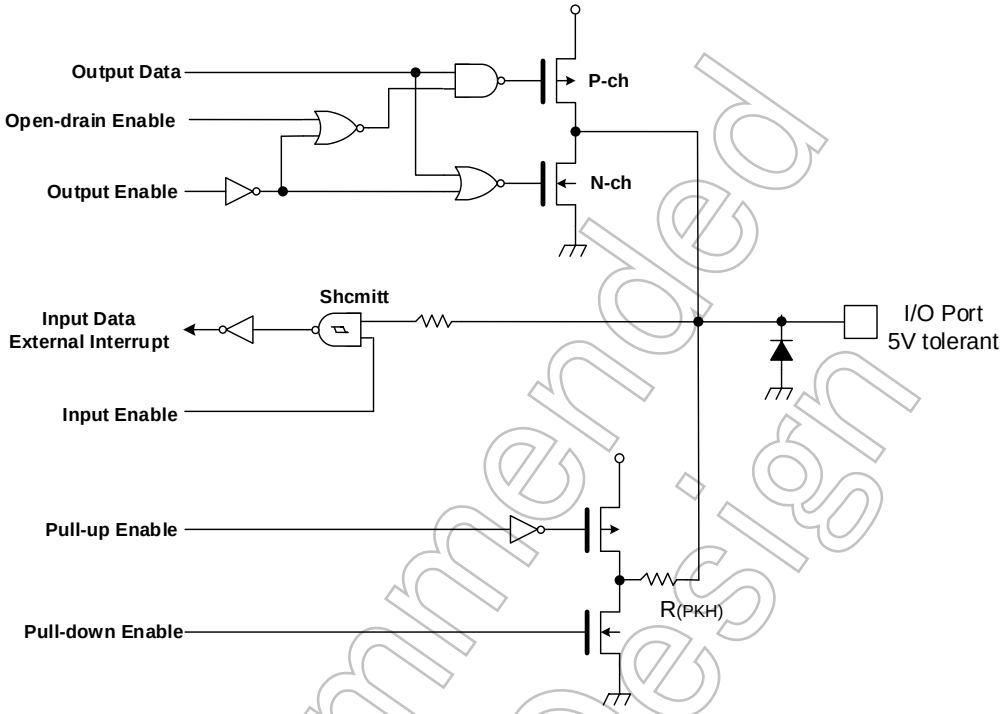
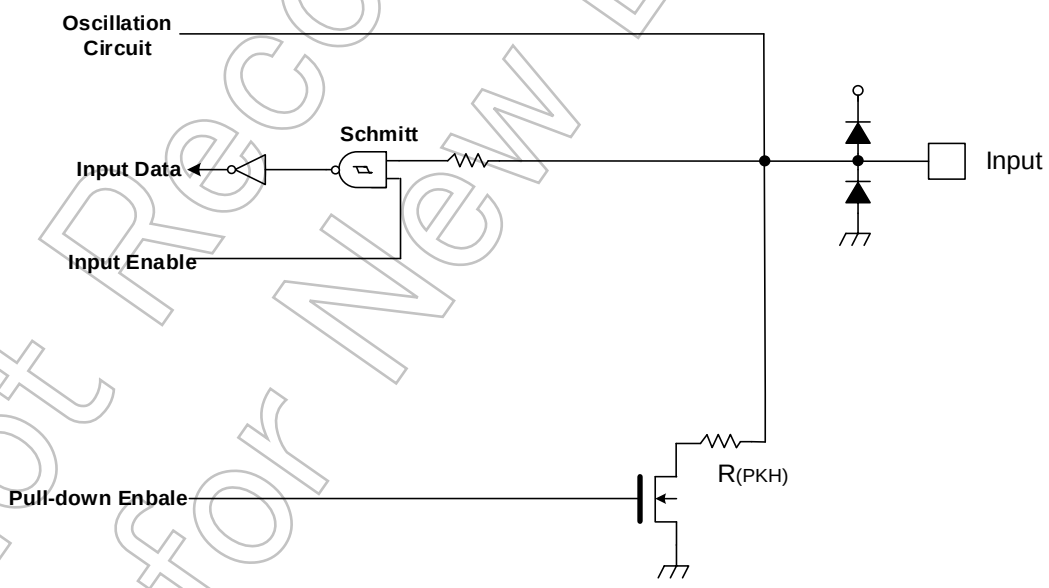
Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

6.1. Port

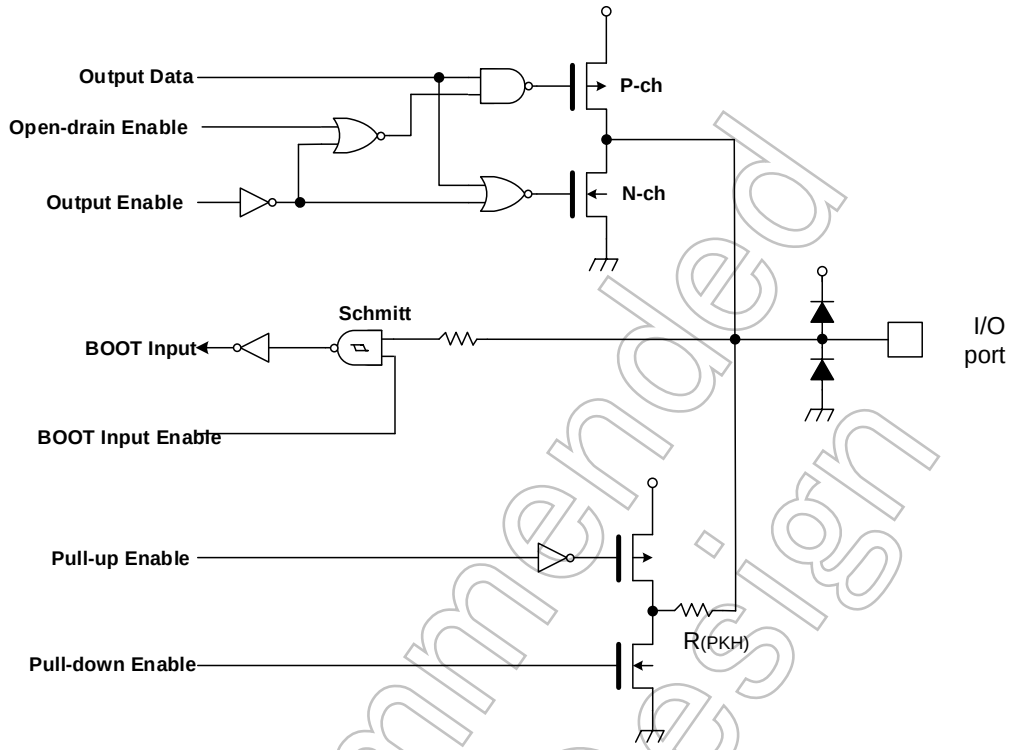
PD0 to PD6 **PE0 to PE5**	**(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt input, Analog input)**



PA2, PF0, PG2 to PG5, PH2, PH3, PJ0 to PJ7, PL0 to PL4	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 
PA0,PA1, PC0 to PC2, PF1,PF2, PG0,PG1, PK0 to PK4	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, External Interrupt Input) 

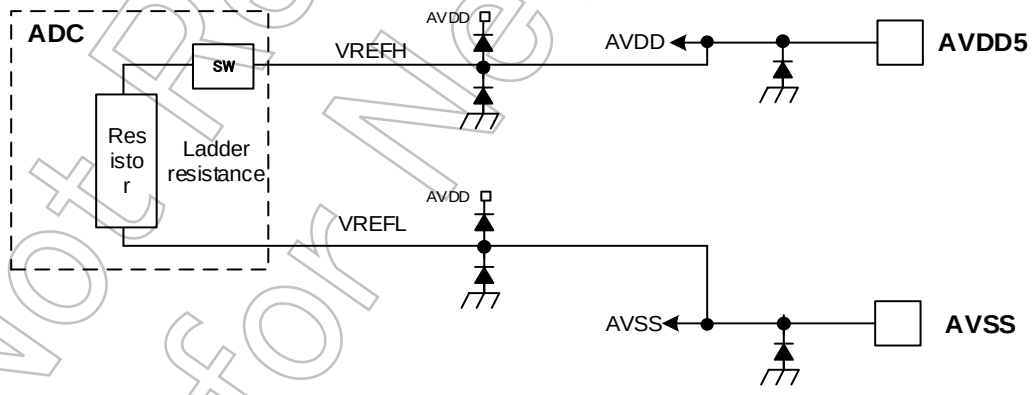
PB0,PB1	(5V tolerant, Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input, External Interrupt Input) 
PH0, PH1	(Programmable Pull-down, Schmitt Input, Oscillation Circuit) 

BOOT_N	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input)



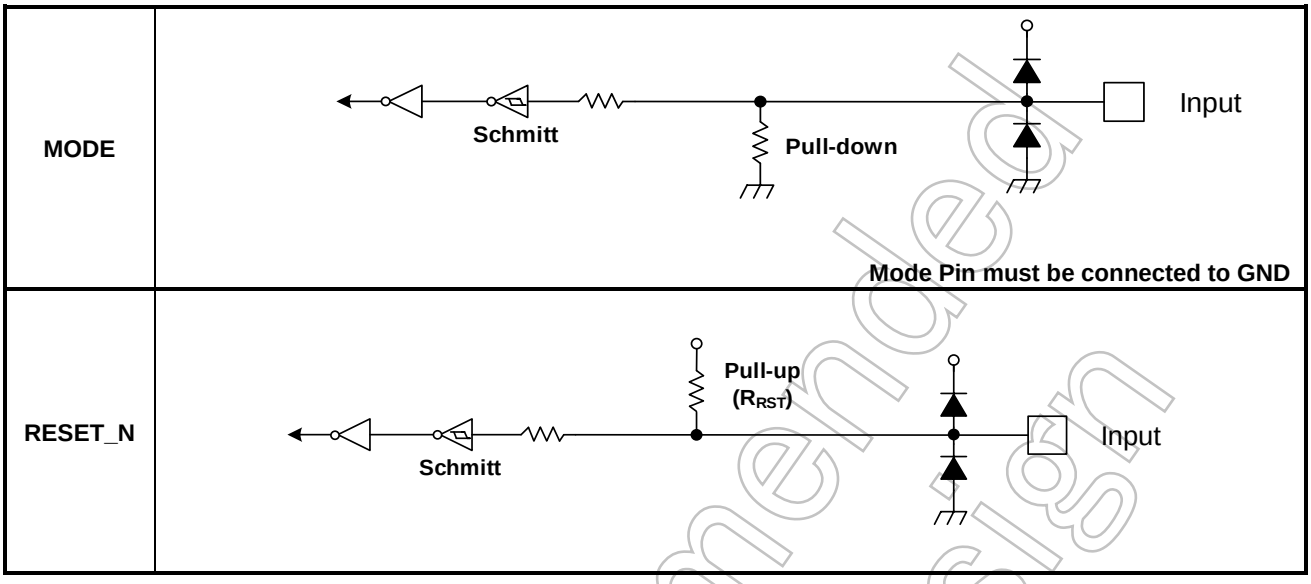
6.2. Analog Power pin

AVDD5 AVSS	

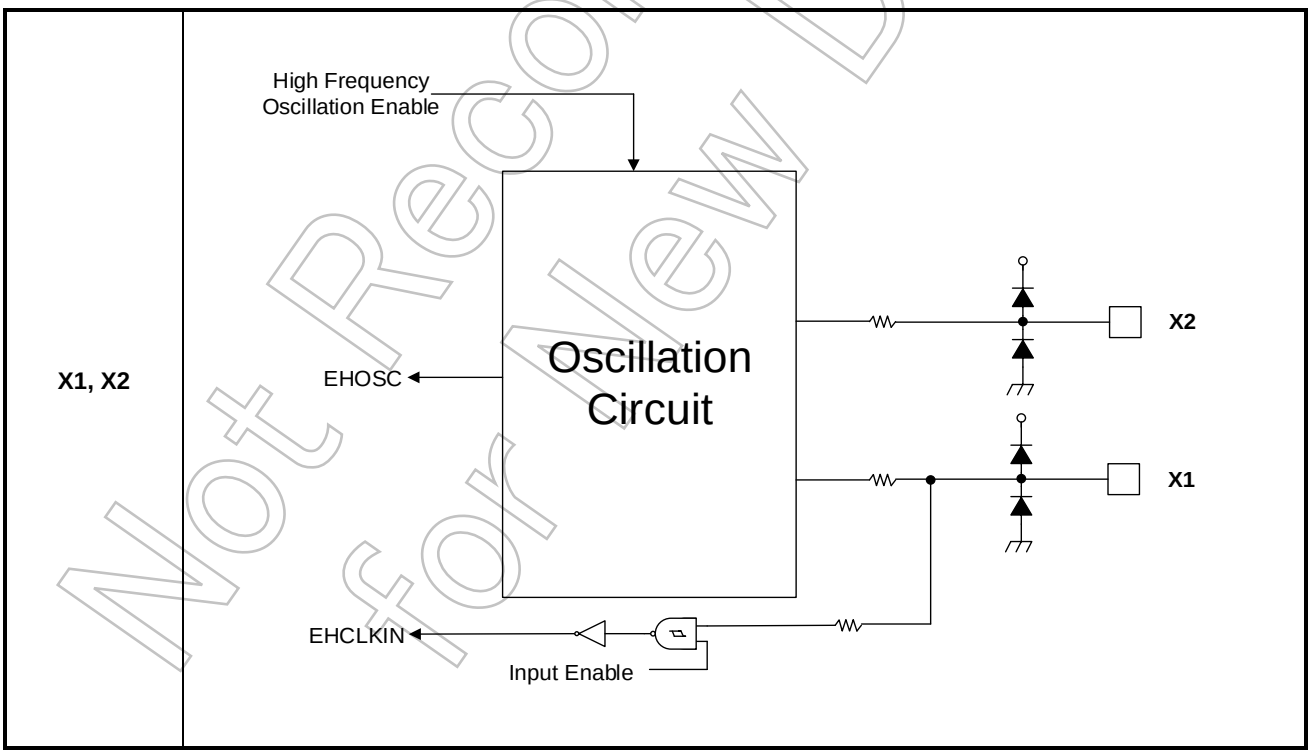


Note: SW: ON/OFF Switch Circuit

6.3. Control Pin



6.4. Clock control



7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5A DVDD5B DVDD5C	-0.3 to 6.0	V
		AVDD5	-0.3 to 6.0	
Capacitor pin voltage for voltage maintenance		REGOUT1	-0.3 to 1.7	V
		REGOUT2	-0.3 to 3.9	
Input voltage	PA0 to PA2, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH0 to PH3, PJ0 to PJ5, PJ7, PK0 to PK4, PL0 to PL4, MODE, RESET_N, BOOT_N	V_{IN1} V_{IN2}	-0.3 to DVDD5+0.3(≤6.0V) (Note1)	V
	PD0 to PD6,PE0 to PE5	V_{IN3}	-0.3 to AVDD5+0.3(≤6.0V)	
	PB0, PB1	V_{IN4}	-0.3 to 6.0	
Low level output current	Per pin PA0 to PA2, PC0 to PC2, PD0 to PD6, PE0 to PE5, PF0 to PF2, PG0 to PG5, PH2 to PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4	I_{OL}	5	mA
	Per pin PB0 to PB1	I_{OL4}	25	
	Total of all pins	ΣI_{OL}	50	
High level output current	Per pin PA0 to PA2, PC0 to PC2, PD0 to PD6, PE0 to PE5, PF0 to PF2, PG0 to PG5, PH2 to PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4, PB0, PB1	I_{OH}	-5	
	Total of all pins	ΣI_{OH}	-50	
Power consumption		PD	500 (Ta= 85°C) 250 (Ta= 105°C)	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operational temperature		T_{OPR}	-40 to 105	°C

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

7.2. DC Electrical Characteristics (1/2)

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V
DVSS = AVSS=0V
Ta=-40 to 105 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B,DVDD5C AVDD5	VDD	f_{OSC} = 6 to 12MHz fsys = 1 to 80MHz	4.5	-	5.5	V
Low level Input voltage	PA0 to PA2,PC0 to PC2, PF0 to PF2,PG0 to PG5, PH0 to PH3,PJ0 to PJ5,PJ7, PK0 to PK4,PL0 to PL4, MODE, RESET_N,BOOT_N	V_{IL1} V_{IL2}	-	-0.3	-	DVDD5×0.25	V
	PD0 to PD6, PE0 to PE5	V_{IL3}	-			AVDD5×0.25	
	PB0, PB1	V_{IL4}	-			DVDD5×0.3	
High level Input voltage	PA0 to PA2, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH0 to PH3, PJ0 to PJ5, PJ7, PK0 to PK4, PL0 to PL4, MODE, RESET_N, BOOT_N	V_{IH1} V_{IH2}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PD0 to PD6,PE0 to PE5	V_{IH3}	-	AVDD5×0.75		AVDD5+0.3	
	PB0, PB1	V_{IH4}	-	DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PA0 to PA2, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH2, PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4	V_{OL1} V_{OL2}	DVDD5=4.5V I_{OL}=1.6mA	-	-	0.4	V
	PD0 to PD6, PE0 to PE5	V_{OL3}	AVDD5=4.5V I_{OL}=1.6mA	-	-	0.4	
	PB0, PB1	V_{OL4}	DVDD5=4.5V I_{OL}=8mA	-	-	1.0	
High level output voltage	PA0 to PA2,PB0, PB1, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH2, PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4	V_{OH1} V_{OH2}	DVDD5=4.5V I_{OH} = -1.6mA	DVDD5-0.4	-	-	V
	PD0 to PD6, PE0 to PE5	V_{OH3}	AVDD5=4.5V I_{OH} = -1.6mA	AVDD5-0.4	-	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Output leak current		I_{LO}	0.2 ≤ VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		V_{TH}	DVDD5=AVDD5=5.0V	-	1.0	-	V
Reset pull-up resistor		R_{RST}	-	25	30	100	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	25	30	100	kΩ
			Pull-down	25	50	100	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin except PB0, PB1	I_{OL}	DVDD5=AVDD5=5.0V	-	-	2 (Note4)	mA
	Per pin PB0, PB1	I_{OL4}	DVDD5=5.0V	-	-	12 (Note4)	
	Total of PH2,PH3,PA0 to PA2, PB0, PB1,PC0 to PC2, PJ0 to PJ7	ΣI_{OL1}	DVDD5=5.0V	-	-	35 (Note5)	
	Total of PF0 to PF2, PG0 to PG5, PK0 to PK4, PL0 to PL4	ΣI_{OL2}	DVDD5=5.0V	-	-	35 (Note5)	
	Total of PD0 to PD6, PE0 to PE5	ΣI_{OL3}	AVDD5=5.0V	-	-	20 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=AVDD5=5.0V	-2 (Note4)	-	-	mA
	Total of PH2,PH3,PA0 to PA2, PB0, PB1, PC0 to PC2, PJ0 to PJ7	ΣI_{OH1}	DVDD5=5.0V	-35 (Note5)	-	-	
	Total of PF0 to PF2, PG0 to PG5, PK0 to PK4, PL0 to PL4	ΣI_{OH2}	DVDD5=5.0V	-35 (Note5)	-	-	
	Total of PD0 to PD6, PE0 to PE5	ΣI_{OH3}	AVDD5=5.0V	-20 (Note5)	-	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage toDVDD5 and AVDD5.

Note4: The sum of the terminal currents in each group should not exceed the total current of each group.

Note5: The sum of each group current should not exceed the absolute maximum rating.

2.7V ≤DVDD5=AVDD5< 4.5V
DVSS=AVSS=0V
Ta=-40 to 105 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B,DVDD5C AVDD5	VDD	f_{OSC} = 6 to 12MHz fsys = 1 to 80MHz	2.7	-	4.5	V
Low level Input voltage	PA0 to PA2,PC0 to PC2, PF0 to PF2,PG0 to PG5, PH0 to PH3,PJ0 to PJ5,PJ7, PK0 to PK4,PL0 to PL4, MODE, RESET_N,BOOT_N	V_{IL1} V_{IL2}	-	-0.3	-	DVDD5×0.25	V
	PD0 to PD6, PE0 to PE5	V_{IL3}	-			AVDD5×0.25	
	PB0, PB1	V_{IL4}	-			DVDD5×0.3	
High level Input voltage	PA0 to PA2, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH0 to PH3, PJ0 to PJ5, PJ7, PK0 to PK4, PL0 to PL4, MODE, RESET_N, BOOT_N	V_{IH1} V_{IH2}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PD0 to PD6,PE0 to PE5	V_{IH3}	-	AVDD5×0.75		AVDD5+0.3	
	PB0, PB1	V_{IH4}	-	DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PA0 to PA2,PC0 to PC2, PF0 to PF2,PG0 to PG5, PH2, PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4	V_{OL1} V_{OL2}	DVDD5=2.7V I_{OL}=0.8mA	-	-	0.4	V
	PD0 to PD6, PE0 to PE5	V_{OL3}	AVDD5=2.7V I_{OL}=0.8mA	-	-	0.4	
	PB0, PB1	V_{OL4}	DVDD5=2.7V I_{OL}=4mA	-	-	1.0	
High level output voltage	PA0 to PA2,PB0, PB1, PC0 to PC2, PF0 to PF2, PG0 to PG5, PH2, PH3, PJ0 to PJ7, PK0 to PK4, PL0 to PL4	V_{OH1} V_{OH2}	DVDD5=2.7V I_{OH}= -0.8mA	DVDD5-0.4	-	-	V
	PD0 to PD6, PE0 to PE5	V_{OH3}	AVDD5=2.7V I_{OH}= -0.8mA	AVDD5-0.4	-	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 3.0V, unless otherwise noted.

Note3: Apply same voltage toDVDD5 and AVDD5.

2.7V ≤DVDD5=AVDD5< 4.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Output leak current		I_{LO}	0.2 ≤ VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		V_{TH}	DVDD5=AVDD5=3.0V	-	0.5	-	V
Reset pull-up resistor		R_{RST}	-	25	100	200	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	25	100	200	kΩ
			Pull-down	25	100	200	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin except PB0, PB1	I_{OL}	DVDD5=AVDD5=3.0V	-	-	1 (Note4)	mA
	Per pin PB0, PB1	I_{OL4}	DVDD5=3.0V	-		6 (Note4)	
	Total of PJ2,PH3,PA0 to PA2, PB0, PB1,PC0 to PC2, PJ0 to PJ7	ΣI_{OL1}	DVDD5=3.0V	-	-	18 (Note5)	
	Total of PF0 to PF2, PG0 to PG5, PK0 to PK4, PL0 to PL4	ΣI_{OL2}	DVDD5=3.0V	-	-	18 (Note5)	
	Total of PD0 to PD6, PE0 to PE5	ΣI_{OL3}	AVDD5=3.0V	-	-	10 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=AVDD5=3.0V	-1 (Note4)	-	-	mA
	Total of PH2,PH3,PA0 to PA2, PB0, PB1,PC0 to PC2, PJ0 to PJ7	ΣI_{OH1}	DVDD5=3.0V	-18 (Note5)	-	-	
	Total of PF0 to PF2,PG0 to PG5, PK0 to PK4, PL0 to PL4	ΣI_{OH2}	DVDD5=3.0V	-18 (Note5)	-	-	
	Total of PD0 to PD6, PE0 to PE5	ΣI_{OH3}	AVDD5=3.0V	-10 (Note5)	-	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 3.0V, unless otherwise noted.

Note3: Apply same voltage toDVDD5 and AVDD5.

Note4: The sum of the terminal currents in each group should not exceed the total current of each group.

Note5: The sum of each group current should not exceed the absolute maximum rating.

7.3. DC Electrical Characteristics (2/2)

Ta= -40 to 105°C

Parameter	Symbol	Conditions			Min	Typ.	Max	Unit
		Supply voltage	High-speed clock	Operating condition				
NORMAL	I_{DD}	DVDD5= AVDD5= 5.5V	Refer to the table 7.2 and 7.3 for detail		-	25.3	45.0	mA
IDLE			Oscillation	Refer to the table 7.2 and 7.3 for detail	-	2.7	16	
STOP1			Stop	Refer to the table 7.2 and 7.3 for detail	-	0.16	13	mA

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.
Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.
Note3: Apply same voltage to DVDD5 and AVDD5.
Note4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1
Pin setting	DVDD5= AVDD5=	5.0V(Typ.), 5.5V(max)		
	X1, X2	Oscillator connected (10MHz)		
	Input pins	Fixed		
	Output pins	Open		
Operation condition (Oscillation Circuit)	System clock (fsys)	80MHz		Stop
	External High-speed frequency oscillator (EHOSC)	Oscillation		Stop
	Internal High-speed frequency oscillator (IHOSC1)	Stop		
	PLL	Run(8 times)		Stop

Table 7.3 IDD measurement condition (CPU, Peripheral)

Peripheral circuit	unit number	NORMAL	IDLE	STOP1
CPU	1	Run (DhrystoneVer.2.1)	Stop	
DMAC	1	(Request from UARTch0 TX destination: RAM)	Stop	
ADC	1	Run (0.5µs, Repeated conversion)	Stop	
OPAMP	3	All ch Run	Stop	
RAMP	1	Run	Stop	
T32A	6	All ch: Run	Stop	
A-PMD	2	All ch Run	Stop	
A-ENC	1	Run	Stop	
A-VE+	1	Run	Stop	
SIWDT	1	Run	Stop	
UART	4	2ch: Transmission(5Mbps)	Stop	
I^2C	1	Stop		
TSPI	4	2ch: Transmission(20MHz)	Stop	
CRC	1	Stop		
LVD	1	Stop		
OFD	1	Stop		
Debug	1	Stop		
NBDIF	1	Stop		
Input/Output Port	-	Run	Stop	

fsys=80MHz
Ta= -40 to 105°C

Item	Symbol	Condition	Min	Typ.	Max	Unit
Power consumption (ADC, OPAMP run)	I_{AVDD}	AVDD5=5.0V, AVSS=0V	-	11.2	17.3	mA

7.4. 12-bit AD Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	Reference is supplied from AVDD5/VREFH pin	AVDD5-0.3	-	AVDD5+0.3	V
		Reference is supplied from AINA15/VREFH pin(Note5)	4.5	-	AVDD5	
Analog input voltage	VAIN	-	AVSS(VREFL)	-	VREFH	V
Integral nonlinear error (INL)	-	4.5V ≤ AVDD5 ≤ 5.5V 4.5V ≤ VREFH ≤ 5.5V AVSS=(VREFL)=0V 0 ≤ AVDD5-VREFH ≤ 0.5V VREFH(=AINA15)(Note5) AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 0.5μs	-14	-	10	LSB
Differential nonlinear error (DNL)			-1	-	15	
Zero-scale error			-6	-	6	
Full-scale error			-6	-	6	
Total errors			-15.5	-	8	
Integral nonlinear error (INL)	-	4.5V ≤ AVDD5 ≤ 5.5V 4.5V ≤ VREFH ≤ 5.5V AVSS=(VREFL)=0 0 ≤ AVDD5-VREFH ≤ 0.5V VREFH(=AINA15)(Note5) AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 0.62μs	-7	-	7	LSB
Differential nonlinear error (DNL)			-5	-	5	
Zero-scale error			-6	-	6	
Full-scale error			-6	-	6	
Total errors			-7	-	7	
Integral nonlinear error (INL)	-	4.5V≤AVDD5=VREFH≤5.5V AVSS=(VREFL)=0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 0.85μs	-5	-	5	LSB
Differential nonlinear error (DNL)			-5	-	5	
Zero-scale error			-3	-	3	
Full-scale error			-3	-	3	
Total errors			-6	-	6	
Integral nonlinear error (INL)	-	2.7V≤AVDD5=VREFH<4.5V AVSS=(VREFL)=0V 0 ≤ AVDD5-VREFH ≤ 0.5V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 2.0μs	-4	-	4	LSB
Differential nonlinear error (DNL)			-3	-	3	
Zero-scale error			-5	-	5	
Full-scale error			-5	-	5	
Total errors			-8	-	8	
Stable time	t_{sta}	After ***[ADAMOD0]***<DACON> =1 is set.	3	-	-	μs
Conversion time	t_{conv}	4.5V ≤ AVDD5 ≤ 5.5V SCLK=120MHz	0.5	-	0.85	
		2.7V ≤ AVDD5 < 4.5V SCLK=30MHz	-	2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 4096 [V]

Note4: The characteristic when single unit AD convert operates only.

Note5: Set [ADAMOD0]<REFBSEL> to 0.

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter	Conditions	Min	Typ.	Max	Unit
Reference power	ch18 select	1.1	-	1.3	V

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.5. Operational amplifier Characteristics

DVDD5=AVDD5= 4.5V to 5.5V
DVSS=AVSS= 0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Gain (magnification) (Note2)	VGAIN	-	2.0	-	15	Mag
Amp input voltage range (Common mode)	VAMPINP VAMPINN	-	AVSS-0.3	-	(AVDD5×0.99) /VGAIN	V
Amp input voltage range (Differential)	VAMPINP VAMPINN	Min GAIN = 2.0	0	-	AVDD5 /(Min Gain)	
Amp output voltage	VVOLT	-	AVDD5 x 0.01	-	AVDD5 x 0.99	
Differential step offset voltage	VOFF	-	-5	-	5	mV
Gain error range	-	-	-3	-	3	%
Slew rate	Vthr	10pF	6	10	-	V/μs
AMPEN→Output stable time	t_{sta1}	Time meets the following condition. Upper limit: +5mV Lower limit: -5mV CL=10pF	-	-	2	μs

Note1: The characteristic when the amplifier unit operates only.

Note2: Gain can selected 2.5,3,3.5,4,4.5,6,7,8,10,and 12

Note3: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note4: Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

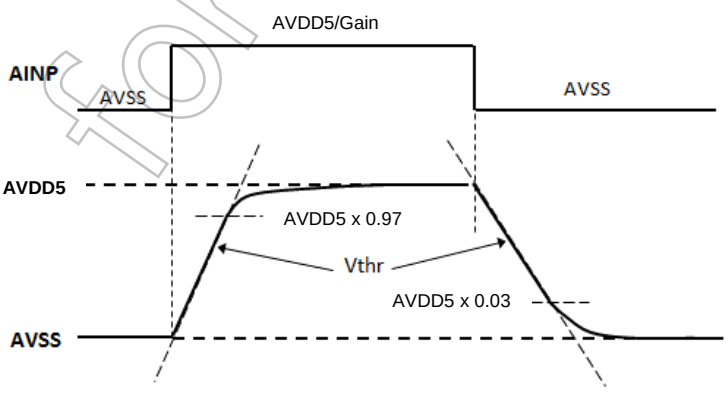


Figure 7.1 Slew rate

7.6. Characteristics of Internal processing at RESET

DVSSA=DVSSB=DVSSC=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Initialized time	t_{IINIT}	Power On	-	-	1.85	ms
Internal processing time for Reset	t_{IRST}	-	0.16	-	0.2	
Waiting time till CPU running	t_{CPUWT}	Cold Reset	12	-	15	µs
		Warm Reset	70	-	90	
Power-on rising gradient	V_{PON}	-	0.01	-	100	mV/µs

7.7. Characteristics of Power on Reset

DVSSA=DVSSB=DVSSC=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power On	2.25	2.4	2.55	V
	V_{PDET}	Power Down	2.2	2.35	2.5	
Detection pulse width	t_{PDET}	-	200	-	-	µs

7.8. Characteristics of Voltage Detection Circuit

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power On	2.55	2.65	2.75	V
		Power Down	2.5	2.6	2.7	
	V_{LVL1}	Power On	2.65	2.75	2.85	V
		Power Down	2.6	2.7	2.8	
	V_{LVL2}	Power On	2.75	2.85	2.95	V
		Power Down	2.7	2.8	2.9	
	V_{LVL3}	Power On	2.85	2.95	3.05	V
		Power Down	2.8	2.9	3.0	
	V_{LVL4}	Power On	3.95	4.05	4.15	V
		Power Down	3.9	4.0	4.1	
	V_{LVL5}	Power On	4.15	4.25	4.35	V
		Power Down	4.1	4.2	4.3	
	V_{LVL6}	Power On	4.35	4.45	4.55	V
		Power Down	4.3	4.4	4.5	
	V_{LVL7}	Power On	4.55	4.65	4.75	V
		Power Down	4.5	4.6	4.7	
Detection response time	t_{VDDT1}	Power Down	-	50	200	µs
Release response time	t_{VDDT2}	Power On	-	250	-	
Setup time	t_{LVDEN}	-	-	-	100	
Detection Minimum pulse width	t_{LVDPW}	-	200	-	-	

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9. AC Electrical Characteristics

7.9.1. Serial Peripheral Interface (TSPI)

7.9.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

(1) SIO Master mode

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 13	-	12	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 13	-	12	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - 2×T (Note1)	-	10	-	
		35 - T (Note2)				
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2×T - 5 (Note1)	-	20	-	
		T - 5 (Note2)				
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note1: When ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note2: When [TSPIxCR2]<RXDLY>=0, fsys=40MHz

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 16	-	9	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 16	-	9	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45 - 2×T (Note1)	-	20	-	
		45 - T (Note2)	-			
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2×T - 5 (Note1)	-	20	-	
		T - 5 (Note2)				
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note1: When ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note2: When [TSPIxCR2]<RXDLY>=0, fsys=40MHz

(2) SIO Slave mode

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	36		36	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Calculation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	55	-	55	

(1) 2nd clock edge sampling (Master)

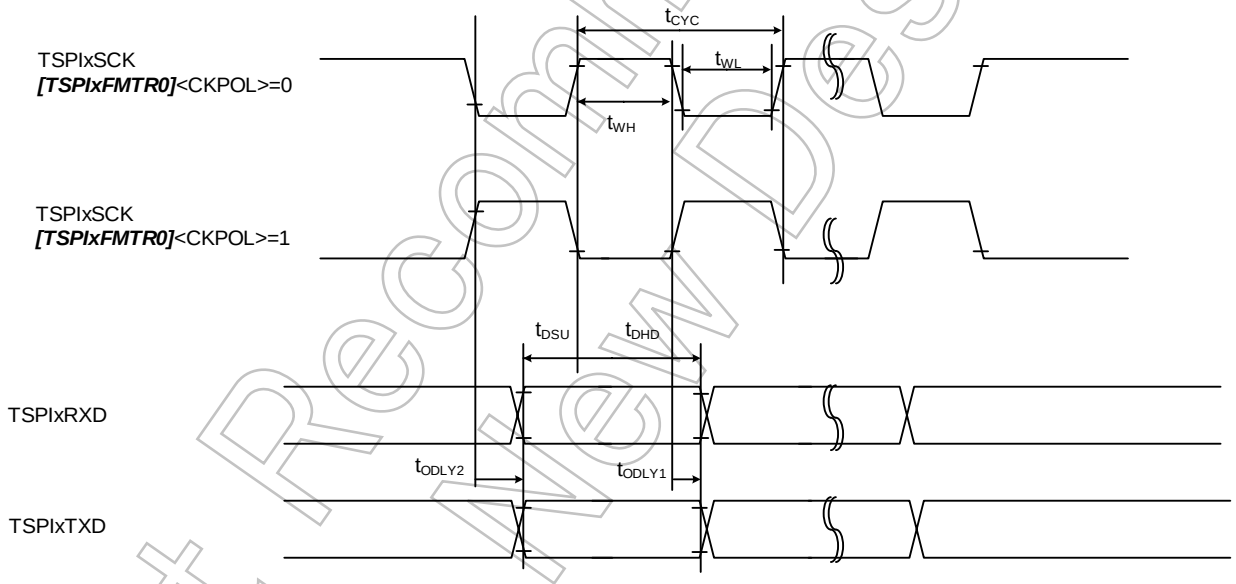


Figure 7.2 2nd clock edge sampling (Master)

(2) 2nd clock edge sampling (slave)

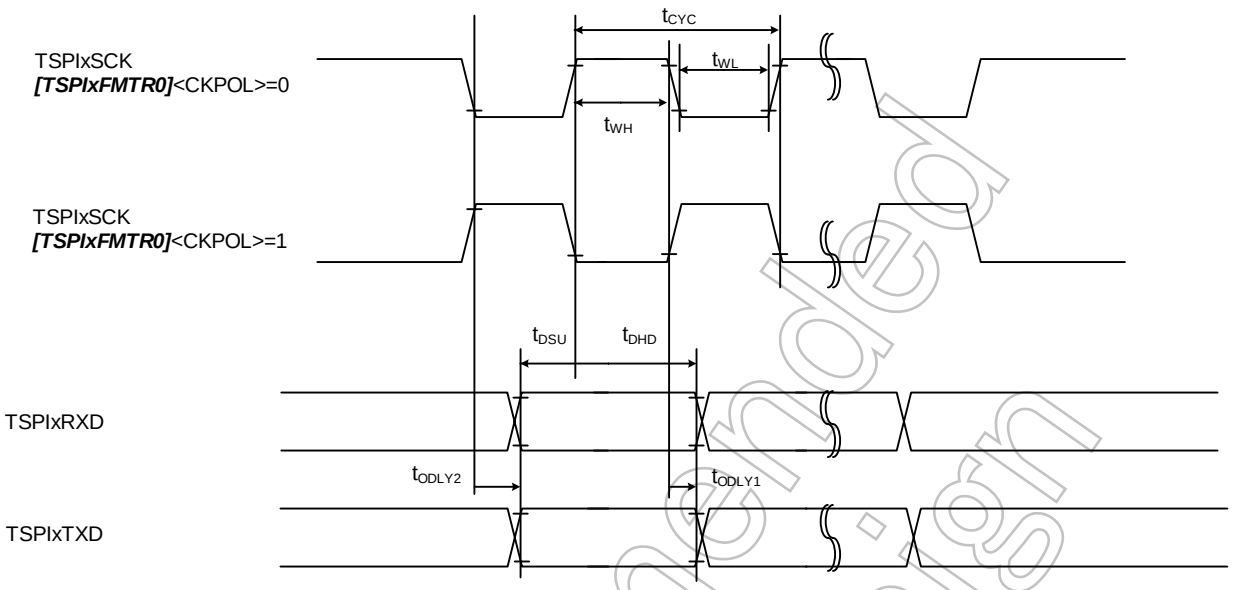


Figure 7.3 2nd clock edge sampling (Slave)

7.9.2. I²C Interface (I²C)

7.9.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.2.2. AC Electrical Characteristics

"T" indicates a clock cycle of the I²C. "n" indicates a frequency of SCL output clock specified with ***[I2CxCR]***<SCK>. "p" indicates a prescaler division ratio specified with ***[I2CxPRS]***<PRSCK>.

Parameter		Symbol	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
SCL clock frequency		f_{SCL}	0	100	0	400	kHz
Start condition hold time		$t_{HD, STA}$	4.0	-	0.6	-	µs
SCL clock Low width (Input) (Note1)		t_{LOW}	4.7	-	1.3	-	
SCL clock High width (Input) (Note2)		t_{HIGH}	4.0	-	0.6	-	
Re-start condition setup time	<SREN>=0	$t_{SU, STA}$	4.7 (Note5)	-	0.6 (Note5)	-	
	<SREN>=1	$t_{SU, STA}$	4.7 (Note5)	-	0.6	-	
Data hold time (Input) (Note3, 4)		$t_{HD, DAT}$	0	-	0	-	
Data setup time		$t_{SU, DAT}$	250	-	100	-	ns
Stop condition setup time		$t_{SU, STO}$	4.0	-	0.6	-	µs
Bus free time between stop condition and start condition (Note5)		t_{BUF}	4.7	-	1.3	-	
pulse width of spikes that must be suppressed by the input filter		t_{SP}	-	-	0	50	ns
rise time of both SDA and SCL signals		t_r	-	1000	20	300	
fall time of both SDA and SCL signals		t_f	-	300	20 × (V_{DD}/5.5V)	300	

Note1: SCL clock low level width (output): $p \times (2^{n+1}+10)/T$ (***[I2CxOP]***<NFSEL>=0)

Note2: SCL clock high level width (output): $p \times (2^{n+1}+6)/T$ (***[I2CxOP]***<NFSEL>=0)
On I²C bus standard, the maximum speed of standard mode/fast mode is 100kHz/400 kHz respectively. Note that an internal SCL clock frequency is determined by the fsys and the calculation of Note1 and Note2 above-mentioned.

Note3: The data hold time (output) is equal to four cycles of the prescaler clock (Tprsck) started from the internal SCL.

Note4: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note5: To keep the time by software.

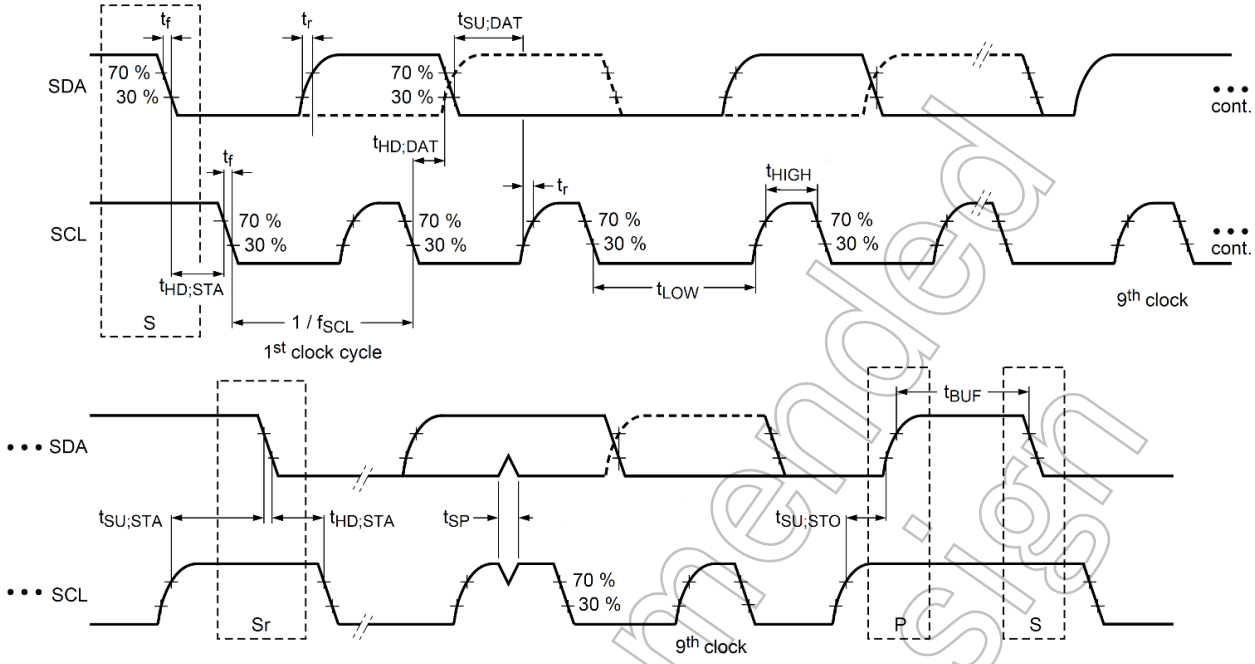


Figure 7.4 AC timing of I²C

7.9.3. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.9.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.3.2. AC Electrical Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0 clock. This cycle is depending on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Calculation		ΦT0=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	45	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	45	-	

(2) At the pulse count

Parameter	Symbol	Calculation		ΦT0=80 MHz NF=4		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1) × T +20	-	82.5	-	
Input hold	t_{ABH}	(NF+1) × T +20	-	82.5	-	

NF Value depends on the ***[T32AxPLSCR]***<NF[1:0]> setting as follows.

[T32AxPLSCR]<NF[1:0]>	NF Value of Formula
00	0
01	2
10	4
11	8

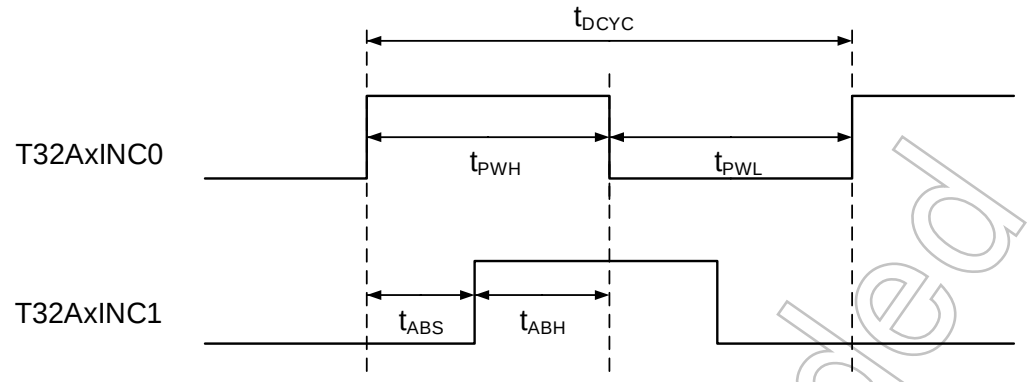


Figure 7.5 Count Pulse input

7.9.4. External Interrupt

7.9.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.4.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL,IDLE mode

Parameter	Symbol	Calculation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	112.5	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	112.5	-	

(2) STOP1 mode

Parameter	Symbol	Calculation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	125	-	125	-	ns
High level pulse width	t_{INTCH2}	125	-	125	-	

7.9.5. Trigger Input (TRGINx)

7.9.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

Parameter	Symbol	Calculation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{ADL}	2T + 20	-	45	-	ns
High level pulse width	t_{ADH}	2T + 20	-	45	-	

7.9.6. Debug Communication

7.9.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.8 ×DVDD5, Low = 0.2×DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.6.2. SWD Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from on the rising edge of CLK	t_{d1}	4	-	
Output data valid from on the rising edge of CLK	t_{d2}	-	31	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from on the rising edge of CLK	t_{d1}	4	-	
Output data valid from on the rising edge of CLK	t_{d2}	-	45	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

7.9.6.3. JTAG Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	83.3	-	ns
Output data hold from on the falling edge of CLK	t_{d3}	4	-	
Output data valid from on the falling edge of CLK	t_{d4}	-	33	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	83.3	-	ns
Output data hold from on the falling edge of CLK	t_{d3}	4	-	
Output data valid from on the falling edge of CLK	t_{d4}	-	45	
Rising edge of CLK from input data valid	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

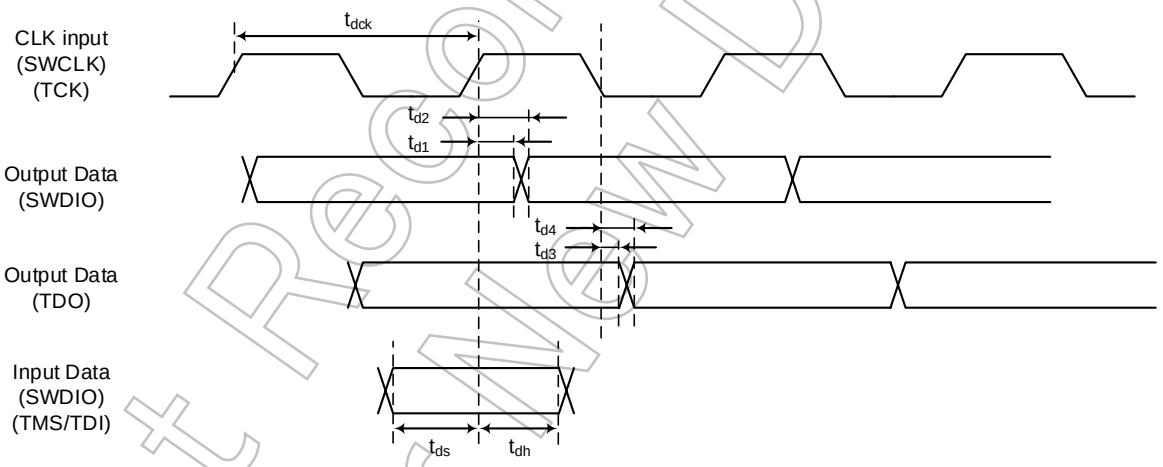


Figure 7.6 JTAG/SWD waveform

7.9.6.4. ETM Trace

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	50	-	ns
Data valid from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold from on the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid from on the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold from on the falling edge of TRACECLK	t_{holdf}	1	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	100	-	ns
Data valid from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold from on the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid from on the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold from on the falling edge of TRACECLK	t_{holdf}	1	-	

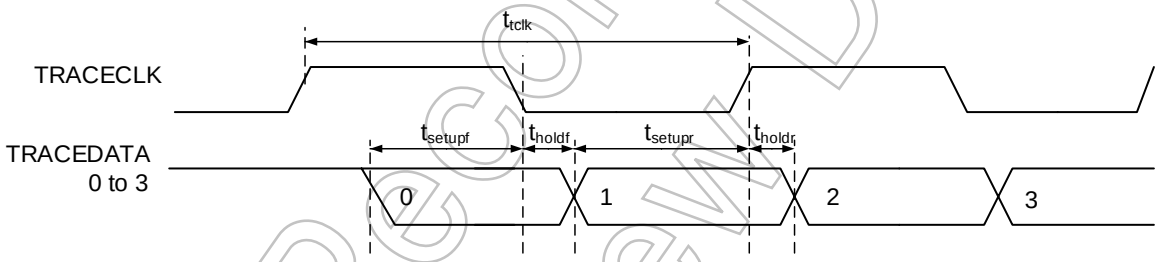


Figure 7.7 Trace signal waveform

7.9.6.5. NBD Interface

Parameter	Symbol	Min	Max	Unit
NBDCLK cycle	t_{NDCYC}	80	-	ns
NBDCLK low level pulse width	t_{NDL}	35	-	
NBD DATA output delay time	t_{NDD}	-	t_{NDCYC} - 20	
NBD DATA output hold time	t_{NDHD}	5	-	
NBD DATA setup time	t_{NDS}	20	-	
NBD DATA hold time	t_{NDH}	5	-	
NBDSYNC setup time	t_{NDSYS}	20	-	
NBDSYNC output hold time	t_{NDSYH}	5	-	

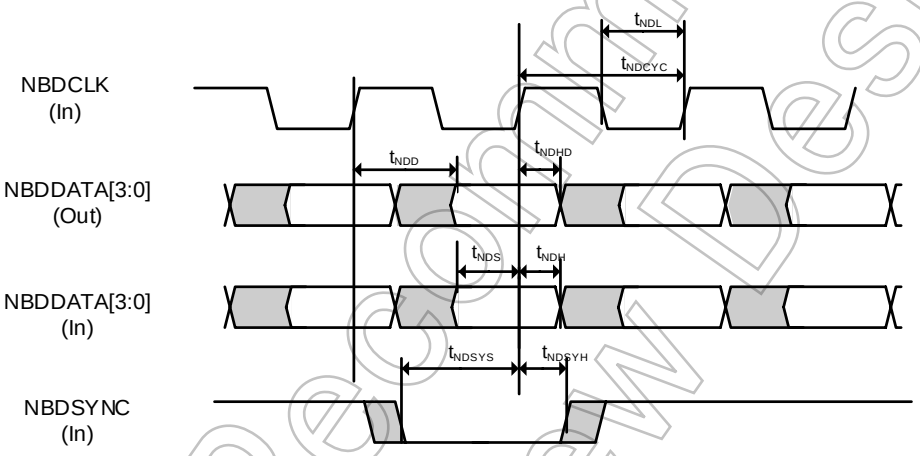


Figure 7.8 AC timing of NBDIF

7.9.7. SCOUT Pin

7.9.7.1. AC Measurement Conditions

The AC characteristics are the result of the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.7.2. AC Electrical Characteristics

"T" in the table indicates the cycle of the SCOUT output waveform.

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Calculation		SCOUT = 20MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{SCL}	0.5T- 10	-	11	-	ns
High level pulse width	t_{SCH}	0.5T- 10	-	11	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Calculation		SCOUT = 20MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{SCL}	0.5T- 12	-	4	-	ns
High level pulse width	t_{SCH}	0.5T- 12	-	4	-	

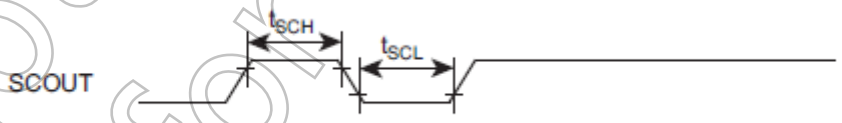


Figure 7.9 SCOUT wave output

7.9.8. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	DVDD5 = 2.7 to 5.5V Ta = -40 to 105°C	15	30	60	ns

7.9.9. External Clock Input

7.9.9.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.9.9.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	12	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

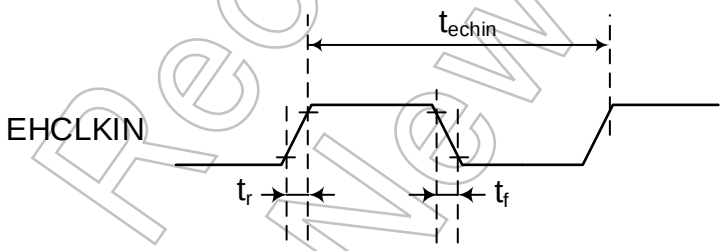


Figure 7.10 External clock input waveform

7.10. Flash Memory Characteristics

7.10.1. Code Flash

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	DVDD5=2.7V to 5.5V Ta=-40 to 105°C	-	-	10,000	cycles
Programming time	Word Program time	-	29.5	-	µs
Erase time	Page Erase time	1.1	-	4.3	ms
	Block Erase time	8.6	-	34	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: No block with effective protection.

7.10.2. Chip Erase

DVDD5= 2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Erasing of Code Flash, Protect Bits(Code), User Information Area and Security Bits	12.5	-	22.1	ms

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: When Chip Erase command executes, no block with effective protection.

7.11. Regulator

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor	DVDD5=2.7V to 5.5V Ta=-40 to 105°C	-	4.7	-	µF
Capacitance of REGOUT2 capacitor		-	4.7	-	

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

7.12. Oscillation Circuit

7.12.1. Internal Oscillation

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	Factory out, IC data (Note2)	-	10	-	MHz
	f_{IHOSC2}		-	10	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Not included the influence depend on the variations after Factory shipping. Please execute oscillator adjustment by the trimming register, if trimming of IHOSC1 is required. However, IHOSC2 cannot execute trimming.

7.12.2. External Oscillator

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}	-	6	-	12	MHz

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

7.12.3. Oscillation Circuit

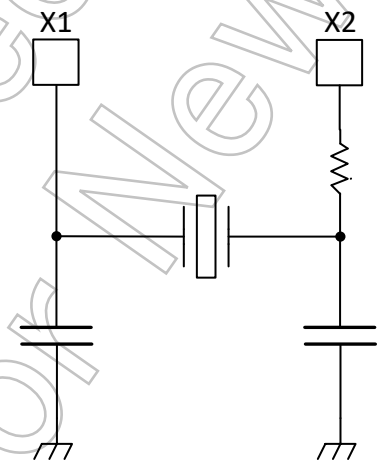


Figure 7.11 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

7.12.4. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.
Please refer to the company's website for details.

7.12.5. Crystal Oscillator

This product has been evaluated by the crystal oscillator by KYOCERA Corporation.
Please refer to the company's website for details.

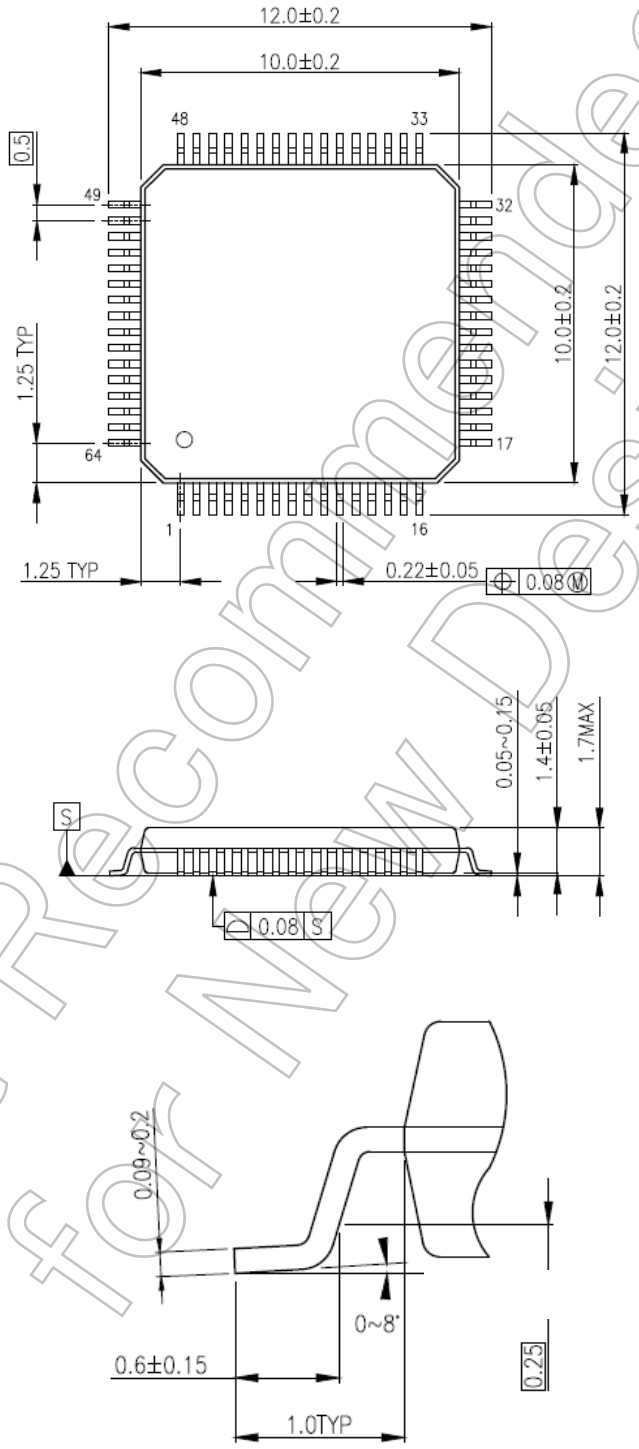
7.12.6. Precautions for designing printed circuit board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

8. Package Dimensions

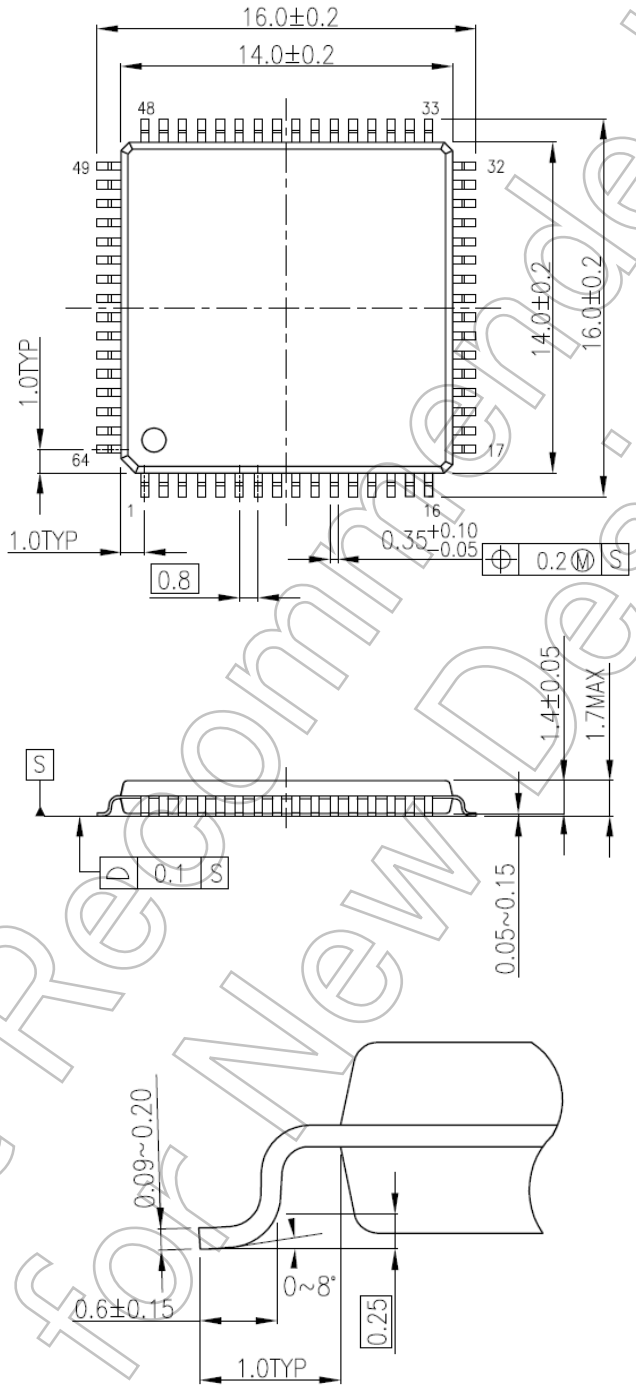
8.1. P-LQFP64-1010-0.50-003

Unit: mm



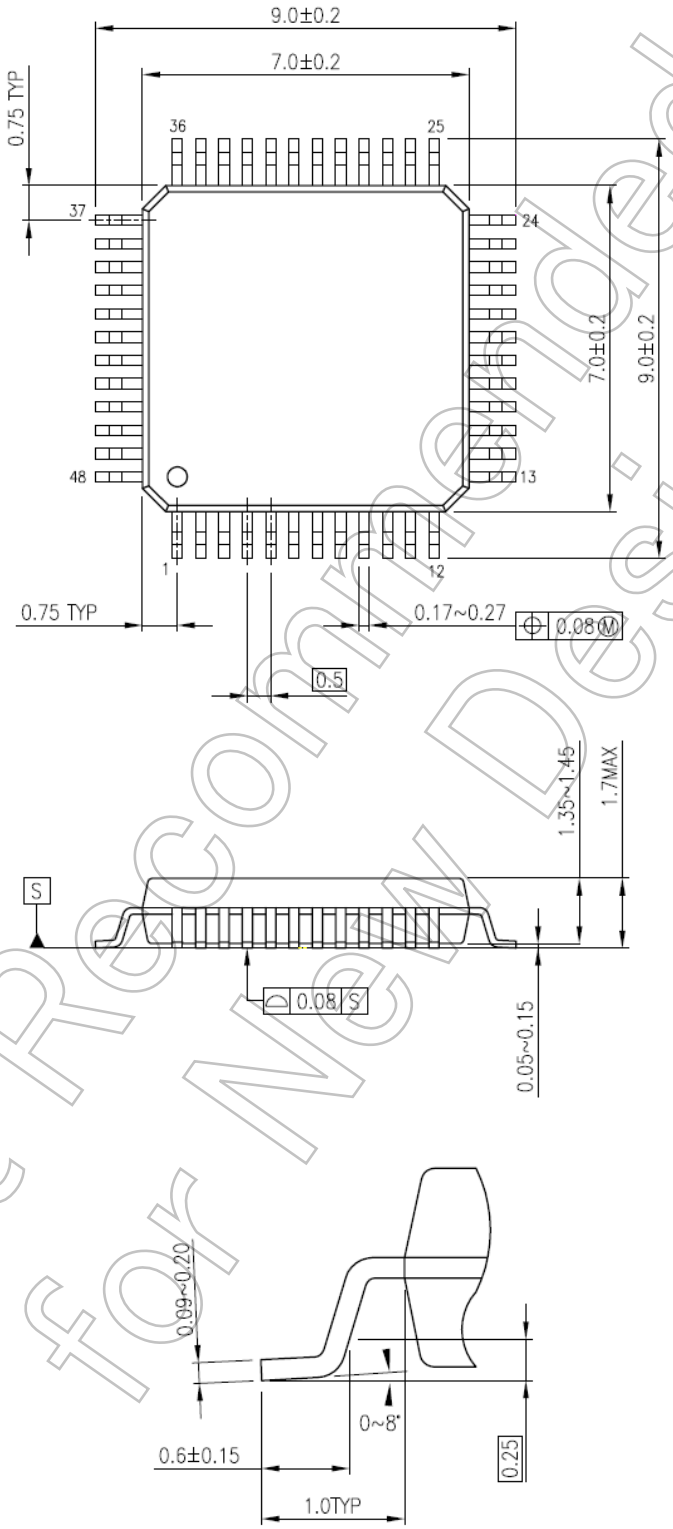
8.2. P-LQFP64-1414-0.80-002

Unit: mm



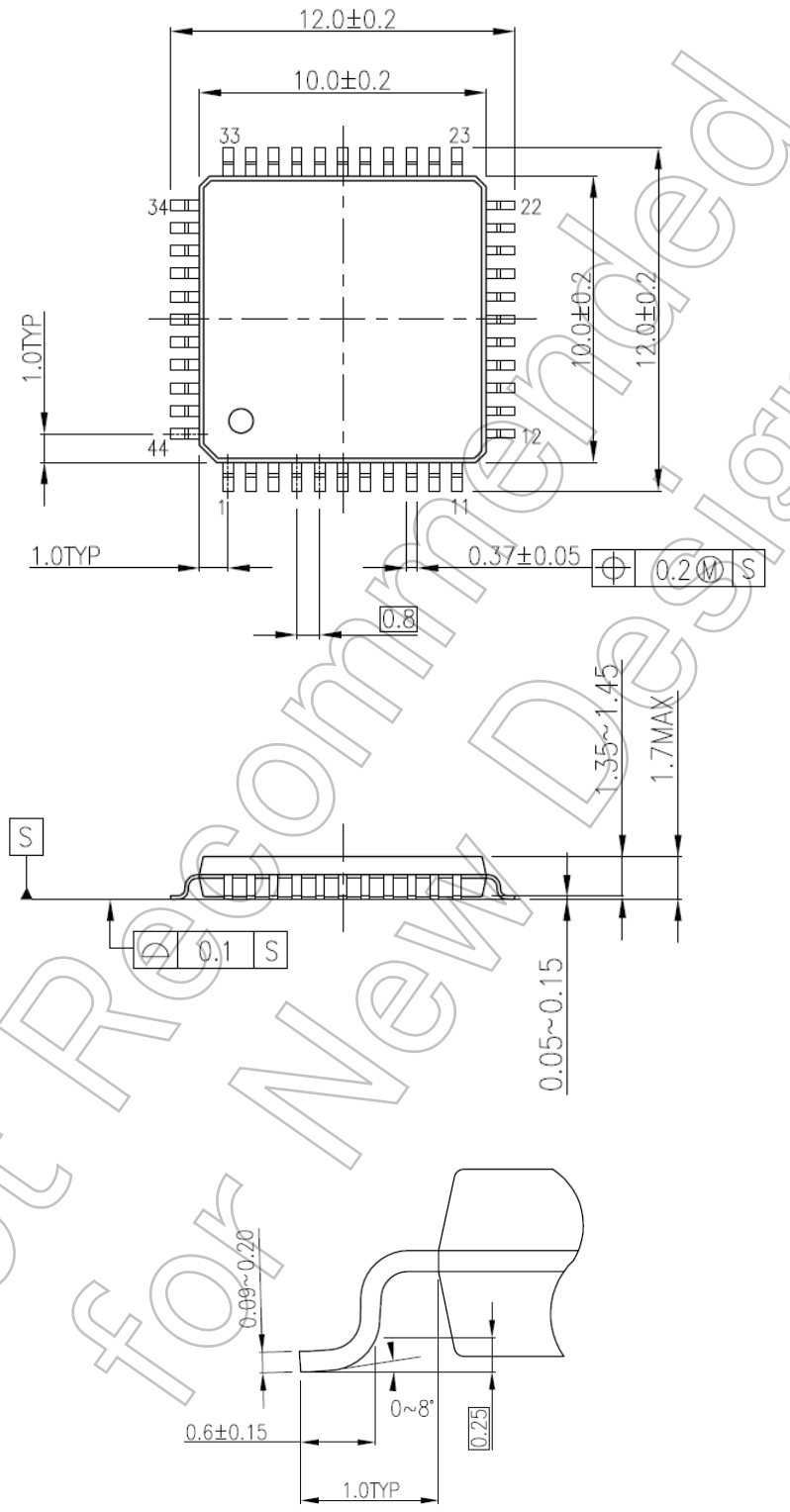
8.3. P-LQFP48-0707-0.50-002

Unit: mm



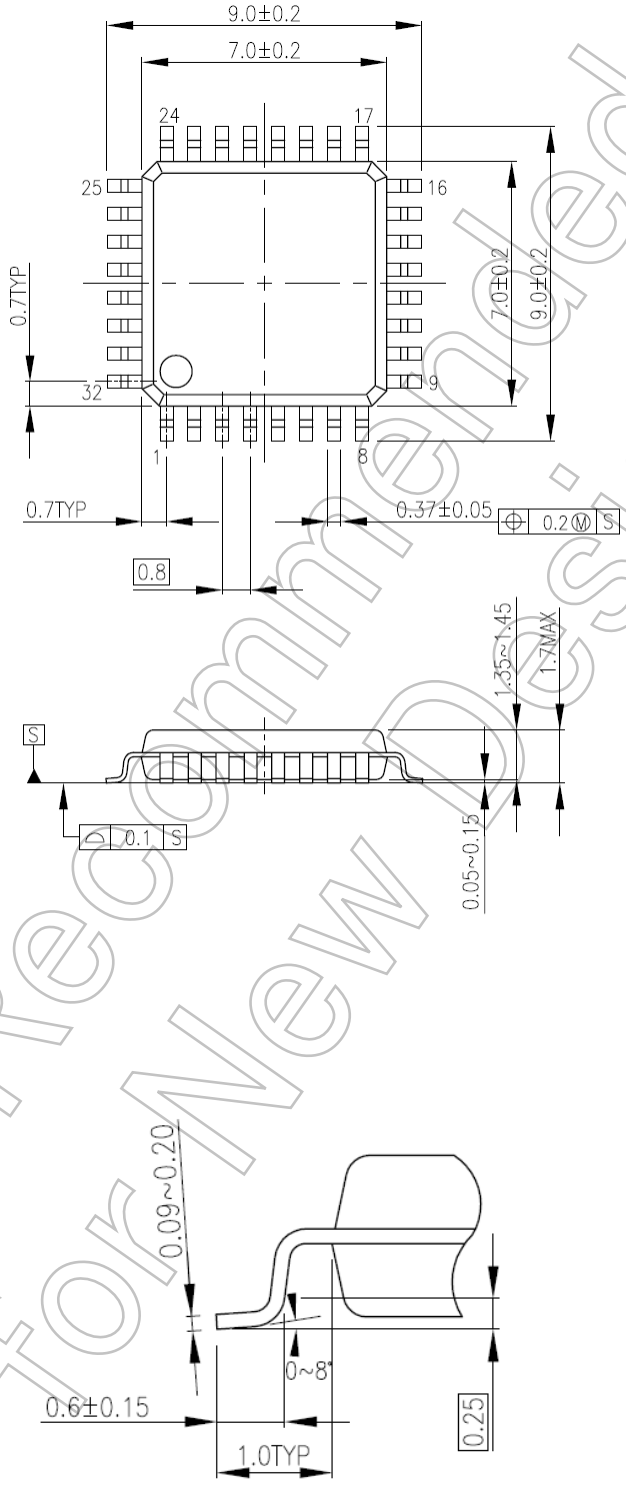
8.4. P-LQFP44-1010-0.80-003

Unit: mm



8.5. P-LQFP32-0707-0.80-002

Unit: mm



9. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power on

At power on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power on reset, pins of the MCUs that use the internal power on reset are undefined until power supply voltage reaches the voltage at which power on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
1.0	2018-01-24	First release
2.0	2018-05-10	-Words changed as following. (Op-Amp → OPAMP, NBD → NBDIF, Watchdog timer → Watchdog Timer) -5.1. Corrected Flash Memory name in Table 5.1. -6. Revised Figure of 6.1 Port and 6.4 Clock control, PJ6/BOOT -Appendix: Revised Note6 of "List of All pins"
3.0	2018-07-05	- Features Number of Interrupt ,Internal (72 → 66) - added "Commercial Production Date" on the Footer of top page -5.13 Function overview modified -7.2 Conditions of the Power supply modified (fsys at 2.7V) -7.3 IDLE condition modified -7.4 Note4 modified -7.5 Note1 added -7.9.1.2 Parameter modified of t_{ODLY1}(hold time → delay time) -Figure 7.5 Pin name modified (INAn → INCn)
3.1	2018-09-06	-Preface modified Trademark of SST. -Terms and Abbreviations: modified the content of Fm -2.3. LQFP44: modified the PKG figure -4.1.4. added Note5. -5.16. revised the title -7.4. added power supply specification in 1st Line. modified the contents of "Analog reference voltage(+). added Note5. - 7.5. changed title from "OPAMP" to " Operational amplifier Characteristics ", Corrected AVDD to AVDD5 in Figure 7.1 -7.5., 7.6., 7.7. changed the letter of T from uppercase to child character - RESTRICTIONS revised the contents and added the URL.
3.2	2019-09-17	- 2. LQFP48: Added "TRST_N" in 4 pin Deleted "TSPI1RXD" in 13 pin LQFP44: Added "UT3TXDA/UT3RXD/TSPI3TXD" in 24 pin - 4.1.5. Note: Added and changed - 4.2. Table 4.10: Added EHCLKIN row - 4.3. Deleted "The right-hand side of the port shows specification with the symbol." and "The symbols have the following meanings:" - 5.6. Modified "high speed oscillator" to "high speed oscillator 1" - 5.21. Modified "WDT" to "SIWDT" "internal oscillator" to "internal oscillator 1" "internal oscillator for the OFD" to "internal oscillator 2" - 6.3. Added "(R_{RST})" in the figure - 7.8. Parameter: Modified "Detection Release time" to "Release response time" - 7.9.1.2. Deleted "The number of cycles .... value of k1 ... value of K2 ... values are 1 to 16." - 7.9.2.2 Table: Changed $t_{SU,STA}$ row Added t_{SP}, t_r, t_f row Changed Figure7.4. - 7.9.3.2. (1) Modified: "fsys" → "ΦT0" (2) Modified: "fsys=80MHz" → "ΦT0=80MHz NF=4" Figure 7.5 Modified signal name: "t_{PWMH}" → "t_{PWH}", "t_{PWML}" → "t_{PWL}" - 7.9.6.2. Modified "from rising edge" and "from on rising edge" to "from on the rising edge" Modified "Input data valid from on the rising edge of CLK"

		to "Rising edge of CLK from input data valid" - 7.9.6.3. Parameter: Modified "the rising edge of CLK" to "the falling edge of CLK" Modified "Input data valid from on the rising edge of CLK" to "Rising edge of CLK from input data valid" - 7.12.1. Note2: Modified "if it is required" to "if trimming of IHOSC1 is required" Added "However, IHOSC2 cannot execute trimming" - List of All pins PH0 / Combination Function B: Added "EHCLKIN" PE5 / Combination Function A: Modified "AINA15" to "AINA15/VREFH"
3.3	2021-10-15	- Terms and Abbreviations: modified the content of TSPI - 7.8. Modified Min/Max value of V_{LVL4} to V_{LVL7}

Appendix
List of All pins

Combination Function A, B: These are the functions which become effective without setting up port function registers.
Combination Function 1 to 7: These are the functions which become effective with setting up port function registers.
Depending on the product, the functions of the gray hatch in the table below may not be available.

M4K4 LQFP64	M4K2 LQFP 48	M4K1 LQFP 44	M4K0 LQFP32	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Combination Function 7	Input/ Output	PU/PD	5V_T	SMT/ CMOS	Under Reset	After Reset
1	2	1	1	PK2		INT02a	UT0RXD	UT0TXDA	TSPI0RXD				TMS/SWDIO	I/O	PU/PD	N/A	SMT	PU (Note)	PU (Note)
2	3	2	2	PK3		INT03a	UT0TXDA	UT0RXD	TSPI0TXD				TCK/SWCLK	I/O	PU/PD	N/A	SMT	PD (Note)	PD (Note)
3	4	3	-	PK4		INT06			TSPI0SCK			NBDSYNC	TRST_N	I/O	PU/PD	N/A	SMT	PU (Note)	PU (Note)
4	-	-	-	PL3								NBDDATA3	TRACEDATA3	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
5	-	-	-	PL2								NBDDATA2	TRACEDATA2	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
6	-	-	-	PL1								NBDDATA1	TRACEDATA1	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
7	-	-	-	PL0								NBDDATA0	TRACEDATA0	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
8	-	-	-	PL4								NBDCLK	TRACECLK	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
9	5	4	3	DVDD5A										-	-	-	-	-	-
10	6	5	4	REGOUT2										-	-	-	-	-	-
11	7	6	5	REGOUT1										-	-	-	-	-	-
12	-	7	-	PH3										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
13	8	8	-	PH2							EMG0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
14	9	9	6	DVSSA										-	-	-	-	-	-
15	10	10	7	PH0	X1	EHCLKIN								Input	PD	N/A	SMT	Hi-z	Hi-z
16	11	11	8	PH1	X2									Input	PD	N/A	SMT	Hi-z	Hi-z
17	12	12	9	RESET_N										-	PU	-	SMT	-	-
18	13	-	-	PA1		INT09	UT1RXD	UT1TXDA	TSPI1RXD	T32A01INA0	T32A01INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
19	14	13	-	PA0		INT07a	UT1TXDA	UT1RXD	TSPI1TXD	T32A01INB0	T32A01OUTB			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
20	-	-	-	PA2					TSPI1SCK	T32A01INA1	T32A01INC1	T32A01OUTA	T32A01OUTC	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
21	-	-	-	PJ7							OVV0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
22	15	14	10	PJ6	BOOT_N						EMG0			I/O	PU/PD	N/A	SMT	PU	Hi-z
23	16	15	11	PJ5							ZO0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
24	17	16	12	PJ4							WO0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
25	18	17	13	PJ3							YO0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
26	19	18	14	PJ2							VO0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
27	20	19	15	PJ1							XO0		PMD1DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
28	21	20	16	PJ0							UO0	SCOUT	PMD0DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
29	22	21	17	DVSSB										-	-	-	-	-	-
30	-	-	-	DVDD5B										-	-	-	-	-	-
31	23	22	-	PB0		INT02b			I2C0SDA	T32A05OUTA	T32A05OUTC		PMD0DBG	I/O	PU/PD	YES	SMT	Hi-z	Hi-z
32	24	23	-	PB1		INT03b	T32A05OUTB		I2C0SCL	T32A05INA0	T32A05INC0	TRGIN1	PMD1DBG	I/O	PU/PD	YES	SMT	Hi-z	Hi-z
33	-	-	-	PC2		INT07b			TSPI3SCK	T32A03INA1	T32A03INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
34	-	-	-	PC1		INT10	UT3RXD	UT3TXDA	TSPI3RXD	T32A03INA0	T32A03INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
35	25	24	-	PC0		INT08	UT3TXDA	UT3RXD	TSPI3TXD	T32A03OUTA	T32A03OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
36	26	25	18	AVSS										-	-	-	-	-	-
37	27	26	19	PD0	AINA00									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
38	28	27	20	PD1	AINA01									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
39	29	28	21	PD2	AINA03									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
40	30	29	-	PD3	AINA04									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
41	31	30	22	PD4	AINA06									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
42	32	31	-	PD5	AINA07									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
43	33	32	23	PD6	AINA09						EMG0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
44	34	33	-	PE0	AINA10									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
45	35	34	-	PE1	AINA11									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

M4K4 LQFP64	M4K2 LQFP 48	M4K1 LQFP 44	M4K0 LQFP32	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Combination Function 7	Input/ Output	PU/PD	5V_T	SMT/ CMOS	Under Reset	After Reset
46	36	-	-	PE2	AINA12									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
47	-	-	-	PE3	AINA13									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
48	-	-	-	PE4	AINA14									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
49	37	35	24	PE5	AINA15/ VREFH									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
50	38	36	25	AVDD5										-	-	-	-	-	-
51	-	-	-	PF2		INT01b				T32A04INA1	T32A04INC1	TRGIN2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
52	-	-	-	PF1		INT00b				T32A04INA0	T32A04INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
53	-	-	-	DVDD5C										-	-	-	-	-	-
54	39	37	26	DVSSC										-	-	-	-	-	-
55	40	38	-	PF0						T32A04OUTA	T32A04OUTC	TRGIN0	EMG1	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
56	41	39	27	PG0		INT04	UT2TXDA	TSPI2TXD	T32A02OUTA	T32A02OUTC	ENC0A	UO1	PMD0DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
57	42	40	28	PG1		INT05	UT2RXD	TSPI2RXD	T32A02INA0	T32A02INC0	ENC0B	VO1	PMD1DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
58	43	41	29	PG2				TSPI2SCK	T32A02INA1	T32A02INC1	ENC0Z	WO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
59	44	-	-	PG3								XO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
60	45	-	-	PG4								YO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
61	46	-	-	PG5								ZO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
62	47	42	30	MODE										-	PD	-	SMT	-	-
63	48	43	31	PK0		INT00a	UT0RXD	UT0TXDA		T32A00OUTA	T32A00OUTC		TDI	I/O	PU/PD	N/A	SMT	PU (Note)	PU (Note)
64	1	44	32	PK1		INT01a	UT0TXDA	UT0RXD		T32A00INA0	T32A00INC0		TDO/SWV	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

Note: The Initial value of built-in Pull-up/Pull-down resistor is effective.

Note1: TRST_N is not available in M4K0.

Note2: TRACE and NBDIF are not available in M4K2/M4K1/M4K0.

Note3: UART ch1 is not available in M4K1/M4K0, ch3 is not in M4K2/M4K1/M4K0.

Note4: TSPI ch0 is not available in M4K0, ch1 and 3 are not in M4K2/M4K1/M4K0.

Note5: I^2C ch0 is not available in M4K0.

Note6: INT00b, INT01b, INT07b and INT10 are not available in M4K2/M4K1/M4K0,
INT09 is not in M4K1/M4K0, INT02b, INT03b, INT06, INT07a and INT08 are not in M4K0.

Part Naming Conventions

TMP M4K 4 F Y x UG

The identification of Toshiba microcontrollers

Core

Symbol	Core
M4	Arm Cortex-M4 processor with FPU
M3	Arm Cortex-M3
M0	Arm Cortex-M0

Product Group

Family	Group	Application
TXZ	H	For General-purpose/Consumer electronic equipment
	K	For Motor/Inverter control industrial equipment(MCU+AMP/COMP)
	G	For OA/Digital equipment/industrial equipment
	E	For Robotics, Precision instruments control
	P	For Healthcare/ Battery equipment

Pin Count

Symbol	Pin count	Symbol	Pin count
0, G	Under 32pin	8, Q	129pin to 144pin
1, H	33pin to 44pin	9, R	145pin to 176pin
2, J	45pin to 48pin	A, S	177pin to 200pin
3, K	49pin to 52pin	B, T	201pin to 224pin
4, L	53pin to 64pin	C, U	225pin to 250pin
5, M	65pin to 80pin	D, V	251pin to 300pin
6, N	81pin to 100pin		
7, P	101pin to 128pin		

Revision

Package

Symbol	Package
QG	Plastic shrink quad outline non-leaded package; dry-packed
UG,DUG,FG, DFG	Plastic quad flat package; dry-packed
MG,DMG	Plastic small-outline package; dry-packed
XBG	Plastic ball grid array; dry-packed

ROM Size

Symbol	Size[KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
E	768
10	1,023
15	1,536
20	2,048
40	4,096
80	8,192

ROM Type

Symbol	Type
F	Flash
C	Mask

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