

Toshiba Intelligent Power Device Silicon Monolithic Power MOS Integrated Circuit

# TPD1046F

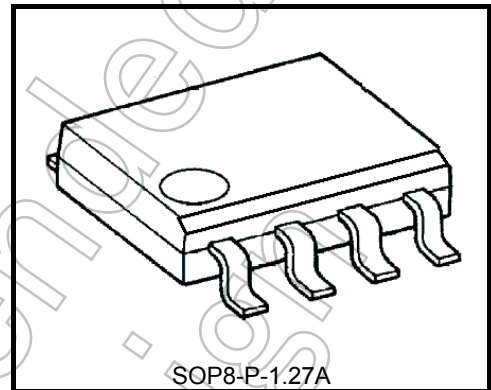
## 2-IN-1 Low-Side Power Switch for Motor, Solenoid and Lamp Drive

The TPD1046F is a 2-IN-1 low-side switch.

The IC has a vertical MOSFET output which can be directly driven from a CMOS or TTL logic circuit (e.g., an MPU). The IC is equipped with intelligent self-protection functions.

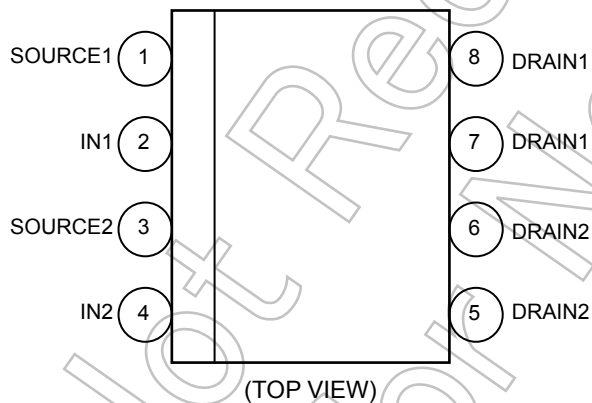
### Features

- Two built-in power IC chips with a structure combining a control block and a vertical power MOSFET (L<sup>2</sup>-π-MOS) on each chip.
- Can directly drive a power load from a CMOS or TTL logic.
- Built-in protection circuits against overvoltage (active clamp), overtemperature (thermal shutdown), and overcurrent (current limiter).
- Low Drain-Source ON-resistance:  $R_{DS(ON)} = 0.2 \Omega$  (max) (@ $V_{IN} = 5\text{ V}$ ,  $I_D = 1\text{ A}$ ,  $T_{ch} = 25^\circ\text{C}$ )
- Low Leakage Current:  $I_{DSS} = 10 \mu\text{ A}$  (max) (@ $V_{IN} = 0\text{ V}$ ,  $V_{DS} = 30\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$ )
- Low Input Current:  $I_{IN} = 600 \mu\text{ A}$  (max) (@ $V_{IN} = 5\text{ V}$ ,  $T_{ch} = -40\sim 125^\circ\text{C}$ )
- 8-pin SOP package with embossed-tape packaging.

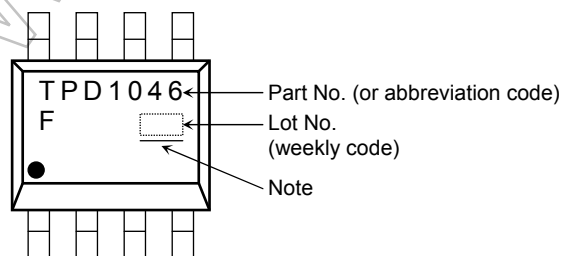


Weight: 0.08 g (typ.)

### Pin Assignment (top view)



### Marking



Note: A line under a Lot No. identifies the indication of product Labels  
 Not underlined: [[Pb]]/INCLUDES > MCV  
 Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

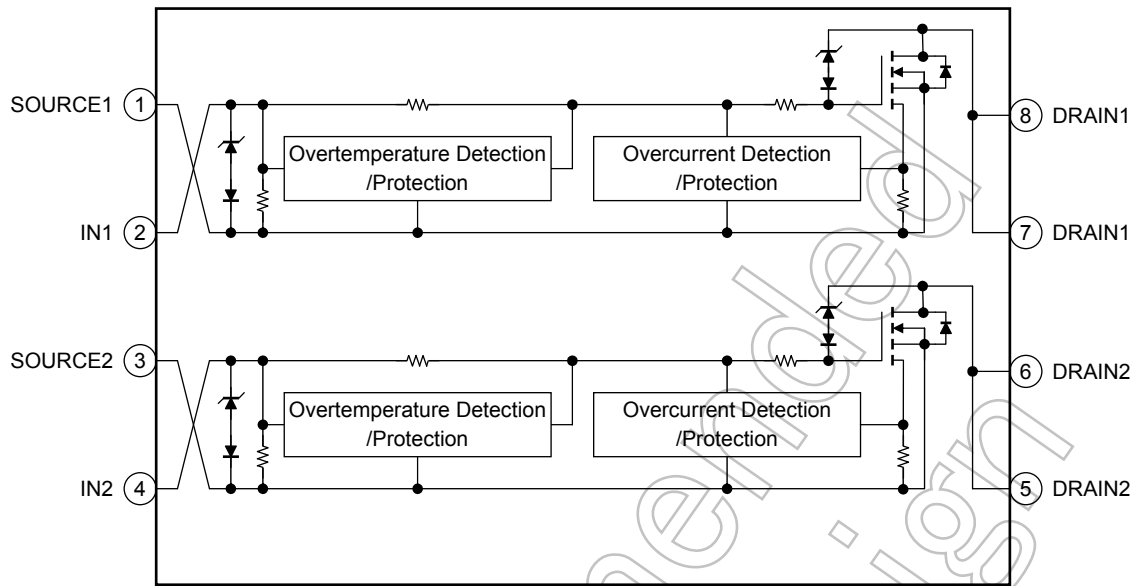
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Due to its MOS structure, this product is sensitive to static electricity.

Start of commercial production  
2005-05

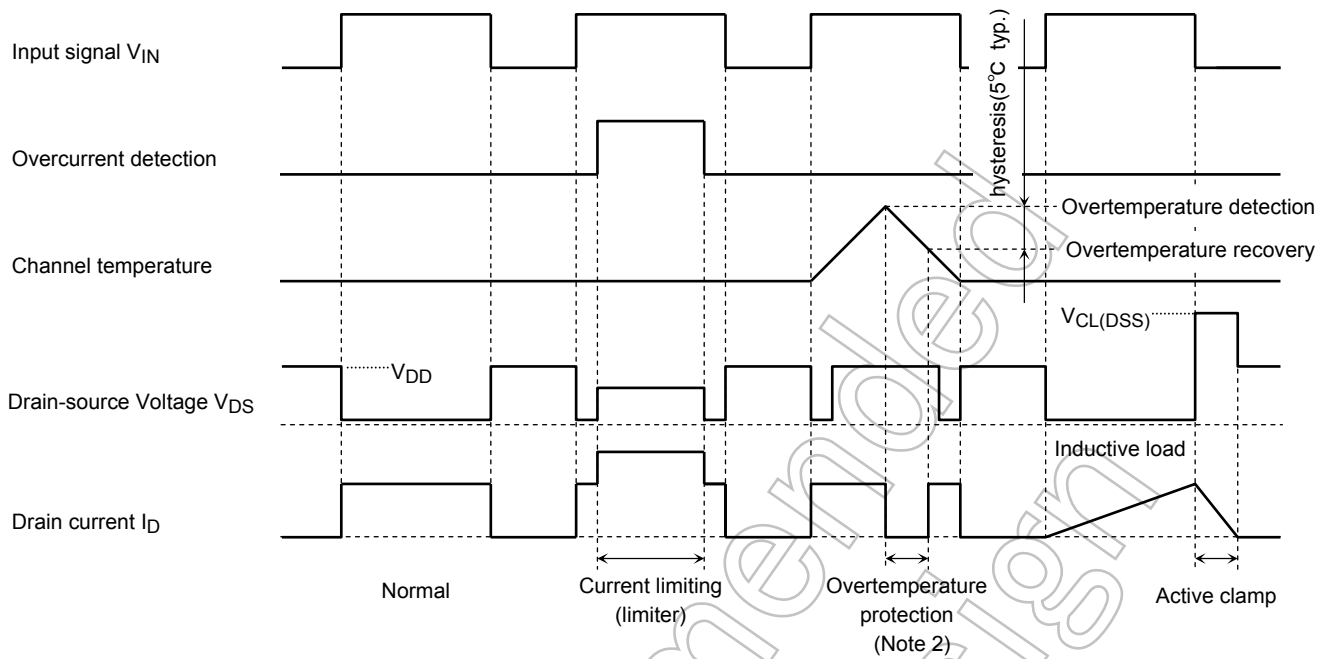
**Block Diagram**



**Pin Description**

Pin No.	Symbol	Pin Description
1	SOURCE1	Source pin 1
2	IN1	Input pin 1 This pin is connected to a pull-down resistor internally, so that even when input wiring is open-circuited, output can never be turned on inadvertently.
3	SOURCE2	Source pin 2
4	IN2	Input pin 2 This pin is connected to a pull-down resistor internally, so that even when input wiring is open-circuited, output can never be turned on inadvertently.
5, 6	DRAIN2	Drain pin 2 Drain current is limited (by current limiter) if it exceeds 3 A (min) in order to protect the IC.
7, 8	DRAIN1	Drain pin 1 Drain current is limited (by current limiter) if it exceeds 3 A (min) in order to protect the IC.

**Timing Chart**



Note 2: The overtemperature detector circuits feature hysteresis. After overtemperature is detected, normal operation is restored only when the channel temperature falls by the hysteresis amount (5°C typ.) in relation to the overtemperature detection temperature.

**Truth Table**

$V_{IN}$	$V_{DS}$	Output State	Operating State
L	H	OFF	Normal
H	L	ON	
L	H	OFF	Overcurrent
H	H	current limiting(limiter)	
L	H	OFF	Overtemperature
H	H	OFF	

## Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DS(DC)}$	40	V
Drain current		$I_D$	Internally Limited	A
Input voltage		$V_{IN}$	-0.3~7	V
Power dissipation (Ta = 25°C) (Note 3-a)	1device operation (Note 4a)	$P_{D(1)}$	0.95	W
	2 devices operation per device (Note 4b)	$P_{D(2)}$	0.54	W
Power dissipation (Ta = 25°C) (Note 3-b)	1device operation (Note 4a)	$P_{D(1)}$	0.38	W
	2 devices operation per device (Note 4b)	$P_{D(2)}$	0.20	W
Single pulse active clamp tolerance (Note 5)		$E_{AS}$	97	mJ
Active clamp current		$I_{AR}$	3	A
Repetitive active clamp tolerance (Note 3-a) (Note 6)		$E_{AR}$	54	$\mu$ J
Operating temperature		$T_{opr}$	-40~125	°C
Channel temperature		$T_{ch}$	150	°C
Storage temperature		$T_{stg}$	-55~150	°C

## Thermal Characteristics

Characteristics		Symbol	max	Unit
Thermal resistance, channel to ambient (Note 3-a)	1device operation (Note 4a)	$R_{th(ch-a)(1)}$	132	°C/W
	2 devices operation per device (Note 4b)	$R_{th(ch-a)(2)}$	231	
Thermal resistance, channel to ambient (Note 3-b)	1device operation (Note 4a)	$R_{th(ch-a)(1)}$	330	°C/W
	2 devices operation per device (Note 4b)	$R_{th(ch-a)(2)}$	625	

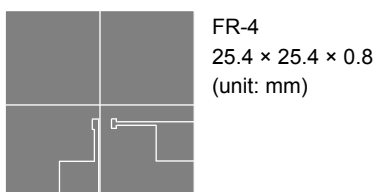
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

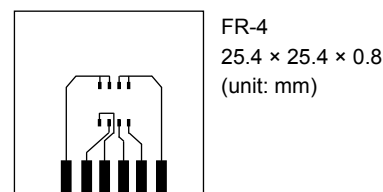
Note 3:

3-a : glass epoxy board (a)

3-b : glass epoxy board (b)



(a)



(b)

Note 4:

- a) 1 device operation : power dissipation value or thermal resistance of one side device.
- b) 2 devices operation per device : power dissipation value or thermal resistance per device when power is impressed evenly.

Note 5:  $V_{DD} = 25\text{ V}$ ,  $T_{ch} = 25^{\circ}\text{C}$ (initial),  $L = 10.8\text{ mH}$ ,  $I_{AR} = 3\text{ A}$ ,  $R_G = 25\ \Omega$

Note 6: Repetitive rating : Pulse width limited by maximum channel temperature.

Not Recommended  
for New Design

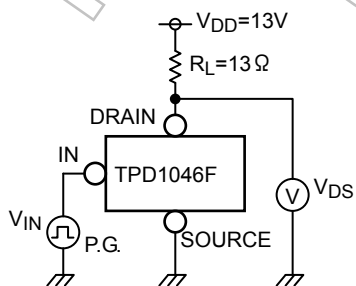
## Electrical Characteristics

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Drain-source clamp voltage	$V_{(CL) DSS}$	-	-	$T_{ch} = 25^{\circ}C$	40	49	60	V
				$T_{ch} = -40 \sim 125^{\circ}C$				
Input threshold voltage	$V_{th}$	-	-	$T_{ch} = 25^{\circ}C$	1.0	1.6	2.8	V
				$T_{ch} = -40 \sim 125^{\circ}C$				
Protective circuit operation input voltage range	$V_{IN (opr)}$	-	-	$T_{ch} = -40 \sim 125^{\circ}C$	4	-	7	V
Drain cut-off current	$I_{DSS}$	-	-	$T_{ch} = 25^{\circ}C$	-	-	10	$\mu A$
				$T_{ch} = -40 \sim 125^{\circ}C$				
High level input current	$I_{IH (1)}$	-	-	$T_{ch} = 25^{\circ}C$	-	130	600	$\mu A$
				$T_{ch} = -40 \sim 125^{\circ}C$				
High level input current	$I_{IH (2)}$	-	-	$T_{ch} = -40 \sim 125^{\circ}C$	-	-	2000	$\mu A$
				$V_{IN} = 5 V,$ when protective circuit is actuated				
Drain-source on resistance	$R_{DS (ON)}$	-	-	$T_{ch} = 25^{\circ}C$	-	0.14	0.2	$\Omega$
				$T_{ch} = -40 \sim 125^{\circ}C$				
Load-short tolerance	$V_{DS}$	-	-	$T_{ch} = -40 \sim 125^{\circ}C$	20	-	-	V
Overtemperature detection	temperature detection	$T_{OT(1)}$	-	-	150	160	-	$^{\circ}C$
	temperature recovery	$T_{OT(2)}$	-	-	125	155	-	$^{\circ}C$
Overcurrent detection	$I_{OC}$	-	-	$T_{ch} = 25^{\circ}C$	3.0	3.7	-	A
				$T_{ch} = -40 \sim 125^{\circ}C$				
Switching time	$t_{on}$	1	-	$T_{ch} = 25^{\circ}C$	-	15	100	$\mu s$
				$T_{ch} = -40 \sim 125^{\circ}C$				
	$T_{ch} = 25^{\circ}C$	-	30	100				
	$T_{ch} = -40 \sim 125^{\circ}C$	-	-	100				
Drain-source diode forward voltage	$V_{DSF}$	-	-	$T_{ch} = 25^{\circ}C$	-	-	1.7	V

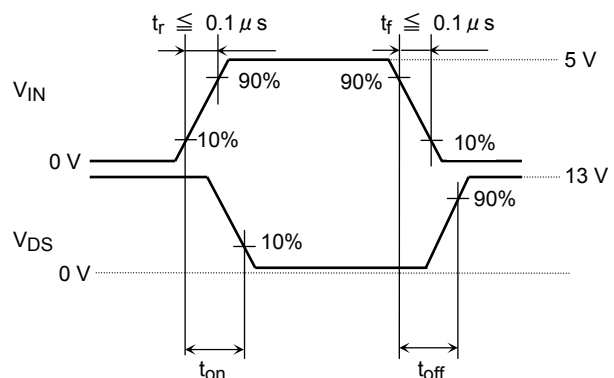
### Test Circuit 1

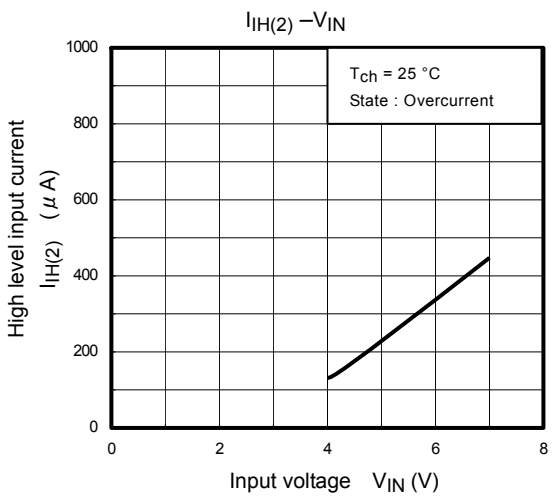
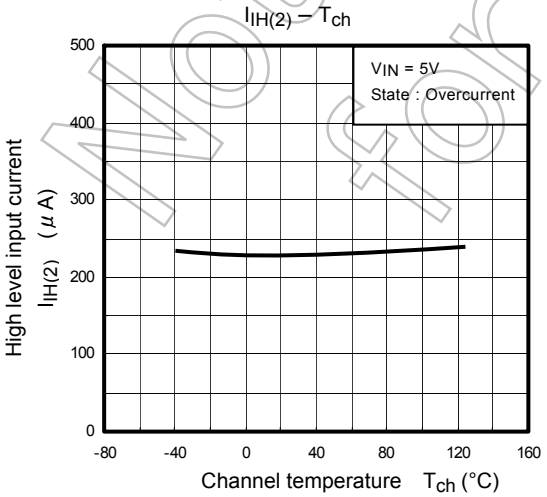
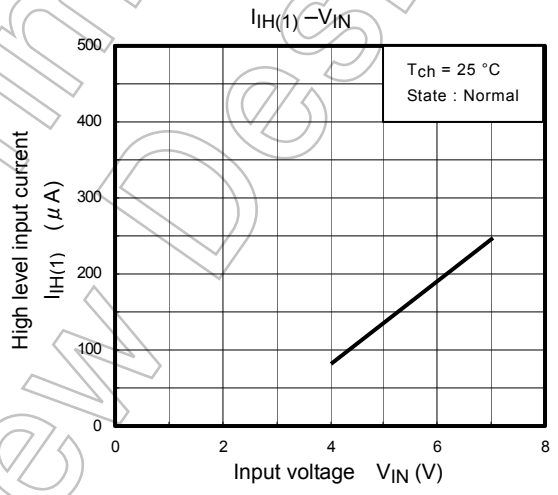
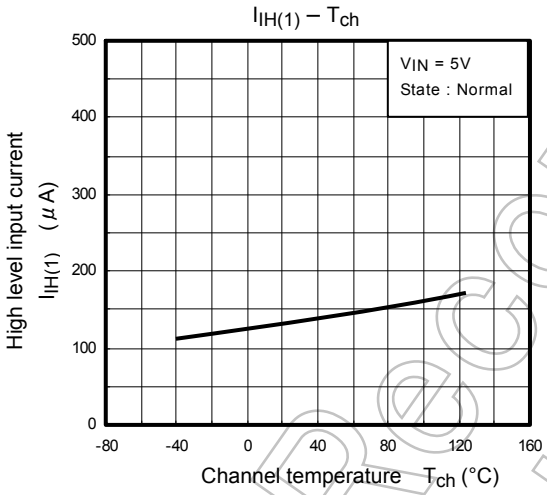
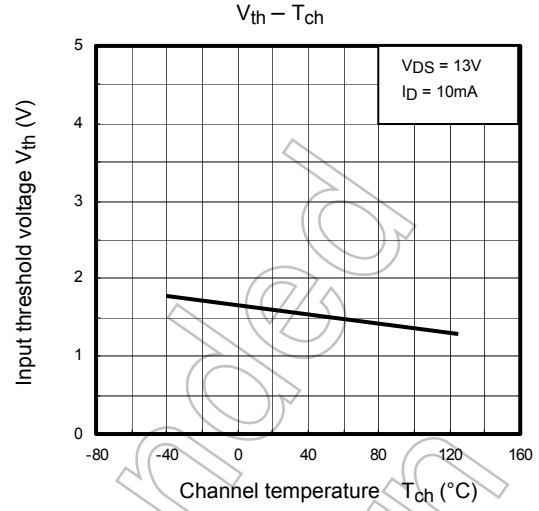
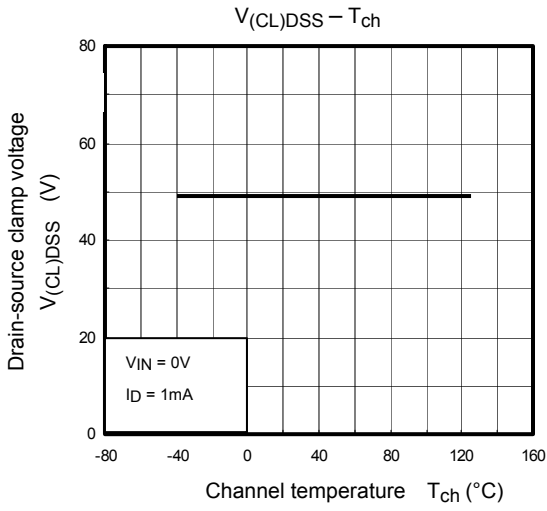
#### Switching time measuring circuit

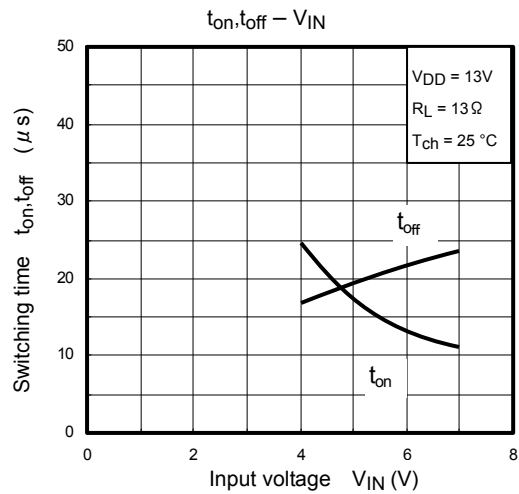
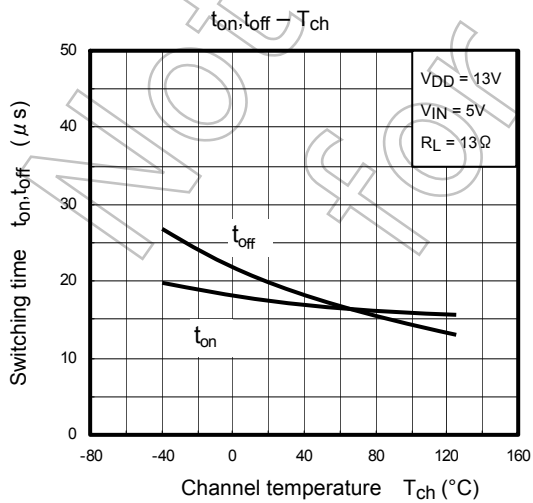
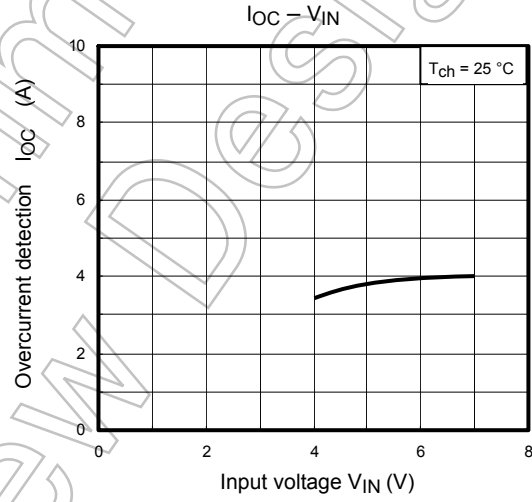
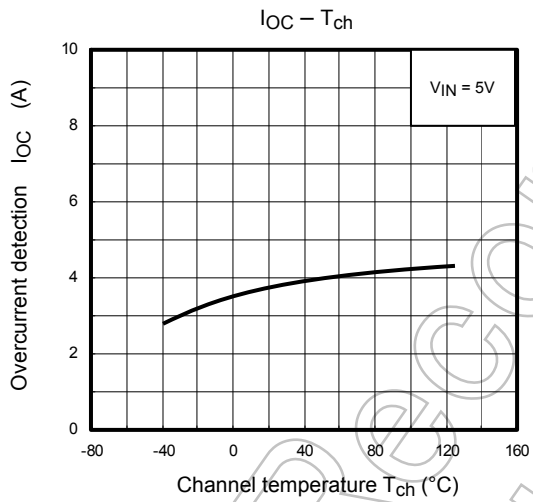
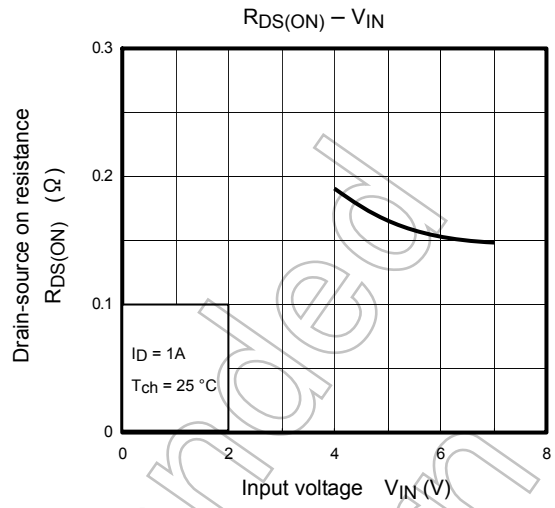
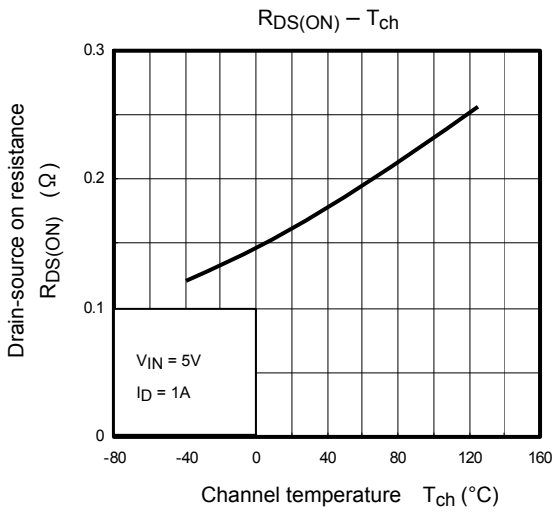
##### Test circuit



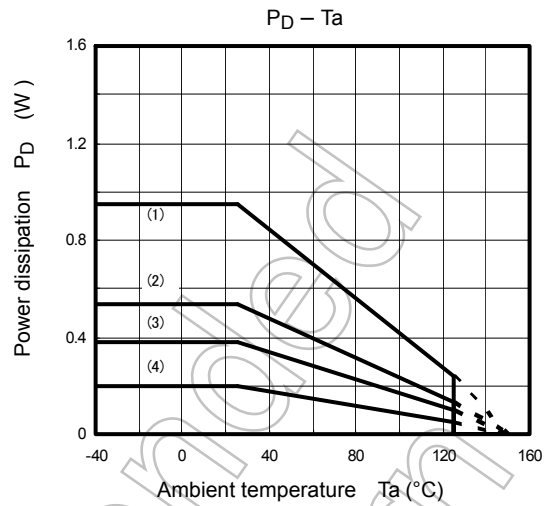
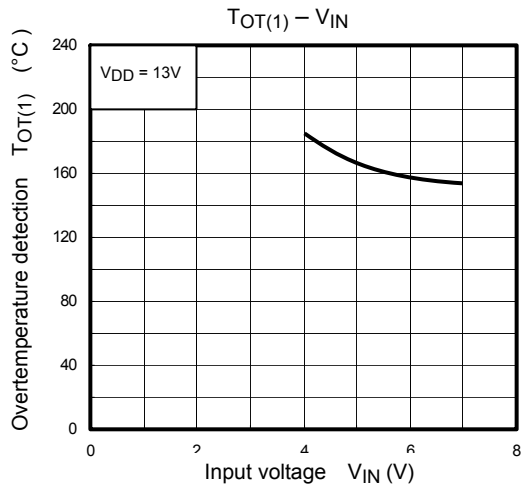
##### Measured waveforms



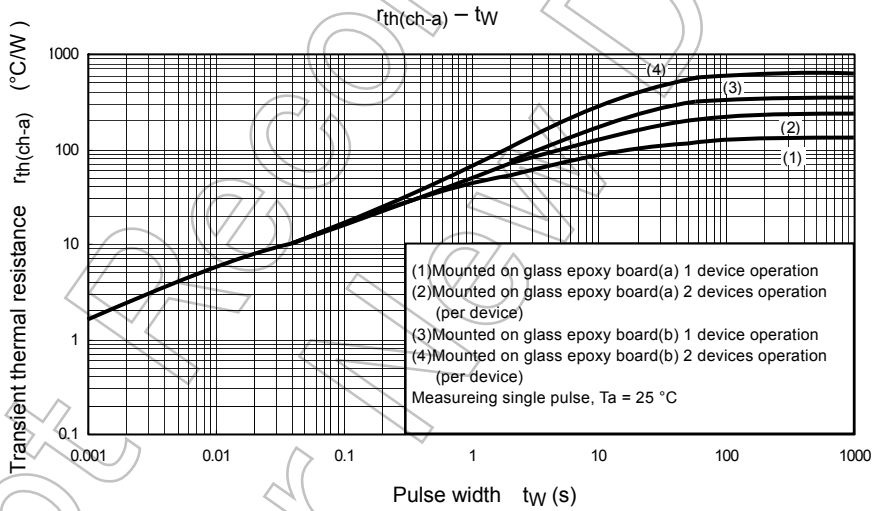






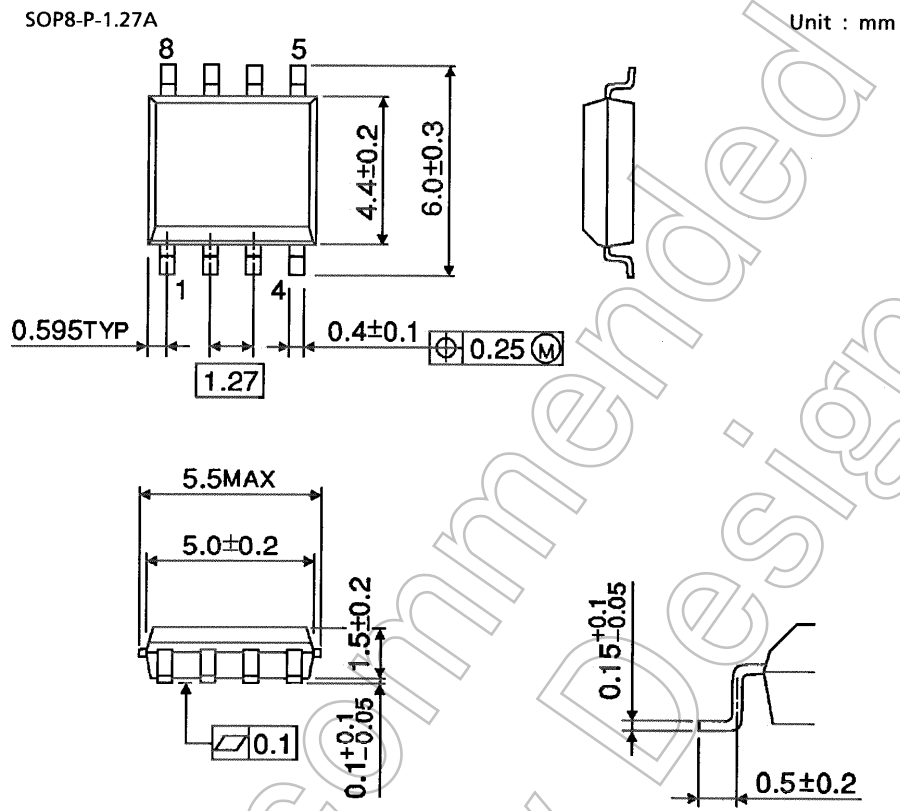


- (1) Mounted on glass epoxy board(a) 1 device operation
- (2) Mounted on glass epoxy board(a) 2 devices operation (per device)
- (3) Mounted on glass epoxy board(b) 1 device operation
- (4) Mounted on glass epoxy board(b) 2 devices operation (per device)



- (1) Mounted on glass epoxy board(a) 1 device operation
  - (2) Mounted on glass epoxy board(a) 2 devices operation (per device)
  - (3) Mounted on glass epoxy board(b) 1 device operation
  - (4) Mounted on glass epoxy board(b) 2 devices operation (per device)
- Measuring single pulse,  $T_a = 25\text{ }^\circ\text{C}$

Package Dimensions



Weight: 0.08 g (typ.)

Not Recommended for New Design

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