

# TC7SPN3125TU

## 1. Functional Description

- Low-Voltage, Low-Power 1-Bit Dual-Supply Bus Buffer

## 2. General

The TC7SPN3125TU is an advanced high-speed CMOS 1-bit dual supply voltage interface bus buffer fabricated with silicon gate CMOS technology.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Designed for use as an interface between a 1.2 V, 1.5 V, 1.8 V, or 2.5 V bus and a 1.8 V, 2.5 V or 3.3 V bus in mixed 1.2 V, 1.5 V, 1.8 V or 2.5 V/1.8 V, 2.5 V or 3.3 V supply systems.

The A-input interfaces with the 1.2 V, 1.5 V, 1.8 V or 2.5 V bus, the B-output with the 1.8 V, 2.5 V, 3.3 V bus.

The enable input ( $\overline{OE}$ ) can be used to disable the device so that the signal lines are effectively isolated.

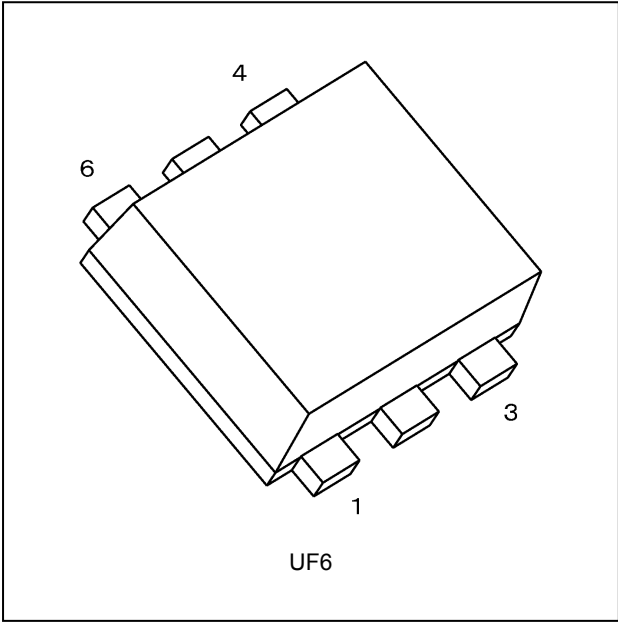
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features (Note)

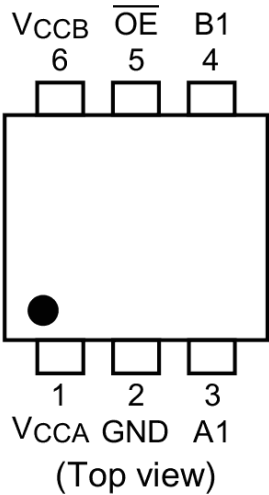
- Level converter for interfacing 1.2 V to 1.8 V, 1.2 V to 2.5 V, 1.2 V to 3.3 V, 1.5 V to 2.5 V, 1.5 V to 3.3 V, 1.8 V to 2.5 V, 1.8 V to 3.3 V, 2.5 V to 3.3 V system.
- High-speed operation:  $t_{pd} = 13.7$  ns (max) ( $V_{CCA} = 2.5 \pm 0.2$  V,  $V_{CCB} = 3.3 \pm 0.3$  V)  
 $t_{pd} = 14.8$  ns (max) ( $V_{CCA} = 1.8 \pm 0.15$  V,  $V_{CCB} = 3.3 \pm 0.3$  V)  
 $t_{pd} = 16.0$  ns (max) ( $V_{CCA} = 1.5 \pm 0.1$  V,  $V_{CCB} = 3.3 \pm 0.3$  V)  
 $t_{pd} = 29$  ns (max) ( $V_{CCA} = 1.2 \pm 0.1$  V,  $V_{CCB} = 3.3 \pm 0.3$  V)  
 $t_{pd} = 18.5$  ns (max) ( $V_{CCA} = 1.8 \pm 0.15$  V,  $V_{CCB} = 2.5 \pm 0.2$  V)  
 $t_{pd} = 19.7$  ns (max) ( $V_{CCA} = 1.5 \pm 0.1$  V,  $V_{CCB} = 2.5 \pm 0.2$  V)  
 $t_{pd} = 33$  ns (max) ( $V_{CCA} = 1.2 \pm 0.1$  V,  $V_{CCB} = 2.5 \pm 0.2$  V)  
 $t_{pd} = 43$  ns (max) ( $V_{CCA} = 1.2 \pm 0.1$  V,  $V_{CCB} = 1.8 \pm 0.15$  V)
- Output current:  $|I_{OHB}|/|I_{OLB}| = \pm 3$  mA (min) ( $V_{CCB} = 3.0$  V)  
 $|I_{OHB}|/|I_{OLB}| = \pm 2$  mA (min) ( $V_{CCB} = 2.3$  V)  
 $|I_{OHB}|/|I_{OLB}| = \pm 0.5$  mA (min) ( $V_{CCB} = 1.65$  V)
- Ultra-small package: UF6
- Low power dissipation: By using the new circuit, the power consumption is reduced significantly when  $\overline{OE} = "H"$ .  
 Suitable for battery-driven applications such as PDAs and cellular phones.
- Floating A-bus is permitted. (when  $\overline{OE} = "H"$ )
- 3.6 V tolerance and power-down protection are provided to all inputs and outputs.

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

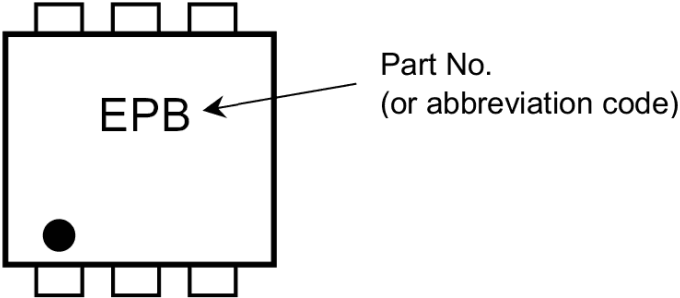
4. Packaging



5. Pin Assignment



6. Marking

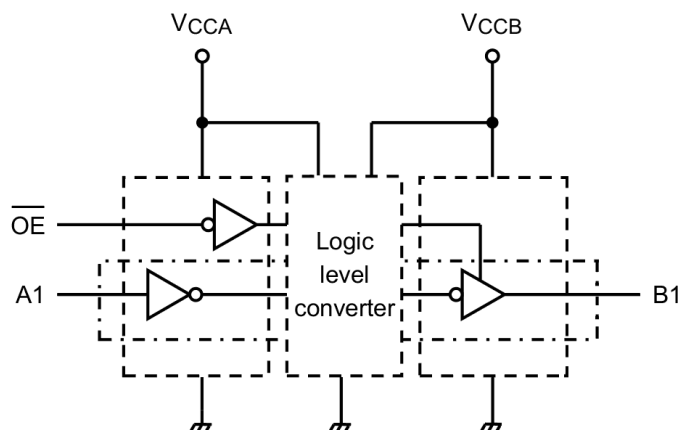


### 7. Truth Table

Input OE	Input A1	Output B1
L	L	L
L	H	H
H	X	Z

X: Don't care  
Z: High impedance

### 8. Block Diagram



### 9. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CCA}$	(Note 1)	-0.5 to 4.6	V
	$V_{CCB}$		-0.5 to 4.6	
Input voltage (A1, $\overline{OE}$ )	$V_{IN}$		-0.5 to 4.6	V
Output voltage (B1)	$V_{OUTB}$	(Note 2)	-0.5 to 4.6	V
		(Note 3)	-0.5 to $V_{CCB} + 0.5$	
Input diode current	$I_{IK}$		-25	mA
Output diode current	$I_{OK}$	(Note 4)	$\pm 50$	mA
Output current	$I_{OUTB}$		$\pm 6$	mA
$V_{CC}$ /ground current per supply pin	$I_{CCA}$		$\pm 25$	mA
	$I_{CCB}$		$\pm 50$	
Power dissipation	$P_D$		200	mW
Storage temperature	$T_{stg}$		-65 to 150	$^\circ\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Don't supply a voltage to  $V_{CCB}$  pin when  $V_{CCA}$  is in the OFF state.

Note 2: Output in OFF state.

Note 3: High (H) or Low (L) state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < \text{GND}$ ,  $V_{OUT} > V_{CC}$

### 10. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	$V_{CCA}$		—	1.1 to 2.7	V
	$V_{CCB}$			1.65 to 3.6	
Input voltage (A1, $\overline{OE}$ )	$V_{IN}$		—	0 to 3.6	V
Output voltage (B1)	$V_{OUTB}$	(Note 1)	—	0 to 3.6	V
		(Note 2)		0 to $V_{CCB}$	
Output current (B1)	$I_{OUTB}$		$V_{CCB} = 3.0$ to $3.6$ V	$\pm 3$	mA
			$V_{CCB} = 2.3$ to $2.7$ V	$\pm 2$	
			$V_{CCB} = 1.65$ to $1.95$ V	$\pm 0.5$	
Operating temperature	$T_{opr}$		—	-40 to 85	°C
Input rise and fall times	dt/dv		$V_{IN} = 0.8$ to $2.0$ V, $V_{CCA} = 2.5$ V, $V_{CCB} = 3.0$ V	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND.

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state.

### 11. Electrical Characteristics

#### 11.1. DC Characteristics

1.1 V ≤ V<sub>CCA</sub> ≤ 2.7 V, 1.65 V < V<sub>CCB</sub> ≤ 3.6 V  
(Unless otherwise specified, T<sub>a</sub> = -40 to 85 °C)

Characteristics	Symbol	Test Condition	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min	Max	Unit	
High-level input voltage	V <sub>IHA</sub>	$\overline{OE}$ , A1	1.1 ≤ V <sub>CCA</sub> ≤ 1.4	1.65 to 3.6	0.65×V <sub>CCA</sub>	—	V	
			1.4 ≤ V <sub>CCA</sub> ≤ 1.65	1.65 to 3.6	0.65×V <sub>CCA</sub>	—		
			1.65 ≤ V <sub>CCA</sub> ≤ 2.3	2.3 to 3.6	0.65×V <sub>CCA</sub>	—		
			2.3 ≤ V <sub>CCA</sub> ≤ 2.7	2.7 to 3.6	1.6	—		
Low-level input voltage	V <sub>IILA</sub>	$\overline{OE}$ , A1	1.1 ≤ V <sub>CCA</sub> ≤ 1.4	1.65 to 3.6	—	0.3×V <sub>CCA</sub>	V	
			1.4 ≤ V <sub>CCA</sub> ≤ 1.65	1.65 to 3.6	—	0.3×V <sub>CCA</sub>		
			1.65 ≤ V <sub>CCA</sub> ≤ 2.3	2.3 to 3.6	—	0.35×V <sub>CCA</sub>		
			2.3 ≤ V <sub>CCA</sub> ≤ 2.7	2.7 to 3.6	—	0.7		
High-level output voltage	V <sub>OHB</sub>	A1 = V <sub>IH</sub>	I <sub>OHB</sub> = -100 μA	1.1 to 2.7	1.65 to 3.6	V <sub>CCB</sub> -0.2	V	
			I <sub>OHB</sub> = -0.5 mA	1.1 to 1.65	1.65	1.25		
			I <sub>OHB</sub> = -2 mA	1.1 to 2.3	2.3	1.7		
			I <sub>OHB</sub> = -3 mA	1.1 to 2.7	3.0	2.2		
Low-level output voltage	V <sub>OLB</sub>	A1 = V <sub>IL</sub>	I <sub>OLB</sub> = 100 μA	1.1 to 2.7	1.65 to 3.6	—	V	
			I <sub>OLB</sub> = 0.5 mA	1.1 to 1.65	1.65	—		0.3
			I <sub>OLB</sub> = 2 mA	1.1 to 2.3	2.3	—		0.6
			I <sub>OLB</sub> = 3 mA	1.1 to 2.7	3.0	—		0.55
3-state output OFF-state leakage current	I <sub>OZB</sub>	A1 = V <sub>IHA</sub> or V <sub>IILA</sub> B1 = 0 to 3.6 V	1.1 to 2.7	1.65 to 3.6	—	±2.0	μA	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V	1.1 to 2.7	1.65 to 3.6	—	±1.0	μA	
Power-off leakage current	I <sub>OFF1</sub>	V <sub>IN</sub> , B1 = 0 to 3.6 V	0	0	—	2.0	μA	
	I <sub>OFF2</sub>	$\overline{OE}$ = V <sub>CCA</sub>	1.1 to 2.7	0	—	2.0		
	I <sub>OFF3</sub>	A1, B1 = 0 to 3.6 V	1.1 to 2.7	Open	—	2.0		
Quiescent supply current	I <sub>CCA</sub>	V <sub>IN</sub> = V <sub>CCA</sub> or GND	1.1 to 2.7	1.65 to 3.6	—	2.0	μA	
	I <sub>CCB</sub>	V <sub>IN</sub> = V <sub>CCA</sub> or GND	1.1 to 2.7	1.65 to 3.6	—	2.0		
	I <sub>CCA</sub>	V <sub>CCA</sub> ≤ V <sub>IN</sub> ≤ 3.6 V	1.1 to 2.7	1.65 to 3.6	—	±2.0		
	I <sub>CCB</sub>	V <sub>IN</sub> = V <sub>CCA</sub> V <sub>CCB</sub> ≤ B1 ≤ 3.6 V	1.1 to 2.7	1.65 to 3.6	—	±2.0		

#### 11.2. AC Characteristics

11.2.1. V<sub>CCA</sub> = 2.5 ± 0.2 V, V<sub>CCB</sub> = 3.3 ± 0.3 V  
(Unless otherwise specified, T<sub>a</sub> = -40 to 85 °C, Input: t<sub>r</sub> = t<sub>f</sub> = 2.0 ns)

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	t <sub>PLH</sub> /t <sub>PHL</sub>		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	13.7	ns
3-state output enable time ( $\overline{OE}$ → B1)	t <sub>PZL</sub> /t <sub>PZH</sub>		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	16.6	
3-state output disable time ( $\overline{OE}$ → B1)	t <sub>PLZ</sub> /t <sub>PHZ</sub>		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	7.2	

### 11.2.2. $V_{CCA} = 1.8 \pm 0.15 \text{ V}$ , $V_{CCB} = 3.3 \pm 0.3 \text{ V}$ (Unless otherwise specified, $T_a = -40$ to $85 \text{ }^\circ\text{C}$ , Input: $t_r = t_f = 2.0 \text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	$t_{PLH}/t_{PHL}$		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	14.8	ns
3-state output enable time ( $\overline{OE} \rightarrow B1$ )	$t_{PZL}/t_{PZH}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	18.9	
3-state output disable time ( $\overline{OE} \rightarrow B1$ )	$t_{PLZ}/t_{PHZ}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	8.7	

### 11.2.3. $V_{CCA} = 1.5 \pm 0.1 \text{ V}$ , $V_{CCB} = 3.3 \pm 0.3 \text{ V}$ (Unless otherwise specified, $T_a = -40$ to $85 \text{ }^\circ\text{C}$ , Input: $t_r = t_f = 2.0 \text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	$t_{PLH}/t_{PHL}$		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	16.0	ns
3-state output enable time ( $\overline{OE} \rightarrow B1$ )	$t_{PZL}/t_{PZH}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	22.8	
3-state output disable time ( $\overline{OE} \rightarrow B1$ )	$t_{PLZ}/t_{PHZ}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	10.2	

### 11.2.4. $V_{CCA} = 1.2 \pm 0.1 \text{ V}$ , $V_{CCB} = 3.3 \pm 0.3 \text{ V}$ (Unless otherwise specified, $T_a = -40$ to $85 \text{ }^\circ\text{C}$ , Input: $t_r = t_f = 2.0 \text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	$t_{PLH}/t_{PHL}$		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	29	ns
3-state output enable time ( $\overline{OE} \rightarrow B1$ )	$t_{PZL}/t_{PZH}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	63	
3-state output disable time ( $\overline{OE} \rightarrow B1$ )	$t_{PLZ}/t_{PHZ}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	23	

### 11.2.5. $V_{CCA} = 1.8 \pm 0.15 \text{ V}$ , $V_{CCB} = 2.5 \pm 0.2 \text{ V}$ (Unless otherwise specified, $T_a = -40$ to $85 \text{ }^\circ\text{C}$ , Input: $t_r = t_f = 2.0 \text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	$t_{PLH}/t_{PHL}$		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	18.5	ns
3-state output enable time ( $\overline{OE} \rightarrow B1$ )	$t_{PZL}/t_{PZH}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	23.6	
3-state output disable time ( $\overline{OE} \rightarrow B1$ )	$t_{PLZ}/t_{PHZ}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	6.9	

### 11.2.6. $V_{CCA} = 1.5 \pm 0.1 \text{ V}$ , $V_{CCB} = 2.5 \pm 0.2 \text{ V}$ (Unless otherwise specified, $T_a = -40$ to $85 \text{ }^\circ\text{C}$ , Input: $t_r = t_f = 2.0 \text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	$t_{PLH}/t_{PHL}$		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	19.7	ns
3-state output enable time ( $\overline{OE} \rightarrow B1$ )	$t_{PZL}/t_{PZH}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	26.6	
3-state output disable time ( $\overline{OE} \rightarrow B1$ )	$t_{PLZ}/t_{PHZ}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	8.3	

### 11.2.7. $V_{CCA} = 1.2 \pm 0.1 \text{ V}$ , $V_{CCB} = 2.5 \pm 0.2 \text{ V}$ (Unless otherwise specified, $T_a = -40 \text{ to } 85 \text{ }^\circ\text{C}$ , Input: $t_r = t_f = 2.0 \text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	$t_{PLH}/t_{PHL}$		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	33	ns
3-state output enable time ( $\overline{OE} \rightarrow B1$ )	$t_{PZL}/t_{PZH}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	66	
3-state output disable time ( $\overline{OE} \rightarrow B1$ )	$t_{PLZ}/t_{PHZ}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	20	

### 11.2.8. $V_{CCA} = 1.2 \pm 0.1 \text{ V}$ , $V_{CCB} = 1.8 \pm 0.15 \text{ V}$ (Unless otherwise specified, $T_a = -40 \text{ to } 85 \text{ }^\circ\text{C}$ , Input: $t_r = t_f = 2.0 \text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	$t_{PLH}/t_{PHL}$		See Fig. 12.1, 13.1 Table 12.1.1, 12.1.2, 13.1.1	1.0	43	ns
3-state output enable time ( $\overline{OE} \rightarrow B1$ )	$t_{PZL}/t_{PZH}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	78	
3-state output disable time ( $\overline{OE} \rightarrow B1$ )	$t_{PLZ}/t_{PHZ}$		See Fig. 12.1, 13.2 Table 12.1.1, 12.1.2, 13.1.1	1.0	20	

### 11.3. Capacitive Characteristics (Unless otherwise specified, $T_a = 25 \text{ }^\circ\text{C}$ )

Characteristics	Symbol	Note	$V_{CCA} \text{ (V)}$	$V_{CCB} \text{ (V)}$	Typ.	Unit	
Input capacitance	$C_{IN}$		$\overline{OE}$ , A1	2.5	3.3	7	pF
Output capacitance	$C_{OUT}$		B1	2.5	3.3	8	pF
Power dissipation capacitance	$C_{PDA}$	(Note 1)	$\overline{OE} = \text{"L"}$	2.5	3.3	3	pF
		(Note 1)	$\overline{OE} = \text{"H"}$	2.5	3.3	0	
	$C_{PDB}$	(Note 1)	$\overline{OE} = \text{"L"}$	2.5	3.3	13	
		(Note 1)	$\overline{OE} = \text{"H"}$	2.5	3.3	0	

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2 \text{ (per bit)}$$

## 12. AC Test Circuit

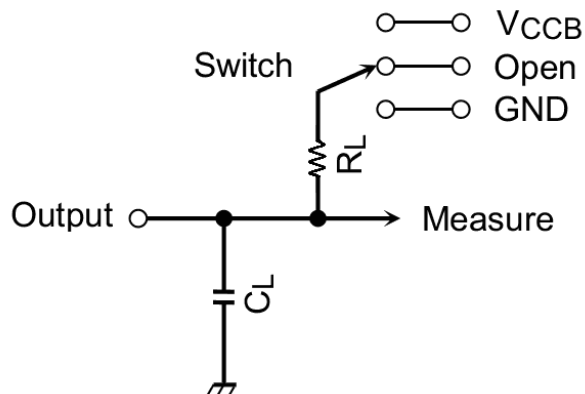


Fig. 12.1 AC Test Circuit

Table 12.1.1 Parameter for AC Test Circuit

Parameter	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PLZ}$ , $t_{PZL}$	$V_{CCB}$
$t_{PHZ}$ , $t_{PZH}$	GND

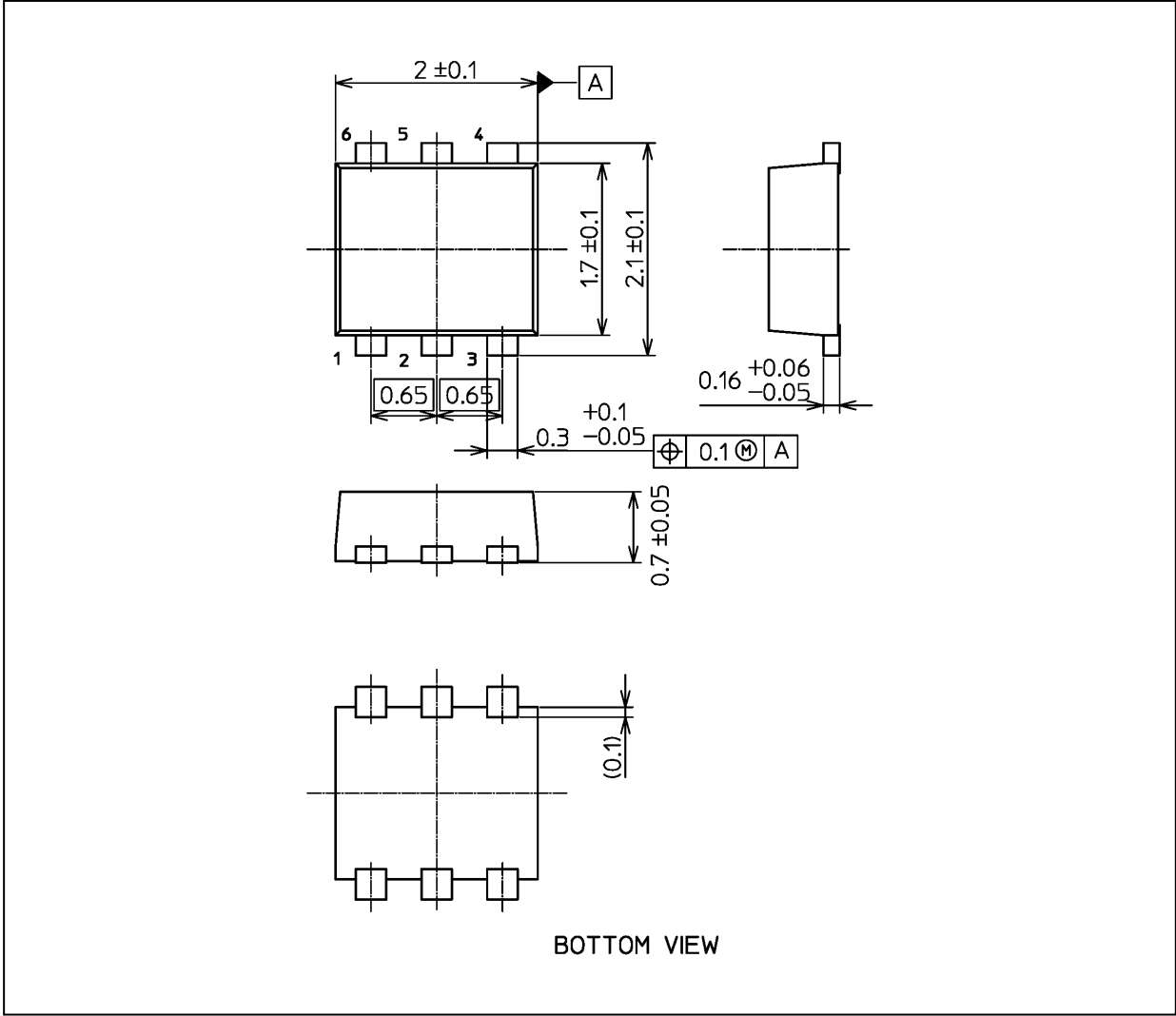
Table 12.1.2 Parameter for AC Test Circuit

Symbol	$V_{CCB} = 3.3 \pm 0.3 \text{ V}$ $V_{CCB} = 2.5 \pm 0.2 \text{ V}$	$V_{CCB} = 1.8 \pm 0.15 \text{ V}$
$R_L$	1 k $\Omega$	1 k $\Omega$
$C_L$	30 pF	30 pF



Package Dimensions

Unit: mm



Weight: 7.0 mg (typ.)

Package Name(s)
Nickname: UF6

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