

TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62781FNG

9-Channel Constant-Current LED Driver of the 3.3-V and 5-V Power Supply Voltage Operation

The TB62781FNG is a constant-current driver designed for LED and LED display lighting.

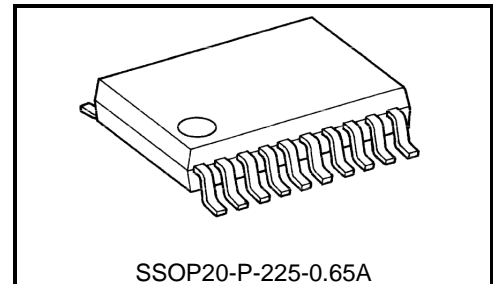
This product incorporates 7-bit PWM dimming controllers and 9 channels of constant-current drivers. 9 constant-current drivers are divided into three blocks, and each block can be independently adjusted by the relevant external resistor.

This IC is controlled using the SDA and SCLK input signals, and capable of high-speed data transfers.

This product can be set addresses with ID setting pins. (Up to 64 addresses can be controlled independently.)

High-speed transferring is capable by applying Bi-CMOS process.

This product operates with a supply voltage of 3.3 V or 5 V.



SSOP20-P-225-0.65A

Weight: 0.10 g (typ.)

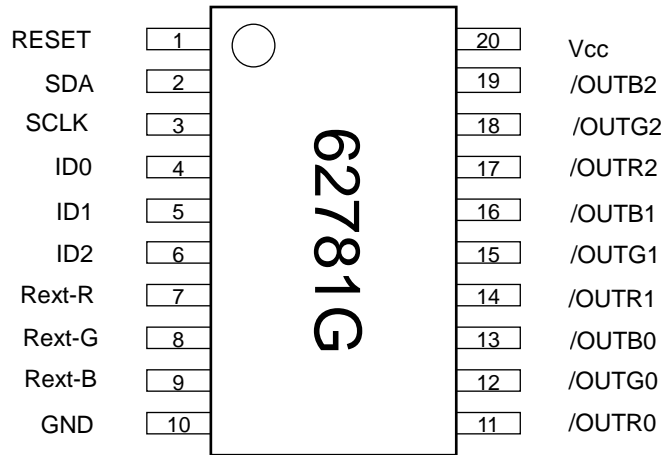
1. Features

- Power supply voltage: $V_{CC} = 3.3\text{ V}/5\text{ V}$
- Maximum output current capability: $80\text{ mA (max)} \times 9\text{ channels}$
- Constant-current characteristics setting range: 5 to 40 mA
- Output voltage at constant-current drive: 0.4 V (min, $I_{OUT} = 5\text{ to }40\text{ mA}$)
- Designed for common-anode LEDs
- The input interface is controlled by the SDA and SCLK signal lines
- Built-in thermal shutdown (TSD)
- Logical input and output: 3.3-V and 5-V CMOS interfaces (Schmitt trigger input)
- Maximum output voltage: 28 V
- Incorporating PWM control circuitry: Provides 7-bit PWM control.
- Driver identification: Up to 64 driver ICs can be controlled individually.
- Operating temperature range: $T_{opr} = -40\text{ to }85^\circ\text{C}$
- Package: SSOP20-P-225-0.65A

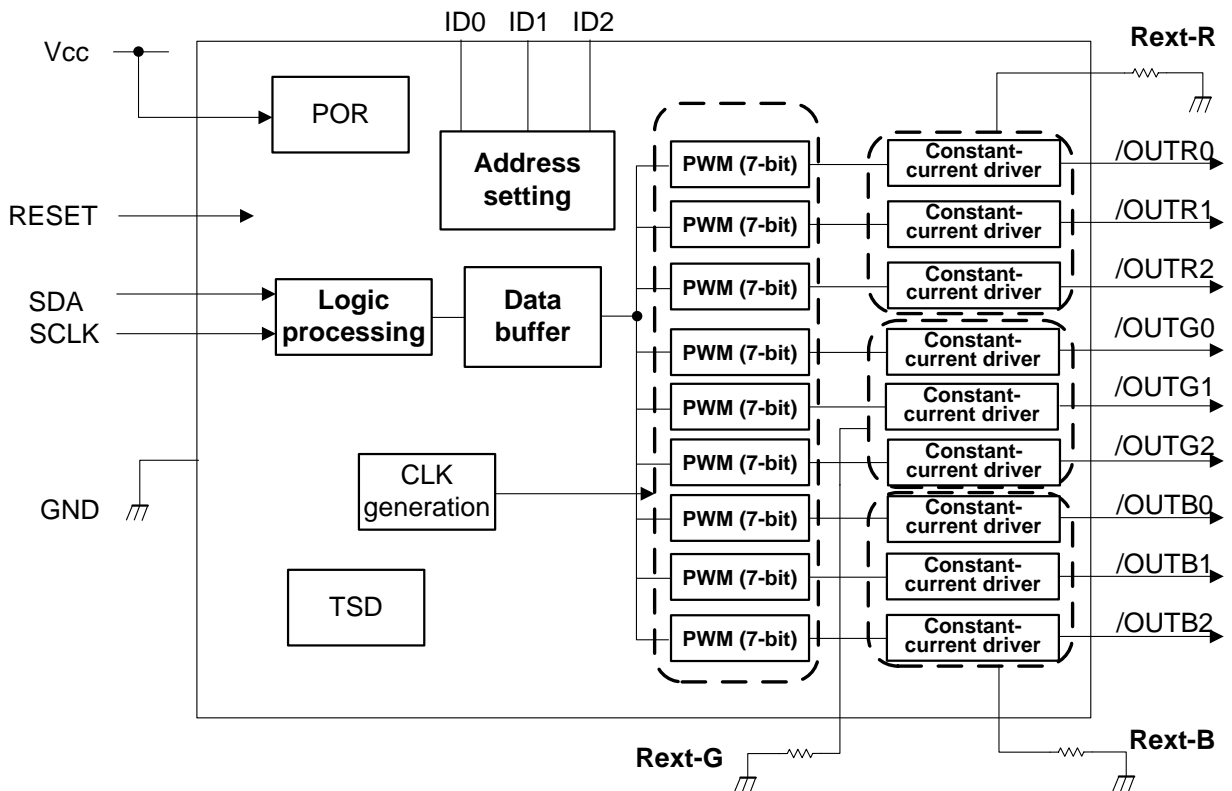
- Constant-current accuracy

Condition	Constant-current accuracy between channels	Constant-current accuracy between ICs
Output voltage: 0.4 V Output current: 15 mA	$\pm 3.0\%$	$\pm 6.0\%$

2. Pin Assignment (Top View)



3. Block Diagram



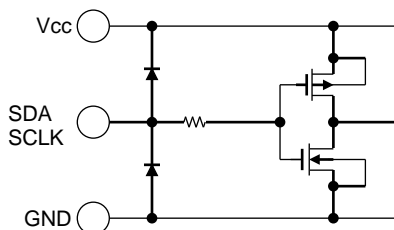
4. Pin Description

Pin Number	Symbol	Description
1	RESET	Reset signal input pin (Setting this pin High resets internal data.) (Note)
2	SDA	Serial data input pin
3	SCLK	Serial data transfer clock input pin
4	ID0	ID configuration pin (Note)
5	ID1	ID configuration pin (Note)
6	ID2	ID configuration pin (Note)
7	Rext-R	External resistor connection pin for output current configuration (/OUTR0, /OUTR1, /OUTR2)
8	Rext-G	External resistor connection pin for output current configuration (/OUTG0, /OUTG1, /OUTG2)
9	Rext-B	External resistor connection pin for output current configuration (/OUTB0, /OUTB1, /OUTB2)
10	GND	Ground pin
11	/OUTR0	Constant-current output pin (Open-collector type)
12	/OUTG0	Constant-current output pin (Open-collector type)
13	/OUTB0	Constant-current output pin (Open-collector type)
14	/OUTR1	Constant-current output pin (Open-collector type)
15	/OUTG1	Constant-current output pin (Open-collector type)
16	/OUTB1	Constant-current output pin (Open-collector type)
17	/OUTR2	Constant-current output pin (Open-collector type)
18	/OUTG2	Constant-current output pin (Open-collector type)
19	/OUTB2	Constant-current output pin (Open-collector type)
20	Vcc	Supply voltage input pin

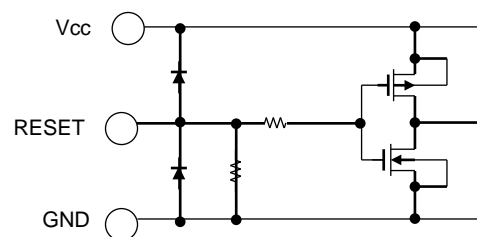
Note : After releasing the reset, make sure to perform the ID setting (Slave setting).

5. Equivalent Circuits for Inputs and Outputs

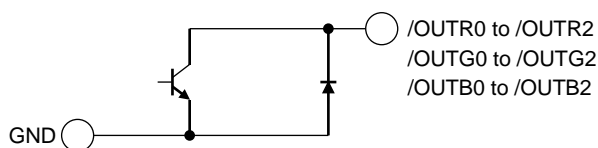
SDA pin (2pin),and SCLK pin (3pin)



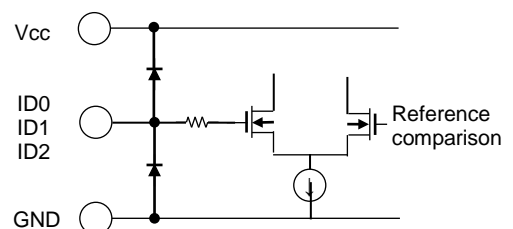
RESET pin (1pin)



Constant-current output pin (11pin to 19pin)



ID0, ID1, and ID2 pin



6. Programming the TB62781FNG

The TB62781FNG can be programmed by DATA (2pin, SDA) and CLK (3pin, SCLK) pins.

The TB62781FNG should be programmed using one of the following formats: (1) Serial Packet Format in Normal Programming Mode or (3) Serial Packet Format in Special Mode.

(1) Serial Packet Format in Normal programming Mode

<Typical>

Start command [11111111]	Slave address 8 bits	Sub address (channel selecting) 8 bits	Data byte (PWM configuration) 8 bits	Period command [10000001]
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(2) Data settings

a) Slave address

Input voltage and logic states of the ID0, ID1, and ID2 pins are determined as follows.

(MSB =0, and LSB (except of all selection) =0)

Vcc="11", 2/3Vcc="10", 1/3Vcc="01", GND="00"

Slave address	ID2	ID1	ID0
00000000	GND	GND	GND
00000010	GND	GND	1/3Vcc
00000100	GND	GND	2/3Vcc
00000110	GND	GND	Vcc
00001000	GND	1/3Vcc	GND
00001010	GND	1/3Vcc	1/3Vcc
00001100	GND	1/3Vcc	2/3Vcc
00001110	GND	1/3Vcc	Vcc
00010000	GND	2/3Vcc	GND
00010010	GND	2/3Vcc	1/3Vcc
00010100	GND	2/3Vcc	2/3Vcc
00010110	GND	2/3Vcc	Vcc
00011000	GND	Vcc	GND
00011010	GND	Vcc	1/3Vcc
00011100	GND	Vcc	2/3Vcc
00011110	GND	Vcc	Vcc
00100000	1/3Vcc	GND	GND
00100010	1/3Vcc	GND	1/3Vcc
00100100	1/3Vcc	GND	2/3Vcc
00100110	1/3Vcc	GND	Vcc
00101000	1/3Vcc	1/3Vcc	GND
00101010	1/3Vcc	1/3Vcc	1/3Vcc
00101100	1/3Vcc	1/3Vcc	2/3Vcc
00101110	1/3Vcc	1/3Vcc	Vcc
00110000	1/3Vcc	2/3Vcc	GND
00110010	1/3Vcc	2/3Vcc	1/3Vcc
00110100	1/3Vcc	2/3Vcc	2/3Vcc
00110110	1/3Vcc	2/3Vcc	Vcc
00111000	1/3Vcc	Vcc	GND
00111010	1/3Vcc	Vcc	1/3Vcc
00111100	1/3Vcc	Vcc	2/3Vcc
00111110	1/3Vcc	Vcc	Vcc
01000000	2/3Vcc	GND	GND
01000010	2/3Vcc	GND	1/3Vcc
01000100	2/3Vcc	GND	2/3Vcc
01000110	2/3Vcc	GND	Vcc
01001000	2/3Vcc	1/3Vcc	GND
01001010	2/3Vcc	1/3Vcc	1/3Vcc

01001100	2/3V _{cc}	1/3V _{cc}	2/3V _{cc}
01001110	2/3V _{cc}	1/3V _{cc}	V _{cc}
01010000	2/3V _{cc}	2/3V _{cc}	GND
01010010	2/3V _{cc}	2/3V _{cc}	1/3V _{cc}
01010100	2/3V _{cc}	2/3V _{cc}	2/3V _{cc}
01010110	2/3V _{cc}	2/3V _{cc}	V _{cc}
01011000	2/3V _{cc}	V _{cc}	GND
01011010	2/3V _{cc}	V _{cc}	1/3V _{cc}
01011100	2/3V _{cc}	V _{cc}	2/3V _{cc}
01011110	2/3V _{cc}	V _{cc}	V _{cc}
01100000	V _{cc}	GND	GND
01100010	V _{cc}	GND	1/3V _{cc}
01100100	V _{cc}	GND	2/3V _{cc}
01100110	V _{cc}	GND	V _{cc}
01101000	V _{cc}	1/3V _{cc}	GND
01101010	V _{cc}	1/3V _{cc}	1/3V _{cc}
01101100	V _{cc}	1/3V _{cc}	2/3V _{cc}
01101110	V _{cc}	1/3V _{cc}	V _{cc}
01110000	V _{cc}	2/3V _{cc}	GND
01110010	V _{cc}	2/3V _{cc}	1/3V _{cc}
01110100	V _{cc}	2/3V _{cc}	2/3V _{cc}
01110110	V _{cc}	2/3V _{cc}	V _{cc}
01111000	V _{cc}	V _{cc}	GND
01111010	V _{cc}	V _{cc}	1/3V _{cc}
01111100	V _{cc}	V _{cc}	2/3V _{cc}
01111110	V _{cc}	V _{cc}	V _{cc}
0XXXXX1	All selection		

b) Sub address

Output channel setting, All channels setting or Special mode setting can be set.

In output channel setting, a channel which defines PWM configuration is selected. In all channels setting, PWM is configured for all channels. In Special mode setting, it is set according to the description of page 6. (MSB and LSB must be set 0.)

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	Channel setting
0	0	0	0	0	0	1	0	/OUTR0
0	0	0	0	0	1	0	0	/OUTG0
0	0	0	0	0	1	1	0	/OUTB0
0	0	0	0	1	0	0	0	/OUTR1
0	0	0	0	1	0	1	0	/OUTG1
0	0	0	0	1	1	0	0	/OUTB1
0	0	0	0	1	1	1	0	/OUTR2
0	0	0	1	0	0	0	0	/OUTG2
0	0	0	1	0	0	1	0	/OUTB2
0	0	1	0	0	0	0	0	All channels selection
0	1	1	0	0	0	0	0	Special mode

c) Data bytes (PWM configuration)

Data bytes set PWM dimming. (LSB must be set 0.)

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	PWM dimming (reference)
0	0	0	0	0	0	0	0	0/127 (default)
0	0	0	0	0	0	1	0	1/127
0	0	0	0	0	1	0	0	2/127
								omitted
1	1	1	1	1	1	0	0	126/127
1	1	1	1	1	1	1	0	127/127

Note: Any data other than those specified above must not be programmed.

(3) Serial Packet Format in Special Mode

When data of 01100000 is input to the sub address, the operation moves to the special mode where all channels are selected in order. Data of 9 channels should be input.

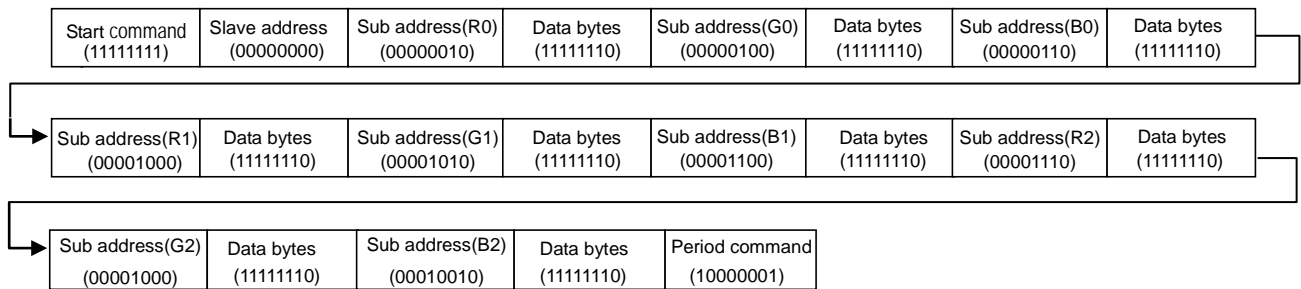
(If data of more than 9 channels are provided, the 10th and subsequent data are treated as invalid. If data of less than 9 channels are provided, those data are written to the channels in order and the remaining channels retain the previous data.)

To return to the normal mode, input data from the start command (all "H" 8 bits). In case of using this mode configuration, volume data can be omitted.

Start command [11111111]	Slave address	Sub address (Special mode setting) [01100000]	Data OUTR0	Data OUTG0	Data OUTB0	Data OUTR1	Data OUTG1	Data OUTB1	Data OUTR2	Data OUTG2	Data OUTB2	Period command [10000001]
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(4) Input example of data setting

a) In case PWM 127 /127 (100% ON) are configured to all channels of slave address 00h.

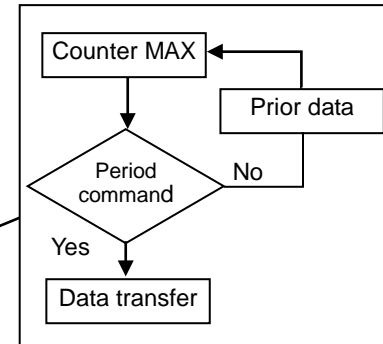
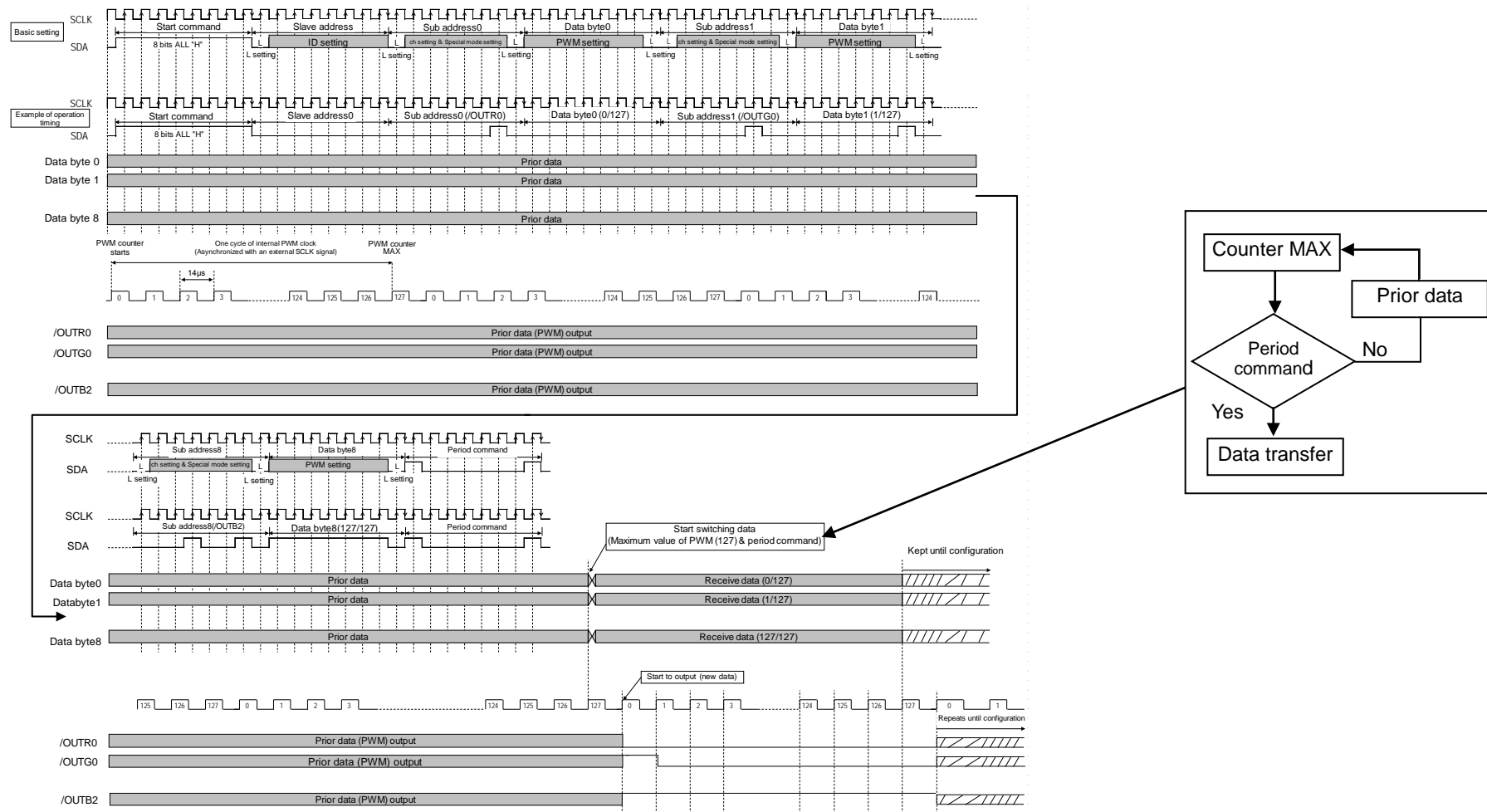


b) In case PWM 127 /127 (100% ON) are configured to only /OUTR0 pin and /OUTB2 pin of slave address 02h.

Start command (11111111)	Slave address (00000010)	Sub address(R0) (00000010)	Data bytes (11111110)	Sub address(B2) (00010010)	Data bytes (11111110)	Period command (10000001)
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Output pins other than /OUTR0 and /OUTB2 pins in the above configuration, which have already completed data setting, continue to output prior data. (In case of changing only outputting data which is required to be changed, this configuration is valid.)

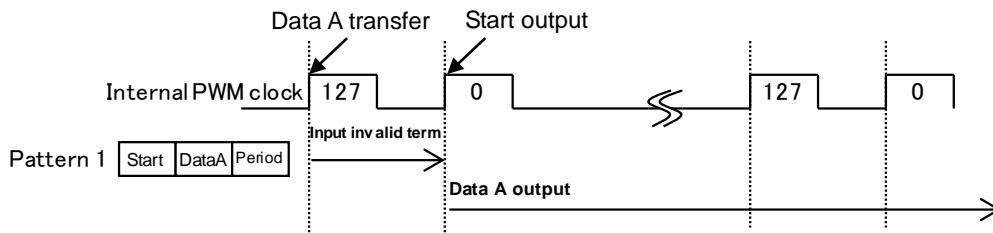
(5) Data settings and timing of outputs



Note: Data are transferred by synchronizing the period command (10000001) with the internal PWM counter (max). Therefore, after input the period command, when data are input before the internal counter value is maximum, the input data after the period command input are not accepted. In order to set data to the same ID (IC), next data should be input after input of the period command and elapsing 3 ms (128 internal PWM clocks). However, if data are set to the different ID, the interval of 3 ms (128 internal PWM clocks) is unnecessary.

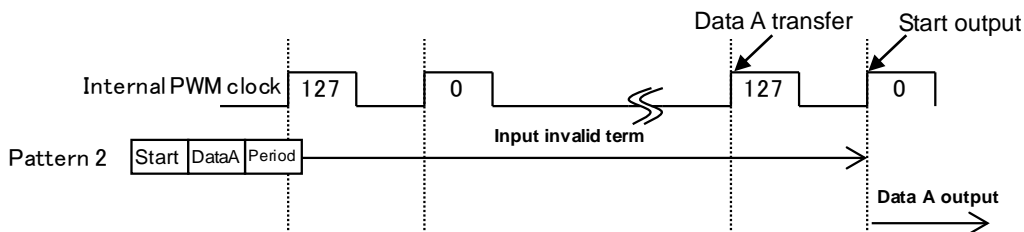
(6) Example of data input to the same ID

a) When data A is input up to the rising edge of 127th internal PWM clock



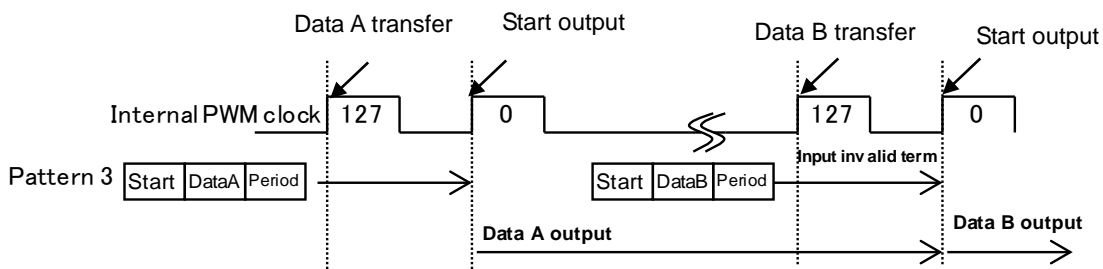
Data A output starts at the rising edge of 0th internal PWM clock.
 The input is invalid from the rising edge of 127th internal PWM clock to the rising edge of 0th internal PWM clocks which is just after these 127th PWM clock.

b) When data A is input after the rising edge of 127th internal PWM clock



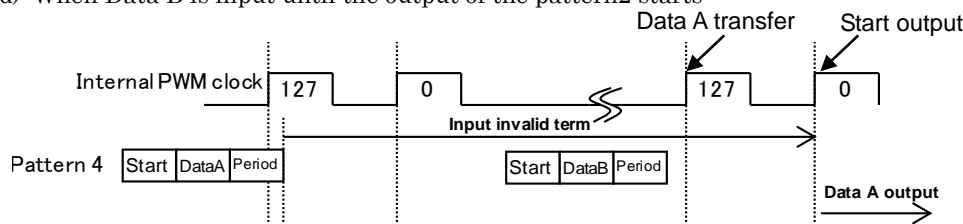
Data A output does not start at the rising edge of 0th internal PWM clock just after inputting data A. Data A starts to output at the next rising edge of 0th internal PWM clock.
 Inputting is invalid from the data A (period) input to the rising edge of after the next 0th internal PWM clocks.

c) When data B is input after starting output of pattern 1



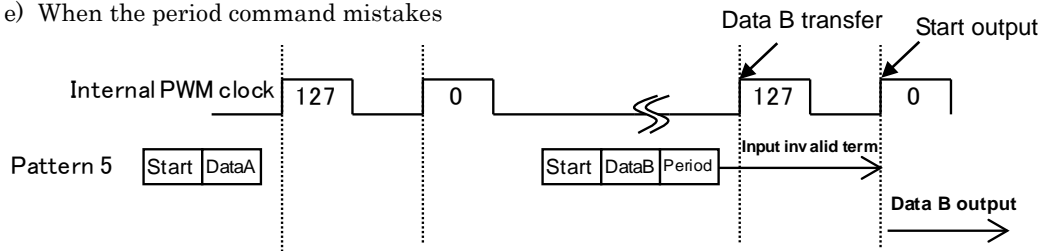
Data A output starts at the rising edge of 0th internal PWM clock just after the data A is input.
 Data B output starts at the next rising edge of 0th internal PWM clock which is just after the data B input.
 Inputting is invalid in the following term.
 From the rising edge of 127th internal PWM clock which is just after the Data A is input to the rising edge of 0th internal PWM clock which is just after this 127th clock.
 From the rising edge of 127th internal PWM clock which is just after the Data B input to the rising edge of 0th internal PWM clock which is just after this 127th clock.
 Pay attention that the IC does not operate according to the configuration while the following patterns (patterns 4 and 5) are input.

d) When Data B is input until the output of the pattern2 starts



Inputting is invalid from the data A (period) input to the rising edge of the second internal clock. So, data B is invalid and data A is output.

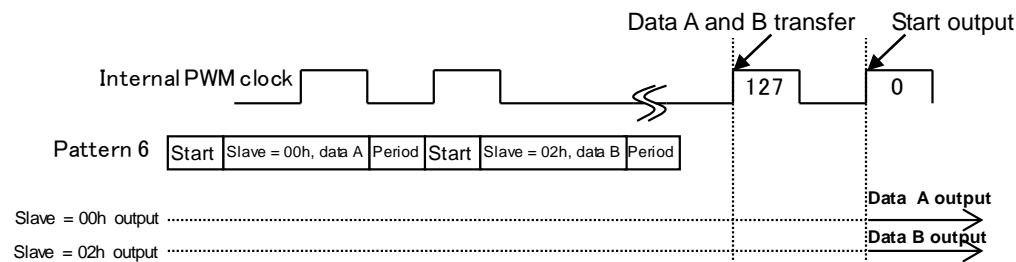
e) When the period command mistakes



Data A output does not start at the rising edge of 0th internal clock which is just after the data A input. Data B output starts at the next rising edge of 0th internal PWM clock which is just after the data B input.

(7) Example of data input to the different ID

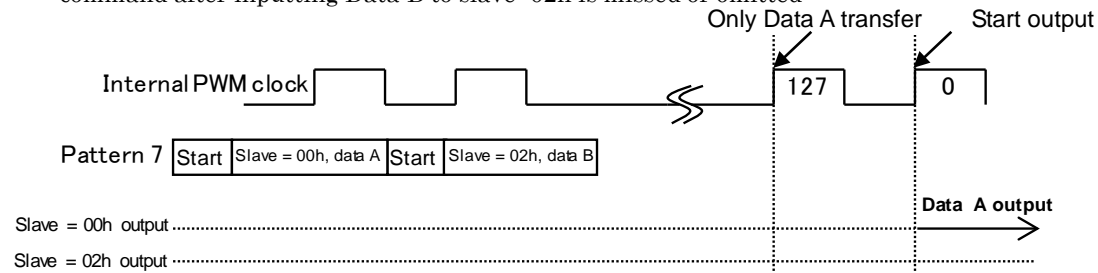
a) When Data B is input to Slave=02h just after Data A is input to Slave=00h



Both Data A and Data B are output at the rising edge of 0th PWM clock just after inputting Data A and Data B.

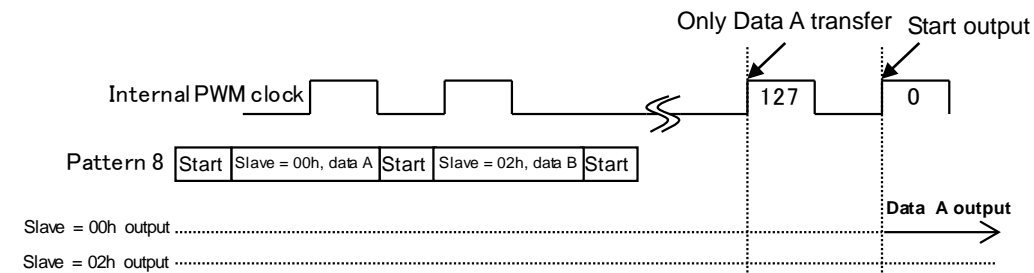
Pay attention that the IC does not operate according to the configuration while following patterns (pattern 7 and 8) are input.

b) When the period command after inputting Data A to slave=00h is missed or omitted, or when the period command after inputting Data B to slave=02h is missed or omitted



Data A is output. However, Data B is not output.

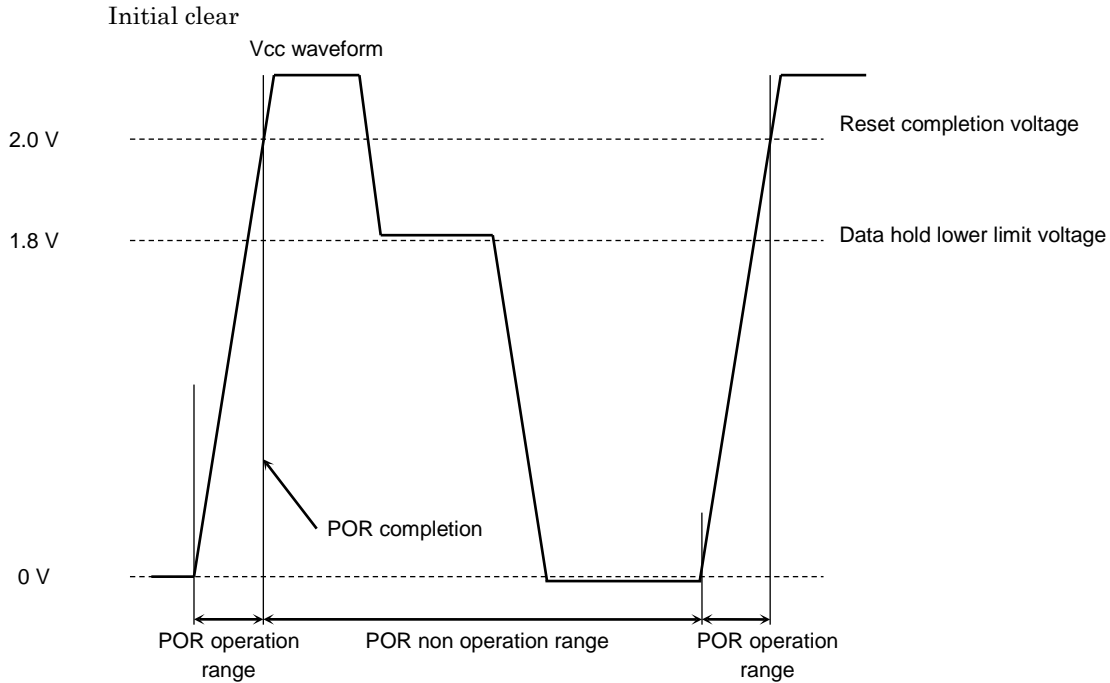
c) When the start command is input after inputting Data B of Pattern7



Data A is output. However, Data B is not output.

7. Power-On Reset (POR)

This function works for preventing malfunction by resetting all IC internal data and returning default settings at power-on. The POR circuit operates only when Vcc rises from 0 V. To re-activated POR, Vcc should be set to 0 V. The internal hold voltage is ensured after Vcc reaches 3.0 V or more.



8. Thermal Shutdown (TSD)

When the IC internal temperature reaches 150°C, the thermal shutdown circuit operates and all constant current outputs are turned off. When the temperature falls, the constant current outputs restart.

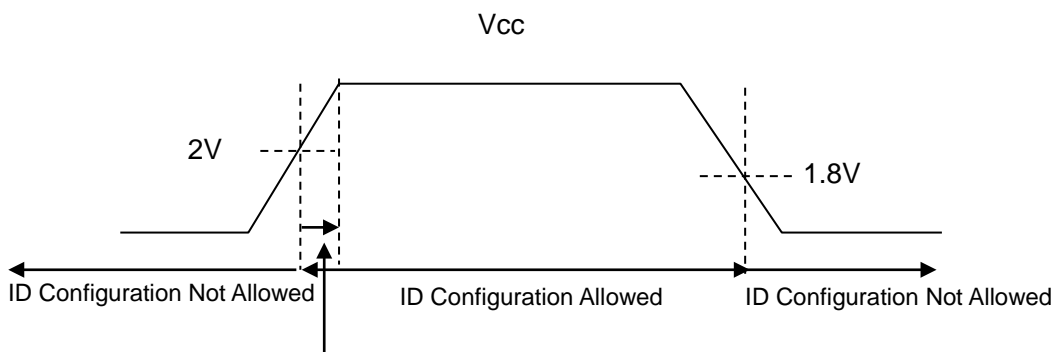
TSD operating temperature: 150°C to 180°C

TSD release temperature: 30°C below TSD operating temperature

*Please avoid positively using TSD because TSD is a detecting function of the product.

9. Precautions on Setting

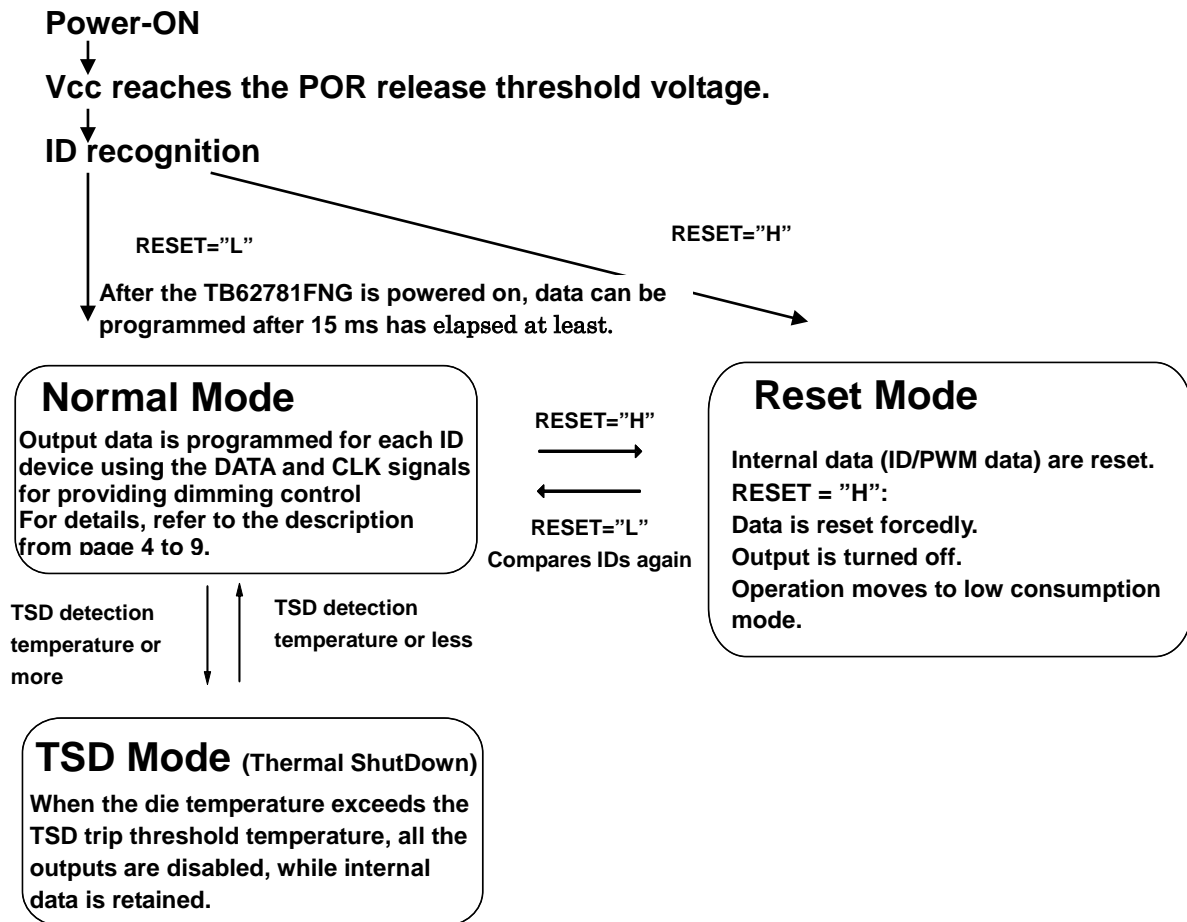
1. External resistors for specifying the LED driving current (Rext-R, Rext-G, and Rext-B)
External resistors should be separately connected to the Rext-R, Rext-G and Rext-B pins. Three resistors must not be collected as one resistor. If they are collected, current error is generated in each RGB.
2. External resistors for ID configuration
The total resistance value of three external resistors used for specifying a device ID (which are connected between Vcc and GND) should be about 30 kΩ or lower.
3. ID configuration sequence
ID configuration can be performed after POR is released upon powering on. However, to avoid false operation of the ID configuration, transient input signals of less than two clock cycles of the reference clock for the internal oscillator are not accepted.



Care should be taken during the period between the POR released timing and the timing when power supply has reached the rated Vcc voltage.

4. ID configuration
Make sure to set IDs after releasing reset condition.
5. Data configuration
Do not input the data which is not on the list of the data configuration table in page 4 and 5.
6. Special mode
Data which corresponds to 9 channels should be input. If data of more than 9 channels are provided, the 10th and subsequent data are treated as invalid. If data of less than 9 channels are provided, those data are written to the channels in order and the remaining channels retain the previous data.
7. Timing of data configuration
In order to set data to the same slave address, next data should be input after 3ms which corresponds to 128 internal PWM clocks is passed since the period command is input. However, in order to set data to the different slave address, terminal of 3 ms which corresponds to 128 internal PWM clocks should not be taken.

10. State Transition Diagram



11. Absolute Maximum Rating (Ta= 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	6.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3 (Note1)	V
Output current	I _{OUT}	85	mA/ch
Output voltage	V _{OUT}	-0.3 to 29	V
Power dissipation	P _d	1.02 (Note2,3)	W
Saturation thermal resistance	R _{th(j-a)}	122 (Note2)	°C/W
Operating temperature range	T _{opr}	-40 to 85	°C
Storage temperature range	T _{stg}	-55 to 150	°C
Maximum junction temperature	T _j	150	°C

Note 1: Do not exceed 6.0 V.

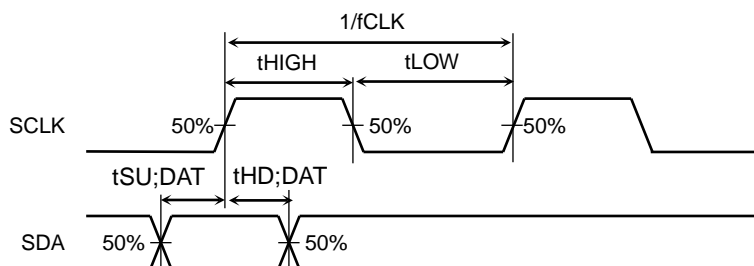
Note 2: When mounted on a PCB (76.2 × 114.3 × 1.6 mm; Cu = 30%; 35-μm thickness; SEMI-compliant)

Note 3: Power dissipation is the value obtained by subtracting the reciprocal (1/R_{th(j-a)}) of the saturated thermal resistance value every time the ambient temperature exceeds 25°C by 1°C.

12. Operating Condition (Ta= -40 to 85°C, Unless Otherwise Specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply voltage	V _{CC}	—	3	—	5.5	V
Output voltage	V _{OUT(ON)}	All outputs	0.4	—	4	V
Constant output current	I _{OUT}	All outputs	5	—	40	mA/ch
Input voltage	V _{IH}	SDA, SCLK, and RESET	0.7 × V _{CC}	—	V _{CC}	V
	V _{IL}		GND	—	0.3 × V _{CC}	
	V _{ID0}	ID0, ID1, and ID2	0	—	0.3	
	V _{ID1}		1/3V _{CC} -0.3	1/3 V _{CC}	1/3V _{CC} +0.3	
	V _{ID2}		2/3V _{CC} -0.3	2/3 V _{CC}	2/3V _{CC} +0.3	
	V _{ID3}		V _{CC} -0.3	—	V _{CC}	
SCLK clock frequency	f _{CLK}	SCLK Note 4	—	—	10	MHz
Data setup time	t _{SU;DAT}	SDA-SCLK (Note 4)	10	—	—	ns
Data hold time	t _{HD;DAT}	SCLK-SDA (Note 4)	10	—	—	
"L" term of SCLK clock	t _{LOW}	SCLK (Note 4)	50	—	—	
"H" term of SCLK clock	t _{HIGH}	SCLK (Note 4)	50	—	—	

Note 4: Please refer to the following timing chart.

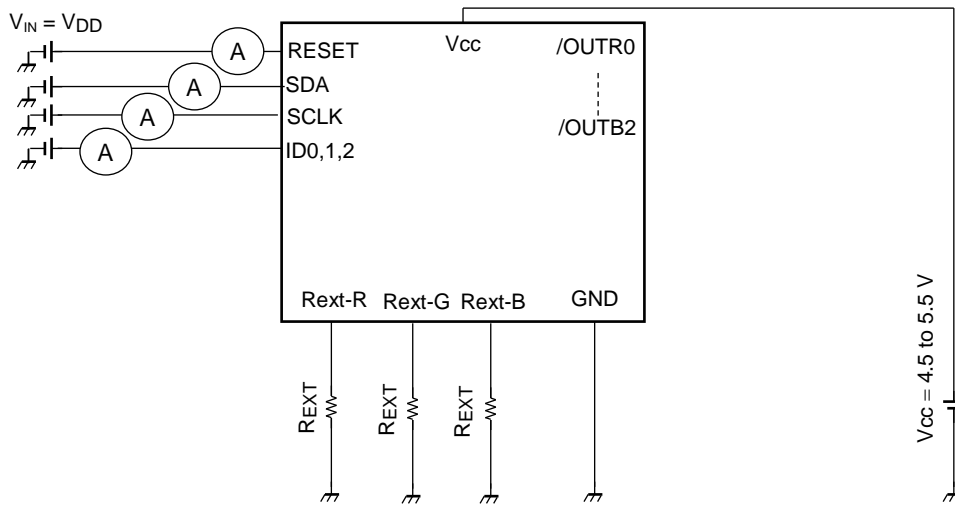


13. Electrical Characteristics (Ta= 25°C, Vcc=4.5 to 5.5V, Unless Otherwise Specified)

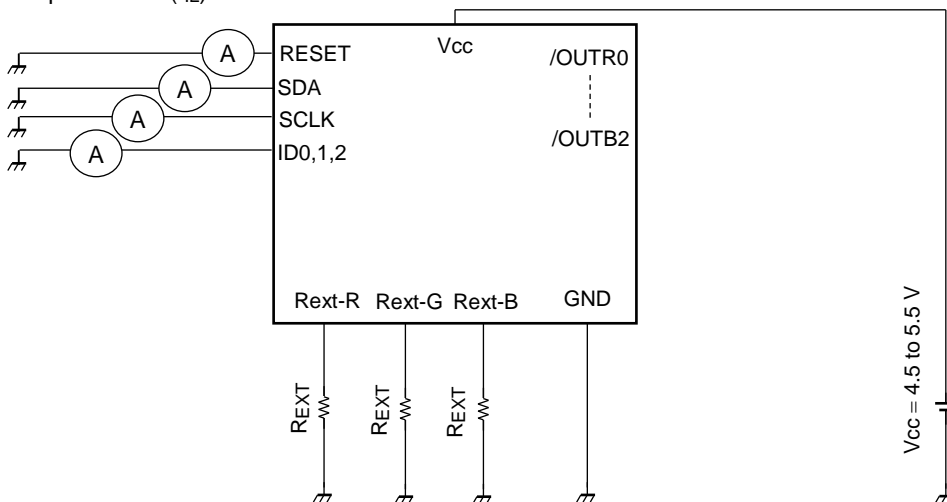
Characteristics	Symbol	Test circuit	Test condition	Min	Typ.	Max	Unit
Output current	I _{OUT1}	4	V _{OUT} = 0.4 V, R _{EXT} = 1.2 kΩ V _{CC} = 5 V,	12.69	13.5	14.31	mA
Output current accuracy between channels	ΔI _{OUT2}	4	V _{OUT} = 0.4 V, R _{EXT} = 1.2 kΩ All channels ON, V _{CC} = 5 V	—	—	±3.0	%
Output leakage current	I _{OZ}	4	V _{OUT} = 28 V	—	—	1	μA
Input current	I _{IH}	1	SDA and SCLK,	—	—	1	μA
			RESET(V _{CC} =5V)	25	50	75	
	I _{IL}	2	SDA, SCLK, and RESET	—	—	-1	
	I _{ID}	1, 2	ID0, ID1, and ID2	—	—	±0.1	
Output current dependent on V _{CC}	%V _{CC}	4	V _{CC} = 4.5 V to 5.5 V changing	—	1	2	%
Supply current at operating	I _{CC 1}	3	R _{EXT} = 1.2 kΩ, V _{OUT} = 0.4 V, RESET= L	—	8	12	mA
Current consumption in Reset mode	I _{CC (PS)}	3	R _{EXT} = 1.2kΩ, V _{OUT} = 0.4 V, RESET= H (The input current of the RESET pin is excluded.)	—	—	1	μA
Time required for a mode transition from Reset mode to Normal mode	t _{ON2}	—	Time between a High to Low transition on RESET and the timing when an output current is generated after input data is applied.	—	—	3	ms
Output rising time	T _{or}	5	Voltage waveform 10 to 90%	—	20	150	ns
Output falling time	T _{of}	5	Voltage waveform 90 to 10%	—	125	300	ns

14. Test Circuit

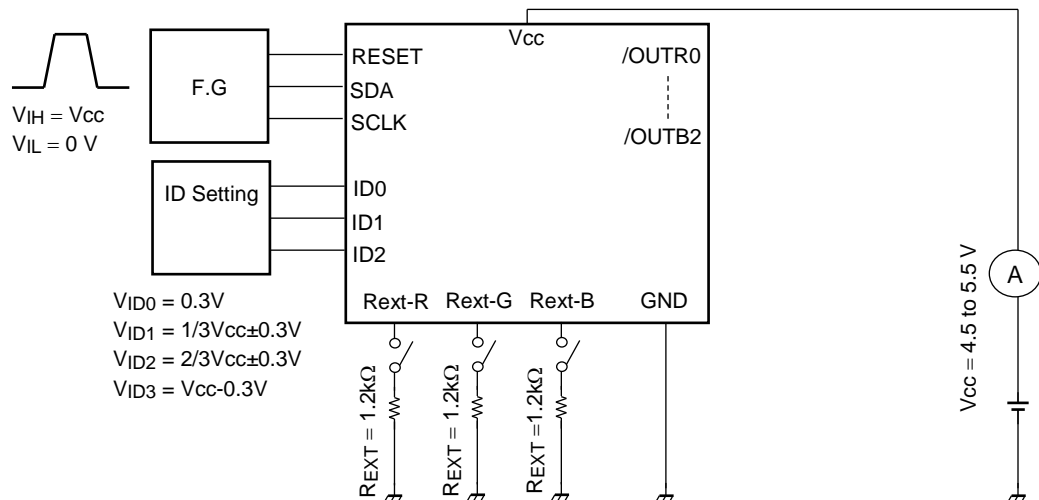
Test circuit 1: Input current (I_{IH})



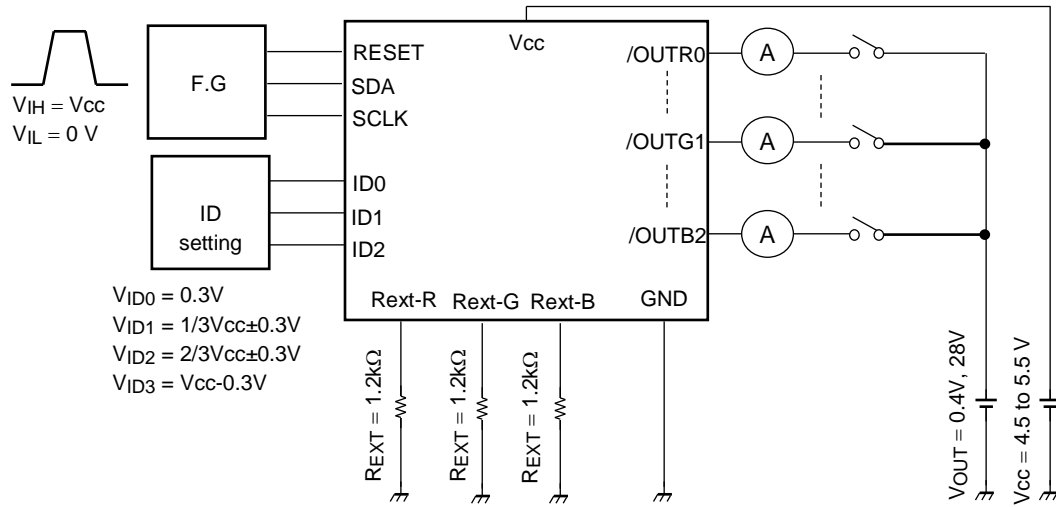
Test circuit 2: Input current (I_{IL})



Test circuit 3: Supply current

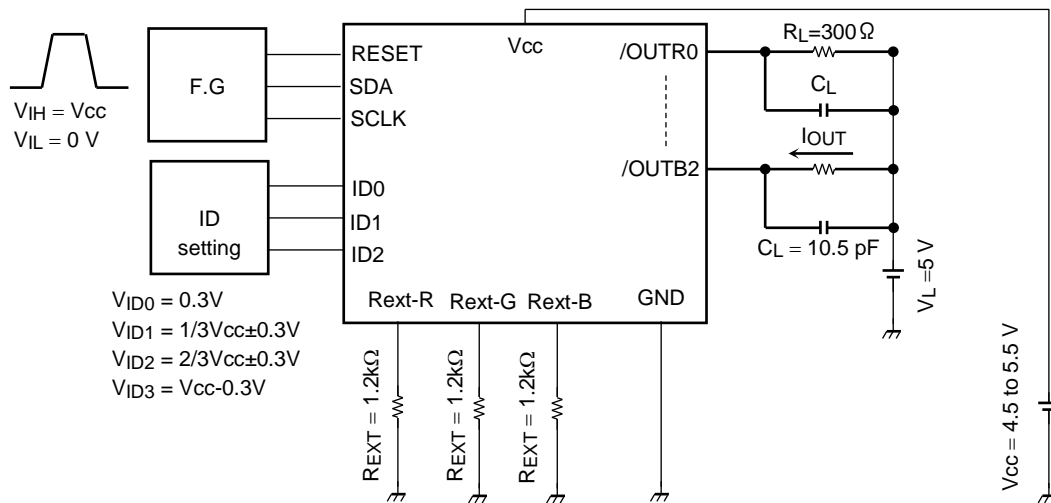


Test circuit 4: Output current / output leak current / output current accuracy / output current dependent on Vcc



Constant current output theory formula = $1.12V \div R_{EXT} \times 14.5$

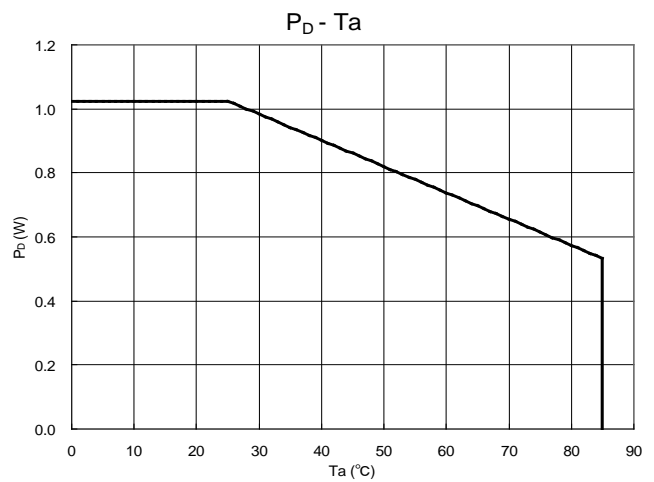
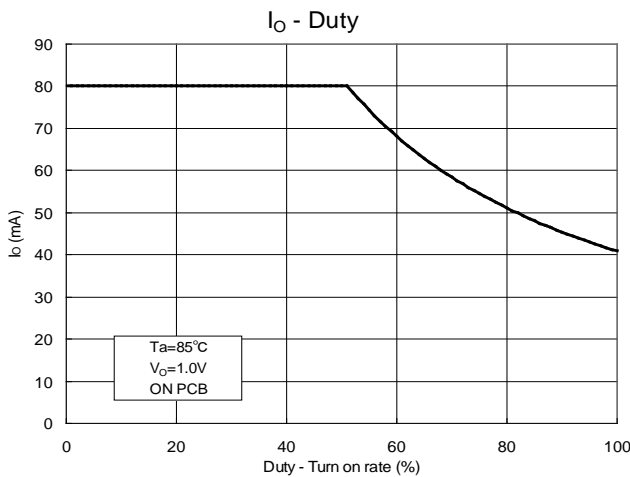
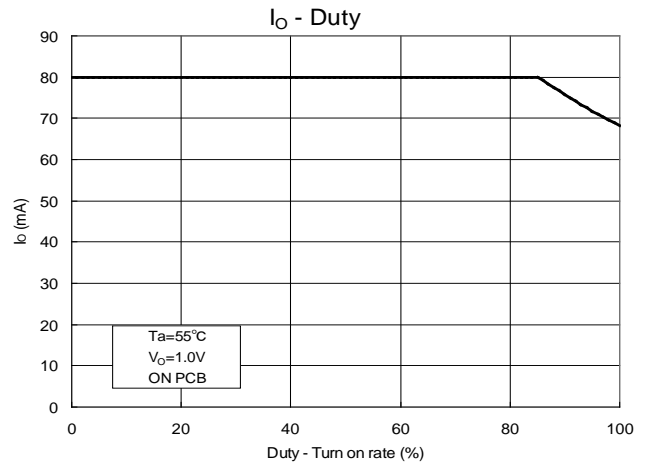
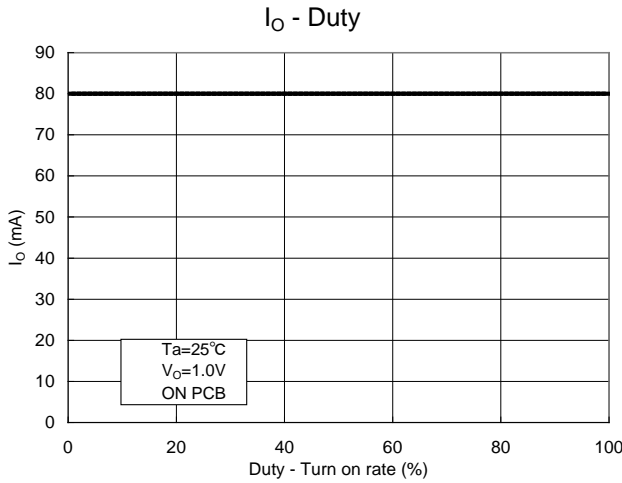
Test circuit 5: Switching characteristics



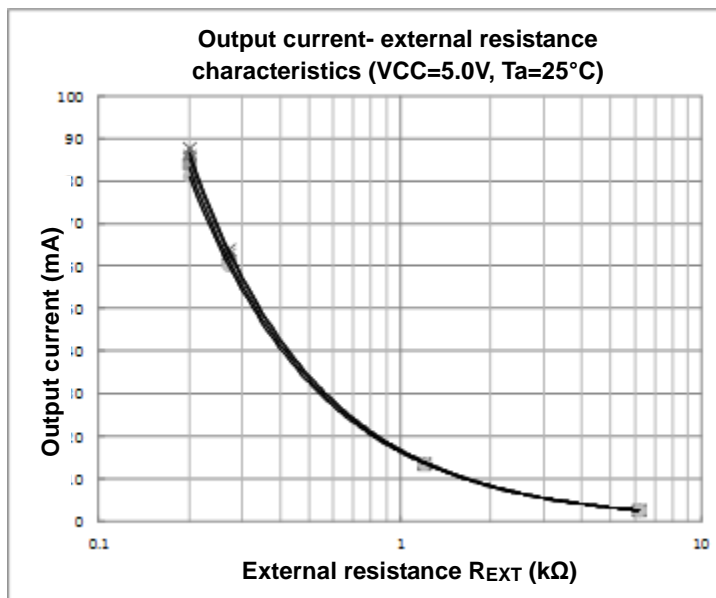
15. Graphs between Output Current and Derating (Lighting Rate)

Board condition: 76.2×114.3×1.6 mm, Cu=30%, 35-μm thickness, SEMI compliant

When the pulse width is 25 ms or more, it is assumed to be DC.



Output current- external resistance characteristics (reference)



(Reference) TB62781FNG IO_{UT} calculation

The typical relational expression of the output-current and external resistor is shown below.

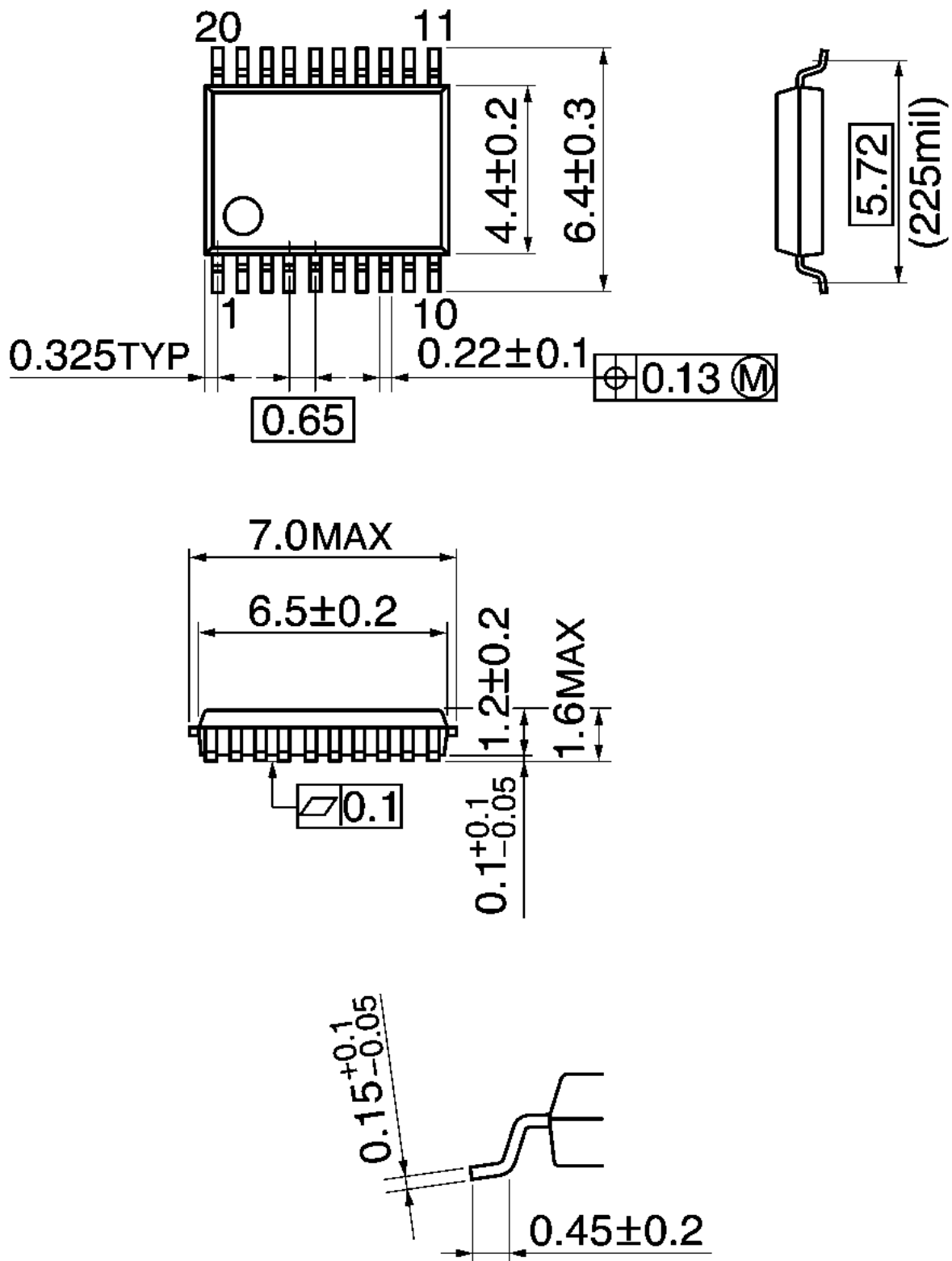
It does not include a current accuracy.

$$\text{Output current (mA)} = 14.5 \times 1.12(\text{V}) \div R_{\text{EXT}} (\text{k}\Omega)$$

17. Package Dimensions

SSOP20-P-225-0.65A

Unit: mm



Weight: 0.10 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

Providing these application circuit examples does not grant a license for industrial property rights.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

- [1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- [2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- [3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- [4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- [5] Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flows back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(3) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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