TB62781FNG / TB62D612FTG / TB62D786FTG / TB62D787FTG
Usage considerations

Summary

TB62781FNG and TB62D612FTG are constant current RGB-LED drivers using 2-wire BUS with a rating of 3.3 V to 5 V.
TB62D786FTG and TB62D787FTG are constant current RGB-LED drivers using a single-wire BUS with a rating of 5 V.
TB62781FNG and TB62D786FTG control three RGB-LEDs by 9 channel constant current outputs.
TB62D612FTG and TB62D787FTG control eight RGB-LEDs by 24 channel constant current outputs.
As for above products, 7-bit PWM control for each channel and configurations of 64 IDs are possible.
TB62D786FTG and TB62D787FTG can operate with the main power supply (7 V to 28 V) by using the internal 5 V regulator.

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Table Contents

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1. Product Comparison (TB62781FNG, TB62D612FTG, TB62D786FTG, and TB62D787FTG)

Main specification of each product is shown in the table 1-1.

Table 1-1 Product comparison

Item	TB62781FNG	TB62D612FTG	TB62D786FTG	TB62D787FTG
Process	BiCD0.6	BiCD0.13	BiCD0.13	BiCD0.13
Interface	2-wire SPI BUS	2-wire SPI BUS	Single-wire BUS	Single-wire BUS
Linear regulator supply voltage	—	—	7.0 to 28 V	7.0 to 28 V
Vcc supply voltage	3.0 to 5.5 V	3.0 to 5.5 V	4.5 to 5.5 V	4.5 to 5.5 V
LED anode supply voltage	28 V	28 V	28 V	28 V
Recommend output current	5 to 40 mA	5 to 40 mA	5 to 40 mA	5 to 40 mA
Number of channels	9 channels	24 channels	9 channels	24 channels
PWM control range	7 bits	7 bits	7 bits	7 bits
Number of IDs (Slave address)	0 to 63	0 to 63	0 to 63	0 to 63
Package	20-pin SSOP	36-pin WQFN	24-pin VQFN	40-pin VQFN

1.1. Block diagram and application circuit examples

Constant current LED drivers with 9 channels or 24 channels controlled by 2-wire inputs (TB62781FNG / TB62D612FTG)

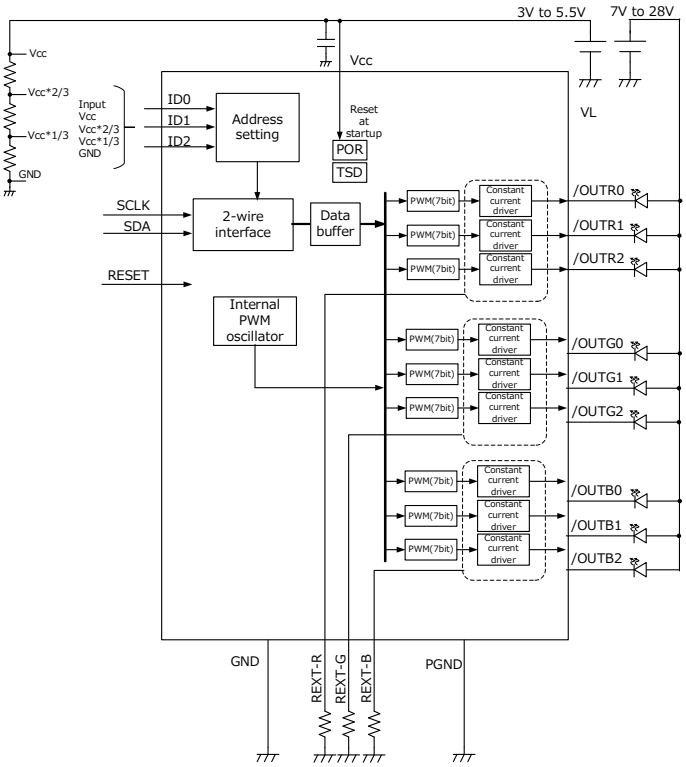


Figure 1.1 Application circuit example (TB62781FNG)

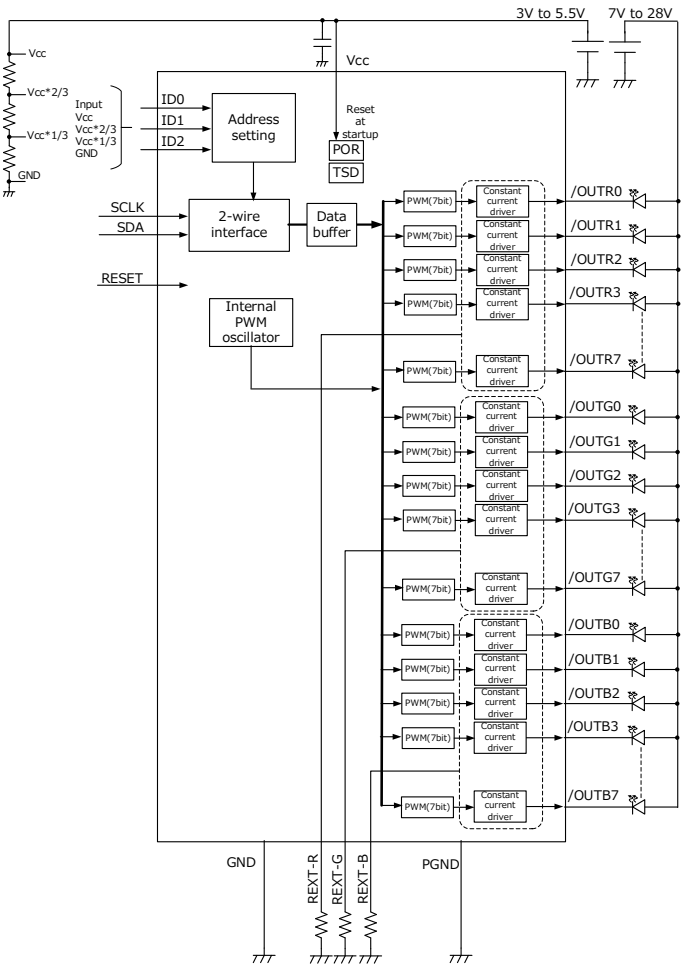


Figure 1.2 Application circuit example (TB62D612FTG)

Constant current LED drivers with 9 channels or 24 channels controlled by single-wire inputs (TB62D786FNG / TB62D787FTG)

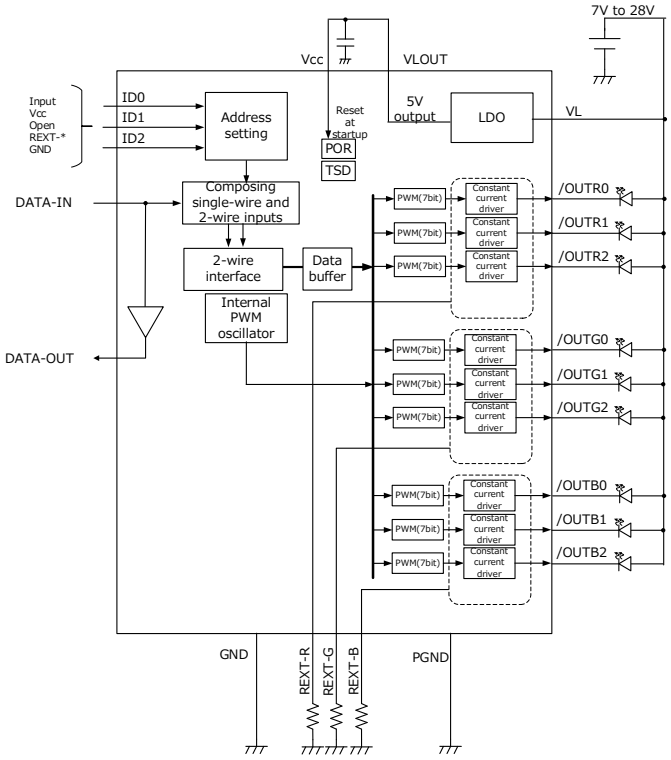


Figure 1.3 Application circuit example (TB62D786FTG)

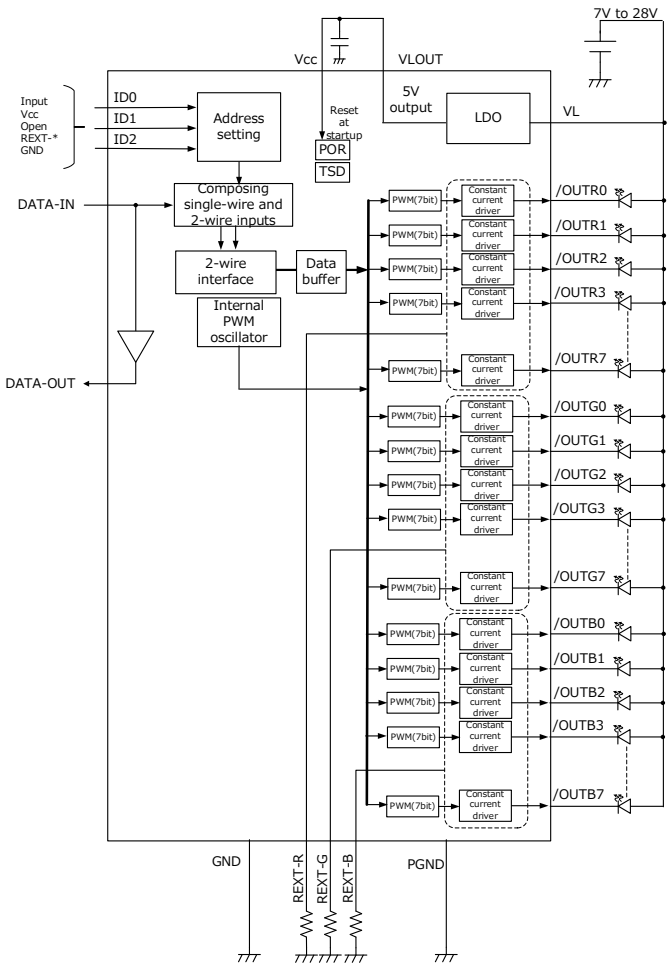


Figure 1.4 Application circuit example (TB62D787FTG)

2. Power Supply Voltage

2.1. Operation range of power supply voltage

Table 2-1 Operation range of power supply voltage (TB62781FNG and TB62D612FTG)

Item	Symbol	Operation range	Absolute maximum ratings	Unit	Note
Supply voltage	Vcc	3.0 to 5.5	6.0	V	Vcc pin

Table 2-2 Operation range of power supply voltage (TB62D786FTG and TB62D787FTG)

Item	Symbol	Operation range	Absolute maximum ratings	Unit	Note
VL pin supply voltage	VL	7.0 to 28	29	V	VL pin VLOUT pin outputs 5 V
Vcc pin supply voltage	Vcc	4.5 to 5.5	6.0	V	Vcc pin Connect to VLOUT pin

Connection of power supply:
TB62D786FTG and TB62D787FTG has a 5 V regulator (VL pin is for input and VLOUT pin is for output.)
VL pin can be used as a main power supply by connecting VLOUT pin and Vcc pin.

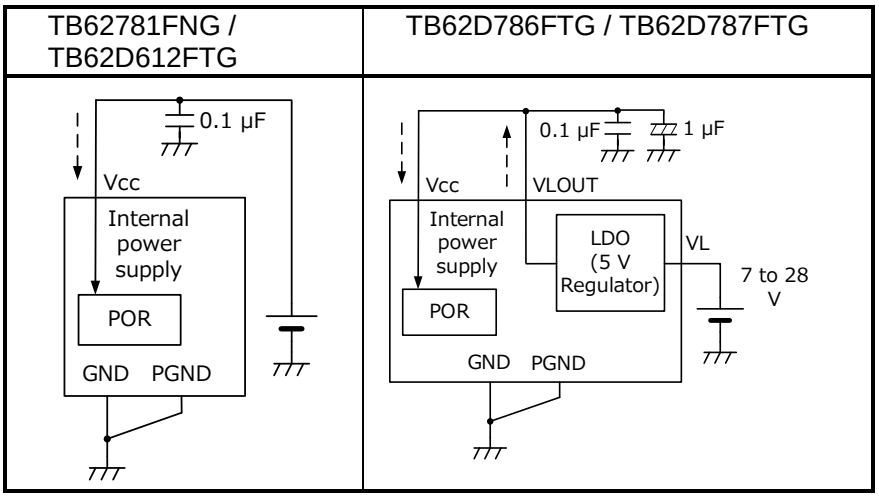


Figure 2-1 Connection of power supply

2.2. Capacitor for power supply pin

Connect the capacitor as close as possible to the IC.

Table 2-3 Recommendation values (capacitor for power supply pin)

Item	Recommendation value	Remarks
Between Vcc pin and GND	≥ 0.1 µF	Ceramic capacitor
Between VLOUT pin and GND	≥ 0.1 µF	Ceramic capacitor
	≥ 1 µF	Electrolytic capacitor

2.3. 5 V regulator input (VL pin) and output (VLOUT pin)

The internal 5 V regulator of TB62D786FTG and TB62D787FTG outputs voltage from VLOUT pin when VL pin voltage exceeds 5 V. Then, the voltage becomes stable when VL pin voltage is 7 V or more.
The charge time (T) for the capacitor (1.0 µF) between VLOUT pin and GND is approximately 0.5 ms.

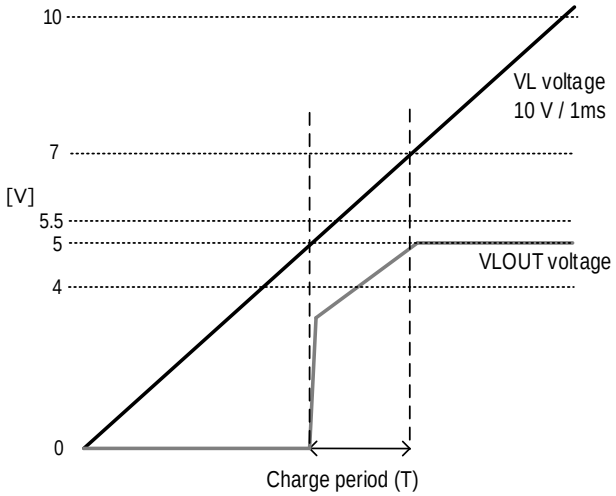


Figure 2-2 VL pin voltage and VOUT pin voltage (TB62D786FTG and TB62D787FTG)

2.4. Power on reset circuit (POR)

Power on reset function (POR) monitors Vcc pin, and reset at startup.
Start DATA input after Vcc voltage reaches the operation threshold. The same procedure should be taken when connecting VLOUT pin and Vcc pin.

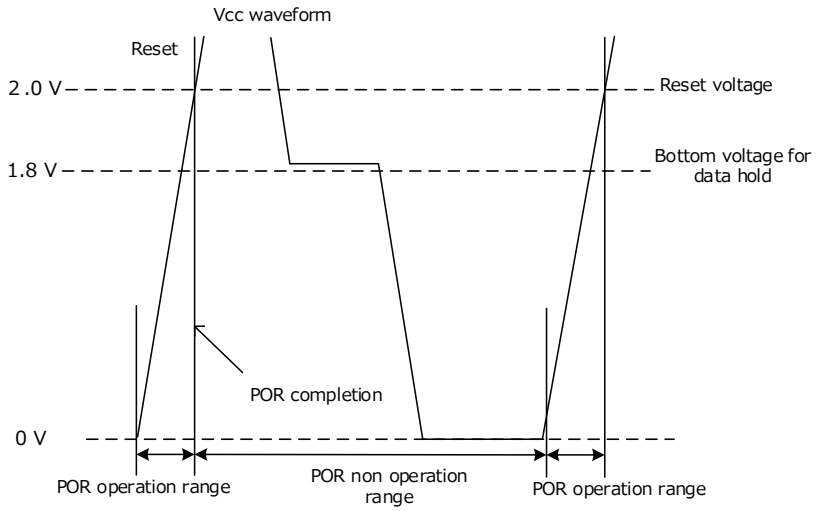


Figure 2-3 Power on reset circuit (POR)

2.5. Setting of DATA input pin in power on and shutdown

Data input setting in Vcc power on is shown in the table 2-4.
In case of TB62781FNG, TB62D612FTG, or TB62D786FTG that has the protection diode between the DATA input pin and Vcc pin, the low level is set in power on and then DATA input starts after Vcc voltage reaches the operation threshold (Shown in the figure 2-4).
Shutdown the power after the data input pin is set to low level.
TB62D787FTG has the tolerance input.

Table 2-4 Data input pin

Product name	Communication voltage system	Power supply input	Data input pin
TB62781FNG / TB62D612FTG	3.3 V to 5 V CMOS	Low	SDA, SCLK
TB62D786FTG	5 V CMOS		DATA-IN
TB62D787FTG		Low / High	

Note: Low: 0.3×Vcc, High: 0.7×Vcc

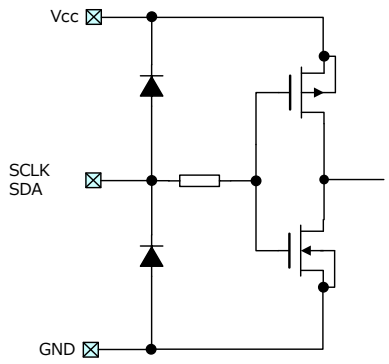
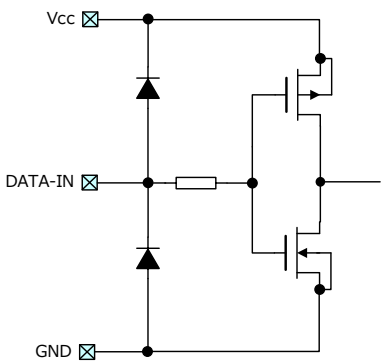
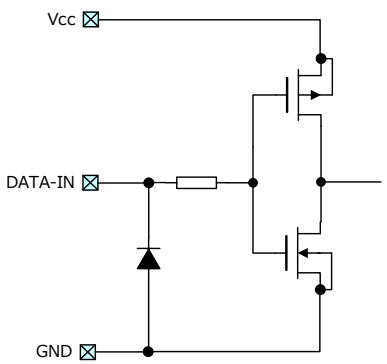
TB62781FNG / TB62D612FTG	TB62D786FTG	TB62D787FTG
		
RESET: It is pulled down internally by the resistor of 10 kΩ.	RESET: Without pin	RESET: Without pin

Figure 2-4 Equivalent circuits (input)

2.6. Rising period and falling period for input pins (tr / tf)

Input pins have the hysteresis of 0.2 V to 0.4 V.
When the voltage ripple of the input waveform is less than 0.2 V, tr and tf can be dulled by using the low pass filter, etc.
Values in the below table are experience ones for your reference.

Table 2.5 tr and tf for input pins

Item	Symbol	Pin name	Max	Unit
Rising period	tr_max	SCLK, SDA, DATA-IN	500	ns
Falling period	tf_max	SCLK, SDA, DATA-IN	500	ns

Be sure to confirm that there is no problem in controlling LEDs.

3. Output Current and Current Accuracy

3.1. Absolute maximum ratings of output block

Since the absolute maximum rating must not be exceeded instantaneously, set the output current up to 80 mA in considering the current accuracy. Also, the output voltage should not exceed 29 V in considering the ripple of the LED power supply.

Table 3-1 Absolute maximum ratings of output block

Item	Symbol	Absolute maximum ratings	Unit	Note
Output current	I_{OUT}	85	mA	Per one channel
Output voltage	V_{OUT}	-0.3 to 29	V	—

3.2. Recommended range of output current

Output current of 5 mA to 40 mA per one channel is recommended.

The constant current characteristics are guaranteed when the output voltage during ON ($V_{OUT(ON)}$) is as follows; TB62781FNG / TB62D612FTG: 0.4 V to 4.0 V, TB62D786FTG / TB62D787FTG: 0.5 V to 4.0 V

Note that the output losses are large when the output voltage is very high.

3.2.1. Output current setting (TB62781FNG and TB62D612FTG)

Table 3-2 Output characteristics (TB62781FNG and TB62D612FTG)

Item	Symbol	Test conditions	Min	Typ.	Max	Unit
Output current	I_{OUT1}	$V_{OUT(ON)}$=0.4 V, R_{EXT}=1.2 kΩ, Vcc=5 V	12.69	13.5	14.31	mA
Output current accuracy between channels	ΔI_{OUT2}	$V_{OUT(ON)}$=0.4 V, R_{EXT}=1.2 kΩ, All channels ON, Vcc=5 V	—	—	±3.0	%
Output voltage	$V_{OUT(ON)}$	All outputs	0.4	—	4	V

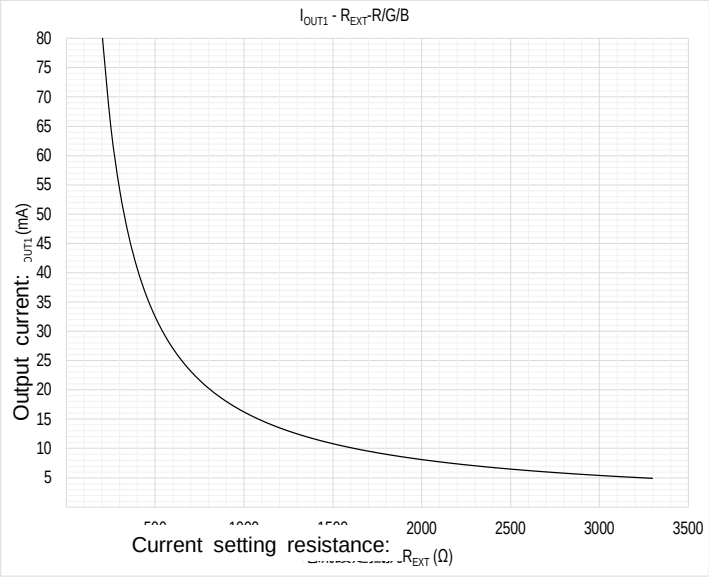


Figure 3-1 Relation of I_{OUT1} and R_{EXT} (TB62781FNG and TB62D612FTG)

Approximate equation: Output current (mA) = 14.5×1.12(V)/R_{EXT} (Ω)

Above graph is only for reference that has a constant current error of R_{EXT} and output current between ICs and between channels.

Pin voltage of Rext-R/G/B is 1.12 V(typ.), and the power consumption of the resistor is as follows;

V^2/R=1.12×1.12/1.2 kΩ=1.04 mW

3.2.2. Output current setting (TB62D786FTG and TB62D787FTG)

Table 3-3 Output characteristics (TB62D786FTG and TB62D787FTG)

Item	Symbol	Test conditions	Min	Typ.	Max	Unit
Output current	I_{OUT1}	$V_{OUT(ON)}$=0.5 V, R_{EXT}=1.2 kΩ, Vcc=5 V	12.5	13.3	14.1	mA
Output current accuracy between channels	ΔI_{OUT2}	$V_{OUT(ON)}$=0.5 V, R_{EXT}=1.2 kΩ, All channels ON, Vcc=5 V	—	—	±3.0	%
Output voltage	$V_{OUT(ON)}$	All outputs	0.5	—	4	V

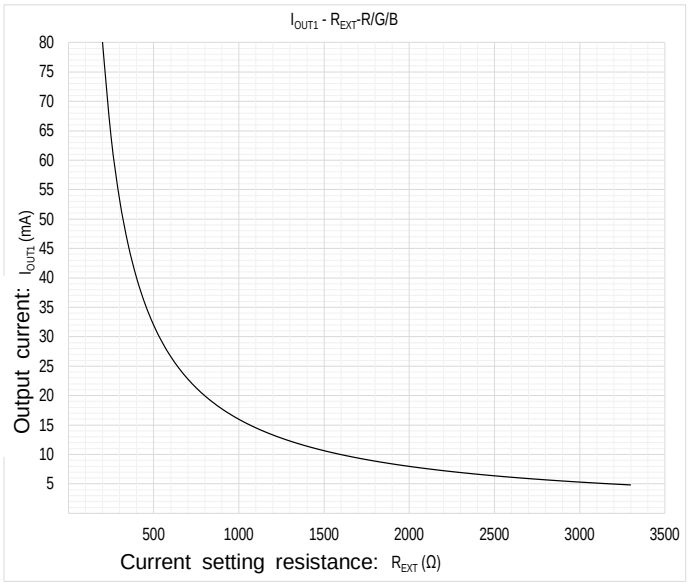


Figure 3-2 Relation of I_{OUT1} and R_{EXT} (TB62D786FTG and TB62D787FTG)

Approximate equation: Output current (mA) = 14.18×1.128(V)/R_{EXT}(Ω)

Above graph is only for reference that has a constant current error of R_{EXT} and output current between ICs and between channels.

Pin voltage of Rext-R/G/B is 1.128 V(typ.), and the power consumption of the resistor is as follows;

V^2/R=1.128×1.128/1.2 kΩ=1.06 mW

3.3. Heat dissipation by using an external resistor for outputs

When the output voltage during ON exceeds 0.4 V (TB62781FNG or TB62D612FTG) or 0.5 V (TB62D786FTG or TB62D787FTG), each output generates heat due to its loss.
In the case 9 channels (TB62781FNG or TB62D786FTG) or 24 channels (TB62D612FTG or TB62D787FTG) are turned on simultaneously, the output loss is concentrated on the IC and so the output current should be limited. To solve this problem, connect the resistor externally to the outputs to reduce the power consumption. (Shown in the figure 3-3)

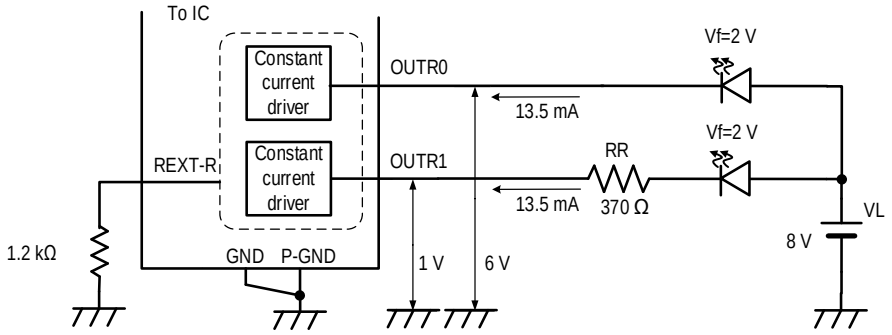


Figure 3-3 Connection of external resistor (RR) example (in case of TB62D786FTG or TB62D787FTG)

The figure 3-3 shows the case of OUTR0 and OUTR1 that illuminate red LEDs.
OUTR0 pin consumes 81 mW that is the product of 6 V (output voltage during ON) and 13.5 mA (LED current).

Pw(OUTR0)≈(VL-Vf)×LED current=(8-2)×13.5 mA=81 mW

OUTR1 consumes 13.5 mW that is the product of 1 V (Note) (output voltage during ON) and 13.5 mA (LED current).

Note: Output voltage during ON is 1 V due to 5 V voltage drop at the external resistor (RR).

Pw(OUTR1)≈(VL-Vf-voltage drop)×LED current=(8-2-5)×13.5 mA=13.5 mW

Select the appropriate resistor (RR) that reduces voltage of 5 V when LED current is 13.5 mA.

RR = 5 V / 13.5 mA=370 Ω

This resistor (RR) is not necessary to be connected, but recommended to use according to the usage conditions in order to suppress heat concentration on the IC.

In case of TB62D786FTG and TB62D787FTG
They are single-wire input type and VL pin is used as a main power supply. So, note that the internal 5 V regulator, which is connected between VL pin and VLOUT pin, also generates the loss.

4. Specification of Communication for each Input

4.1. 2-wire input (TB62781FNG and TB62D612FTG)

Specification of communication for 2-wire input type (TB62781FNG and TB62D612FTG) is described in this section.

4.1.1. Basic specification of DATA input (2-wire input)

Basic unit is shown in the figure 4-1. ”0” or ”1” of SDA (DATA signal) is received at the rising edge of SCLK (clock).
SCLK clock frequency is up to 10 MHz. The frequency can be lower because of the clock synchronization type.
Each input timing is shown in the table 4-1.

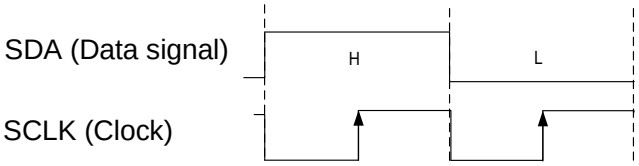


Figure 4-1 Data input (2-wire input)

Table 4-1 Input timing (2-wire input)

Item	Symbol	Test conditions	Min	Typ.	Max	Unit
SCLK clock frequency	fCLK	SCLK	—	—	10	MHz
Data setup time	tSU;DAT	SDA-SCLK	10	—	—	ns
Data hold time	tHD;DAT	SCLK-SDA	10	—	—	
”L” period of SCLK clocks	tLOW	Pulse width of SCLK during low level	50	—	—	
”H” period of SCLK clocks	tHIGH	Pulse width of SCLK during high level	50	—	—	

4.1.2. Input format (2-wire input)

Input format for a single IC is shown in the figure 4-2.
Data is input to the input format in the order of the start command, the slave address, the sub address, the PWM DATA, and the period command with MSB first.

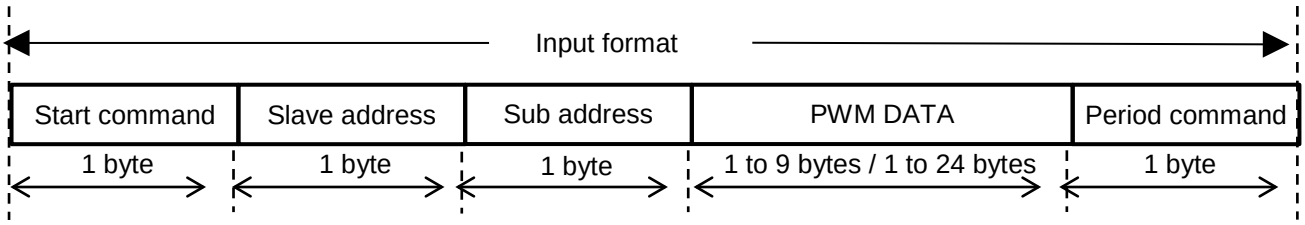


Figure 4-2 Basic format (2-wire input)

Start command (1 byte)	: Judgement of start input
Slave address (1 byte)	: Configures ID numbers of the IC (up to 64).
Sub address (1 byte)	: Specifies LED output where PWM DATA is transmitted.
PWM DATA (1 byte to 9 bytes or 1 byte to 24 bytes (Note))	: Configures 127-grayscale PWM DATA that is transmitted to the specified LED output. TB62781FNG: 1 byte (1 channel) to 9 bytes (9 channels) TB62D612FTG: 1 byte (1 channel) to 24 bytes (24 channels)
Period command (1 byte):	: Judgement of communication completion

Description of each command is following from the next page.

4.1.3. Start command (2-wire input)

As shown in the figure 4-3, the start command is recognized when "1" is received over eight times in succession.
Make sure to receive "0" at the MSB of the slave address and then receive following DATA of the slave address.

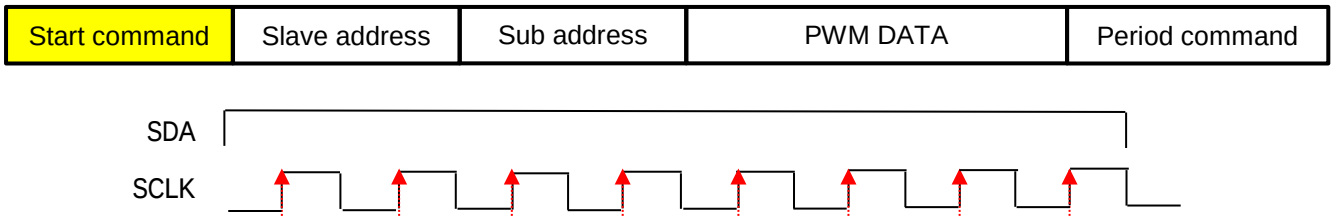


Figure 4-3 Start command (2-wire input)

4.1.4. Period command (2-wire input)

As shown in the figure 4-4, the period command is recognized when receiving “10000001”.
The eighth SCLK falling edge reflects the PWM DATA on the output. Then, the communication waits for the re-input of the start command.

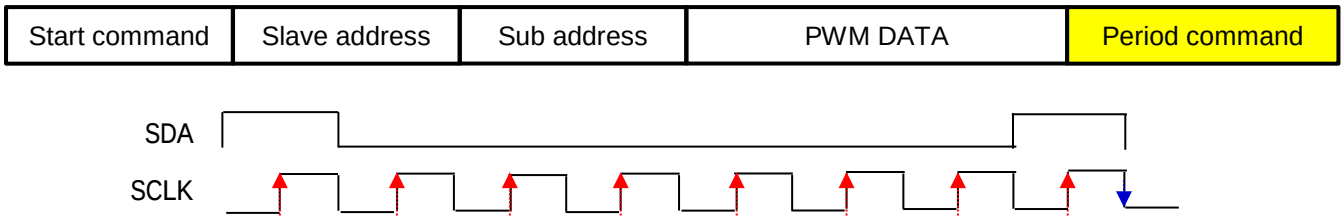


Figure 4-4 Period command (2-wire input)

<Attention>
In using TB62D612FTG, SCLK DATA for the period command should be input until the eighth falling edge. The idle state of SCLK transmission is in high level or low level according to the usage environment. Refer to the figure 4-5 and the figure 4-6.

When SCLK transmission is in the idle state with low level

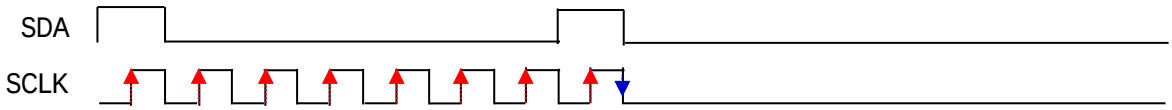


Figure 4-5 Period command (2-wire input) (Example 1)

When SCLK transmission is in the idle state with high level

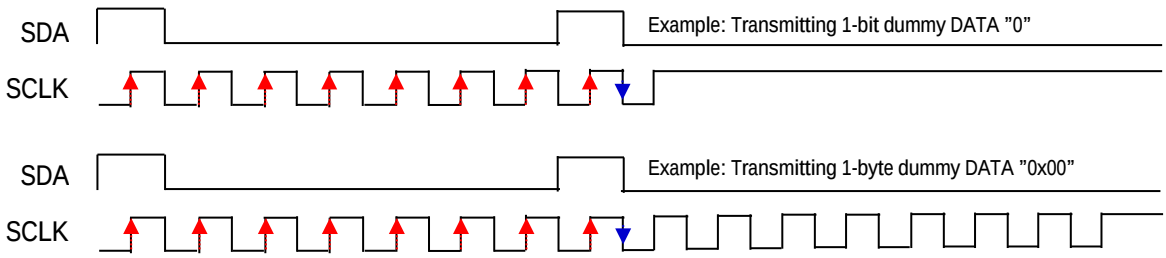


Figure 4-6 Period command (2-wire input) (Example 2)

4.1.5. Slave address (2-wire input) (unique numbers of the IC set by ID0, ID1, and ID2 pins)

As shown in the figure 4-7, ID numbers (0 to 63, up to 64 numbers) are set by ID0, ID1, and ID2 pins and input to the slave address.
MSB is input first. The slave address is configured by intermediate DATA (MSB and LSB are set “0”) except all select setting.
When inputting ”1” to LSB, the PWM DATA of all ICs can be set regardless of the intermediate DATA, allowing it to reset software.

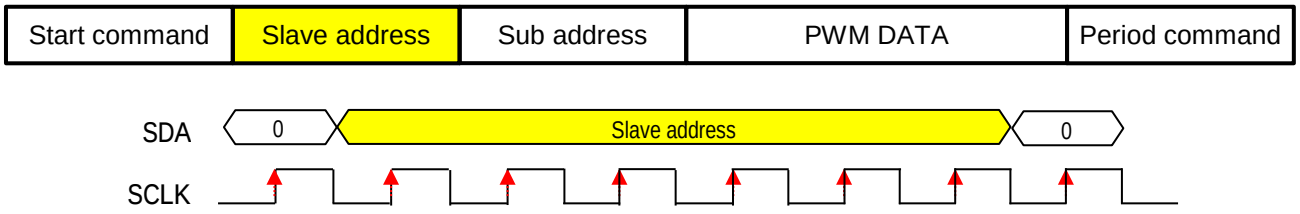


Figure 4-7 Slave address (2-wire input)

The slave address of 0 to 11 and all selection mode are shown in the table 4-2. It is excerpted from the technical DATA.
Though the slave address that is not described in the technical DATA is not received, it is recommended to avoid inputting it for shipment to guarantee safety.

Table 4-2 Slave address (2-wire input) excerpted from the technical DATA

ID	Slave address		ID pin setting		
	Slave address	Decimal number	ID2	ID1	ID0
0	“00000000”	0	GND	GND	GND
1	“00000010”	1	GND	GND	Vcc×1/3
2	“00000100”	2	GND	GND	Vcc×2/3
3	“00000110”	3	GND	GND	Vcc
4	“00001000”	4	GND	Vcc×1/3	GND
5	“00001010”	5	GND	Vcc×1/3	Vcc×*1/3
6	“00001100”	6	GND	Vcc×1/3	Vcc×2/3
7	“00001110”	7	GND	Vcc×1/3	Vcc
8	“00010000”	8	GND	Vcc×2/3	GND
9	“00010010”	9	GND	Vcc×2/3	Vcc×1/3
10	“00010100”	10	GND	Vcc×2/3	Vcc×2/3
11	“00010110”	11	GND	Vcc×2/3	Vcc
~ Snip ~					
—	0XXXXXX1	-	All selection		

4.1.6. Sub address (2-wire input) (Selecting LED output controlled for PWM DATA setting)

As shown in the figure 4-8, LED output is selected in the sub address for PWM DATA setting.
MSB is input first. The sub address is configured by intermediate DATA (MSB and LSB are set “0”).
Output selection has 3 modes.

1. Output channel setting: Select only specified LED outputs.
2. All channels setting: Select all LED outputs, 9 channels (in case of TB62781FNG), or 24 channels (in case of TB62D612FTG).
3. Special mode setting: LED outputs are selected in a sequence. (9 channels of OUTR0 to OUTB2 for TB62781FNG, and 24 channels of OUTR0 to OUTB7 for TB62D612FTG).

LED outputs are incremented as follows; OUTR0→G0→B0, OUTR1→G1→B1 ・・・ OUTR7→G7→B7
(Example in case of TB62D612FTG)

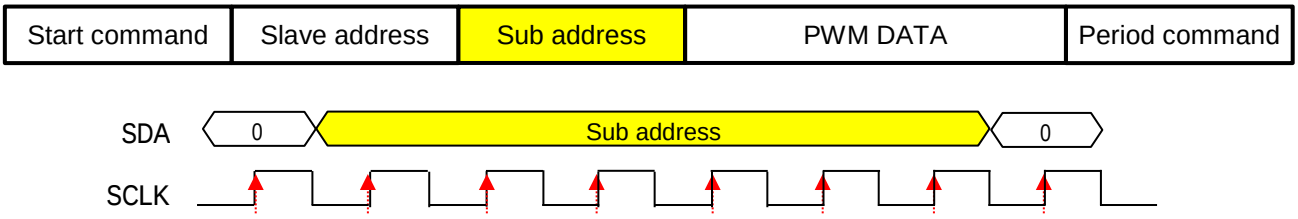


Figure 4-8 Sub address (2-wire input)

Output channel setting mode is shown in the table 4-3. (From OUTR0 to OUTB2 and from OUTR7 to OUTB7 excerpted from the technical DATA, all channel setting mode, and special mode)
Though the sub address that is not described in the technical DATA is not received, it is recommended to avoid inputting it for shipment to guarantee safety.

Table 4-3 Sub address (2-wire input) excerpted from the technical DATA

Sub address	LED output	Setting target of PWM DATA
“00000010”	/OUTR0	Select only specified LED outputs
“00000100”	/OUTG0	
“00000110”	/OUTB0	
“00001000”	/OUTR1	
“00001010”	/OUTG1	
“00001100”	/OUTB1	
“00001110”	/OUTR2	
“00010000”	/OUTG2	
“00010010”	/OUTB2	
~ Snip ~		
“00000010”	/OUTR7	
“00000100”	/OUTG7	
“00000110”	/OUTB7	
“00001000”	All channels setting	Select LED outputs of all 9 channels or all 24 channels.
“00001010”	Special mode setting	Select LED outputs of 9 channels or 24 channel in a sequence.

4.1.7. PWM DATA (2-wire input, 127 grayscales)

As shown in the figure 4-9, PWM DATA is configured to control the selected LED outputs.

1. Output channel setting: 1 byte
2. All channels setting: 1 byte
3. Special mode setting: 9 bytes or 24 bytes

In the case of sub address setting in the special mode, it can be interrupted by replacing the PWM DATA with the period command.
When LED outputs do not receive or update PWM DATA, former PWM DATA is used.
MSB is input first. PWM DATA is set by intermediate DATA (LSB is set “0”).

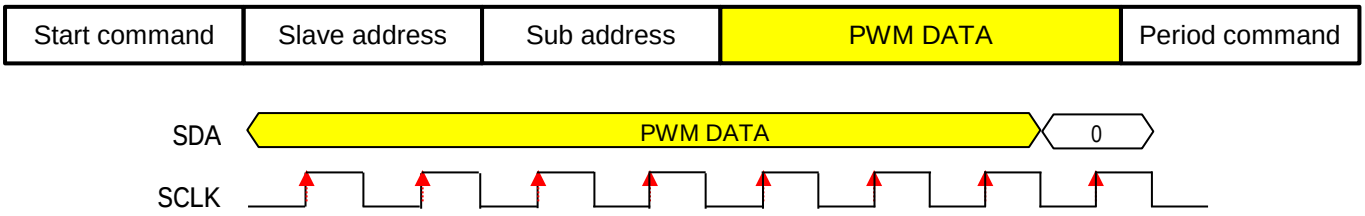


Figure 4-9 PWM DATA (2-wire input)

The table 4-4 shows the PWM DATA of 0/127 to 8/127 and 119/127 to 127/127 excerpted from the technical DATA.
Though the sub address that is not described in the technical DATA is not received, it is recommended to avoid inputting it for shipment to guarantee safety.

Table 4-4 PWM DATA (2-wire input) excerpted from the technical DATA

Data	PWM dimmable	Remarks
00000000	0/127	Initial state: Always off at the setting of 0/127. LSB: Set “0”. Do not set “1”. 127/127: Always on.
00000010	1/127	
00000100	2/127	
00000110	3/127	
00001000	4/127	
00001010	5/127	
00001100	6/127	
00001110	7/127	
00010000	8/127	
~ Snip ~		
11101110	119/127	
11110000	120/127	
11110010	121/127	
11110100	122/127	
11110110	123/127	
11111000	124/127	
11111010	125/127	
11111100	126/127	
11111110	127/127	

4.1.8. Packet input (2-wire input) (Data communication to two or more ICs)

The figure 4-10 shows the communication model of two ICs whose slave addresses are different.
Input format of the two ICs, whose slave addresses are different, are communicated by consecutive packets with a certain frame cycle (fps).
After the packet ends, SDA and SCLK transmissions become the idle states and do not perform DATA communication until the next frame starts.

As for the packet (t=n, n+1, n+2・・・) and the next packet (t=n+1, n+2, n+3・・・), the interval period should be 3 ms or more between 8th down edges of the period commands of the same slave address.
One cycle of the internal PWM counter is up to 3 ms. PWM DATA is updated after the period command ends and the count value becomes maximum. It is because if PWM DATA is transmitted to the same LED output, it is not received while the count value does not reach the maximum.

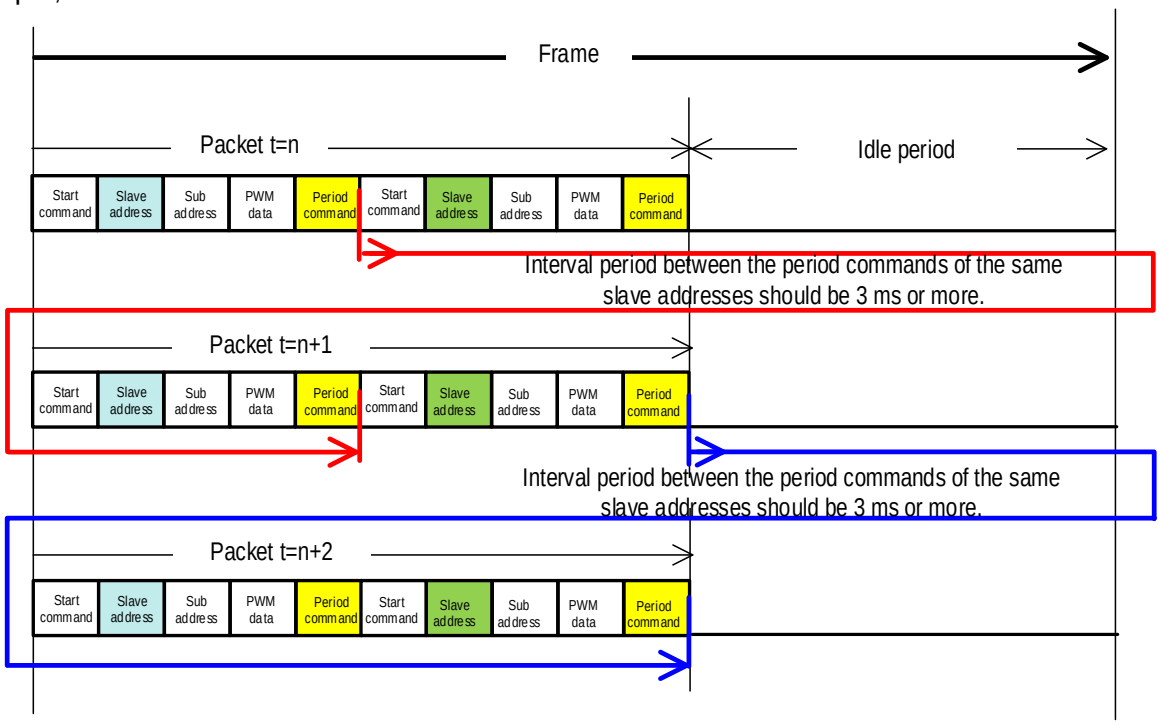


Figure 4-10 Image of packet communication to the IC with the same slave address when using two ICs with different slave addresses (2-wire input)

<Attention>

4.1.9. Errata: Errata make the next input format into non-reception state according to the end timing of SCLK transmission.

Errata occur when **using TB62D612FTG (2-wire input, 24 channels)**, and not occur in using TB62781FNG.
Figure 4-11 shows update and reception reset of PWM data (DATA ”A”) when the first internal PWM counter after the period command is 127.
The period of one packet varies depending on the number of input formats and the frequency of the SCLK. Since transmissions of the SCLK and the internal PWM clocks are asynchronous, the timing of the period command and that of PWM DATA transmission and reception reset exist randomly in one cycle (up to 3 ms) of the internal PWM counter.

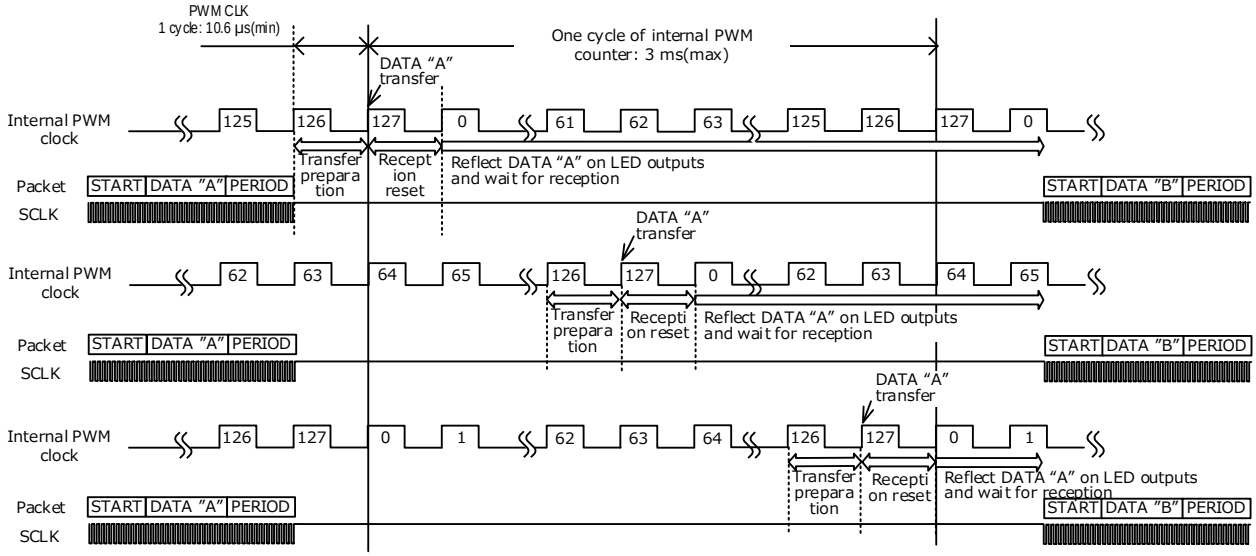


Figure 4-11 Update and reception reset timing of PWM DATA after the period command (2-wire input)

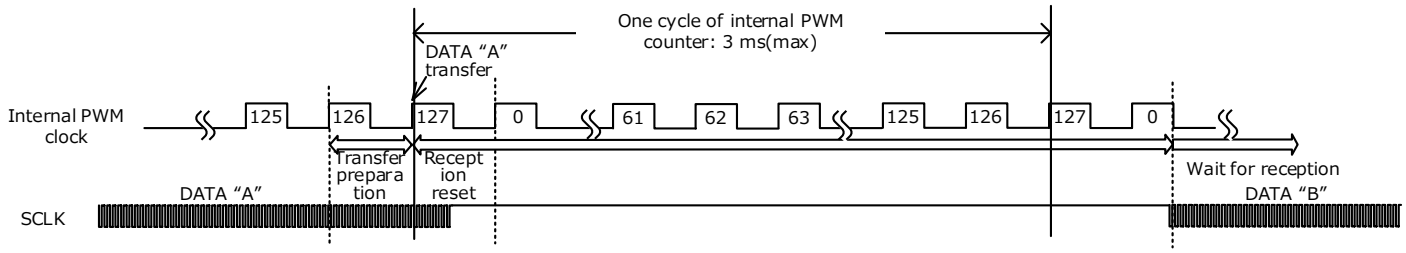


Figure 4-12 Timing of SCLK transmission when errata occur (2-wire input)

Errata occur in accordance with the end timing of SCLK transmission.
The timing of the Figure 4-12 nearly corresponds to the top timing chart in the Figure 4-11.
In this timing, SCLK transmission stops during reception reset.
Therefore, the reception reset continues until the next packet starts. After it finishes at the beginning of the next packet, the packet moves to the reception waiting status. So, DATA “B” at the beginning of the packet is not received.
When errata occur, the communication continues with the received DATA “A” even in the next packet from above reasons.
Errata do not occur when the SCLK transmission stops during the transfer preparation (10.6 µs (min)).

<Attention>

4.1.10. Errata generation and their avoidance method (2-wire input)

The reception reset that continues until the beginning of the next packet is completed with one SCLK input. Therefore, when errata occur, **it is recommended to adopt the avoidance methods shown in the figure 4-14 and the figure 4-15** to finish the reception reset.

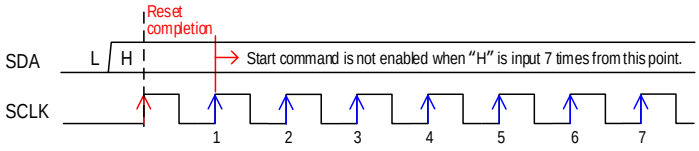


Figure 4-13 Errata generation by start command error

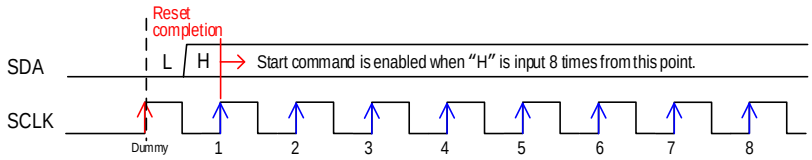


Figure 4-14 Errata avoidance method (1): Adding one SCLK (2-wire input) (Example)

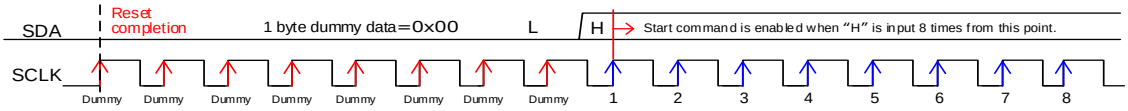


Figure 4-15 Errata avoidance method (2): Adding 8 SCLK (1 byte dummy DATA) (2-wire input) (Example)

4.1.11. Detail description of errata (2-wire input)

Occurrence of errata depends on the PWM counter timing. Figure 4-16 and the figure 4-17 show the timing charts, where errata do not occur (charts of SCLK(1) and (2)) and occur (charts of SCLK(3), (4), and (5)). Figure 4-16 shows the example when 127th PWM counter timing comes earlier, and the figure 4-17 shows when it comes later.

In the charts of SCLK (3), (4), and (5), SCLK transmission stops during the period between (B) and (C) where PWM DATA updates and resets. Therefore, the reset is not completed until the up edge of SCLK is recognized at (D). So, the MSB DATA at (D) is invalidated and the start command is not enabled. As a result, its input format is not received.

At this time, the IC operation continues by the received PWM DATA, and does not freeze.

When the packet is consisted of two or more input formats, the second and subsequent input formats are always received because the reset that had been interrupted at (D) finishes and the packet is in the reception status.

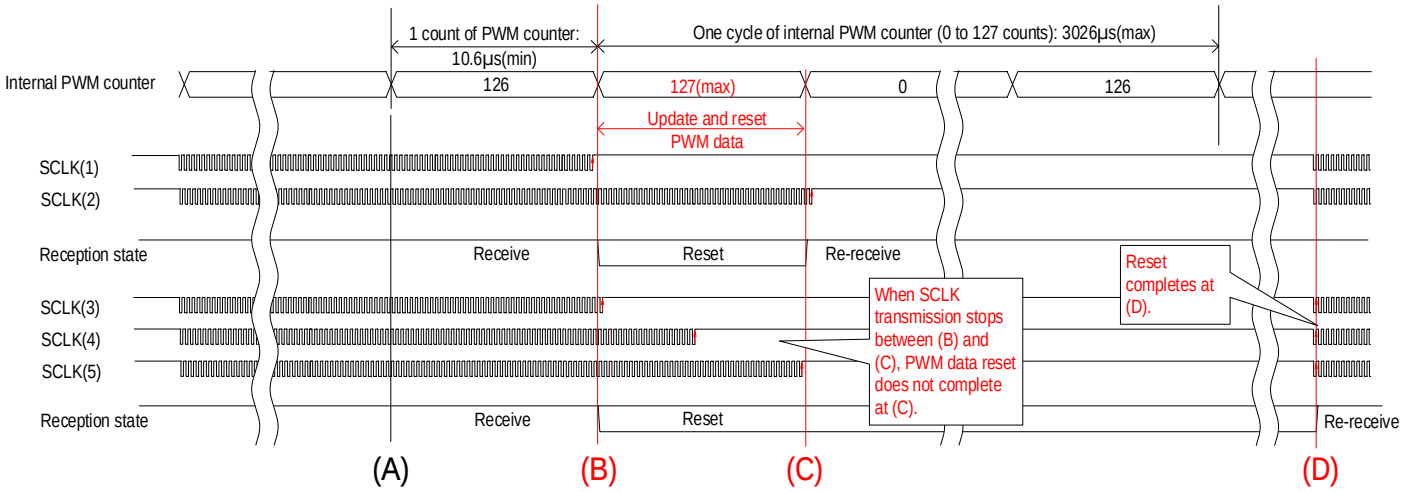


Figure 4-16 Relation of SCLK and PWM counter: 127th PWM counter timing comes earlier (2-wire input)

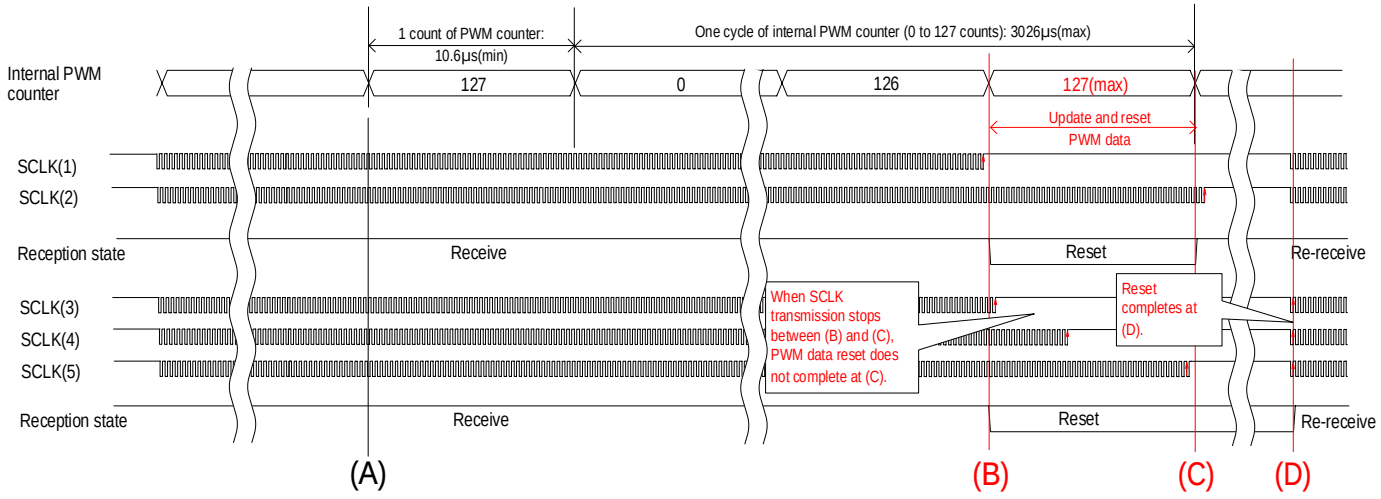


Figure 4-17 Relation of SCLK and PWM counter: 127th PWM counter timing comes later (2-wire input)

126th PWM counter (10.6 µs (min)) has a preparation period of DATA transference without SCLK transmission. Also, the maximum period of the PWM counter cycle, where the 127th PWM counters exist randomly, is 3026 µs. Therefore, the length of the packet, in which errata do not occur, can be calculated as follows.

Condition example: SCLK transmission: 28 bytes per 1 format, 8 clocks per 1 byte, frequency = 1 MHz.
When SCLK packet is short: Shorter than the following value; 8 clocks÷1 MHz×28 bytes+10.6 µs = 224 µs+10.6 µs = 234.6 µs
When SCLK packet is long: Longer than the following value; 8 clocks÷1 MHz×28 bytes+3026 µs = 224 µs+3026 µs = 3250 µs

However, it is difficult to visually recognize the occurrence of errata even if the DATA of the beginning input format of the next packet is not received, because the LED can illuminate by using the prior PWM DATA which is not influenced by errata. Therefore, it is difficult to verify errata existence. Moreover, the control of the packet length is complicated. So, the errata avoidance method described in the chapter 4.1.10 is recommended.

4.2. Specification of communication: A single-wire input (TB62D786FTG and TB62D787FTG)

Specification of a single-wire input communication (TB62D786FNG and TB62D787FTG) is described in this section.

4.2.1. Basic specification of input DATA (Single-wire input)

Basic sequence is shown in the figure 4-18. This is the Manchester coding. ”0” or ”1” of 1 bit DATA is indicated according to the direction of the potential transition input to the DATA-IN pin.
When voltage transits in the tW range, it is recognized as a DATA and received, but when the voltage does not transit in this range, it is judged as a communication error and ignored. In this case, it is re-received at the next start command.
As for input signal, the voltage transition for Data "0" and Data "1" should be in the same phase, and its fluctuation should be within the allowable jitter (tJIT).
Refer to the figure 4-19 and the table 4-5 for each timing.

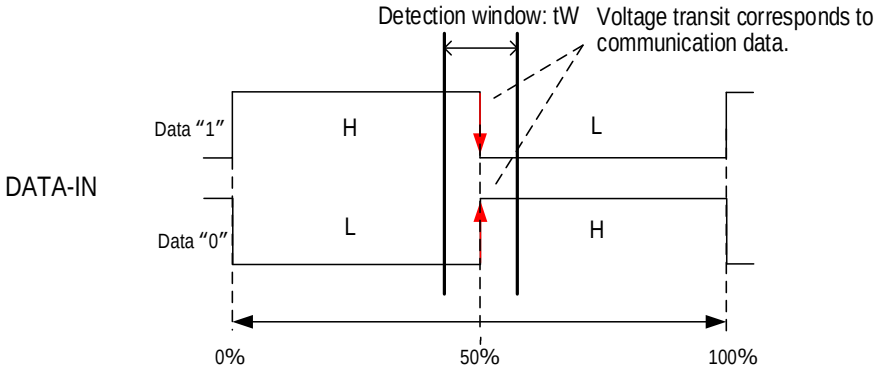


Figure 4-18 Input DATA (Single-wire input)

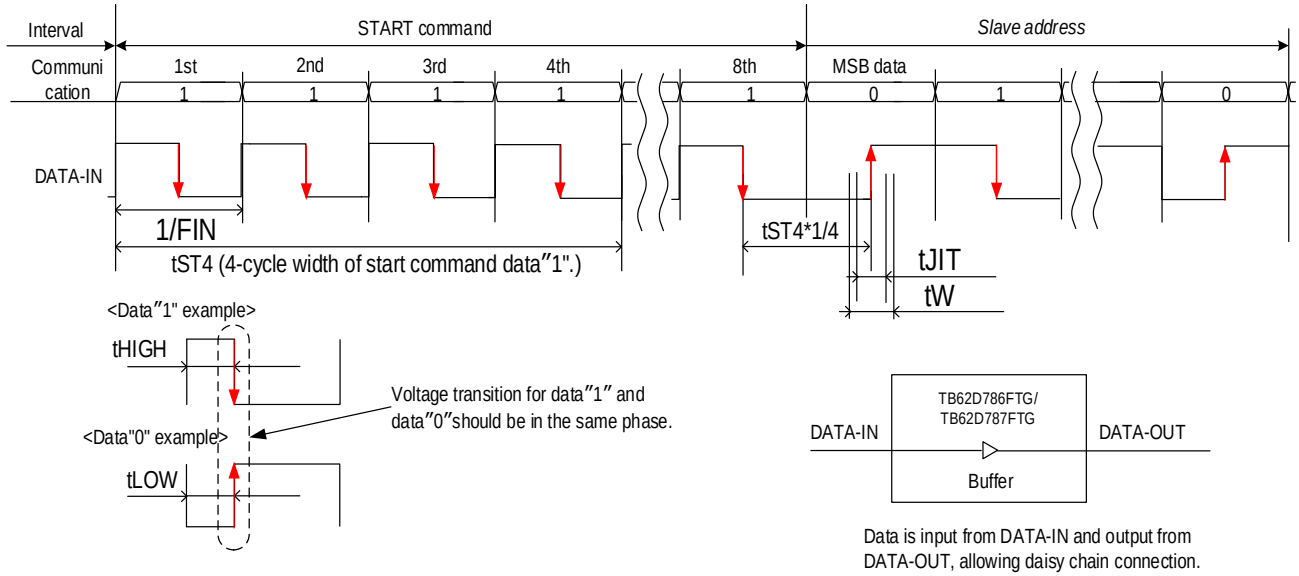


Figure 4-19 Communication timing (Single-wire input)

Table 4-5 Input timing (Single-wire input)

Item	Symbol	Test condition	Min	Typ.	Max	Unit
DATA input frequency	FIN	DATA-IN	0.5	—	2.0	MHz
Window width of DATA detection	tW	—	135	—	—	ns
Width of DATA allowable jitter	tJIT	"H" and "L" communications are in the same phase.	—	—	±54	ns
Minimum pulse width of DATA input	tLOW, tHIGH	—	100	—	—	ns

4.2.2. Input format (Single-wire input)

Input format for one IC is shown in the figure 4-20.
After the interval period, input DATA to the input format in the order of the start command, the slave address, the sub address, the PWM DATA, and the period command with MSB first.
Except for the interval period, the order is the same as 2-wire input.

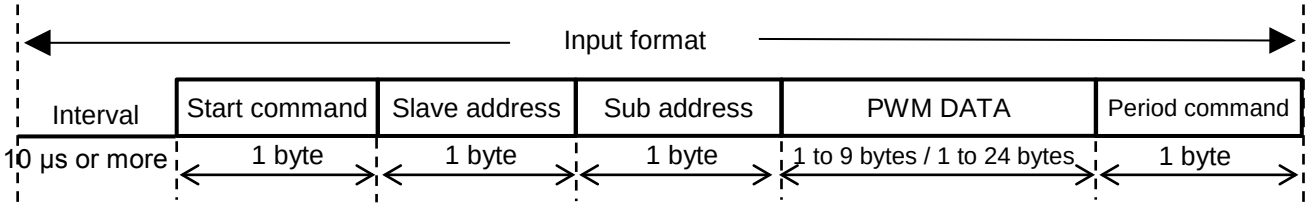


Figure 4-20 Basic format (Single-wire input)

Interval (10 µs or more)	: Resets the learned result of the DATA cycle and waits for communication input
Start command	: Judges input start and learn the DATA cycle
Slave address	: Configures ID numbers of the IC (up to 64).
PWM DATA	: Specifies LED output where PWM DATA is transmitted.
	: Configures 127-grayscale PWM DATA that is transmitted to the specified LED output. TB62D786FTG: 1 byte (1 channel) to 9 bytes (9 channels) TB62D612FTG: 1 byte (1 channel) to 24 bytes (24 channels)
Period command	: Judgement of communication completion

The DATA cycle is learned in the start command. And after the slave address, the DATA is received with the DATA detection window width based on the learned results.
The results of learned DATA cycle are reset at the interval period (10 µs or more). And the DATA cycle is learned again in the next start command. This is because even if an incorrect DATA cycle is learned due to a noise or the like and the DATA cannot be received, the correct DATA cycle is learned and the DATA can be received in the next start command.

Each command is described in the following pages.

4.2.3. Start command (Single-wire input)

As shown in the figure 4-21, the start command is recognized when the DATA "1" is received over eight times (i.e., 2 bytes) consecutively.
DATA-IN communication: 0xAA, 0xAA (b10101010_10101010)
Make sure to receive "0" at the MSB of the slave address and then receive following DATA of the slave address.
Since the DATA cycle is learned in the start command, the DATA detection window width has no meaning.

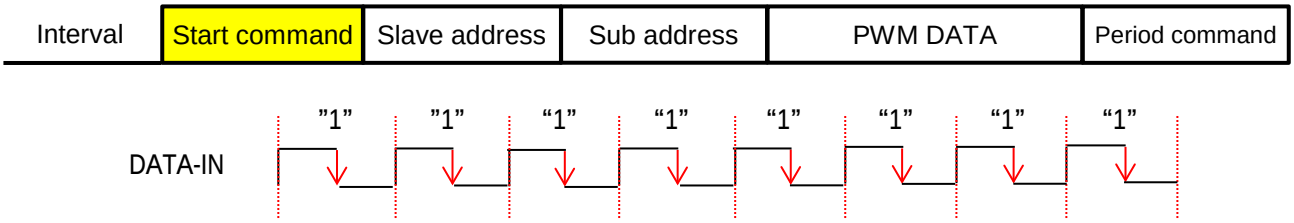


Figure 4-21 Start command (Single-wire input)

4.2.4. Period command (Single-wire input)

As shown in the figure 4-22, the period command is recognized when receiving "10000001".
DATA-IN communication: 0x95, 0x56 (b10010101_01010110)
After reflecting the PWM DATA on the outputs, the communication waits for the re-input of the start command.

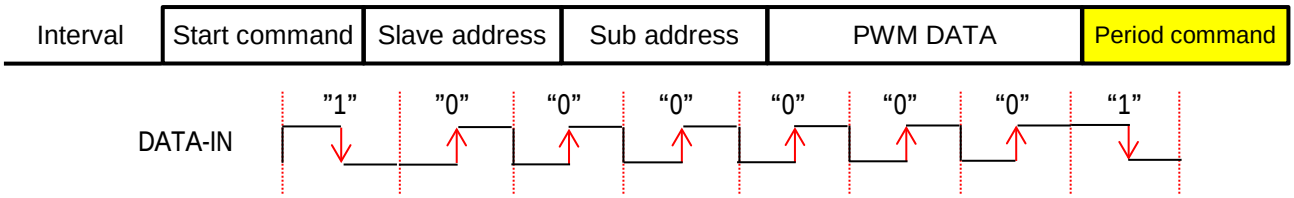


Figure 4-22 Period command (Single-wire input)

4.2.5. Slave address (unique number of ICs set by ID0, ID1, and ID2 pins) (Single-wire input)

As shown in the figure 4-23, ID numbers (0 to 63, up to 64 numbers) are set by ID0, ID1, and ID2 pins and input to the slave address.
MSB is input first. The slave address is configured by intermediate DATA (MSB and LSB are set “0”) except all select setting.
When inputting ”1” to LSB, the PWM DATA of all ICs can be set regardless of the intermediate DATA, allowing it to reset software.

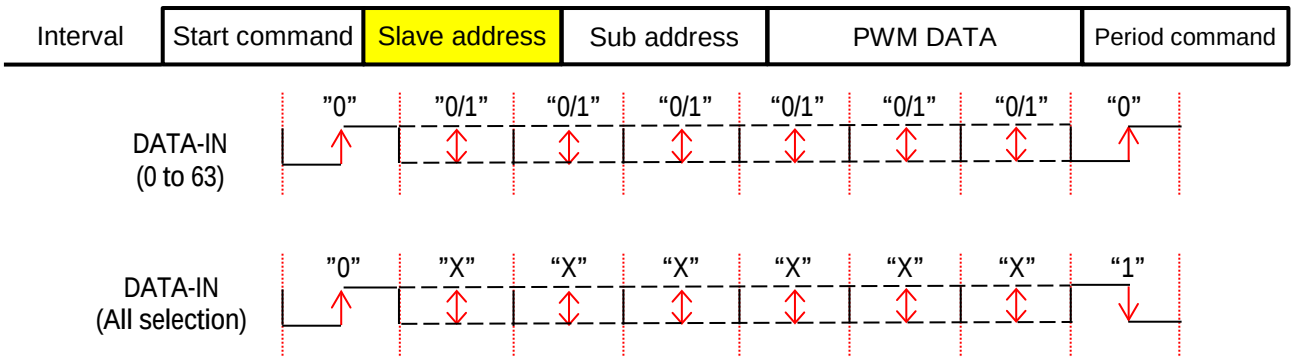


Figure 4-23 Slave address (Single-wire input)

The slave address of 0 to 11 and all selection mode are shown in the table 4-6. It is excerpted from the technical DATA.
Though the slave address that is not described in the technical DATA is not received, it is recommended to avoid inputting it for shipment to guarantee safety.

Table 4-6 Slave address (Single-wire input) excerpted from the technical DATA

ID	Slave address				ID pin setting		
	Slave address	DATA-IN	Hexadecimal number	Decimal-number	ID2	ID1	ID0
0	“00000000”	0101010101010101	0x55, 0x55	85, 85	GND	GND	GND
1	“00000010”	0101010101011001	0x55, 0x59	85, 89	GND	GND	REXT-R/G/B (Note 1)
2	“00000100”	0101010101100101	0x55, 0x65	85, 101	GND	GND	Open
3	“00000110”	0101010101101001	0x55, 0x69	85, 105	GND	GND	Vcc
4	“00001000”	0101010110010101	0x55, 0x95	85, 149	GND	REXT-R/G/B (Note 1)	GND
5	“00001010”	0101010110011001	0x55, 0x99	85, 153	GND	REXT-R/G/B (Note 1)	REXT-R/G/B (Note 1)
6	“00001100”	0101010110100101	0x55, 0xA5	85, 165	GND	REXT-R/G/B (Note 1)	Open
7	“00001110”	0101010110101001	0x55, 0xA9	85, 169	GND	REXT-R/G/B (Note 1)	Vcc
8	“00010000”	0101011001010101	0x56, 0x55	86, 85	GND	Open	GND
9	“00010010”	0101011001011001	0x56, 0x59	86, 89	GND	Open	REXT-R/G/B (Note 1)
10	“00010100”	0101011001100101	0x56, 0x65	86, 101	GND	Open	Open
11	“00010110”	0101011001101001	0x56, 0x69	86, 105	GND	Open	Vcc
~ Snip ~							
—	“0XXXXXX1”	0101010101010110 (Note 2)	0x55, 0x56	85, 86	All selection		

Note 1: Connect to the REXT-R, REXT-G, or REXT-B pin.
Note 2: When X is set 0

4.2.6. Sub address (Single-wire input) (Selecting LED output controlled for PWM DATA setting)

As shown in the figure 4-24, LED output is selected in the sub address for PWM DATA setting.
MSB is input first. The sub address is configured by intermediate DATA (MSB and LSB are set “0”).
Output selection has 3 modes (in case of TB62D768FTG) and 5 modes (in case of TB62D787FTG).

1	Output channel setting	: Select only specified LED outputs.
2	All channels setting	: Select all LED outputs, 9 channels (in case of TB62D786FTG), or 24 channels (in case of TB62D787FTG)
3	Special mode setting	: LED outputs are selected in a sequence. (9 channels of OUTR0 to OUTB2 for TB62D786FTG, and 24 channels of OUTR0 to OUTB7 for TB62D786FTG).
4	12 channels input	: Divide 24 channels by 12 channels and select each 12 channel of LED output.
5	6 channels input	: Divide 24 channels by 6 channels and select each 6 channel of LED output.

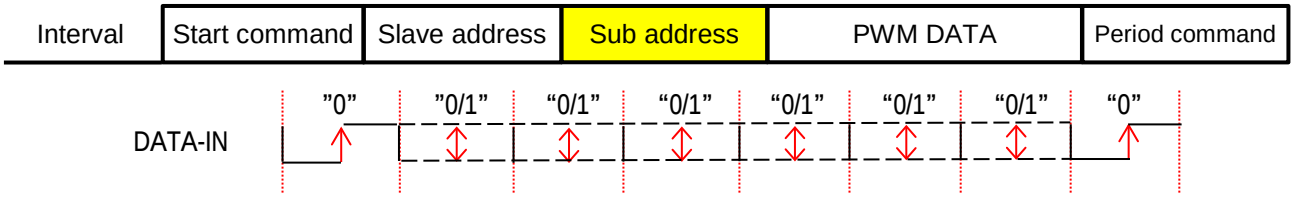


Figure 4-24 Sub address (Single-wire input)

Output channel setting mode is shown in the table 4-7. (From OUTR0 to OUTB2 and from OUTR7 to OUTB7 excerpted from the technical DATA, all channel setting mode, special mode, 12 channel input mode, and 6 channel input mode)
Though the sub address that is not described in the technical DATA is not received, it is recommended to avoid inputting it for shipment to guarantee safety.
When PWM DATA is configured to the different channel groups (i.e., different sub address) in 6 channel input and 12 channel input mode, the slave addresses of the input formats are the same. In this case, the interval period between the input formats does not need to be 3 ms or more that is described in the section 4.2.8. Since the setting LED outputs are different, the communication is possible with only the interval period of 10 μs.

Table 4-7 Sub address (Single-wire input) excerpted from the technical DATA

Sub address				LED output	PWM DATA setting target
Sub address	DATA-IN	Hexadecimal number	Decimal-number		
“00000010”	0101010101011001	0x55, 0x59	85, 89	/OUTR0	Select only specified LED output
“00000100”	0101010101100101	0x55, 0x65	85, 101	/OUTG0	
“00000110”	0101010101101001	0x55, 0x69	85, 105	/OUTB0	
“00001000”	0101010110010101	0x55, 0x95	85, 149	/OUTR1	
“00001010”	0101010110011001	0x55, 0x99	85, 153	/OUTG1	
“00001100”	0101010110100101	0x55, 0xA5	85, 165	/OUTB1	
“00001110”	0101010110101001	0x55, 0xA9	85, 169	/OUTR2	
“00010000”	0101011001010101	0x56, 0x55	86, 85	/OUTG2	
“00010010”	0101011001011001	0x56, 0x59	86, 89	/OUTB2	
“00010100”	0101011001100101	0x56, 0x65	86, 101	/OUTR3	
~ Snip ~					
“00101100”	0101100110100101	0x59, 0xA5	89, 165	/OUTR7	
“00101110”	0101100110101001	0x59, 0xA9	89, 169	/OUTG7	
“00110000”	0101101001010101	0x5A, 0x55	90, 85	/OUTB7	
“01000000”	0110010101010101	0x65, 0x55	101, 85	All channels setting	Select LED outputs of all 9 channels or all 24 channels.
“01100000”	0110100101010101	0x69, 0x55	105, 85	Special mode setting	Select LED outputs of all 9 channels or all 24 channel in a sequence.
“01100010”	0110100101011001	0x69, 0x59	105, 89	12 channel input Channel group: 1/2	Select LED outputs of 12 channels.
“01100100”	0110100101100101	0x69, 0x65	105, 101	12 channel input Channel group: 2/2	
“01100110”	0110100101101001	0x69, 0x69	105, 105	6 channel input Channel group: 1/4	Select LED outputs of 6 channels.
“01101000”	0110100110010101	0x69, 0x95	105, 149	6 channel input Channel group: 2/4	
“01101010”	0110100110011001	0x69, 0x99	105, 153	6 channel input Channel group: 3/4	
“01101100”	0110100110100101	0x69, 0xA5	105, 165	6 channel input Channel group: 4/4	

4.2.7. PWM DATA (Single-wire input)

As shown in the figure 4-25, PWM DATA is configured to control the selected LED outputs.

1. Output channel setting: 1 byte
2. All channels setting: 1 byte
3. Special mode setting: 9 bytes or 24 bytes
4. 12 channels input: 12 bytes
5. 6 channels input: 6 bytes

In the sub address setting of above 3, 4, and 5, the setting can be interrupted by replacing the PWM DATA with the period command.
When LED outputs do not receive PWM DATA, former PWM DATA is used.
MSB is input first. PWM DATA is set by intermediate DATA (LSB is set “0”).

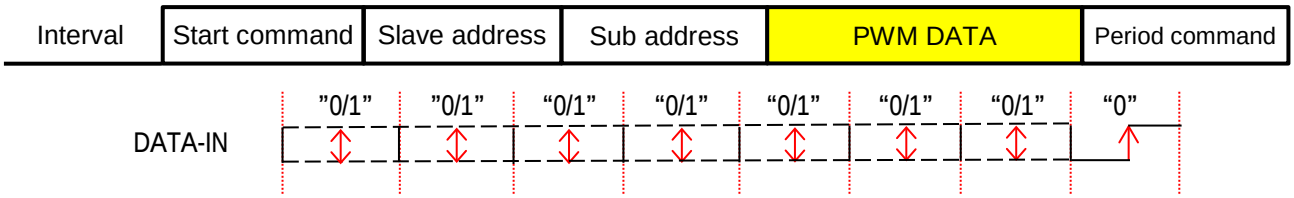


Figure 4-25 PWM DATA (Single-wire input, 127 grayscales)

The table 4-8 shows the PWM DATA of 0/127 to 8/127, 111/127, 112/127, 119/127, 120/127, and 127/127 excerpted from the technical DATA.
Though the sub address that is not described in the technical DATA is not received, it is recommended to avoid inputting it for shipment to safe.

Table 4-8 PWM DATA (Single-wire input) excerpted from the technical DATA

PWM DATA				PWM dimmable	Remarks
PWM DATA	DATA-IN	Hexadecimal number	Decimal-number		
“00000000”	0101010101010101	0x55, 0x55	85, 85	0/127	Initial state: Always off at the setting of 0/127. LSB: Set “0”. Do not set “1”. 127/127: Always on.
“00000010”	0101010101011001	0x55, 0x59	85, 89	1/127	
“00000100”	0101010101100101	0x55, 0x65	85, 101	2/127	
“00000110”	0101010101101001	0x55, 0x69	85, 105	3/127	
“00001000“	0101010110010101	0x55, 0x95	85, 149	4/127	
“00001010“	0101010110011001	0x55, 0x99	85, 153	5/127	
“00001100“	0101010110100101	0x55, 0xA5	85, 165	6/127	
“00001110“	0101010110101001	0x55, 0xA9	85, 169	7/127	
“00010000“	0101011001010101	0x56, 0x55	86, 85	8/127	
~	~	~	~	~	
“11011110“	1010011010101001	0xa6, 0xa9	166, 169	111/127	
“11100000“	1010100101010101	0xa9, 0x55	169, 85	112/127	
~	~	~	~	~	
“11101110“	1010100110101001	0xa9, 0xa9	169, 169	119/127	
“11110000“	1010101001010101	0xaa, 0x55	170, 85	120/127	
~	~	~	~	~	
“11111110“	1010101010101001	0xAA, 0xA9	170, 169	127/127	

4.2.8. Packet input (Single-wire input) (Data communication to two or more ICs)

The figure 4-26 shows the communication model of two ICs whose slave addresses are different.
Input format of the two ICs, whose slave addresses are different, are communicated by consecutive packets with a certain frame cycle (fps).
After the packet ends, DATA-IN transmission becomes the idle state and does not perform the DATA communication until the next frame starts.

As for the packet (t=n, n+1, n+2・・・) and the next packet (t=n+1, n+2, n+3・・・), the interval period should be 3 ms or more between the period commands of the same slave address.
One cycle of the internal PWM counter is up to 3 ms. PWM DATA is updated after the period command ends and the count value becomes maximum. It is because if PWM DATA is transmitted to the same LED output, it is not received while the count value does not reach the maximum.

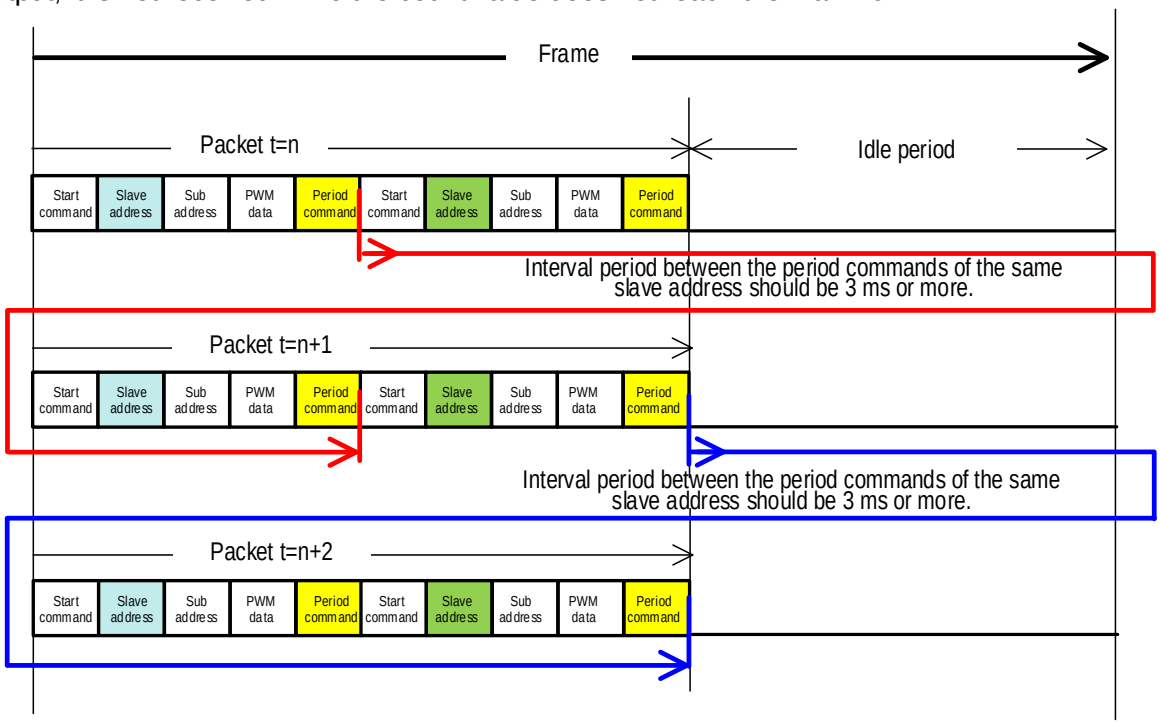


Figure 4-26 Image of packet communication to the IC with the same slave address when using two ICs with different slave addresses (Single-wire input)

< Attention >

4.2.9. Errata: Errata make the next input format into non-reception state according to the end timing of SCLK transmission.

Errata occur when **using both TB62D786FTG with 9 channels and TB62D787FTG with 24 channels (Single-wire input)**.
Figure 4-27 is the timing charts when DATA-IN is demodulated to SCLK internally (hereafter internal SCLK). It shows update and reception reset of PWM DATA (DATA ”A”) when the first internal PWM counter after the period command is 127.
The period of one packet varies depending on the number of input formats and the frequency of the internal SCLK. Since transmissions of the internal SCLK and the internal PWM clocks are asynchronous, the timing of the period command and that of PWM DATA transmission and reception reset exist randomly in one cycle (up to 3 ms) of the internal PWM counter.

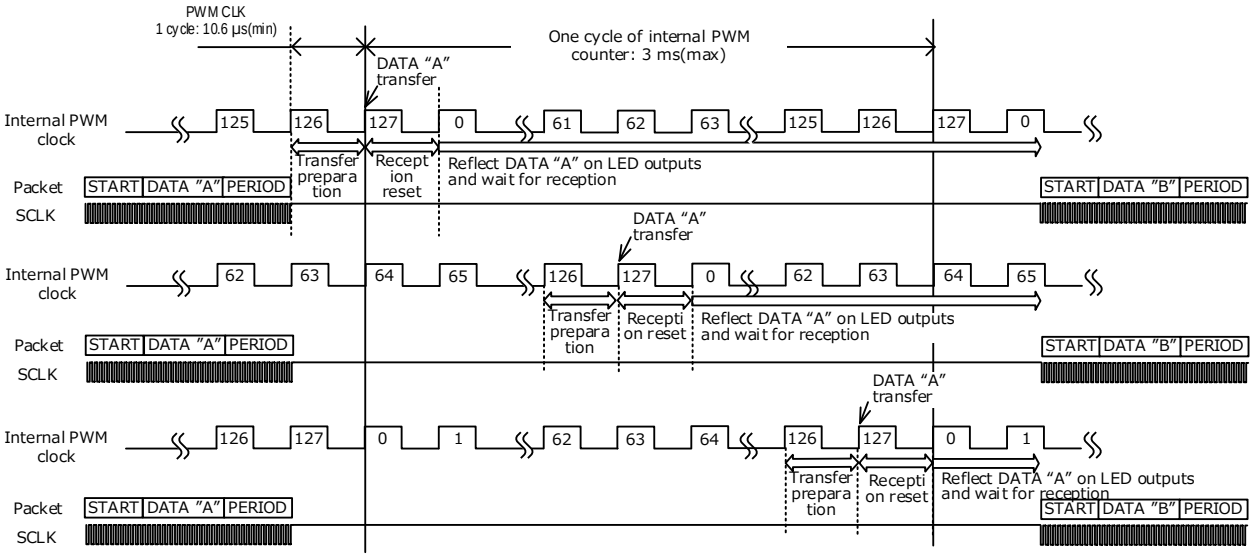


Figure 4-27 Update and reception reset timing of PWM DATA after the period command (after demodulated)

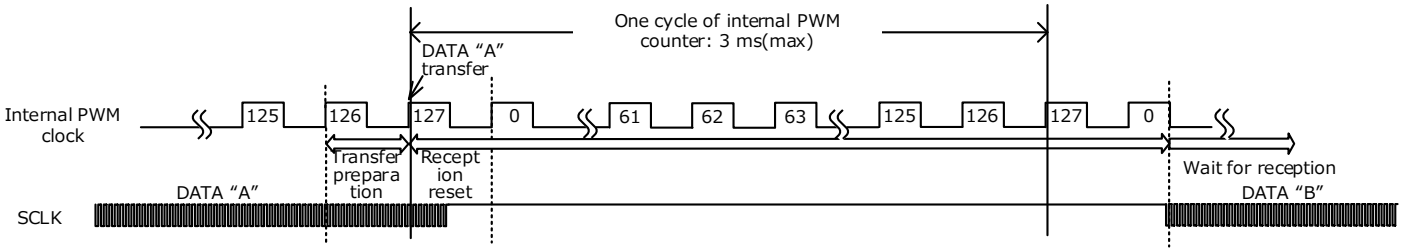


Figure 4-28 Timing of SCLK transmission when errata occur (after demodulated)

Errata occur in accordance with the end timing of the internal SCLK transmission.
The timing of the figure 4-28 nearly corresponds to the top timing chart in the figure 4-28.
In this timing, the internal SCLK transmission stops during reception reset.
Therefore, the reception reset continues until the next packet starts. After it finishes at the beginning of the next packet, the packet moves to the reception waiting status. So, DATA “B” at the beginning of the packet is not received.
When errata occur, the communication continues with the received DATA “A” even in the next packet from above reasons.
Errata do not occur when the internal SCLK transmission stops during the transfer preparation (10.6 µs (min)).

< Attention >

4.2.10. Errata generation and their avoidance method (Single-wire input)

The reception reset that continues until the beginning of the next packet is completed with one internal SCLK input. Therefore, when errata occur, **it is recommended to adopt the avoidance methods shown in the figure 4-30 and the figure 4-31** to finish the reception reset.

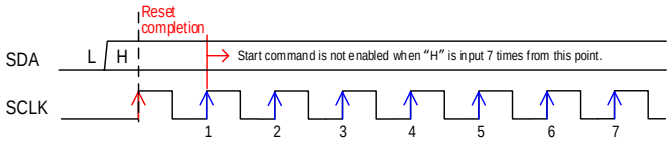


Figure 4-29 Errata generation by start command error (after demodulated)

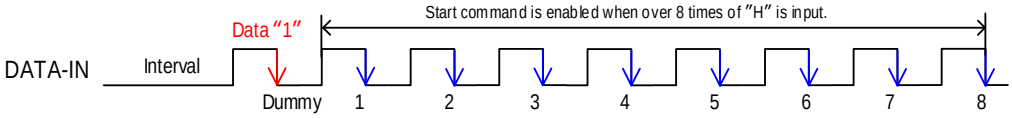


Figure 4-30 Errata avoidance method (1): Adding one data"1". (Single-wire input) (Example)

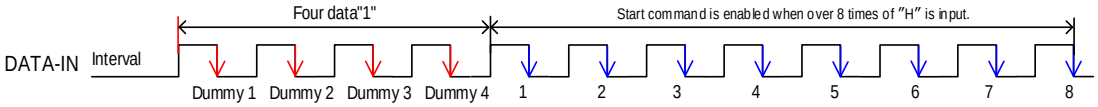


Figure 4-31 Errata avoidance method (2): Adding 4 data "1" (Single-wire input) (Example)

4.2.11. Detail description of errata (Single-wire input)

Occurrence of errata depends on the PWM counter timing. Figure 4-32 and the figure 4-33 show the timing charts, where errata do not occur (charts of DATA-IN (1) and (2)) and occur (charts of DATA-IN (3), (4), and (5)).

Figure 4-32 shows the example when 127th PWM counter timing comes earlier, and the figure 4-33 shows when it comes later.

In the charts of DATA-IN (3), (4), and (5), the internal SCLK transmission stops during the period between (B) and (C) where PWM DATA updates and resets. Therefore, the reset is not completed until the up edge of the internal SCLK is recognized at (D). So, the MSB DATA at (D) is invalidated and the start command is not enabled. As a result, its input format becomes in the non-receiving state.

At this time, the IC operation continues by the received PWM DATA, and does not freeze.

In the case that the packet is consisted of two or more input formats, the second and subsequent input formats are always received because the reset, which had been interrupted at (D), has completed and the reception status becomes enabled.

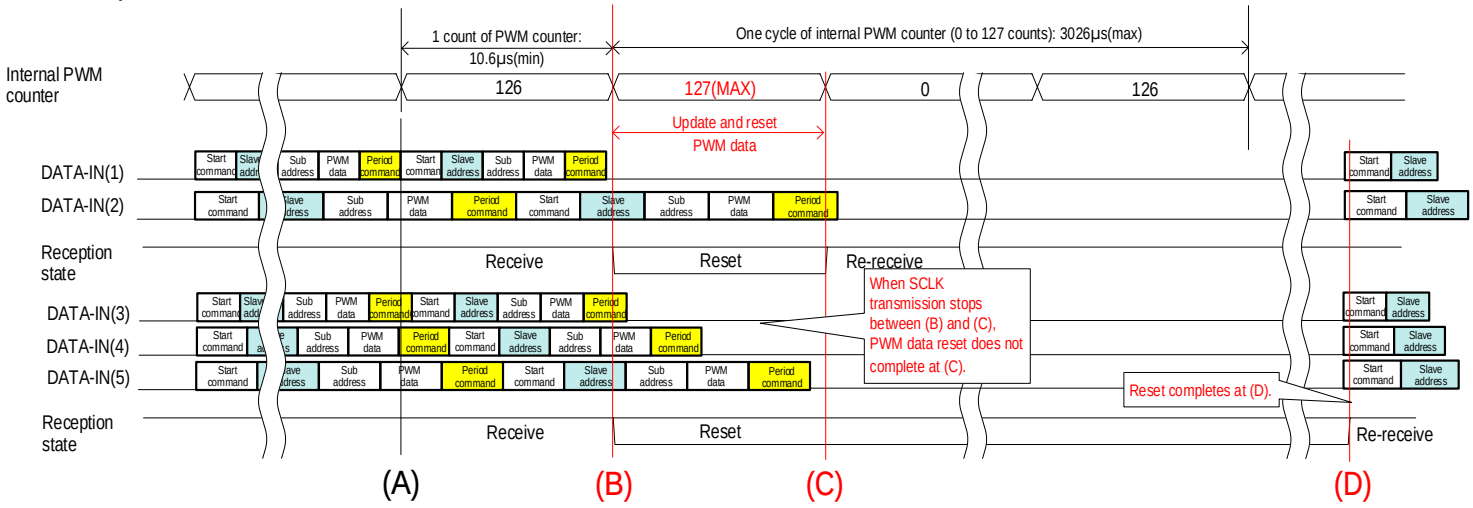


Figure 4-32 Relation of DATA-IN and PWM counter: 127th PWM counter timing comes earlier (Single-wire input)

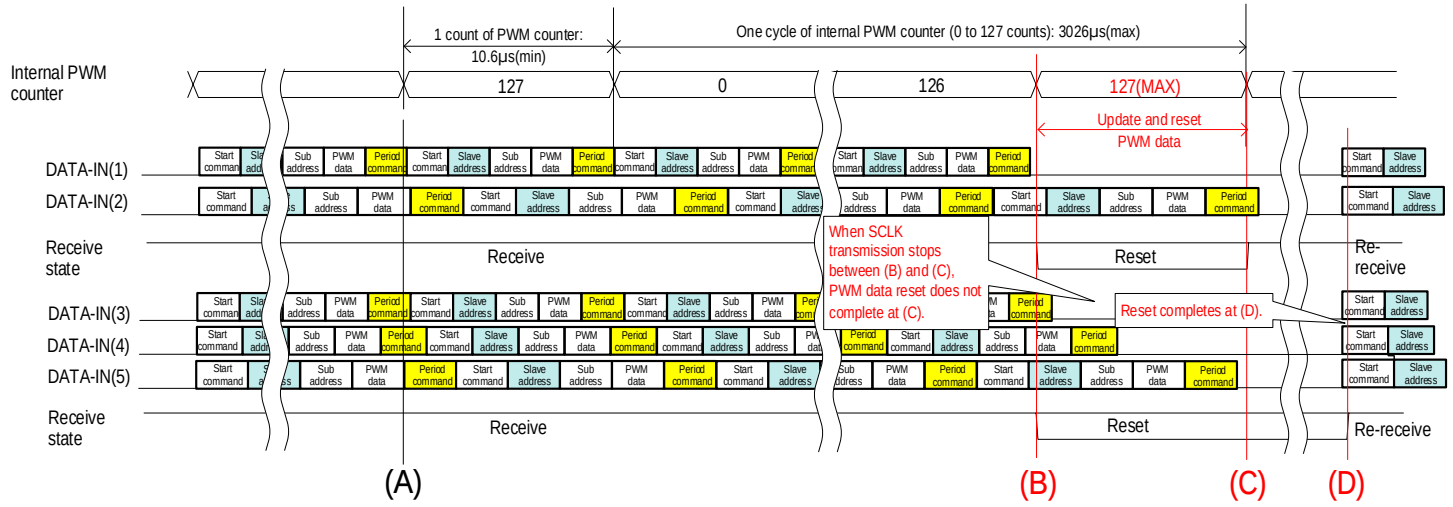


Figure 4-33 Relation of DATA-IN and PWM counter: 127th PWM counter timing comes later (Single-wire input)

126th PWM counter (10.6 µs (min)) has a preparation period of DATA transference that performs without internal SCLK transmission.
Also, the maximum period of the PWM counter cycle, Also, the maximum period of the PWM counter cycle, where the 127th PWM counters exist randomly, is 3026 µs. Therefore, the length of the packet, in which errata do not occur, can be calculated as follows.

Condition example: SCLK transmission: 28 bytes per 1 format, 8 clocks per 1 byte, frequency = 1 MHz.
When SCLK packet is short: Shorter than the following value; 8 clocks÷1 MHz×28 bytes+10.6 µs = 224 µs+10.6 µs = 234.6 µs
When SCLK packet is long: Longer than the following value; 8 clocks÷1 MHz×28 bytes+3026 µs = 224 µs+3026 µs = 3250 µs
However, it is difficult to visually recognize the occurrence of errata even if the DATA of the beginning input format of the next packet is not received, because the LED can illuminate by using the prior PWM DATA which is not influenced by errata. Therefore, it is difficult to verify errata existence. Moreover, the control of the packet length is complicated. So, the errata avoidance method described in the chapter 4.2.10 is recommended.

4.3. Method of generating the single-wire input signal (used for TB62D786FTG and TB62D787FTG) from the 2-wire input signal (used for TB62781FNG and TB62D612FTG)

Input formats are the same for 2-wire input type (TB62781FNG and TB62D612FTG) and for single-wire input type (TB62D786FTG and TB62D787FTG).
The single-wire input signal can be generated by ExOR calculation of the 2-wire input signal. Because SPI signal is an easy-to-handle signal, conversion from the 2-wire input signal to the signal-wire input signal for communication is possible.

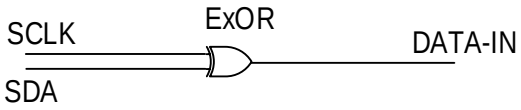


Figure 4-34 Logic description of SCLK and SDA, and DATA-IN

The reference circuit is shown below.
When performing the ExOR calculation, a glitch generates due to SPI signal delays. And a reception error occurs in a single-wire input communication. To avoid this, a glitch avoidance circuit is provided.
Figure 4-35 shows the conversion circuit that uses one ExOR (TC74VHC86) and one D flip-flop (TC7WH74). The timing chart of the conversion circuit is shown in the figure 4-36.

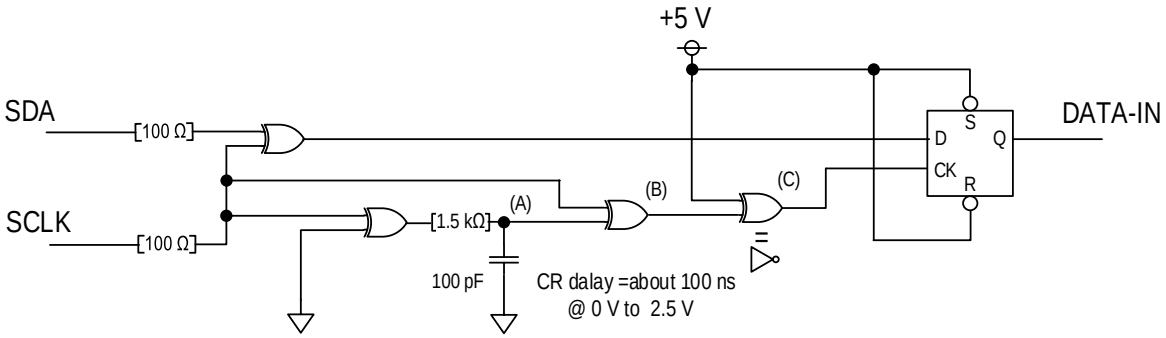


Figure 4-35 Conversion circuit (from SCLK and SDA to DATA-IN)

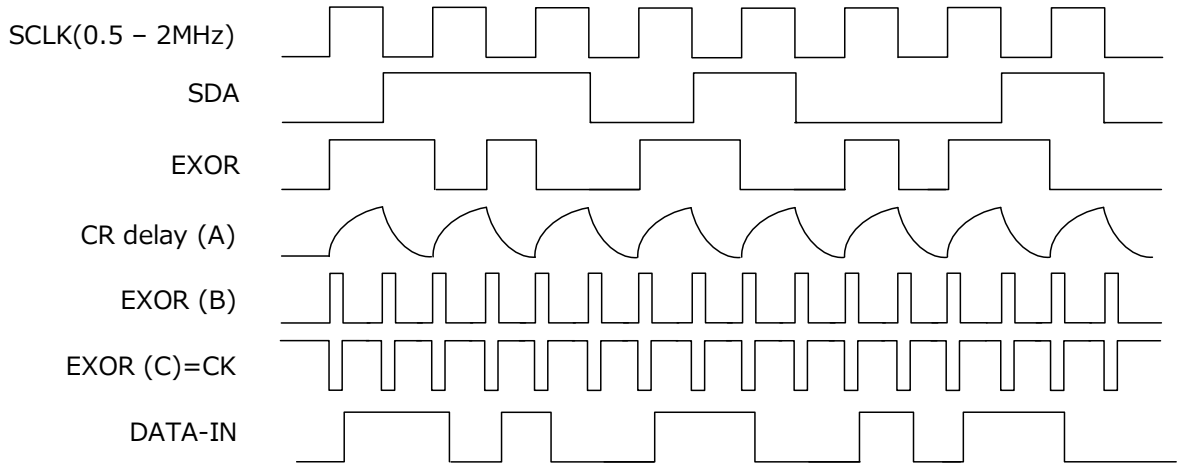


Figure 4-36 Timing charts of the conversion circuit

Note: The delayed waveforms occurred at (A) in the figure are reflected on the ExOR input directly.
Some CMOS logic products do not indicate slow clocks. However, the wire between the gates is shortened for noise reduction. Also, the waveforms continuously rise and fall. So, there are no problems in the circuit operation.
The buffer for the Schmitt trigger input can be inserted between (A) and the ExOR input as required.

5. Power Consumption and Heat Radiation Design

5.1. Power consumption

The power of the constant current LED driver IC is consumed by two parts: “the constant current outputs”, and “the logic block and 5 V regulator circuit”.

5.1.1. Power consumed by the constant current outputs: P(out)

As described in the section 3.3, the difference voltage between LED power supply (VL) and LED (Vf) is applied to the constant current outputs.
Since the constant current drive is enabled when the output voltage exceeds 0.4 V (TB62781FNG or TB62D612FTG) or 0.5 V (TB62D786FTG or TB62D787FTG), connect the external resistor (RR) or control the lighting rate in order to prevent the power consumption from concentrating on the IC.

5.1.2. Power consumed by the logic block and the 5 V regulator circuit

When supplying Vcc from the VLOUT in using TB62D786FNG and TB62D787FTG (Single-wire input), the power consumed by the 5 V regulator circuit must be considered in addition to the power consumed by the logic block.

5.1.2.1. Power consumed by the logic block: P (LOGIC)

Power is consumed at V_{CC} pin where the current of I_{CC} flows. The approximate formula is P(LOGIC) = Vcc×I_{CC}.

5.1.2.2. Power consumed by the 5 V regulator circuit: P (VL)

It is consumed only by a single-wire input LED drivers.
The 5 V regulator, which generates VLOUT (about 5 V) from the main power supply (VL), consumes the power.
The larger the differential voltage between the main power supply (VL) and VLOUT (about 5 V), the larger the power consumption becomes.
The 5 V regulator ensures the current supply of up to 15 mA for external components in addition to I_{CC}.
So, P(VL) can be calculated as follows; P(VL)=(VL-VLOUT)×(ICC + up to 15 mA).

5.2. Heat radiation design

When illuminating multiple channels at the same time with a large current, the heat radiation should be properly designed so as not to exceed the specified junction temperature (Tj) even for a moment.

$T_j = P \times R_{th\ (j\text{-}a)} + T_a$

$R_{th\ (j\text{-}a)}$: junction - T_a heat resistance
T_a: Ambient temperature

The maximum of the junction temperature (Tj) is 150°C. Considering the margin of approximately 20% is recommended for the thermal design.
Rth (j-a) is influenced by IC peripheral conditions. Refer to the power dissipation graph and the absolute maximum rating of each product.

5.3. Derating graphs

5.3.1. Derating graph and power dissipation of TB62781FNG (Vcc=5 V and $V_{OUT(ON)}$=1.0 V, when mounted on a board.)

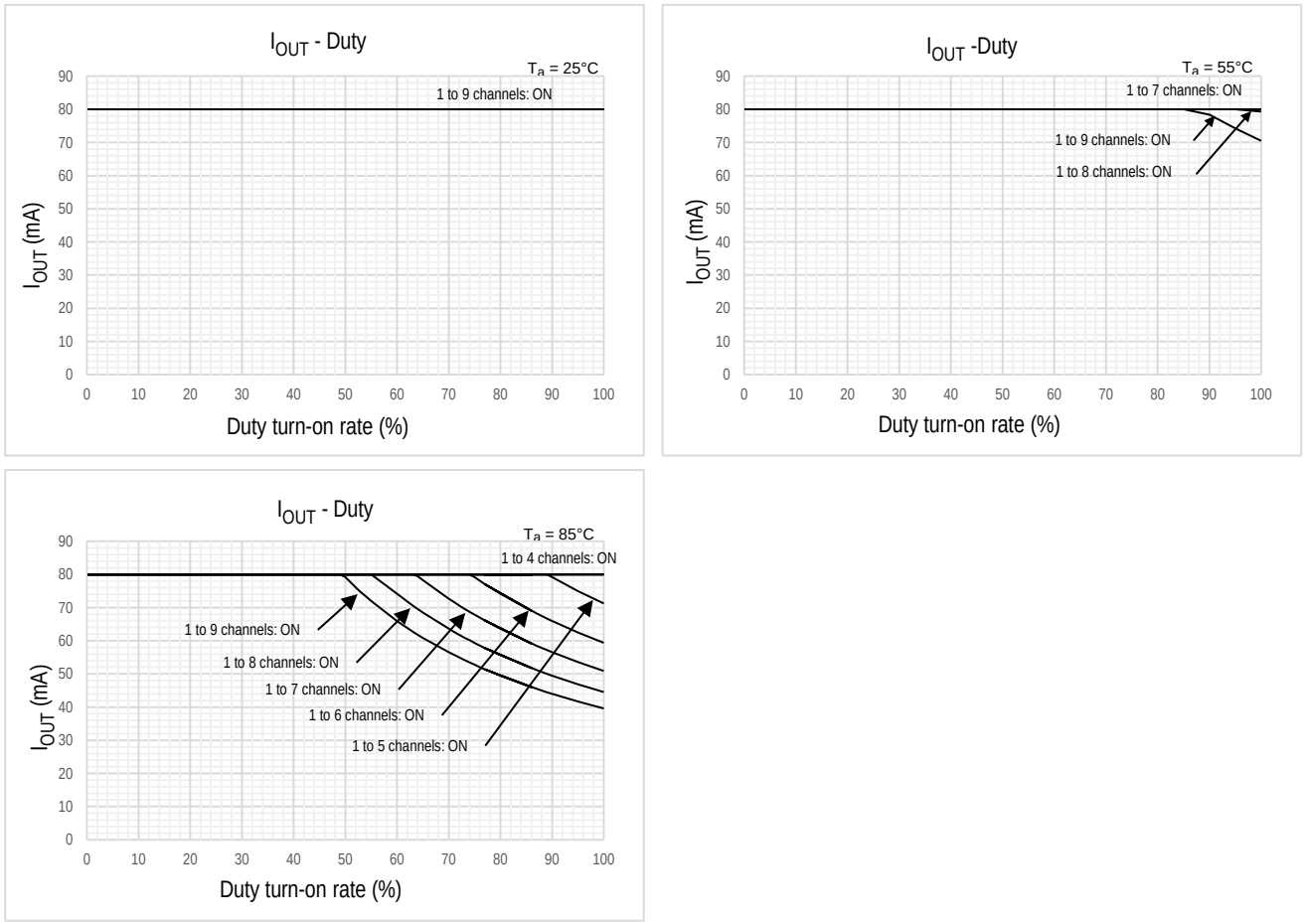


Figure 5-1 Derating graph (Tj=135°C, Ta=25°C, 55°C, or 85°C, and $V_{OUT(ON)}$=1.0 V) (for reference only)

Above three graphs show relations of duty and I_{OUT} at Ta of 25°C, 55°C, and 85°C, respectively (conditions; $V_{OUT(ON)}$=1.0 V and the maximum junction temperature (Tj)=135°C). When $V_{OUT(ON)}$ is higher than 1.0 V, P(out) becomes greater than the value shown in the graph. So, I_{OUT} or duty should be restricted more tightly than conditions of the graph. I_{OUT} range that guarantees a current accuracy is from 5 mA to 40 mA.

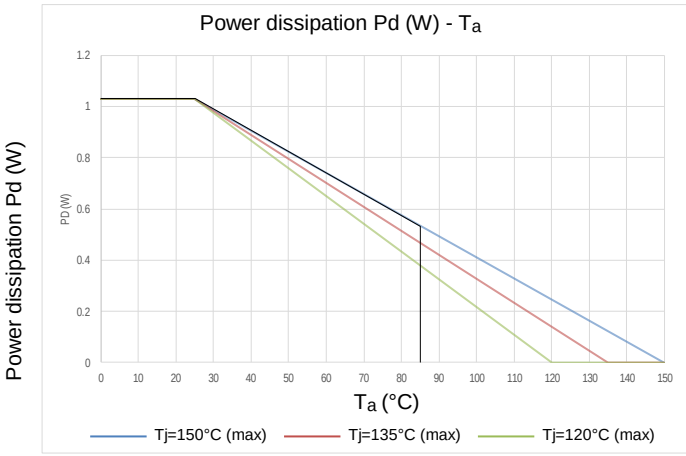


Figure 5-2 Power dissipation when maximum of Tj is 120°C, 135°C, or 150°C

The power dissipation range at Tj=150°C corresponds to the area enclosed with the black line in the figure 5-2. The maximum power dissipation is gained when Ta is from 0°C to 25°C. Upper limit of Ta is 85°C that is the maximum of the operating temperature. For thermal designing, refer to the power dissipations at Tj=135°C and Tj=120°C shown in the figure 5-2 and take the temperature margins.

5.3.2. Derating graph and power dissipation of TB62D612FTG (Vcc=5 V and $V_{OUT(ON)}$=1.0 V, when mounted on a board.)

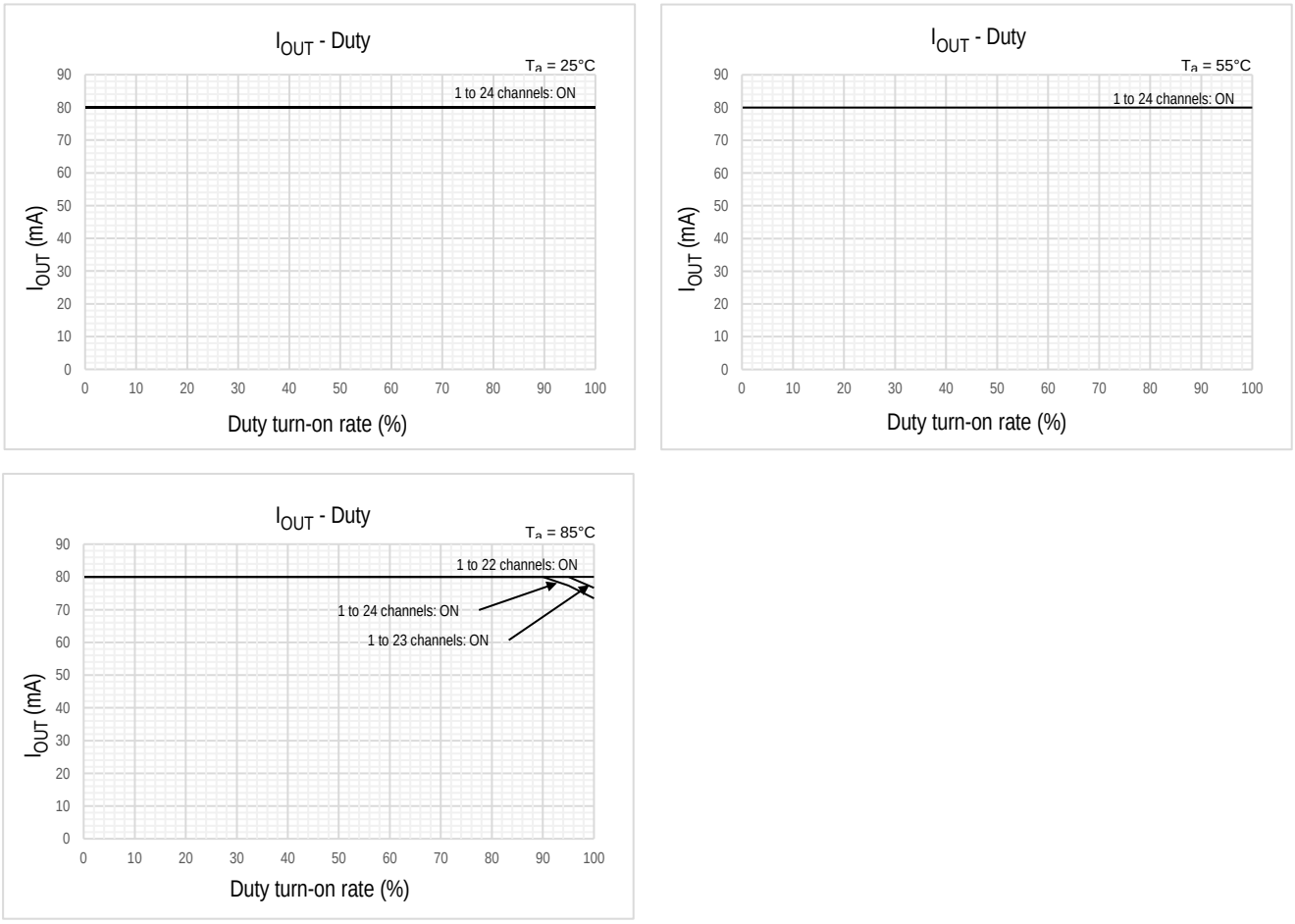


Figure 5-3 Derating graph (Tj=135°C, Ta=25°C, 55°C, or 85°C, and $V_{OUT(ON)}$=1.0 V) (for reference only)

Above three graphs show relations of duty and I_{OUT} at Ta of 25°C, 55°C, and 85°C, respectively (conditions; $V_{OUT(ON)}$=1.0 V and the maximum junction temperature (Tj)=135°C). When $V_{OUT(ON)}$ is higher than 1.0 V, P(out) becomes greater than the value shown in the graph. So, I_{OUT} or duty should be restricted more tightly than conditions of the graph. I_{OUT} range that guarantees a current accuracy is from 5 mA to 40 mA.

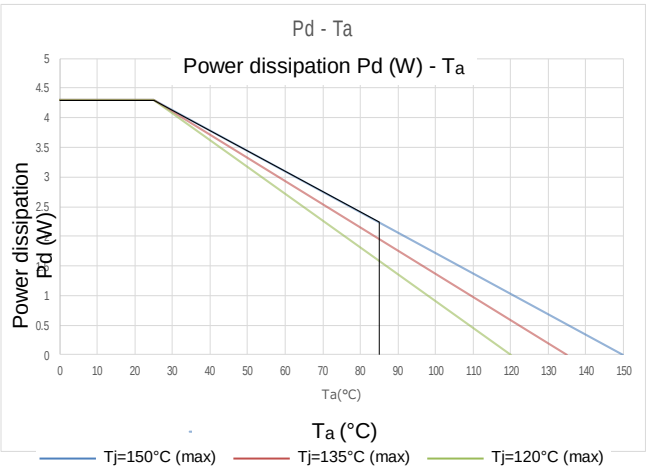


Figure 5-4 Power dissipation when maximum of Tj is 120°C, 135°C, or 150°C

The power dissipation range at Tj=150°C corresponds to the area enclosed with the black line in the figure 5-4. The maximum power dissipation is gained when Ta is from 0°C to 25°C. Upper limit of Ta is 85°C that is the maximum of the operating temperature. For thermal designing, refer to the power dissipations at Tj=135°C and Tj=120°C shown in the figure 5-4 and take the temperature margins.

5.3.3. Derating graph and power dissipation of TB62D786FTG (Vcc=5 V and $V_{OUT(ON)}$=1.0 V, when mounted on a board.)

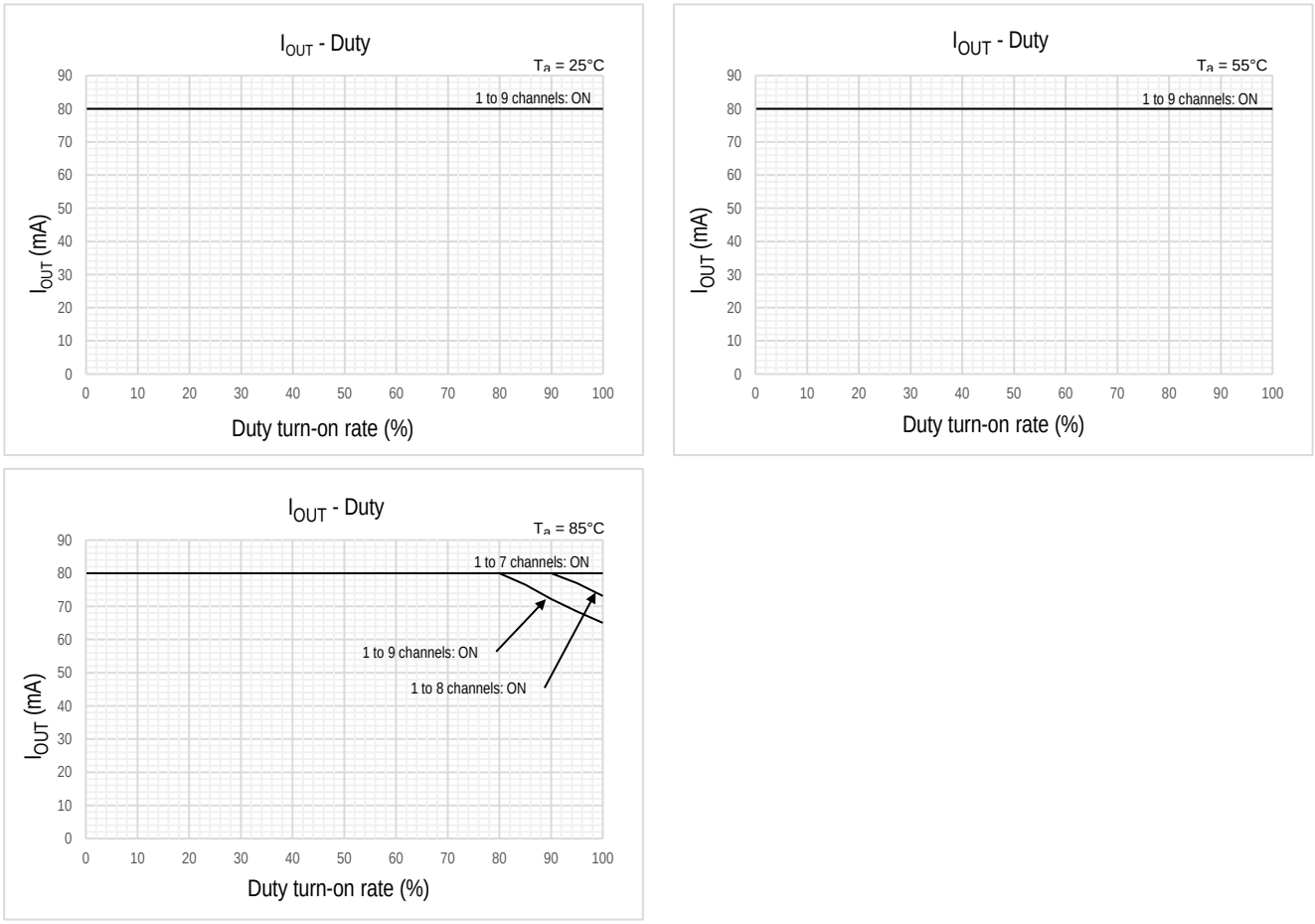


Figure 5-5 Derating graph (Tj=135°C, Ta=25°C, 55°C, or 85°C, and $V_{OUT(ON)}$=1.0 V) (for reference only)

Above three graphs show relations of duty and I_{OUT} at Ta of 25°C, 55°C, and 85°C, respectively (conditions; $V_{OUT(ON)}$=1.0 V and the maximum junction temperature (Tj)=135°C). When $V_{OUT(ON)}$ is higher than 1.0 V, P(out) becomes greater than the value shown in the graph. So, I_{OUT} or duty should be restricted more tightly than conditions of the graph. I_{OUT} range that guarantees a current accuracy is from 5 mA to 40 mA.

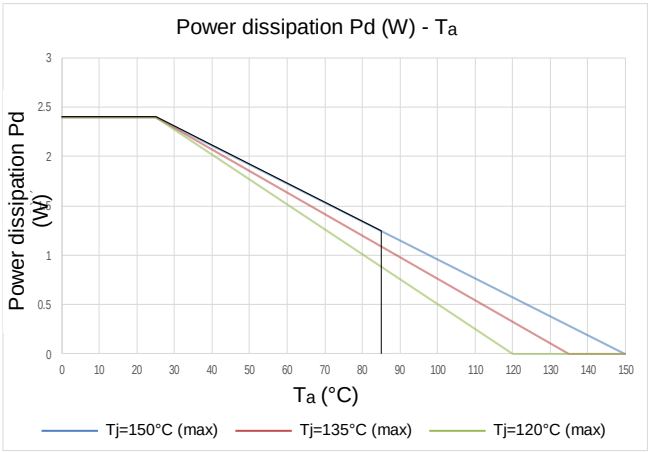


Figure 5-6 Power dissipation when maximum of Tj is 120°C, 135°C, or 150°C

The power dissipation range at Tj=150°C corresponds to the area enclosed with the black line in the figure 5-6. The maximum power dissipation is gained when Ta is from 0°C to 25°C. Upper limit of Ta is 85°C that is the maximum of the operating temperature. For thermal designing, refer to the power dissipations at Tj=135°C and Tj=120°C shown in the figure 5-6 and take the temperature margins.

5.3.4. Derating graph and power dissipation of TB62D787FTG (Vcc=5 V and $V_{OUT(ON)}$=1.0 V, when mounted on a board.)

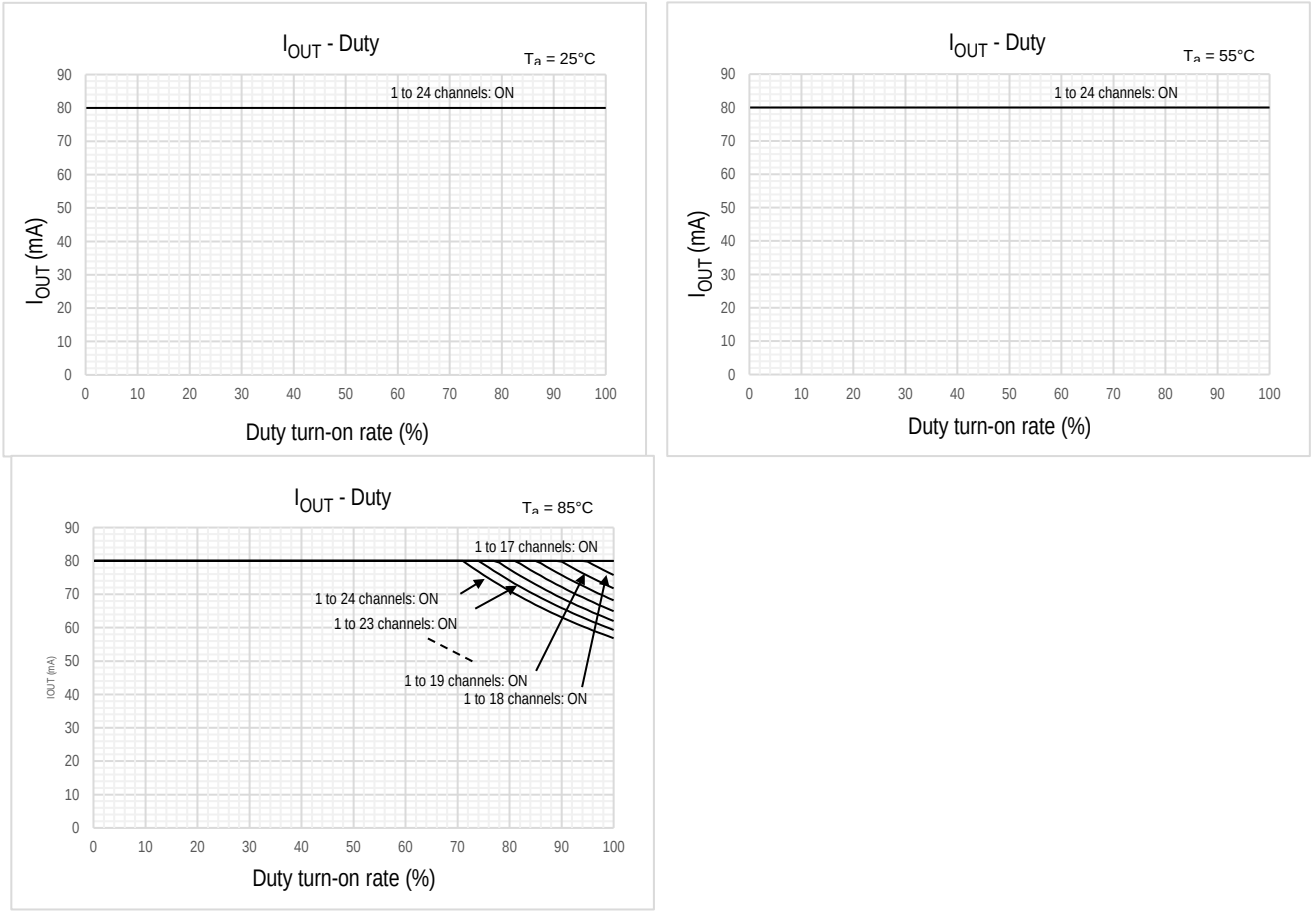


Figure 5-7 Derating graph (Tj=135°C, Ta=25°C, 55°C, or 85°C, and $V_{OUT(ON)}$=1.0 V) (for reference only)

Above three graphs show relations of duty and I_{OUT} at Ta of 25°C, 55°C, and 85°C, respectively (conditions; $V_{OUT(ON)}$=1.0 V and the maximum junction temperature (Tj)=135°C). When $V_{OUT(ON)}$ is higher than 1.0 V, P(out) becomes greater than the value shown in the graph. So, I_{OUT} or duty should be restricted more tightly than conditions of the graph. I_{OUT} range that guarantees a current accuracy is from 5 mA to 40 mA. When output current exceeds 40 mA, supply VLOUT only for TB62D787FTG.

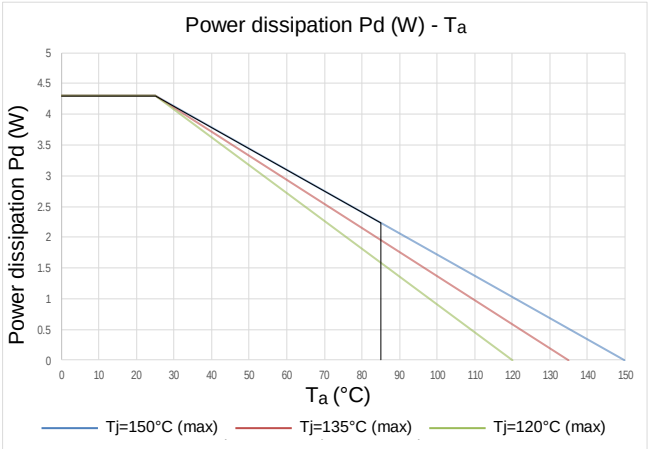


Figure 5-8 Power dissipation when maximum of Tj is 120°C, 135°C, or 150°C

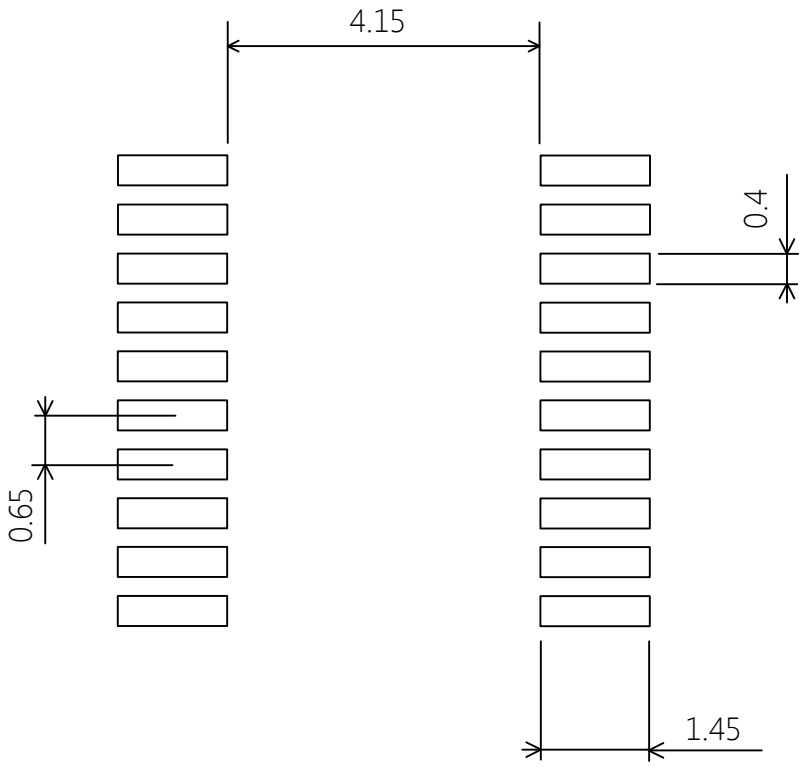
The power dissipation range at Tj=150°C corresponds to the area enclosed with the black line in the figure 5-8. The maximum power dissipation is gained when Ta is from 0°C to 25°C. Upper limit of Ta is 85°C that is the maximum of the operating temperature. For thermal designing, refer to the power dissipations at Tj=135°C and Tj=120°C shown in the figure 5-8 and take the temperature margins.

6. Foot Pattern (for reference only)

6.1. Foot pattern of TB62781FNG (for reference only)

SSOP20-P-225-0.65A

Unit: mm

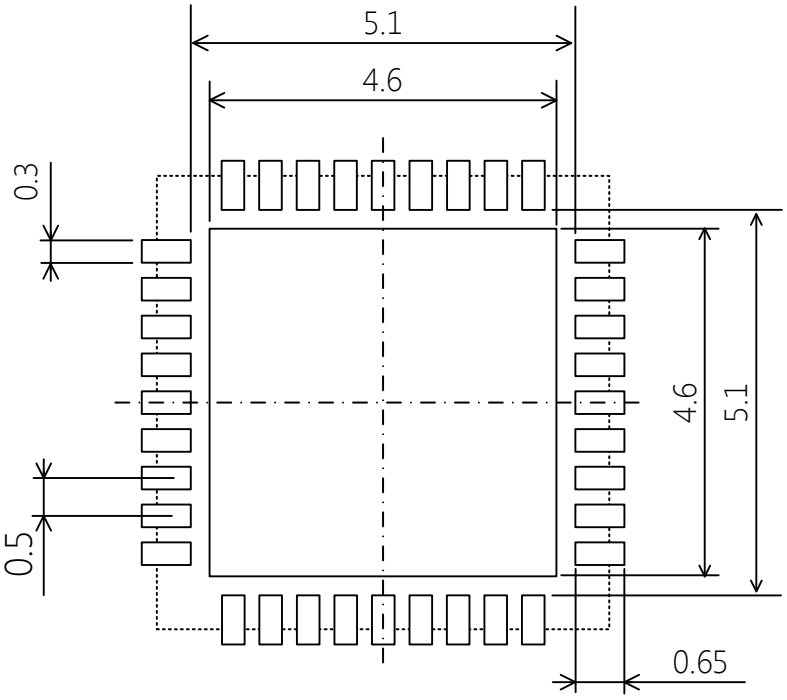


Notes

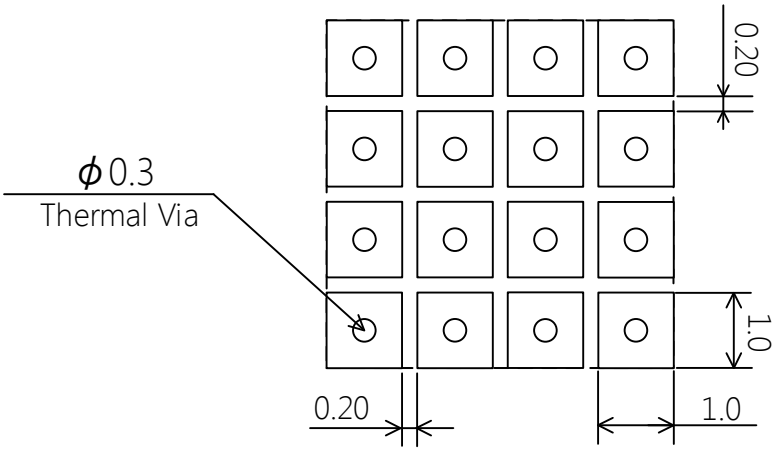
- All linear dimensions are given in millimeters unless otherwise specifies.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. Accuracy and completeness of drawings and information are not guaranteed.
- Customers are solely responsible for all aspects of their own land pattern, including but not limited to soldering processes.
- The drawing in this document may not accurately represent the actual shape or dimensions. Do not design the circuit by estimating the dimensions of the actual product from figures and others in this document.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant information of this document and the instructions for the application that product will be used with or for.

6.2. Foot pattern of TB62D612FTG (for reference only)

P-WQFN36-0606-0.50-001
Unit: mm



Thermal pad via (image)



Place thermal via on the thermal pad that is on the back of the QFN package. And all the grounding patterns of the product should run on the solder mask of the PCB.
Thermal pad size is 4.6 mm×4.6 mm. This via pattern is for reference only.

Notes

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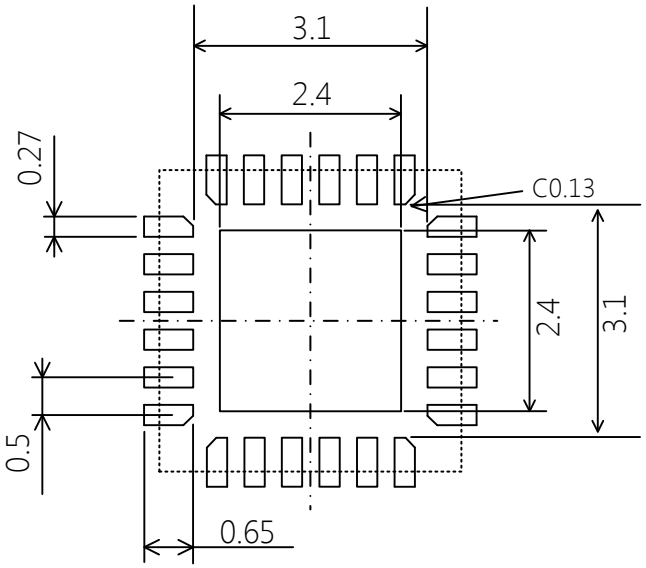
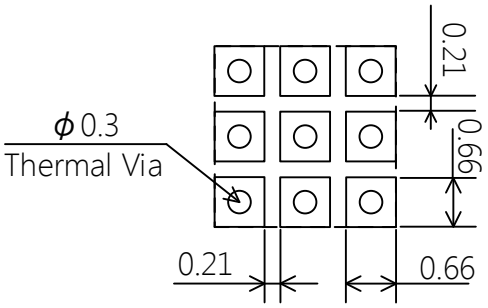
6.3. Foot pattern of TB62D786FTG (for reference only)

P-VQFN24-0404-0.50-001

Unit: mm



Thermal pad via (image)



Place thermal via on the thermal pad that is on the back of the QFN package. And all the grounding patterns of the product should run on the solder mask of the PCB.
Thermal pad size is 2.4 mm×2.4 mm. This via pattern is for reference only.

Notes

- All linear dimensions are given in millimeters unless otherwise specifies.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. Accuracy and completeness of drawings and information are not guaranteed.
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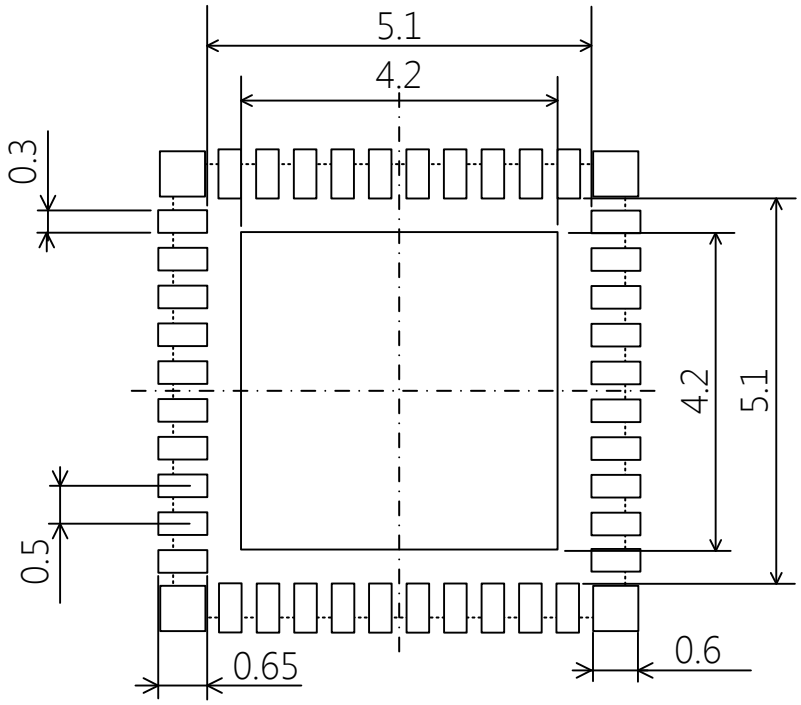
- The drawing in this document may not accurately represent the actual shape or dimensions. Do not design the circuit by estimating the dimensions of the actual product from figures and others in this document.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant information of this document and the instructions for the application that product will be used with or for.

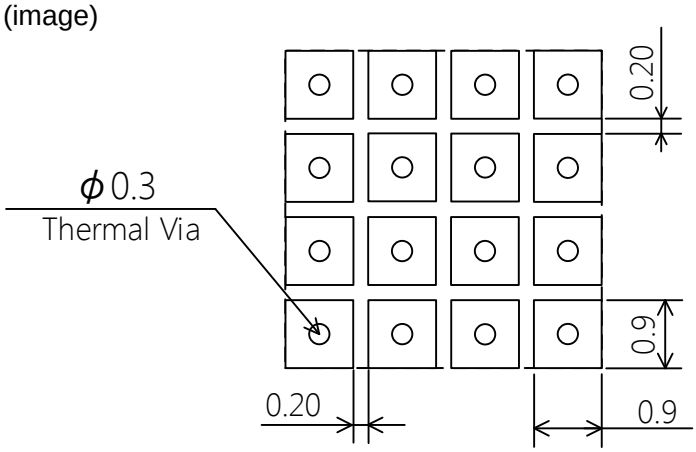
6.4. Foot pattern of TB62D787FTG (for reference only)

P-VQFN40-0606-0.50-001

Unit: mm



Thermal pad via (image)



Place thermal via on the thermal pad that is on the back of the QFN package. And all the grounding patterns of the product should run on the solder mask of the PCB.

Thermal pad size is 4.2 mm×4.2 mm. This via pattern is for reference only.

Notes

- All linear dimensions are given in millimeters unless otherwise specifies.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. Accuracy and completeness of drawings and information are not guaranteed.
- Customers are solely responsible for all aspects of their own land pattern, including but not limited to soldering processes.
- The drawing in this document may not accurately represent the actual shape or dimensions. Do not design the circuit by estimating the dimensions of the actual product from figures and others in this document.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant information of this document and the instructions for the application that product will be used with or for.

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Any license to any industrial property rights is not granted by provision of these application circuit examples.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Points to remember on handling of ICs

(1) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(2) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

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