Bipolar Transistors
Maximum ratings

Description

This document describes the maximum ratings of bipolar transistors.

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1. Ratings of transistors

1.1. Maximum ratings of transistors

For transistors, the maximum allowable current, voltage, power dissipation and other parameters are specified as maximum ratings.

In designing a transistor circuit, understanding maximum ratings is crucial to ensure that transistors operate within the target operating time and with sufficient reliability.

One of the characteristics of semiconductor devices including transistors is that their electrical characteristics are very sensitive to temperature. Therefore, the maximum ratings are determined by considering the temperature rise of the device. When a voltage applied to a transistor is constant, its electrical conductivity increases with the ambient temperature. Consequently, a current flowing through the transistor increases, increasing the power consumed. This, in turn, causes the temperature to rise further. If the temperature exceeds a limit, the transistor is eventually damaged.

In order to ensure the expected useful life and reliability of transistors, their maximum ratings must not be exceeded. Since the maximum ratings are limited by the materials, circuit designs, and manufacturing conditions used, they differ from transistor to transistor. For transistors, the maximum ratings are defined based on the absolute maximum rating approach.

The absolute maximum ratings are the highest values that must not be exceeded during operation even instantaneously. When two or more ratings are specified, two ratings can not be applied to the transistor at the same time.

Exposure to a condition exceeding a maximum rating may cause permanent degradation of its electrical characteristics. Care should be exercised as to supply voltage bounces, variations in the characteristics of circuit components, possible exposure to stress higher than the maximum ratings during circuit adjustment, changes in ambient temperature, and input signal fluctuations.

The maximum ratings of transistors are mainly decided with respect to emitter, base, and collector currents, terminal-to-terminal voltages, collector power dissipation, junction temperature, and storage temperature. These parameters are interrelated and cannot be considered separately. They also depend on external circuit conditions.

1.2. Voltage ratings

A transistor composes an input/ output circuit containing an emitter, base or collector. Either terminal is used as a common terminal in the circuit. Therefore, the collector-base voltage V_{CB}, collector-emitter voltage V_{CE}, and emitter-base voltage V_{EB} ratings are specified for transistors. There are two types of breakdown voltages that determine the voltage ratings: those inherent to a transistor such as $V_{(BR)CBO}$ and $V_{(BR)CEO}$ and those dependent on the base circuit conditions such as $V_{(BR)CER}$ and $V_{(BR)CEX}$.

(1) Collector voltage ratings

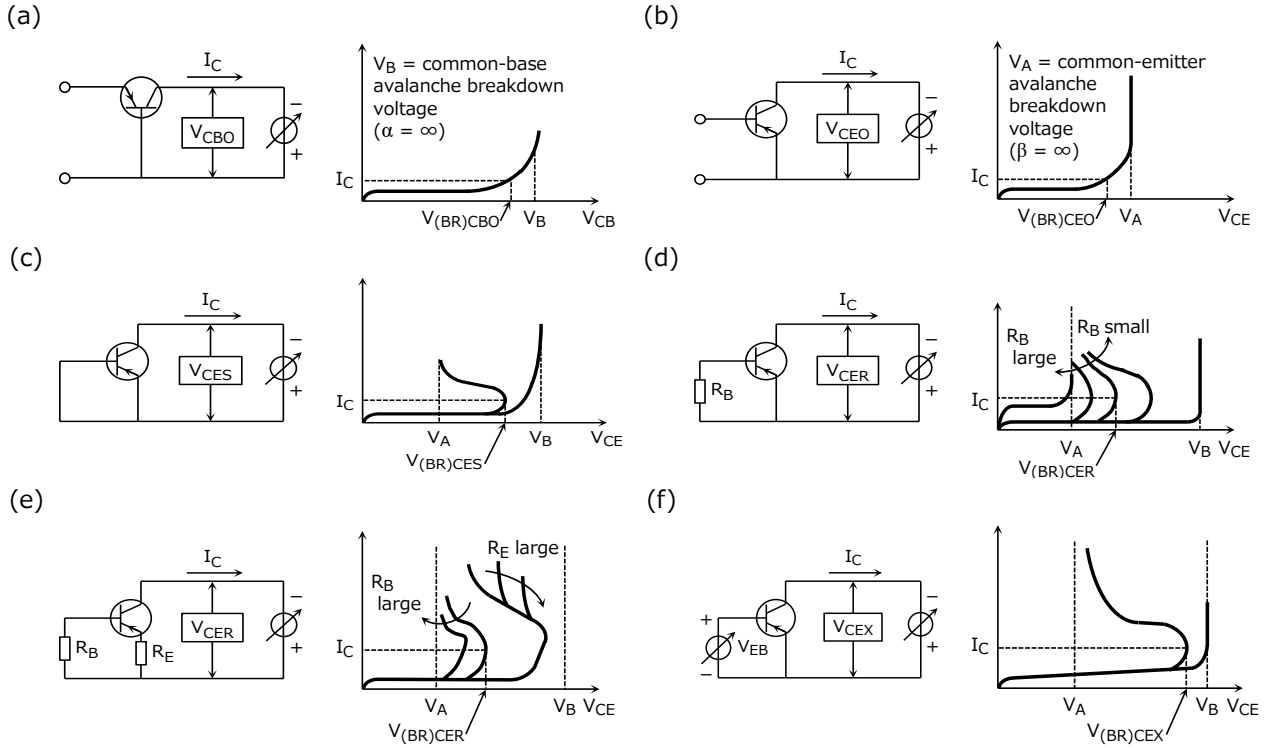


Figure 1.1 Collector breakdown voltages

The collector voltage ratings are important since bipolar transistors are generally used in the common-base or common-emitter configuration.

Figure 1.1 shows various collector breakdown voltages specified for bipolar transistors, which are defined as:

$V_{(BR)CBO}$: Collector-base breakdown voltage with emitter open

$V_{(BR)CEO}$: Collector-emitter breakdown voltage with base open

$V_{(BR)CES}$: Collector-emitter breakdown voltage with base short-circuited to emitter

$V_{(BR)CER}$: Collector-emitter breakdown voltage with resistor between base and emitter

$V_{(BR)CEX}$: Collector-emitter breakdown voltage with base and emitter reverse-biased

The collector breakdown voltages have the following relationship:

$V_{(BR)CBO} > V_{(BR)CES} > V_{(BR)CEX} > V_{(BR)CER} > V_{(BR)CEO}$

The values of $V_{(BR)CBO}$ and $V_{(BR)CES}$ are almost the same.

(a) Collector-base breakdown voltage with emitter open: $V_{(BR)CBO}$

– Common-base avalanche breakdown voltage (V_B) –

$V_{(BR)CBO}$ is equivalent to the characteristics of the collector-base diode of a transistor.

When the collector and base terminals are biased in the reverse direction, a very small cut-off current (I_{CBO}) flows between the collector and base. As the reverse voltage is increased, the electric field in the depletion region of the pn junction increases.

As a result, minority carriers gain sufficient energy from the electric field and the minority carriers collide with silicon atoms in the depletion region, which break the covalent bonds and generate electron-hole pairs. When the electric field is strong enough, the charge carriers are accelerated to high enough speeds to knock other bound electrons free, creating more free charge carriers. This knocking-out process continues, rapidly increasing the current and creating avalanche multiplication. This avalanche breakdown phenomenon limits the maximum voltage that can be applied to a transistor.

The avalanche multiplication coefficient, M, can be empirically determined and given by Equation 1-1:

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{V_B} \right)^n} \quad \cdots\cdots (1\text{–}1)$$

The current amplification factor, α, is:

$$\alpha = \alpha_0 \cdot M \quad \cdots\cdots (1\text{–}2)$$

V_B : Breakdown voltage

V_{CB} : Collector-base voltage

α_0 : Common-base current amplification factor at a voltage that does not cause avalanche multiplication

n : Dependent on the type of a transistor; 2 to 4 for PNP transistors and 2 to 3 for NPN transistors

V_B is determined by the dopant concentration on the high-resistivity side of a junction. The higher the dopant concentration, the smaller the V_B value. The maximum breakdown voltage is determined by V_B. It should be noted, however, that the maximum $V_{(BR)CBO}$ value specified as an absolute maximum rating is a voltage at the specified current. The maximum $V_{(BR)CBO}$ value is smaller than V_B.

The temperature coefficient of V_B is positive because it is related to carrier mobility. Since I_{CBO} increases with temperature, the $V_{(BR)CBO}$ value may become smaller in the low-current region at high temperature.

In a common-base configuration, the collector current I_C is calculated as follows:

$$I_C = \alpha \cdot I_E + M \cdot I_{CBO} \quad \cdots\cdots (1\text{–}3)$$

(b) Collector-emitter breakdown voltage with base open: $V_{(BR)CEO}$

– Common-emitter avalanche breakdown voltage (V_A) –

In a common-emitter configuration, avalanche breakdown occurs when the common-emitter current amplification factor (β) is infinite.

β can be calculated as follows using α_0:

$$\beta = \frac{\alpha_0 \cdot M}{1 - \alpha_0 \cdot M} \quad \cdots\cdots (1\text{–}4)$$

When $\alpha_0 \cdot M = 1$ (i.e., $M = 1/\alpha_0$), β becomes infinite, causing an avalanche multiplication process to occur.

When the voltage applied across the collector and emitter terminals is high, carriers diffuse into the base from the collector. As a result, the base-emitter diode of a transistor is forward-biased, causing the transistor to turn on. When the collector-base voltage V_{CB} reaches V_A, the number of carriers generated by avalanche multiplication equals the number of carriers ($\gamma \cdot \beta_0 = \alpha_0$) that are injected at an emitter injection efficiency of γ and transported to the depletion region at a base transport factor of β_0. This causes the collector current to continue flowing without the need for a base current supply.

Because $M = 1/\alpha_0$, Equation 1-1 can be restated as:

$$\alpha_0 = 1 - \left(\frac{V_{CB}}{V_B} \right)^n \quad \cdots\cdots (1\text{–}5)$$

Solving Equation 1-5 for the common-emitter avalanche breakdown voltage V_A at which $\alpha_0 \cdot M = 1$ gives:

$$V_A = V_B^n \sqrt{1 - \alpha_0} \approx V_{(BR)CEO} \quad \cdots\cdots (1\text{–}6)$$

At a collector voltage lower than V_A, the base current I_B flows in the forward direction, causing β to be positive. At a collector voltage higher than V_A, the base current I_B flows in the reverse direction, causing β to be negative. Figure 1.2 shows the relationship between β and the current amplification factor α as a function of the collector voltage. When the input base current is constant, the collector current I_C of a transistor in a common-emitter configuration can be calculated as follows:

$$I_C = \beta \cdot I_B + (\beta + 1) \cdot M \cdot I_{CBO} \quad \cdots\cdots (1\text{–}7)$$

β : Common-emitter current amplification factor

The temperature dependence of $V_{(BR)CEO}$ is determined by the temperature dependence of V_B, α_0, and I_{CBO} (I_{CEO}). In this case, the temperature coefficient is positive or negative.

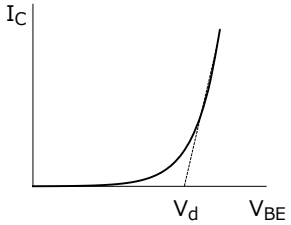
(c) Common-emitter breakdown voltages under different base circuit conditions: $V_{(BR)CER}$, $V_{(BR)CES}$, and $V_{(BR)CEX}$

When the base terminal is connected to the emitter terminal through a resistor (R_B) as shown in Figure 1.1 (d), the collector cut-off current MI_{CBO} flows through the internal base resistor r_b and the external resistor R_B. If the resulting voltage drop $MI_{CBO} \cdot (R_B + r_b)$ causes the base-emitter junction to be forward-biased, emitter injection occurs, leading to collector-emitter breakdown.

The voltage at which this breakdown occurs, $V_{(BR)CER}$, is calculated as follows:

$$V_{(BR)CER} = V_B^n \sqrt{1 - \frac{I_{CBO} \ (R_B + r_b)}{V_d}} \quad \cdots\cdots (1\text{–}8)$$

Vd : Base-emitter threshold voltage



V_{CER} is logarithmically inversely proportional to R_B. Therefore, a transistor exhibits the highest breakdown voltage when $R_B = 0$. $V_{(BR)CES}$ represents the collector-emitter breakdown voltage with base and emitter short-circuited (see Figure 1.1 (c)).

When the base terminal is open-circuited (i.e., when $R_B = \infty$), the transistor behavior is determined by β. At this time, the cut-off current $M \cdot I_{CBO}$ flows through the base terminal of a transistor, causing a collector current equal to $(\beta + 1) \cdot M \cdot I_{CBO}$ to flow. Breakdown occurs at a collector-emitter voltage that causes β to become infinite. This common-emitter voltage is defined above as the common-emitter avalanche voltage V_A.

When R_B is a non-zero value, the breakdown voltage is between V_A and V_B.

When emitter injection begins, the current amplification factor α (= $\alpha_0 \cdot M$) becomes greater than unity while β becomes negative. Figure 1.2 indicates that when $V_{CE} > V_A$, β negatively increases as V_{CE} decreases. At the breakdown point, emitter injection occurs, causing I_C to increase sharply. Due to internal resistance, an increase in I_C causes a drop in collector voltage, which, in turn, causes an increase in β and I_C.

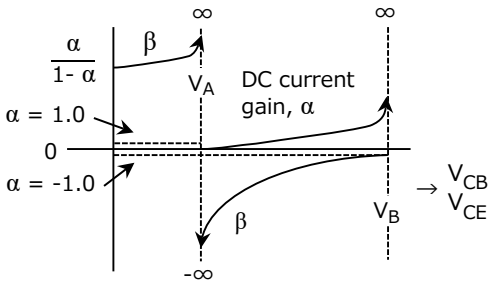


Figure 1.2 Collector voltage vs. current amplification factor

This phenomenon occurs continuously, showing negative resistance characteristics, and causes the breakdown voltage to approach V_A as β tends to ∞.

Figure 1.3 (a) shows the relationship between R_B and breakdown voltage. Figure 1.3 (b) shows the relationships between $V_{(BR)CER}$ and R_B and between I_{CER} and R_B. All these curves depict the same characteristics.

When R_E is connected to the emitter as shown in Figure 1.1 (e), R_E produces a negative feedback effect, causing the breakdown voltage V_A' to increase according to Equation 1-9.

When the base and emitter terminals are reverse-biased as shown in Figure 1.1 (f), a transistor exhibits the highest breakdown voltage at a collector-emitter voltage when emitter injection occurs, as is the case with $V_{(BR)CER}$. As the collector-emitter voltage increases, V_{EB} produces a negative feedback effect, causing the breakdown voltage to approach V_A asymptotically. At this time, the maximum voltage of V_{CEX}, which is given by Equation 1-10, is greater than $V_{(BR)CES}$.

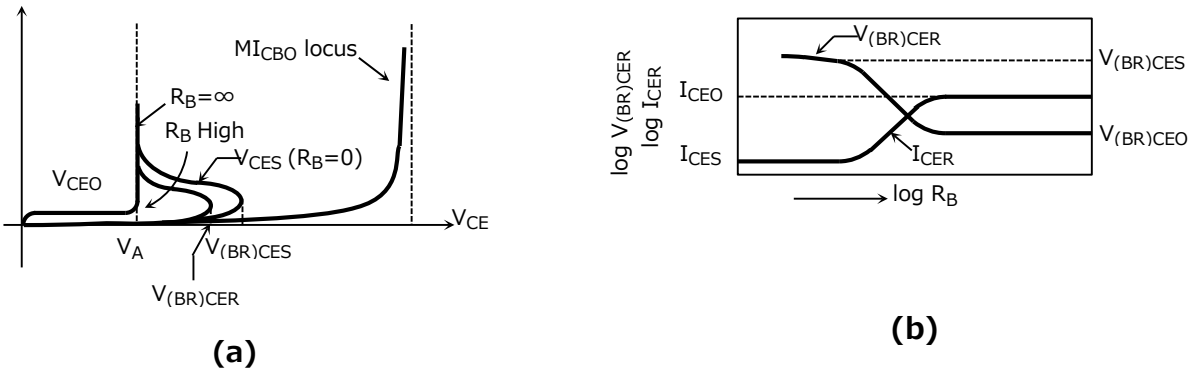


Figure 1.3 Relationship between R_B and breakdown voltage

$$V_A' = V_B^n \sqrt{1 - \frac{\alpha_0 \cdot R_B}{R_B + R_E}} \quad \cdots\cdots (1\text{–}9)$$

$$V_{(BR)CEX} = V_B^n \sqrt{1 - \frac{I_{CBO} \cdot r_b}{V_d + V_{EB}}} \quad \cdots\cdots (1\text{–}10)$$

(2) Emitter-base voltage rating

The emitter-base breakdown voltage with collector open-circuited, $V_{(BR)EBO}$, is qualitatively similar to $V_{(BR)CBO}$. However, since a typical transistor has high dopant concentration in the emitter layer, $V_{(BR)EBO}$ is a few volts. When the breakdown voltage is lower than about 6 V, Zener breakdown occurs due to the tunneling effect instead of the avalanche breakdown described so far.

Care should be exercised to ensure that the base-emitter junction is not reverse-biased at an excessive voltage since this voltage generally degrades or damages a transistor.

(3) Measurement of voltage ratings

The maximum voltage that appears across a given terminal pair is measured by applying a specified current to a specific terminal under specified conditions. Generally, the peak of a half sine wave (e.g., curve tracer) for measurement is adjusted to the specified current value. A DC current must not be used for measurement since a DC current could inflict thermal damage to a device.

1.3. Current ratings

Transistors have plural current ratings: I_{Emax} or the maximum current that can flow through the base-emitter junction in the forward direction and I_{Cmax} or the maximum current that can flow through the collector-base junction in the reverse direction. For most transistors, I_{Cmax} and I_{Emax} are equal. These current ratings are determined, primarily considering the following:

(1) Current that does not lead to an excessive increase in junction temperature, which is caused by a device's power dissipation due to a collector-emitter voltage

(2) Current at which the DC current gain h_{FE} is reduced to one-half to one-third of the peak (Current at which $h_{FE} \approx 10$ for medium-power switching transistors and $h_{FE} \approx 3$ for high-power switching transistors)

(3) Current at which internal wires burn out
Generally, the maximum base current I_{Bmax} is: $I_{Bmax} = \frac{1}{2}$ to $\frac{1}{6} \times I_{Cmax}$

1.4. Temperature ratings

The reliability of a transistor is determined by the constituent materials and the maximum junction temperature, T_{jmax}.

The maximum junction temperature must be considered not only in terms of the functional operation of the transistor but also in terms of its reliability such as device degradation and lifetime.

Generally, the degradation of the transistor accelerates as the junction temperature increases. Let A and B be constants intrinsic to a transistor. Then, the average life in hours of operation, L_m, and the junction temperature in Kelvin (K), T_j, have the following relationship:

$$\log L_m \approx A + \frac{B}{T_j} \quad \cdots\cdots (1\text{–}11)$$

The maximum allowable junction temperature of a transistor is determined, considering its failure rate and reliability. Storage temperature, T_{stg}, is specified as a range over which a transistor can be stored without voltage application. The materials that constitute the transistor and their reliability also determine the storage temperature range.

1.5. Power ratings

The electric power dissipated inside a transistor is converted into thermal energy, increasing its internal temperature.

The power dissipation of a transistor at a given operating point is the sum of the collector power dissipation P_C (= $I_C \cdot V_{CB}$) and the emitter power dissipation (= $I_E \cdot V_{BE}$). Generally, V_{CB} is greater than V_{BE} since the base and emitter terminals are forward-biased. $P_C = I_C \cdot (V_{CB}+V_{BE}) \simeq I_C \cdot V_{CE}$, Because $I_C \simeq I_E$

The maximum collector power dissipation P_{Cmax} of a transistor is limited by the maximum junction temperature T_{jmax} and the reference operating temperature T_O (either the ambient temperature T_a or the case temperature T_c). These parameters have the following relationship using the thermal resistance R_{th}:

$$P_{Cmax} = \frac{T_{j\,max} - T_O}{R_{th}} \quad \cdots\cdots (1\text{–}12)$$

Thermal resistance is a variation in junction temperature divided by the variation in power dissipation. It is a physical property that represents an object's difficulty of dissipating heat. To handle large power dissipation, transistors with a large P_{Cmax} rating are required. Thermal design is particularly important for power transistor applications.

Generally, P_{Cmax} is rated at an ambient temperature (T_a) of 25 °C, or at a case temperature (T_C) of 25 °C when a heat sink is expected to be attached to the package case. The junction-to-ambient thermal resistance $R_{th(j\text{–}a)}$ and the junction-to-case thermal resistance $R_{th(j\text{–}c)}$ can be calculated using Equation 1-12.

1.6. Safe operating area (SOA)

The safe operating area (SOA) is defined as the regions in which a transistor can operate without self-damage or degradation.

The range of a transistor's usability is limited by the maximum ratings such as the maximum voltage, maximum current, and maximum collector power dissipation. However, transistors in high-power amplifiers or circuits driving inductive loads might be degraded or damaged even when they are used within individual maximum ratings. This is attributable to the secondary breakdown of the transistor.

Therefore, transistor-based circuits should be designed, taking SOAs into account.

(1) Secondary breakdown (S/ B)

Figure 1.4 shows secondary breakdown curves. Secondary breakdown is a failure mode that occurs over certain voltage and current conditions ($V_{S/b}$ and $I_{s/b}$) when the current is increased beyond the conditions of primary breakdown. This results in a sharp drop in the collector-emitter voltage, causing a transistor to plunge into a low-impedance region and be destroyed in a few microseconds or less. Both V_{CEO} and V_{CBO} have secondary breakdown points, regardless of whether the base-emitter is forward-or reverse-biased.

The secondary breakdown points ($V_{S/b}$ and $I_{S/b}$) vary along the locus shown in Figure 1.4 depending on the base bias condition. Since secondary breakdown is an energy-dependent phenomenon, the secondary breakdown curve varies depending on the width of the pulse applied. This curve determines the SOA for pulse operation. Figure 1.5 shows the relationship between the pulse width and the secondary breakdown trigger power.

The narrower the pulse width, the higher the secondary breakdown trigger power and the lower the secondary breakdown energy (i.e., the trigger energy, or the energy absorbed by a transistor before it is triggered into secondary breakdown). Secondary breakdown is considered to occur when a current concentrates in a small spot, causing local heating (i.e., a hot spot) and leading to local thermal runaway. The causes of current concentration include a voltage drop and uneven lateral temperature distribution in the base layer.

Also, an uneven base width and junction defects can trigger current concentration.

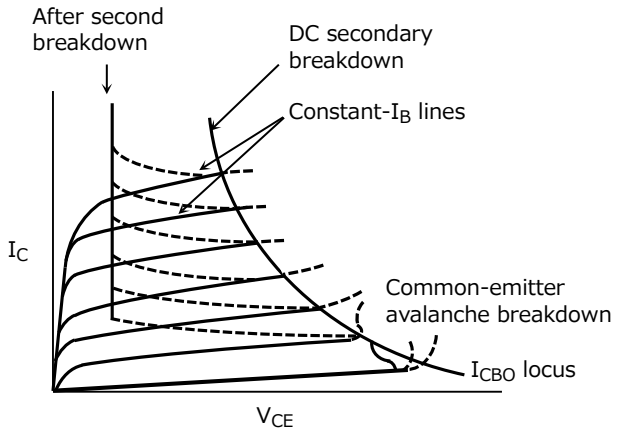


Figure 1.4 Collector current-voltage characteristics showing the secondary breakdown curve

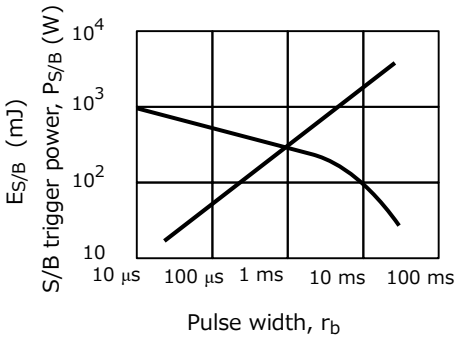


Figure 1.5 Pulse width vs. $E_{S/B}$ and $P_{S/B}$

(2) Forward-bias secondary breakdown

When the base and emitter terminals are forward-biased, a hot spot occurs due to current concentration around the emitter layer.

This is because the horizontal base current traveling immediately below the emitter layer causes a voltage drop in the base layer, leading to a higher forward bias near the edges of the emitter layer than in the center section. This, in turn, results in a higher minority carrier injection and therefore a higher current density at the edges of the emitter layer.

When minority carriers cross the depletion layer in the collector, a power loss occurs and heat is generated locally. This induces further current concentration and results in a hot spot, eventually leading to secondary breakdown.

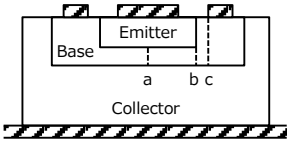


Figure 1.6 Planar transistor

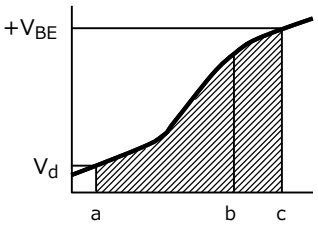


Figure 1.7 Base layer voltage drop when base-emitter forward bias is applied

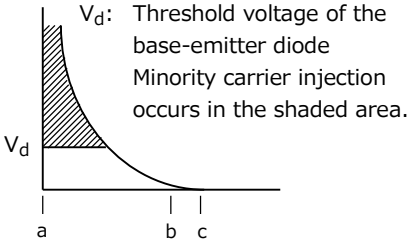
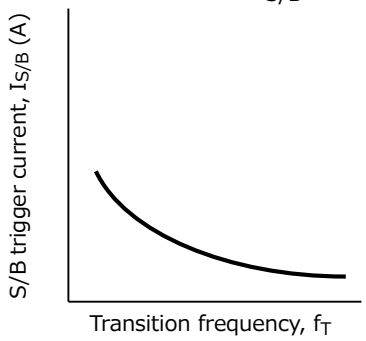


Figure 1.8 Base-emitter reverse bias

Relationship between secondary breakdown and transistor characteristics

When the base and emitter terminals of a transistor are forward-biased, the secondary breakdown trigger current $I_{S/B}$ is closely related to its characteristics. Generally, when carriers are injected into the base layer from the emitter layer, they fan out in a cone-shaped pattern before reaching the collector-base junction. Therefore, if the carrier transit time through the base is long, the carriers further fan out before reaching the depletion layer in the collector, decreasing the current density. As a result, hot spots are less likely to occur. The carrier transit time is determined by the base width and the drift field in the base layer. There is a strong negative correlation between the $I_{S/B}$ and f_T characteristics of a transistor irrespective of the pulse width.

Figure 1.9 shows the $I_{S/B}$-vs-f_T curve.



$$I_{S/B} = \left(\frac{1}{\sqrt{f_T}} \right)^K$$

K : Base width
Constant determined by Drift field and Bias condition

Figure 1.9 $I_{S/B}$ vs. f_T

(3) Reverse-bias secondary breakdown

When the base and emitter terminals are reverse-biased, the direction of a voltage drop in the base layer is opposite to the direction when they are forward-biased. Consequently, the carriers injected from the emitter concentrate in the center section of the emitter layer as shown in Figure 1.8. The state of carrier concentration differs, depending on the type of transistor. Carriers concentrate in one spot at the center of the emitter in the case of a ring-shaped emitter and along the center line of the emitter in the case of a comb-shaped emitter.

A higher reverse bias causes a higher current concentration in a very small area at the center of the emitter. Therefore, the trigger energy (i.e., the energy absorbed by a transistor before going into secondary breakdown) under reverse-bias operation is much less than the trigger energy under forward-bias operation. As is the case with forward-bias operation described above, the carriers injected from the emitter fan out. Therefore, the base width and the drift field in the base layer closely correlate to secondary breakdown.

Reverse-bias secondary breakdown primarily occurs when a transistor circuit has an inductive load. The secondary breakdown trigger energy $E_{S/B}$ depends on the inductance L and the base-emitter conditions as shown in Figure 1.10.

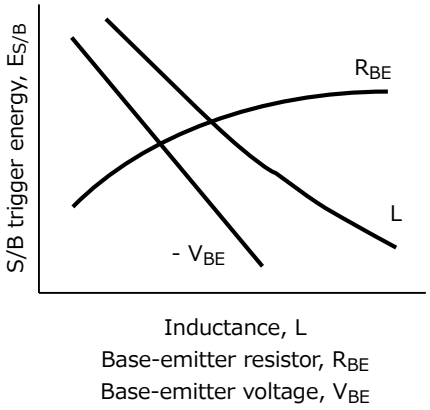


Figure 1.10 Dependence of secondary breakdown trigger energy $E_{S/B}$ on the load inductance and base-emitter conditions

(4) Deterioration and destruction of a transistor due to secondary breakdown

The impact of secondary breakdown on the electrical characteristics depends on the type of transistor. When the applied voltage is low, if the power is shut off at the moment secondary breakdown occurs, it may not change even if secondary breakdown occurs again. However, even with occurrence of S/ B once, characteristics may be degraded or destroyed, so it is necessary to be careful. If a transistor is electrically degraded or destroyed by secondary breakdown, V_{EBO}, V_{CBO}, and V_{CEO} tend to have a soft locus or be short-circuited. A collector-emitter short-circuit in particular is a distinctive failure caused by secondary breakdown that results in pinholes in the emitter. In addition, the secondary breakdown ruggedness might be affected even if the electrical characteristics are not degraded. This is due to a decrease in secondary breakdown trigger energy $E_{S/B}$, which indicates that the transistor is close to destruction.

1.7. SOA test methods

There are many SOA test methods. The method that suits the intended purpose is used according to the circuit configuration and operating conditions.

Measuring SOA directly will cause transistor deterioration and breakdown. For this reason, it is important to measure the state just before the secondary breakdown and check the SOA.

There are three major types of SOA test methods:

(1) Secondary breakdown (S/ B) method

(2) Latching method

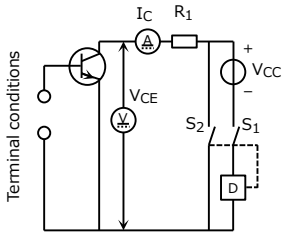
(3) Transient thermal resistance method

The following subsections describe the practical applications of each SOA test method.

(1) Secondary breakdown (S/ B) method

A voltage and a current are applied between the collector and base or between the collector and emitter of a transistor to measure the time when it goes into secondary breakdown. This test requires an adequate protection circuit to prevent deterioration of the transistor.

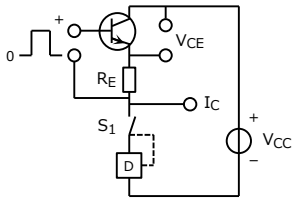
An improvement of the above method is the $T_{S/B}$ method shown in Figure 1.13, which is used to obtain a forward-bias SOA when the width of the applied pulse is relatively long or when a current close to a direct current is used. A transistor is operated at a specified temperature (either case temperature or ambient temperature) by applying the specified V_{CE} and I_C with the base and emitter terminals forward-biased. The parameter measured by this method is the operating time required until I_C fluctuates more than ±10 % or exceeds the specified final value. This measurement is repeated to obtain the operating time at many I_C-V_{CE} points. A plot of this parameter on the I_C-V_{CE} curve provides an SOA locus.



D : S/ B detection and protection circuit

S1, S2 : Switches controlled by signals from D

Figure 1.11 DC-supplied secondary breakdown method



D : Detection and protection circuit

S1: Switch controlled by a signal from D

Figure 1.12 Pulse-supplied secondary breakdown method (pulse to be applied between emitter and base)

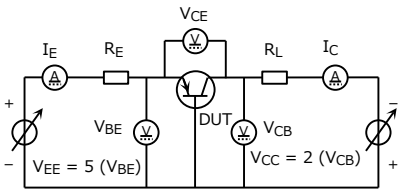


Figure 1.13 Forward-bias SOA test circuit ($T_{S/B}$ method)

(2) Latching method

The latching method places a transistor in the saturation region under the specified constant-current or inductive load conditions in order to determine whether the operating waveform lies within the safe operating area. This method can be used to observe oscillation and other phenomena that occur when a transistor goes into secondary breakdown.

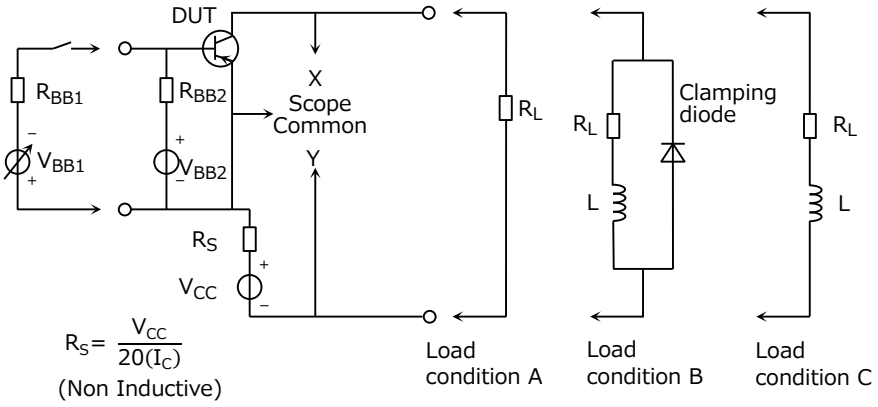
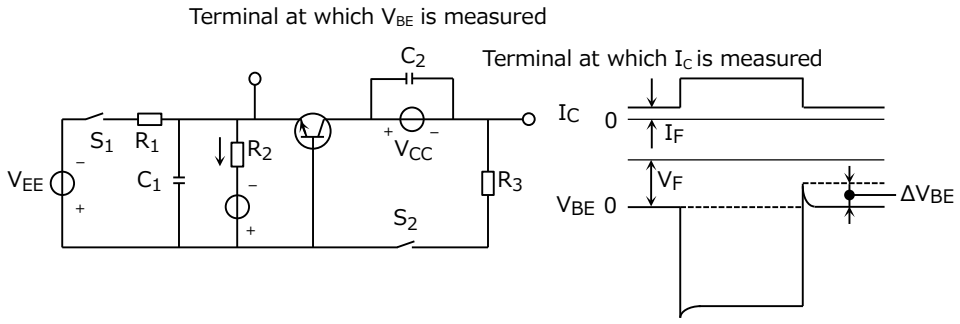


Figure 1.14 Reverse-bias SOA test circuit (latching method)

(3) Transient thermal resistance method (ΔV_{BE} and ΔV_{CE} method)

Since secondary breakdown occurs due to a local temperature rise in the junction of a transistor, the triggering of secondary breakdown can be identified by measuring the junction temperature. Figure 1.15 shows an example. The temperature coefficient of the junction forward voltage is measured in advance. By measuring the difference in forward voltage before and after the application of electric power, a rise in junction temperature and thus transient thermal resistance can be obtained.

This method provides a narrower SOA compared with the two methods described above and cannot be used to measure reverse-bias SOA.



ΔV_{BE}: Temperature drop as a result of removal of the power supply
S_1, S_2: Switches activated depending on the conditions of the terminal at which V_{BE} is measured

Figure 1.15 Transient thermal resistance method (ΔV_{BE} method)

1.8. Forward-bias safe operating area (FBSOA)

Figure 1.16 and Figure 1.17 show examples of forward-bias SOA. The SOA shows the voltage and current ranges over which a transistor is expected to operate without self-damage.

The DC areas shown in the SOA indicate the bounding voltage and current conditions for continuous DC operation. In addition to the continuous rating, separate SOA curves are plotted for short-duration pulse conditions. Pulsed operation provides greater allowable power dissipation than DC operation, but is tolerated only for the period of time indicated.

As shown in Figure 1.16 and Figure 1.17, the low-voltage region is limited by thermal resistance whereas the high-voltage region is limited by secondary breakdown. In the thermally limited region, P_C is constant and hence $I = P \cdot V^{-1}$. Therefore, the bounding line for the thermally limited region has a degree of -45 degrees when plotted on a double logarithmic graph as shown in Figure 1.16.

However, the bounding line for the S/ B-limited region deviates from the iso-power line of "P_C = const" and has an exponent ranging from -1.5 to -4, depending on the type of transistor. It should be noted that since $I_{S/B} = P \cdot V^{-N}$ in this region, a transistor tolerates less power dissipation.

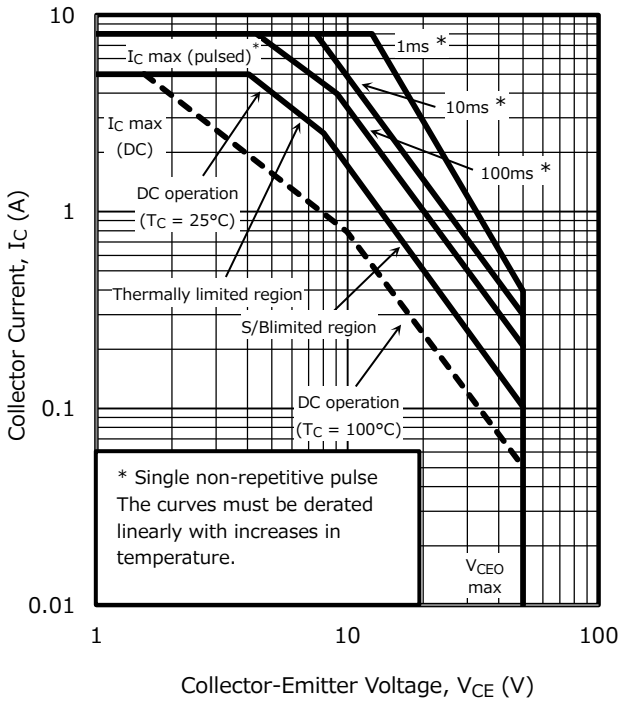


Figure 1.16 SOA for Transistor A and an example of SOA derated for T_C = 100 °C

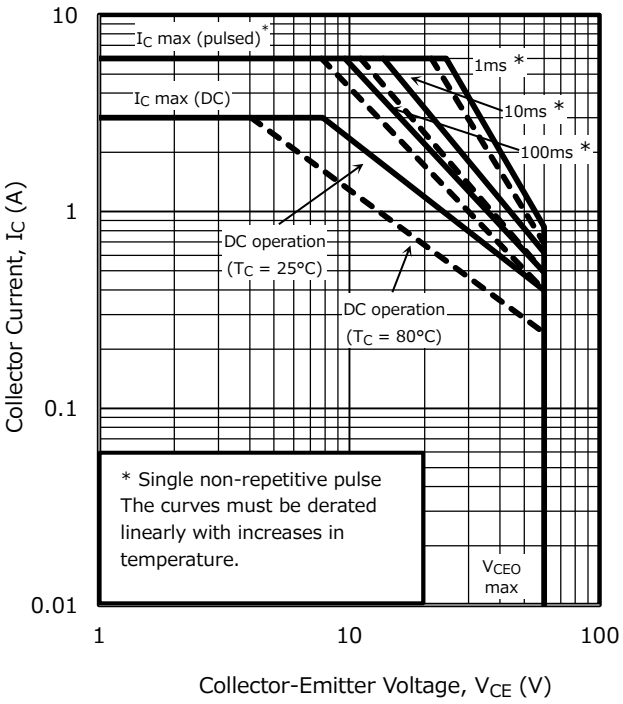


Figure 1.17 SOA for Transistor B and an example of SOA derated for T_C = 80 °C

The SOA becomes smaller as temperature rises. Therefore, the SOA must be derated as shown in Figure 1.18. When temperature rises, the thermally limited region is far more affected by the S/ B-limited region. Figure 1.18 shows an example of derating curves for the S/ B-limited and thermally limited regions over the case temperature. Now, let's consider the derating of the SOA at T_C = 100 °C. Figure 1.16 shows that, at T_C = 100 °C, the thermally limited and S/ B-limited SOA curves are derated by 40 % and 49 % respectively. As a result, the SOA for DC operation is more limited at T_C = 100 °C than at 25 °C as indicated by the dashed line. For the transistor shown in Figure 1.17, when V_{CE} is low and in the thermally limited region, a derating curve for the thermally limited region should be used.

The temperature derating of the S/ B-limited region depends on the transistor structure as shown in Figure 1.18. The derating curve for the S/ B-limited region shown in Figure 1.18 should be used when the S/ B-limited SOA lies in the high-V_{CE} region.

Take Transistor B of Figure 1.17 for example and let the derating percentage for the thermally limited region at a case temperature (T_C) of 80 °C be d_T. Then, d_T is calculated as follows:

$$d_T = \frac{100}{T_j - 25} (T_j - T_C) \quad (\%) \qquad \cdots\cdots (1\text{–}13)$$

Substituting a maximum junction temperature of 150 °C for T_j, d_T is calculated to be 56 %.

Suppose that Transistor B is a triple-diffused transistor. Then, Figure 1.18 (b) shows that, at

150 °C, the S/ B-limited region of the SOA must be derated by 50 %.

Hence, $d_{S/B} = \frac{2}{5}(150 - T_C) + 50$ %. At T_C = 80 °C, $d_{S/B}$ is calculated to be 78 %, In Figure 1.17, the SOA boundary derated at T_C = 80 °C is shown by the dashed line.

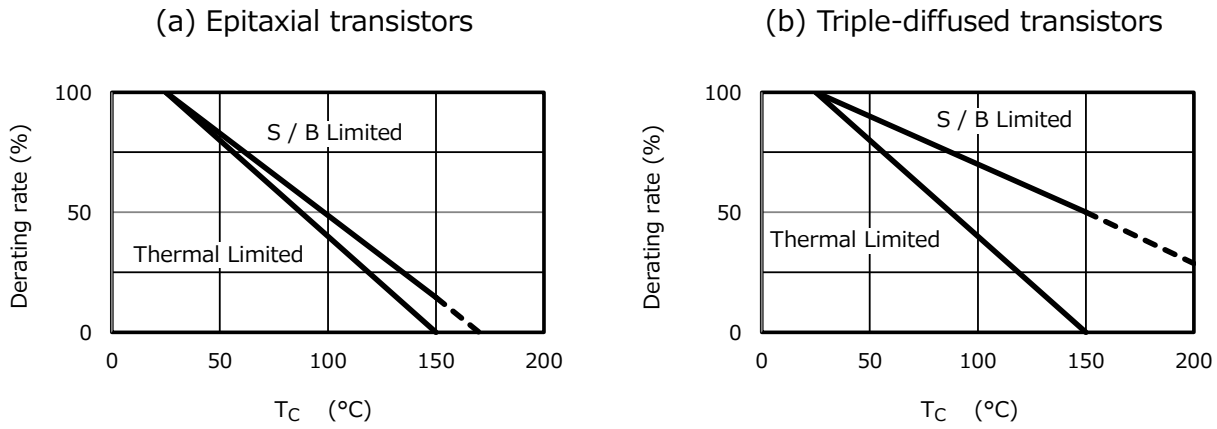


Figure 1.18 Examples of temperature derating of the safe operating area

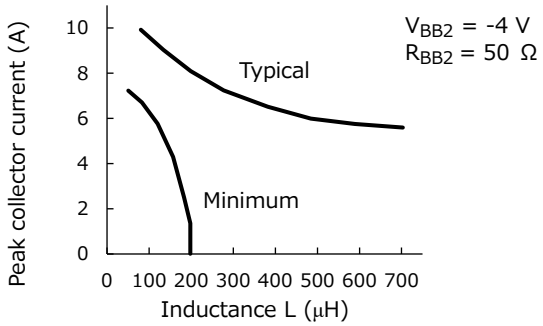
1.9. Reverse-bias safe operating area (RBSOA)

The reverse-bias SOA is more difficult to determine than the forward-bias SOA. However, the reverse-bias SOA is as important as the forward-bias SOA, because in switching circuits with an inductive load or DC-DC converters, the base and emitter terminals of the transistor are frequently reverse-biased at high voltage.

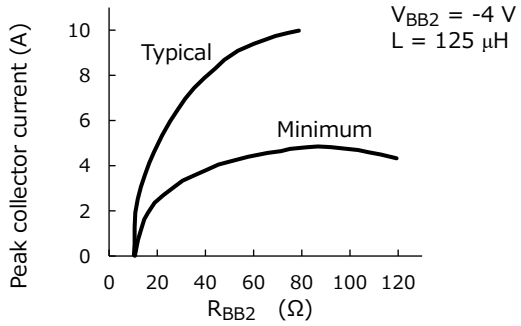
Since the worst load condition is given by an inductive load, the reverse-bias SOA is generally obtained by using the load condition C of the test circuit shown in Figure 1.14. Figure 1.19 (a) shows the I_C–L curves of a transistor under the specified reverse-bias conditions.

Figure 1.19 (b) and Figure 1.19 (c) show the I_C-V_{BB2} and I_C-R_{BB2} curves respectively. For simple circuits with an inductive load, Figure 1.19 can be used to measure the SOA. For complicated circuits, however, it is necessary to calculate effective inductance and use the curves of Figure 1.20.However, it is extremely difficult to obtain an SOA like the ones shown in Figure 1.19 because it is no easy task to calculate effective inductance in an actual circuit. At our company, the SOA is specified under the selected I_C, L, R_{BB2}, V_{BB2}, and other conditions for different transistor applications. Transistors whose load characteristics are outside the region shown in Figure 1.20 are regarded as defective.

(a) Dependence on inductance L



(b) Dependence on the base resistor R_{BB2}



(c) Dependence on the base voltage V_{BB2}

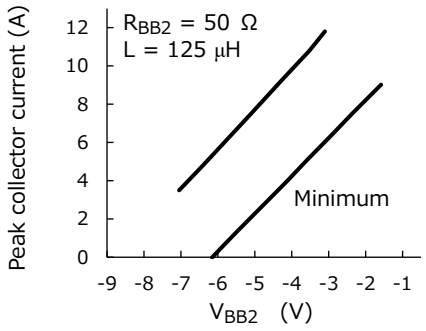
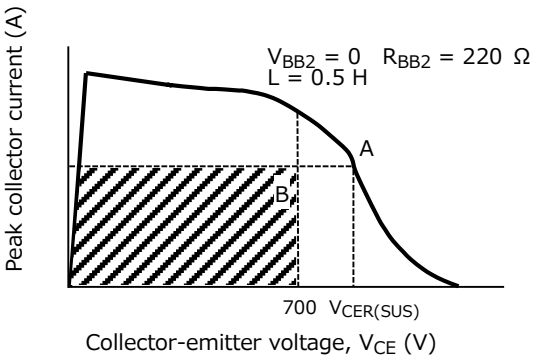


Figure 1.19 Examples of reverse-bias SOAs



A peak collector current of 150 mA is applied, and the collector-emitter voltage at which the collector current drops to 100 mA is measured (A in the above figure).

Figure 1.20 Example of a reverse-bias SOA

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