

MOSFET Secondary Breakdown

Description

This document describes the secondary breakdown of a power MOSFET.

Table of Contents

Description.....	1
Table of Contents.....	2
1. MOSFET secondary breakdown.....	3
1.1. Safe operating area of a MOSFET.....	3
1.2. MOSFET secondary breakdown.....	4
1.3. Mechanism of MOSFET secondary breakdown.....	4
RESTRICTIONS ON PRODUCT USE.....	6

List of Figures

Figure 1 Safe operating area of a MOSFET.....	3
---	---

1. MOSFET secondary breakdown

This section describes the secondary breakdown limit indicated by the safe operating area (SOA) curves of a MOSFET.

1.1. Safe operating area of a MOSFET

The SOA is the voltage and current conditions over which a MOSFET operates without self-damage or degradation. The MOSFET must not be exposed to conditions outside the safe operating area even for an instant. In their early history, MOSFETs were known for the absence of secondary breakdown, which was a failure mode specific to bipolar transistors. The SOA of a MOSFET was bound only by the maximum drain-source voltage, the maximum drain current, and a thermal instability limit between them. However, due to device geometry scaling, recent MOSFETs exhibit a phenomenon resembling secondary breakdown. It is therefore necessary to determine whether the operating locus of the MOSFET falls within the SOA.

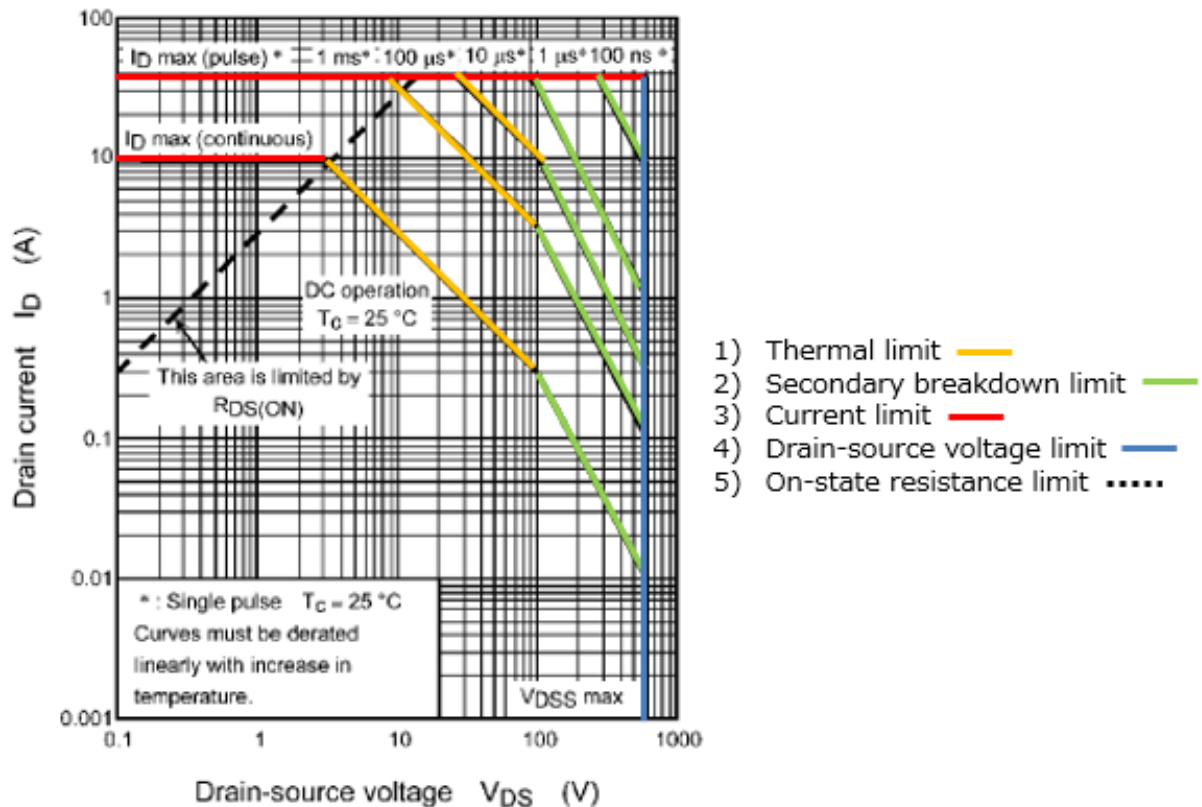


Figure 1 Safe operating area of a MOSFET

The SOA of a MOSFET is divided into the following five regions (Figure 1):

1) Thermal limit

This is the area limited by the power dissipation P_D (absolute maximum rating). The maximum permissible power dissipation is determined by the guaranteed channel temperature and thermal resistance. Therefore, the SOA has a slope that represents the maximum permissible power dissipation (which has a slope of -1 on a double logarithmic graph). The thermal limit depends on the operating conditions of a MOSFET since the maximum permissible power dissipation and the device temperature vary with the conduction time and ambient temperature of the MOSFET.

2) Secondary breakdown limit

3) Current limit

This defines the area limited by the maximum drain current rating. For continuous-current (DC) operation, the SOA is limited by the I_D (absolute maximum rating). For pulsed operation, the SOA is limited by the I_{DP} (absolute maximum rating).

4) Drain-source voltage limit

This defines the area limited by the drain-source voltage V_{DSS} (absolute maximum rating).

5) On-state resistance limit

This defines the area that is theoretically constrained by the on-state resistance $R_{DS(ON)}(\max)$. I_D is equal to $V_{DS}/R_{DS(ON)}(\max)$.

1.2. MOSFET secondary breakdown

Secondary breakdown is a failure mode in bipolar transistors in which negative resistance (current concentration) occurs under high-voltage and high-current conditions. Current concentration causes local heating, resulting in a small hotspot. The impedance of the hotspot decreases, causing further current concentration. This cycle called thermal runaway leads to device degradation and destruction.

In this regard, the secondary breakdown limit in the SOA of a power MOSFET can be considered in the same manner as that of a bipolar transistor. However, the secondary breakdown of a power MOSFET is not defined by the operation of a parasitic bipolar transistor in the MOSFET structure. To be precise, the MOSFET failure mode should not be called secondary breakdown, but the same term has traditionally been used for both bipolar transistors and power MOSFETs.

1.3. Mechanism of MOSFET secondary breakdown

This subsection describes the mechanism of MOSFET secondary breakdown.

When the MOSFET gate is forward-biased, charge carriers are attracted to the interface between the gate electrode and the gate oxide, forming an inversion layer.

The inversion layer provides a channel through which current can pass between source and drain terminals. The gate voltage at which this occurs is called the threshold voltage V_{th} . The MOSFET drain current is controlled by the amount of charge carriers transported to the interface between the gate electrode and the gate oxide.

Since the number of charge carriers increases with temperature, V_{th} decreases with temperature.

The channel resistance is in inverse proportion to the difference between the gate voltage V_{GS} and V_{th} (i.e., $V_{GS} - V_{th}$). (As $(V_{GS} - V_{th})$ increases, the number of carrier charges increases. This causes an increase in the charge carrier density and therefore a decrease in channel resistance.)

As mentioned above, V_{th} decreases with temperature since the number of charge carriers increases with temperature. This means that the channel resistance decreases as $(V_{GS} - V_{th})$ increases.

The following paragraphs discuss the mechanism of MOSFET secondary breakdown based on these facts.

- 1) As the MOSFET temperature increases, the gate threshold voltage V_{th} decreases, reducing the channel resistance.
- 2) Current concentrates in the channel with reduced resistance, causing a further temperature rise, which results in a further decrease in the gate threshold voltage V_{th} .
- 3) Consequently, further current concentration occurs. This cycle eventually leads to device destruction.

As a result of the foregoing, the SOA is limited by the secondary breakdown line, considering changes in channel resistance due to temperature changes. The line constrained by the maximum permissible power and heat dissipation (i.e., ambient temperature and thermal resistance) and the line bound by secondary breakdown, which includes channel resistance (i.e., temperature dependence of the gate threshold voltage) as one of the causative factors, have different slopes.

As described above, the secondary breakdown of a MOSFET is device destruction caused by current concentration. Therefore, MOSFETs with high transconductance g_m^* (i.e., with a high current gain) and those that exhibit significant changes in drain current due to changes in V_{th} in the high V_{DS} region are highly susceptible to destruction.

While current is flowing because of avalanche breakdown, the gate is off, and therefore no current flows through the gate channel. Consequently, the MOSFET is not susceptible to secondary breakdown because it is not affected by the temperature-dependency characteristics of the gate threshold voltage V_{th} .

* Transconductance g_m

Transconductance is the change in the drain current (I_{DS}) divided by a change in the gate-source voltage V_{GS} :

$$g_m = \frac{dI_{DS}}{dV_{GS}}$$

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**