M4G Group (1) Application Note Consumer Electronics Control Circuit (CEC-A)

Outlines

This application note is a reference material for developing products using the Consumer Electronics Control Circuit (CEC) function of M4G group (1).

This document helps the user check operation of the product and develop its program.

Target sample program: CEC_CH_TO_CH



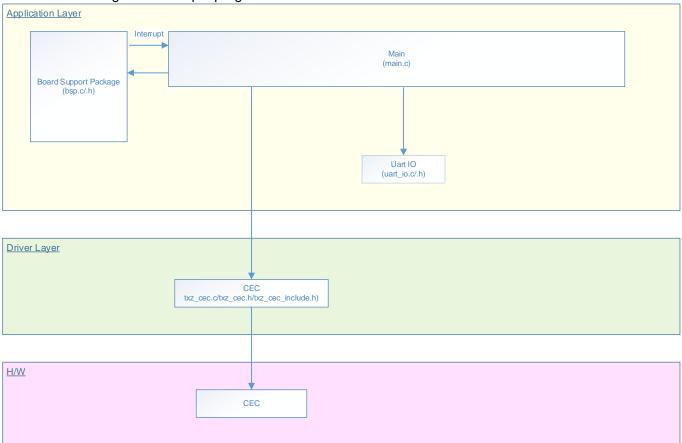
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1. Preface

This sample program is used to check the operation of CEC circuit function.

Structure diagram of Sample program





2. Reference Document

Datasheet

TMPM4G group (1) datasheet Rev1.0 (Japanese edition)

Reference manual

Consumer Electronics Control Circuit (CEC-A) Rev1.0 (Japanese edition)

Asynchronous Serial Communication Circuit (UART-C) Rev3.0 (Japanese edition)

Application note

M4G Group (1) Application Note Startup (CMSIS System & Clock Configuration) Rev1.0

Other reference document

TMPM4G (1) Group Peripheral Driver User Manual (Doxygen)

3. Function to Use

IP	Channel	Port	Operation / Function mode
CEC	-	PT2 (CEC0)	-
Asynchronous Serial Communication Circuit	lch0	PE2 (UT0RXD)	UART mode
Communication Circuit		PE3 (UT0TXDA)	

4. Target Device

The target devices of this application note are as follows;

TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
	TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
	TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG

^{*}This sample program operates on the evaluation board of TMPM4G9F15FG.

If other function than the TMPM4G9F15 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.

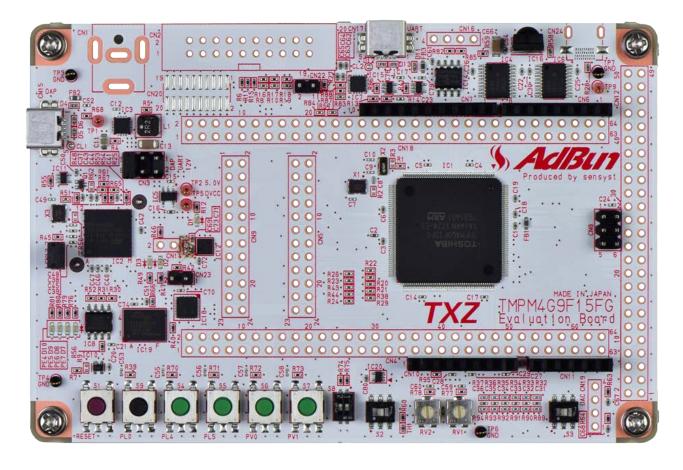
The BSP related file is dedicated to the evaluation board (TMPM4G9F15). If other function than the TMPM4G9F15 one is checked, the BSP related file should be changed properly.



5. Operation Confirmation Condition

Used microcontroller Used board Unified development environment Unified development environment Terminal software Sample program TMPM4G9F15FG
TMPM4G9F15FG Evaluation Board by Sensyst
IAR Embedded Workbench for ARM 8.11.2.13606
µVision MDK Version 5.24.2.0
Tera Term V4.96
V1000

Evaluation board (TMPM4G9F15FG Evaluation Board) Top view



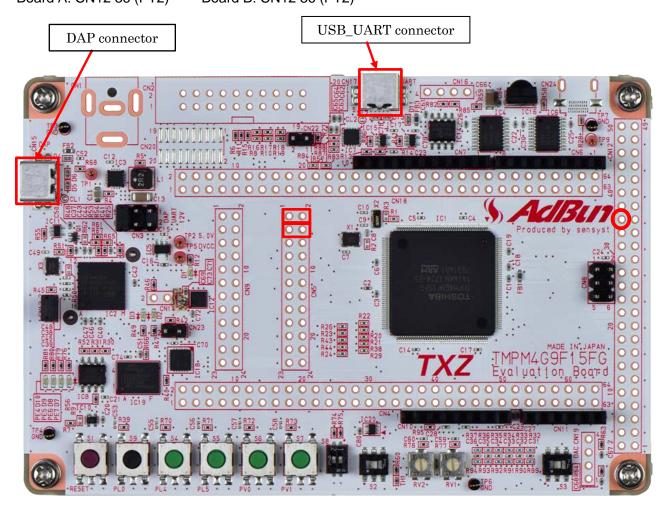
6. Evaluation Board Setting

Two evaluation boards are used. The way of connection is the same.

The following through-holes should be connected on the evaluation board. (Common with board A and board B)

CN5		
Board function	Through-hole No.	Through-hole No.
USB to UART conversion	1: USB_UT_RX	2: PE2
USB to UART conversion	3: USB_UT_TX	4: PE3

The following parts of the board A and board B are connected. Board A: CN12 36 (PT2) - Board B: CN12 36 (PT2)



7. Operation of Evaluation Board

PC and the USB_UART are connected for communication with the terminal software.

Executes the setting of communication after the terminal software (Tera Term) starts up.

Push down the reset button on the evaluation board.

The communication starts with the command input.

For details of command input operations, refer to Sample program main operation.



8. Outline of CEC Control Circuit Function

The brief outline of CEC Control Circuit (CEC) function is shown as follows.

Function Classification	Function	Operation
HDMI standard	-	Compliant with Version 1.3a.
	Sampling clock	Selected from the followings: - fs (Low speed clock) - CECxCLKTRG (Timer trigger for Clock source)
Reception control	Noise reduction	Noise canceling time is adjustable. -"High" detection time Sampling clock selected from 1 to 4 consecutive observations. - "Low" detection time Sampling clock selected from 1 to 4 consecutive observations.
	Data reception	Data reception per Byte - Flexible data sampling point - Data reception is available even when a Destination address does not match.
	Error detection	- Cycle error (Max/Min) - ACK collision - Waveform error
	Data transmission	Data transmission per Byte - Triggered by auto-detection of bus free state
Transmission control	Waveform adjustment	Transmission waveform adjustment - The timing of a rising edge and the cycle time are adjustable.
	Error detection	- Arbitration lost - ACK response error
	Transmission interrupt	 Start transmission Transmission end Arbitration lost ACK Error Underrun
Interrupt	Reception interrupt	 Reception completed Start bit Max cycle error Min cycle error ACK collision Overrun Waveform error



9. Sample Program

Two addresses, address 5 and address 7 are set as the CEC address.

When the header and Data are input on the Tera Term, you can check the transmission and receiving of Data by sample program.

9.1. Initialization

The following initialization is done after power is supplied.

The initialization of each clock setting and the setting of the watchdog timer are done.

9.2. Sample Program Main Operation

After the initialization operation, shift to the main function and do the following initialization.

- (1) Initialization of BSP (Board Support Package)
- (2) Initialization of variables
- (3) Initialization of application

The header and Data are input following "Input =".

The header and Data are displayed following "CEC Snd =", and are transmitted.

When the data are received, the header and received data are displayed following "CEC Rcv =".

9.3. Output Example of Sample Program

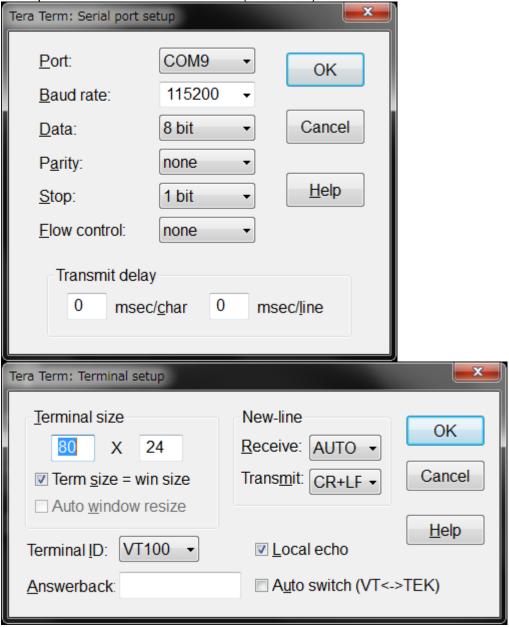
After the sample program starts to operate, the command results are displayed as shown in the following.

"u" shows header, and "abcdef" shows Data in the following example.

```
CEC Address = 5
CEC Address = 7
Input = uabcdef
CEC Snd = uabcdef
Input =
CEC Rcv = W012345
```

9.3.1. Setting Example of Terminal Software

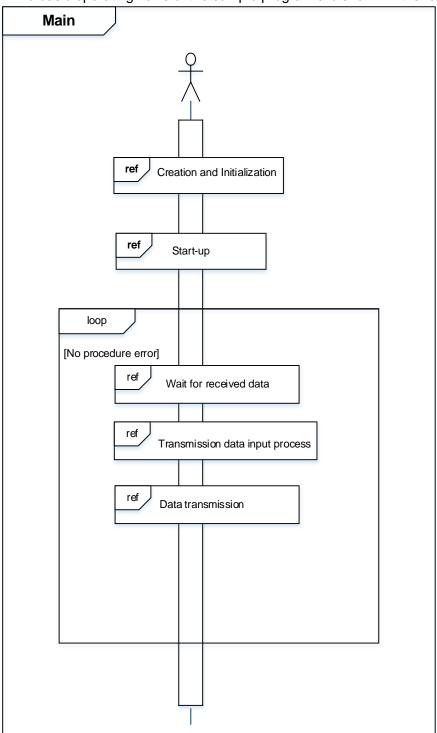
The operation of the terminal software (Tera Term) has been checked with the following settings.

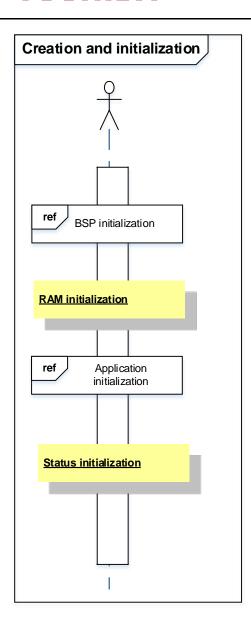


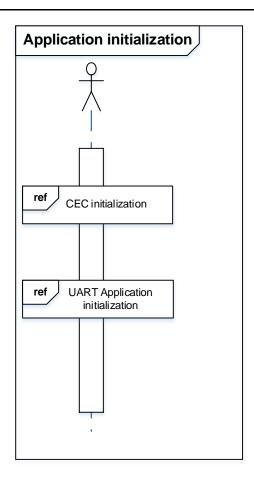


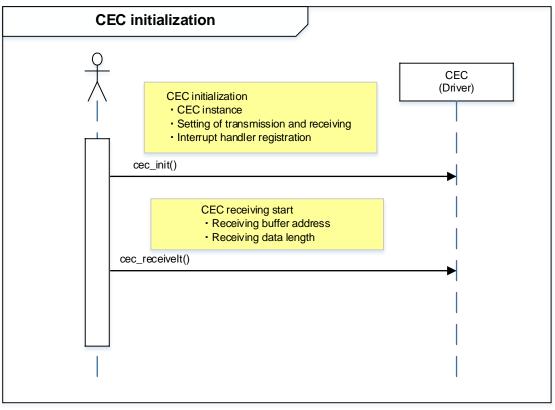
9.4. Operating Flow of Sample Program

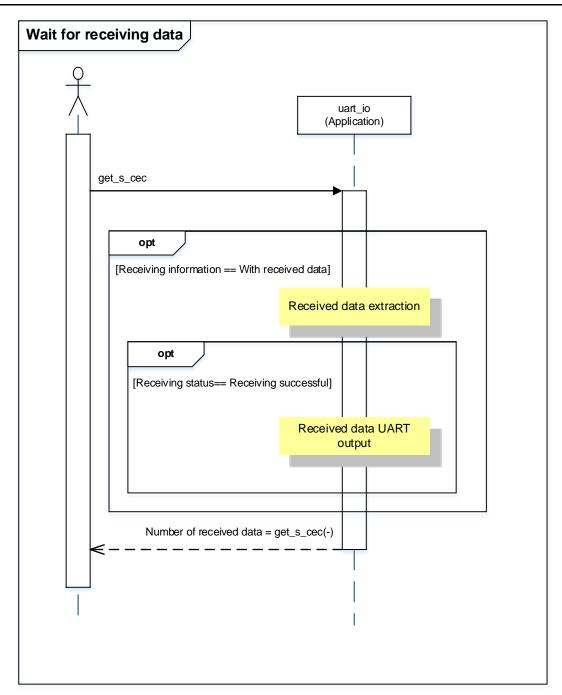
The basic operating flows of the sample program are shown in the following;

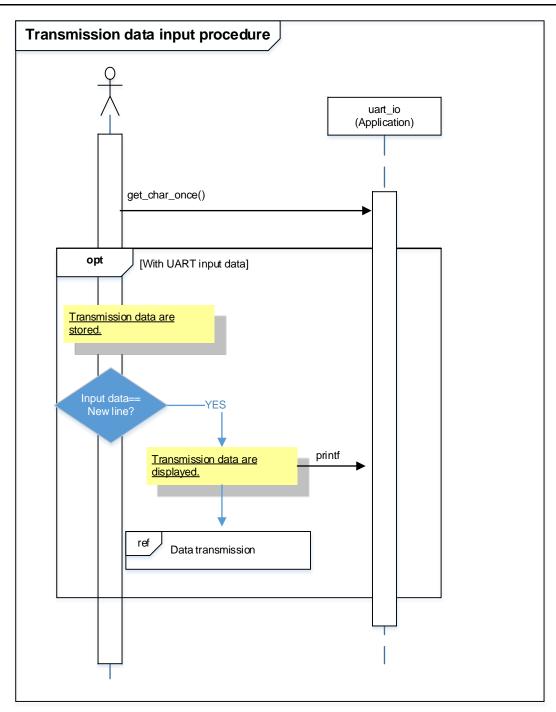


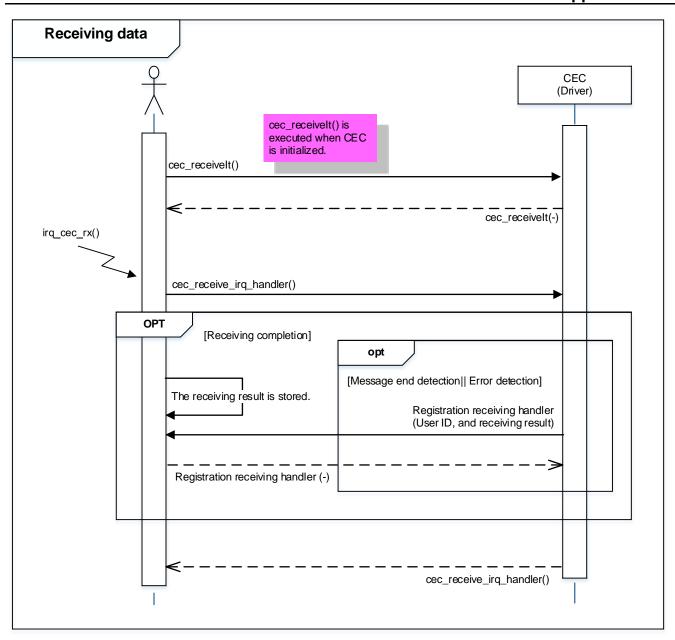




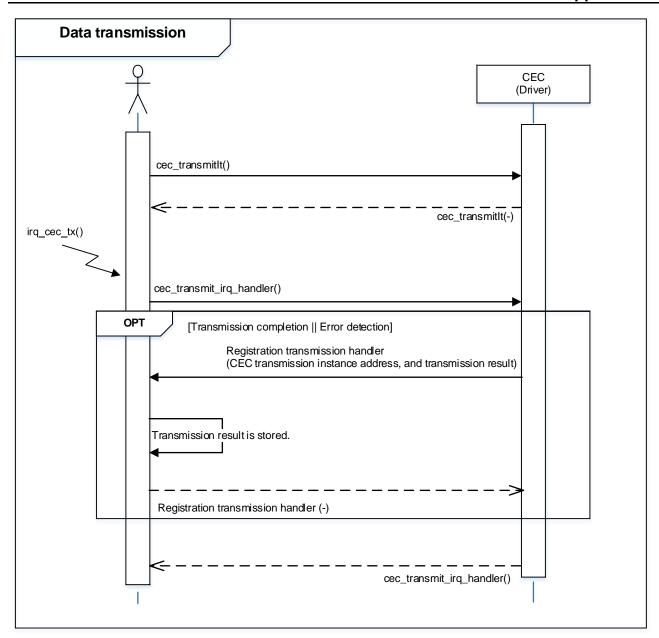














10. Precaution

When using the sample program with CPU other than TMPM4G9F15, please check operation sufficiently.

11. Revision History

R	lev	Date	Description
1.0)	2018-11-26	First release



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