M4G Group (1)
Application Note
External Bus Interface
(EBIF-A)

Outlines

This application note is a reference material for developing products using External bus interface (EBIF) function of M4G group (1).
This document helps the user check operation of the product and develop its program.

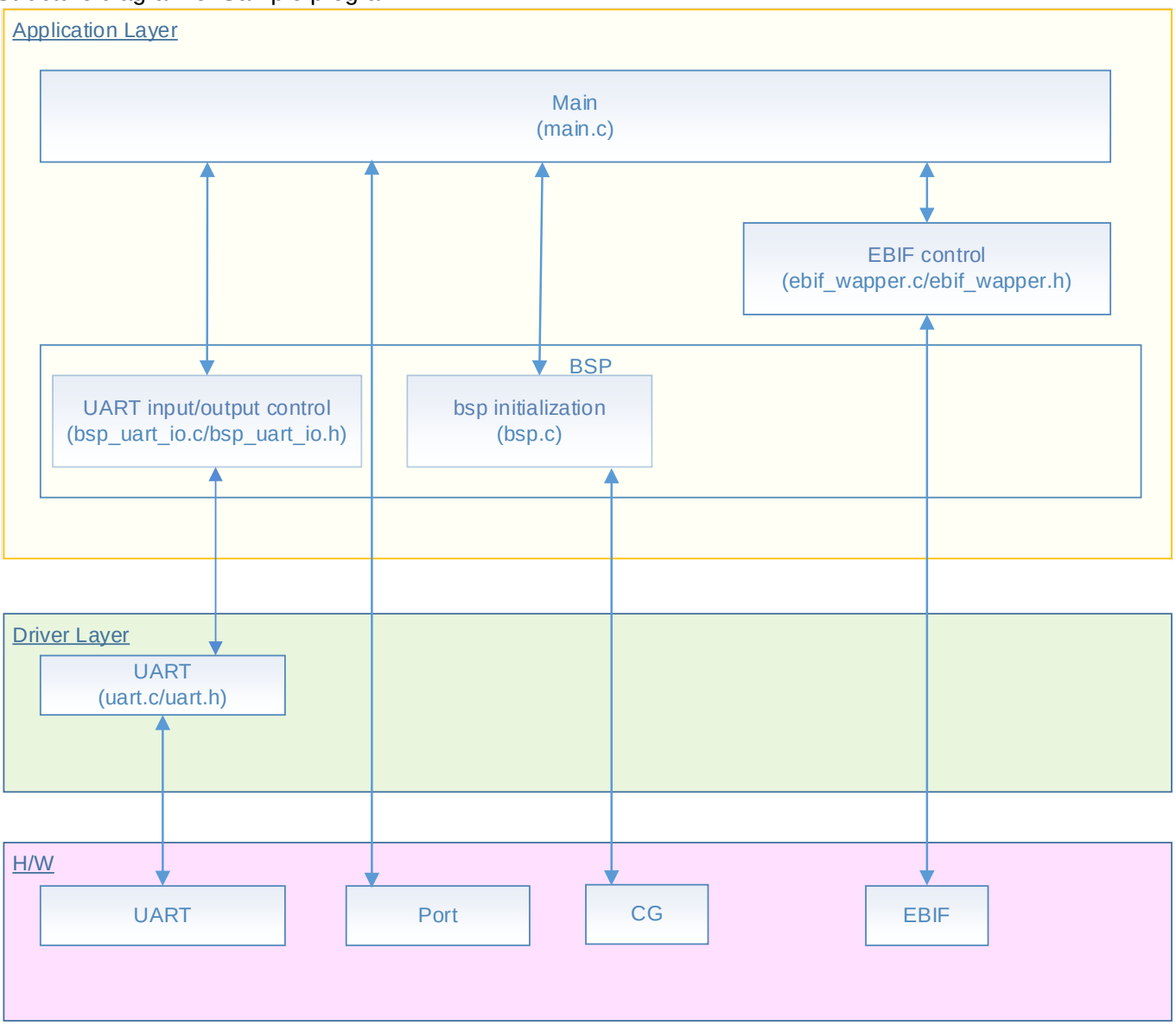
Target sample program: EBIF_SRAM

Table of Contents

1. Preface

This sample program should be used to check the operation of the External bus interface.

Structure diagram of Sample program



2. Reference Document

- Datasheet
  TMPM4G Group (1) datasheet Rev1.0 (Japanese edition)
- Reference manual
  External Bus Interface (EBIF-A) Rev1.0 (Japanese edition)
  Asynchronous Serial Communication Circuit (UART-C) Rev3.0 (Japanese edition)
- Application note
  M4G Group (1) Application Note Startup (CMSIS System & Clock Configuration) Rev1.0
- Other reference document
  TMPM4G (1) Group Peripheral Driver User Manual (Doxygen)

3. Function to Use

IP	Channel	Port	Function/Operation mode
External Bus Interface	-	PD[7:0] (ED07-ED00) PE[7:0] (ED15-ED08) PC[2:0] (EA18-EA16) PK3 (ECS1_N) PF0 (ERD_N) PF1 (EWR_N) PF6 (EBELL_N) PF7 (EBELH_N)	Multiplex bus
Asynchronous Serial Communication Circuit	ch1	PH0 (UT1TXDA) PH1 (UT1RXD)	UART mode

4. Target Device

The target devices of this application note are as follows;

TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
	TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
	TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG

* This sample program operates on the evaluation board of TMPM4G9F15FG.
If other function than the TMPM4G9F15 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.
The BSP related file is dedicated to the evaluation board (TMPM4G9F15). If other function than the TMPM4G9F15 one is checked, the BSP related file should be changed properly.

5. Operation confirmation condition

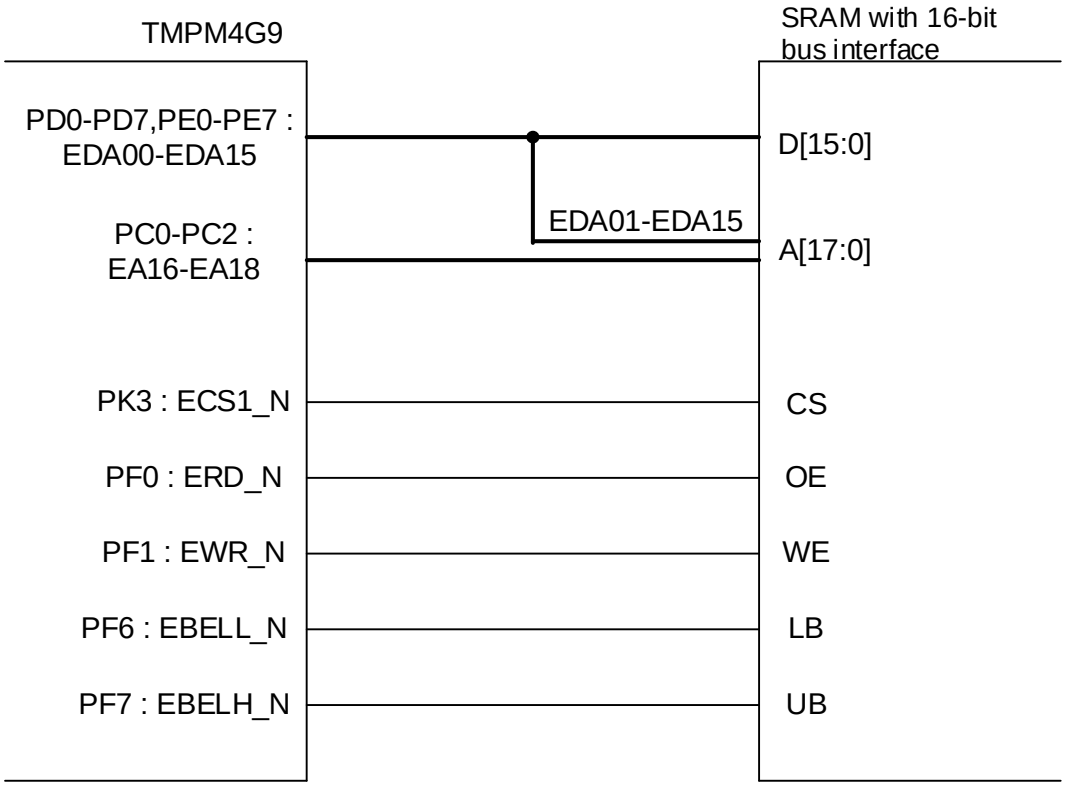
Used microcontroller	TMPM4G9F15FG
Used board	TMPM4G Evaluation Board (Not for sale)
Unified development environment	IAR Embedded Workbench for ARM 8.11.2.13606
Unified development environment	µVision MDK Version 5.24.2.0
Terminal software	Tera Term V4.96
Sample program	V1000

6. Evaluation Board Setting

The external SRAM device should be connected to TMPM4G9F15FG.
The sample program has been checked in the synchronous multiplex mode.

A connection example is shown in the following figure.

Used SRAM device: IS62WV5126BLL-55TLI



7. Outline of External Bus Interface Function

External bus interface (EBIF) is interface to connect to memory and I/Os external of MCU. These features are shown in the following table.

Function classification	Function	Operation explanation
Connection specification	Support Devices	NOR Flash memory, SRAM, Peripheral I/O, etc.
	Mode	Separate bus mode, Multiplexed bus mode
	Data bus width	Either an 8-bit or 16-bit width can be set for each channel.
Memory allocation	Address access area	Supports up to 64MB memory area 0x60000000 to 0x63FFFFFF (Max. 16MB for each CS)
	CS control	4 channels (ECS0_N pin, ECS1_N pin, ECS2_N pin, ECS3_N pin)
External bus control	Clock output	This function can output clock synchronizing with bus cycles.
	Internal wait function	A wait can be inserted up to 15 cycles for each channel.
	External wait function	In addition to the internal wait function, the wait cycle can be extended by EWAIT_N pin.
		Active "Low" or active "High" is selectable.
	ALE assert time setting function	An assert time can be selected from 1, 2, 3, or 5 cycles for each channel.
	Setup cycle insertion function	Read or Write setup cycle can be inserted for each channel.
	Recovery cycle insertion function	In consecutive external bus cycles, a dummy cycle up to 8 clocks can be inserted and this dummy cycle can be specified for each channel.
		Address/ data hold cycle insertion at ECSn_N pin, ERD_N pin, EWR_N pin
	Bus expansion function	Internal wait, ALE assert time, Setup cycle and Recovery cycle can be expanded double or quadruple. (Used in common in all channels)

8. Sample Program

Input write or read command format to Tera Term.
In the case of the write command, the input character is saved in the SRAM.
In the case of the read command, it reads the data saved in SRAM and displays it in Tera Term.

8.1. Initialization

The following initialization is done after power is supplied.
The initialization of each clock setting and the setting of the watchdog timer are done.

8.2. Sample Program Main Operation

After the initialization operation, shift to the main function and do the following initialization.

1. Initialization of BSP (Board Support Package)
2. Initialization of the ports for the EBIF
3. Initialization of EBIF registers
4. Initialization of the application
5. Initialization of memory

After the procedure above has been done, the following operation should be done on the terminal software (Tera Term) on the PC.
"command >" is displayed on the Tera Term. The “write” command or the “read” command should be input according to the following format.
“write” command: The input character is stored to the address of 0x61000000 (SRAM address: 0x00000).
“read” command: The data stored in the address of 0x61000000 (SRAM address: 0x00000) is read, and the data is displayed on the Tera Term.

・Command format:
“write” command
write␣X X: Any character
“read” command
read

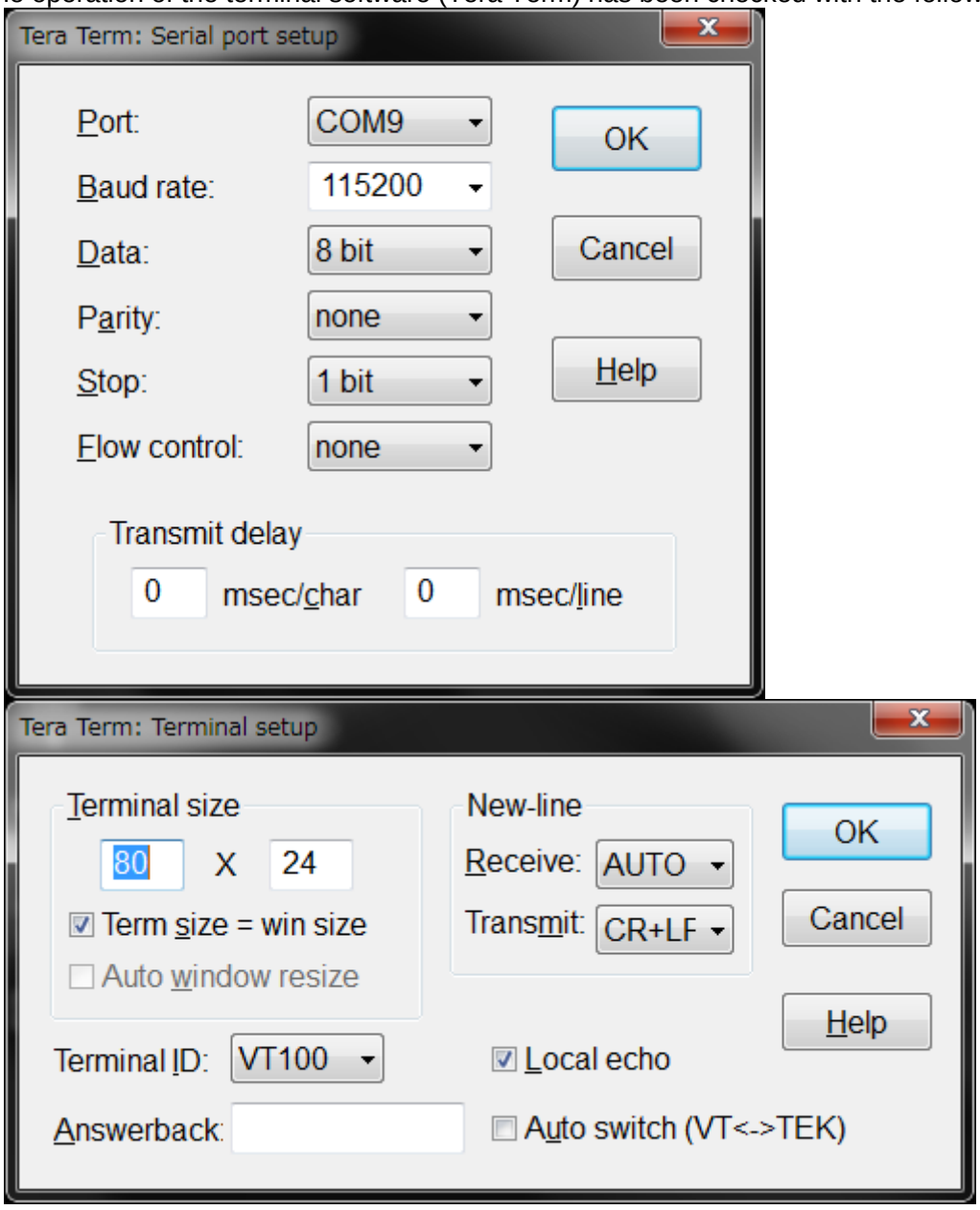
Used memory device	SRAM: IS62WV5126BLL-55TLI

8.3. Output Example of Sample Program

When the sample program executes, the command result is output as shown in the following figure.

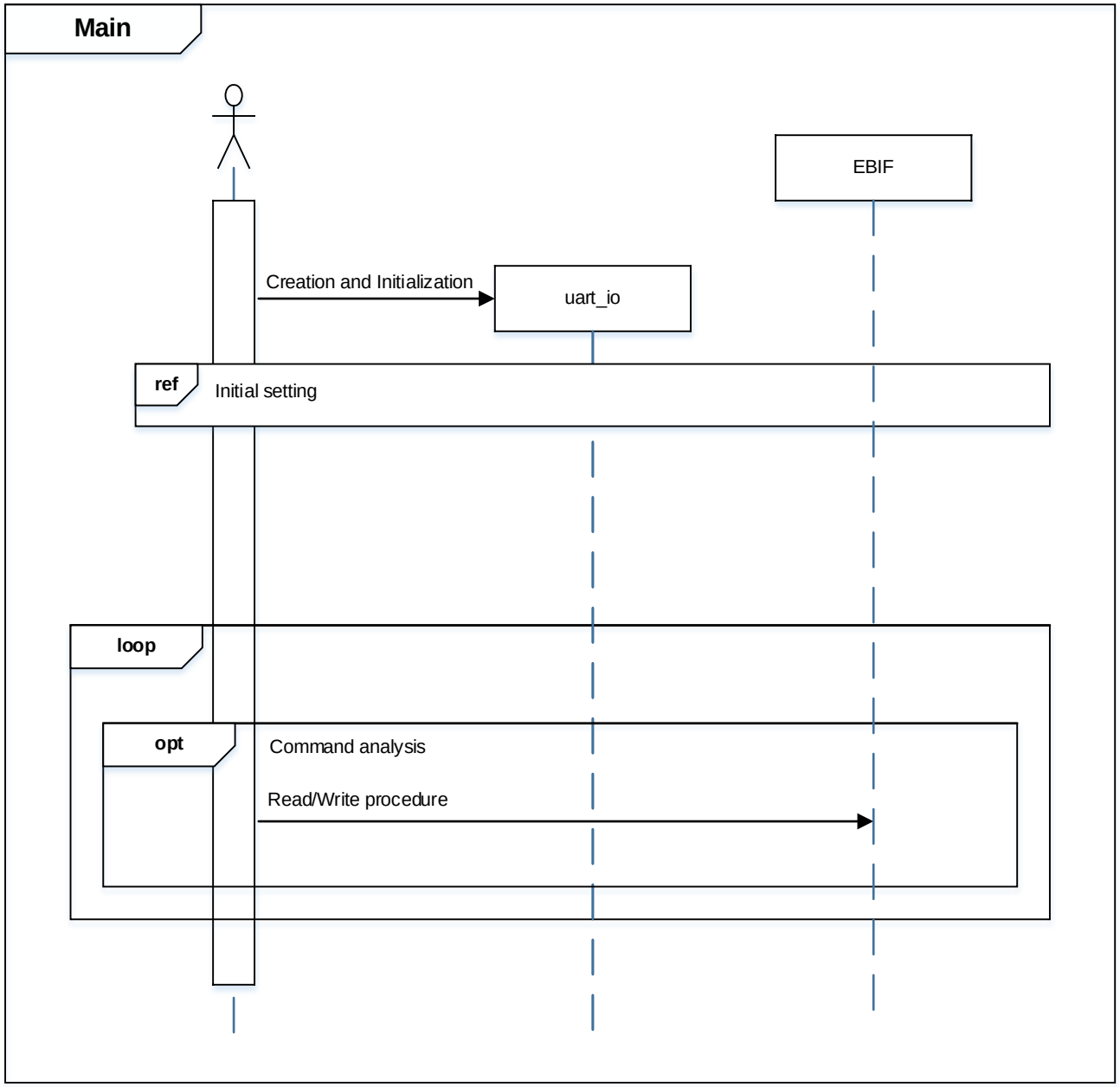
8.3.1. Setting Example of Terminal Software

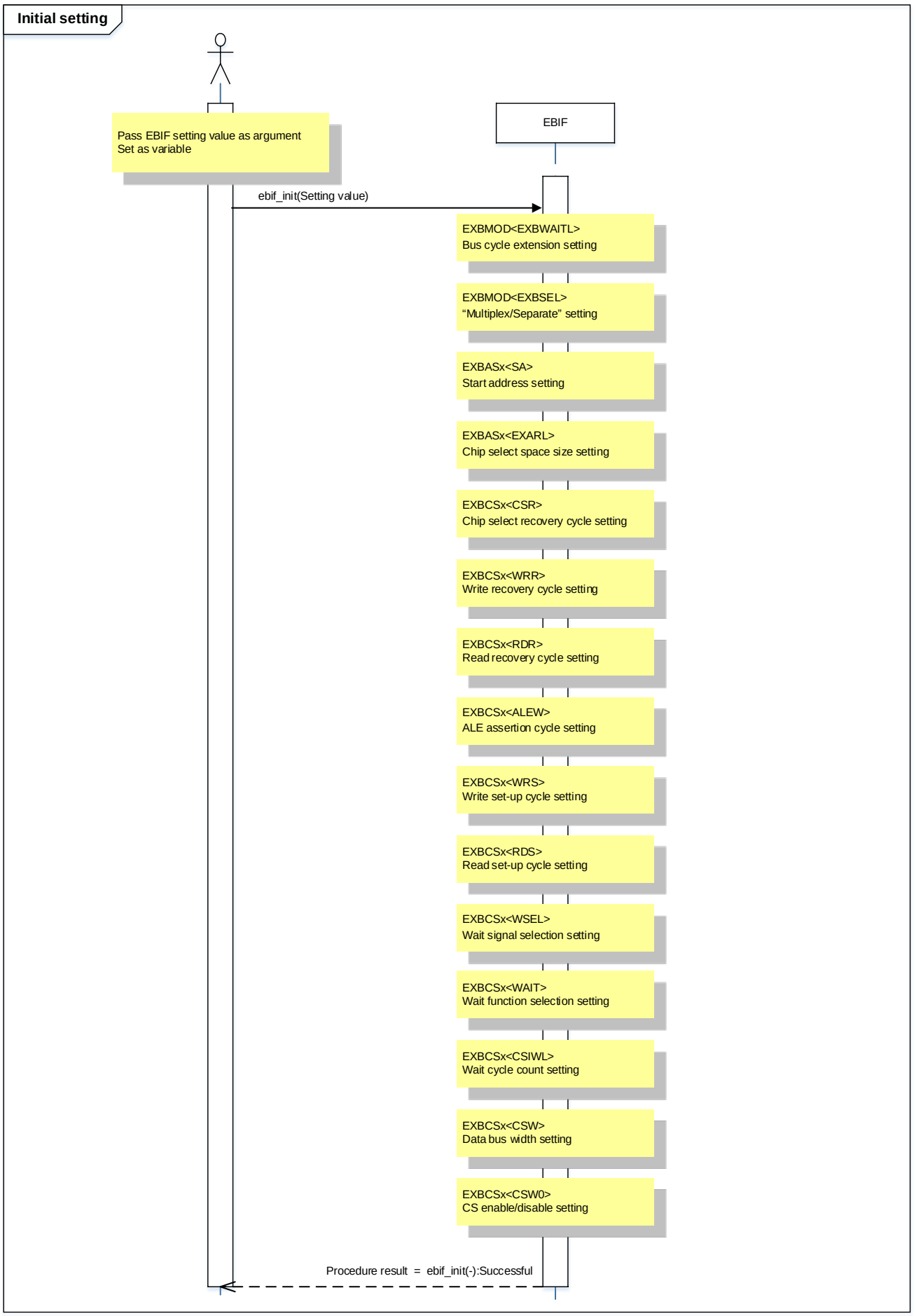
The operation of the terminal software (Tera Term) has been checked with the following settings.

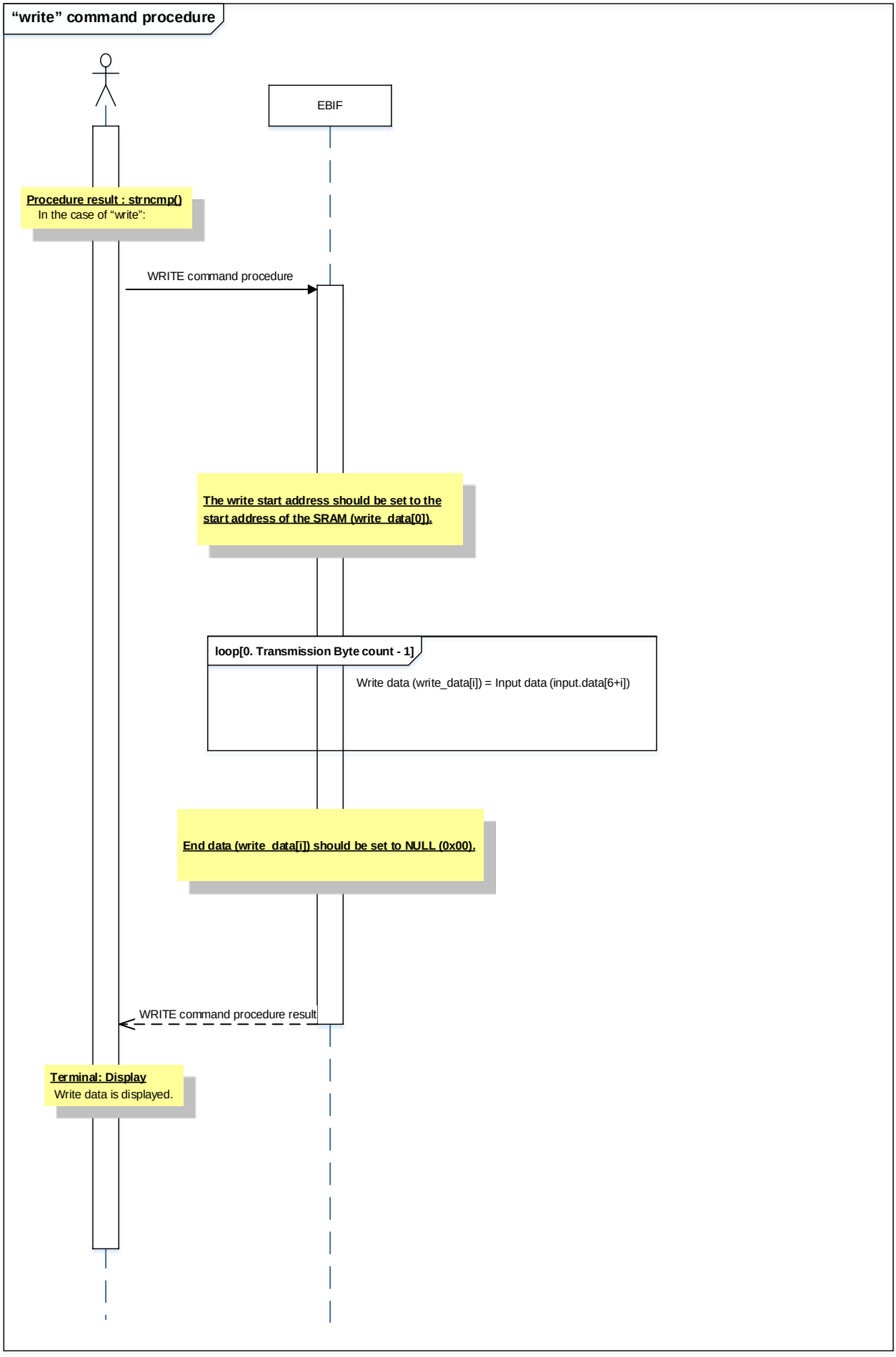


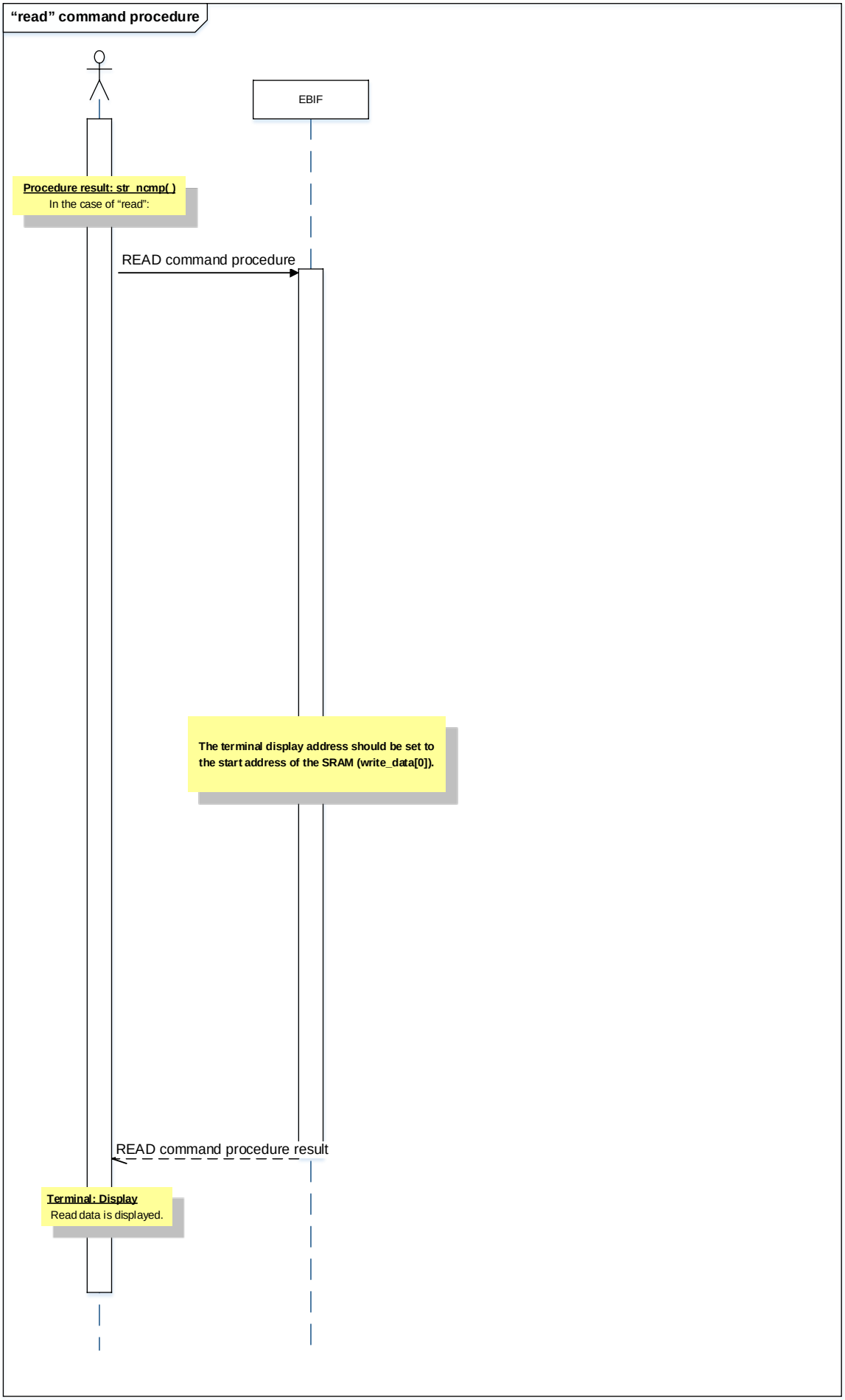
8.4. Operating Flow of Sample Program

The basic operating flows of the sample program are shown in the following;




Initial setting
Pass EBIF setting value as argument
Set as variable
EBIF
ebif_init(Setting value)
EXBMOD<EXBWAITL>
Bus cycle extension setting
EXBMOD<EXBSEL>
“Multiplex/Separate” setting
EXBASx<SA>
Start address setting
EXBASx<EXARL>
Chip select space size setting
EXBCSx<CSR>
Chip select recovery cycle setting
EXBCSx<WRR>
Write recovery cycle setting
EXBCSx<RDR>
Read recovery cycle setting
EXBCSx<ALEW>
ALE assertion cycle setting
EXBCSx<WRS>
Write set-up cycle setting
EXBCSx<RDS>
Read set-up cycle setting
EXBCSx<WSEL>
Wait signal selection setting
EXBCSx<WAIT>
Wait function selection setting
EXBCSx<CSIWL>
Wait cycle count setting
EXBCSx<CSW>
Data bus width setting
EXBCSx<CSW0>
CS enable/disable setting
Procedure result = ebif_init(-):Successful


"write" command procedure
EBIF
Procedure result : strncmp()
In the case of "write":
WRITE command procedure
The write start address should be set to the start address of the SRAM (write_data[0]).
loop[0. Transmission Byte count - 1]
Write data (write_data[i]) = Input data (input.data[6+i])
End data (write_data[i]) should be set to NULL (0x00).
WRITE command procedure result
Terminal: Display
Write data is displayed.


"read" command procedure
EBIF
Procedure result: str_ncmp( )
In the case of "read":
READ command procedure
The terminal display address should be set to the start address of the SRAM (write_data[0]).
READ command procedure result
Terminal: Display
Read data is displayed.

9. Precaution

When using the sample program with CPU other than TMPM4G9F15, please check operation sufficiently.

10. Revision History

Rev	Date	Description
1.0	2018-11-27	First release

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