M4G Group (1)
Application Note
High Speed DMA Controller
(HDMAC-A)
Memory to TSPI

Outlines

This application note is a reference material for developing products that the function of transferring data from memory to peripheral device using high speed DMA controller (HDMAC) of M4G group (1).
This document helps the user check operation of the product and develop its program.

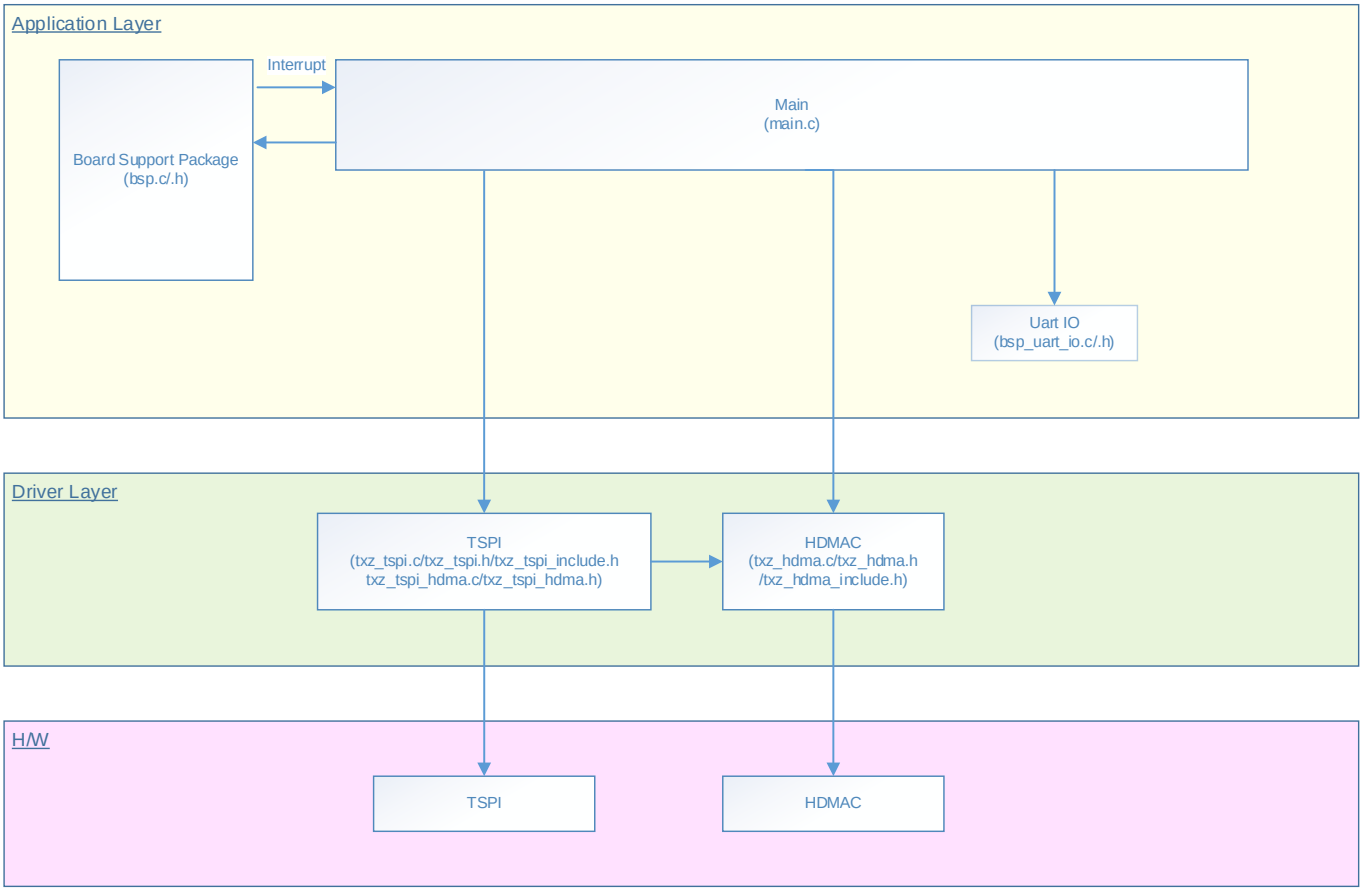
Target sample program: HDMA_TSPI_MEM

Table of Contents

1. Preface

This is a sample program used for operation check of the transferring operation from memory using HDMAC to peripheral functions.
The received data is directly transferred and output from memory to a peripheral device (TSPI), not via CPU.

Structure diagram of Sample program



2. Reference Document

- Datasheet
  TMPM4G group (1) datasheet Rev1.0 (Japanese edition)
- Reference manual
  High Speed DMA Controller (HDMAC-A) Rev1.0 (Japanese edition)
  Serial Peripheral Interface (TSPI-C) Rev1.0 (Japanese edition)
  Asynchronous Serial Communication Circuit (UART-C) Rev3.0 (Japanese edition)
- Application Note
  M4G Group (1) Application Note Startup (CMSIS System & Clock Configuration) Rev1.0
- Other reference document
  TMPM4G (1) Group Peripheral Driver User Manual (Doxygen)

3. Function to Use

IP	Channel	Port	Function Operation mode
Asynchronous Serial Communication Circuit	ch0	PE2(UT0RXD) PE3(UT0TXDA)	UART mode
Serial Peripheral Interface	ch2	PA4(TSPI2TXD) PA5(TSPI2RXD) PA6(TSPI2SCK)	SPI mode
High Speed DMA Controller	ch0 (transfer) ch3 (request)	-	Memory to Peripheral Device (Register) Burst transfer

4. Target Device

The target devices of this application note are as follows;

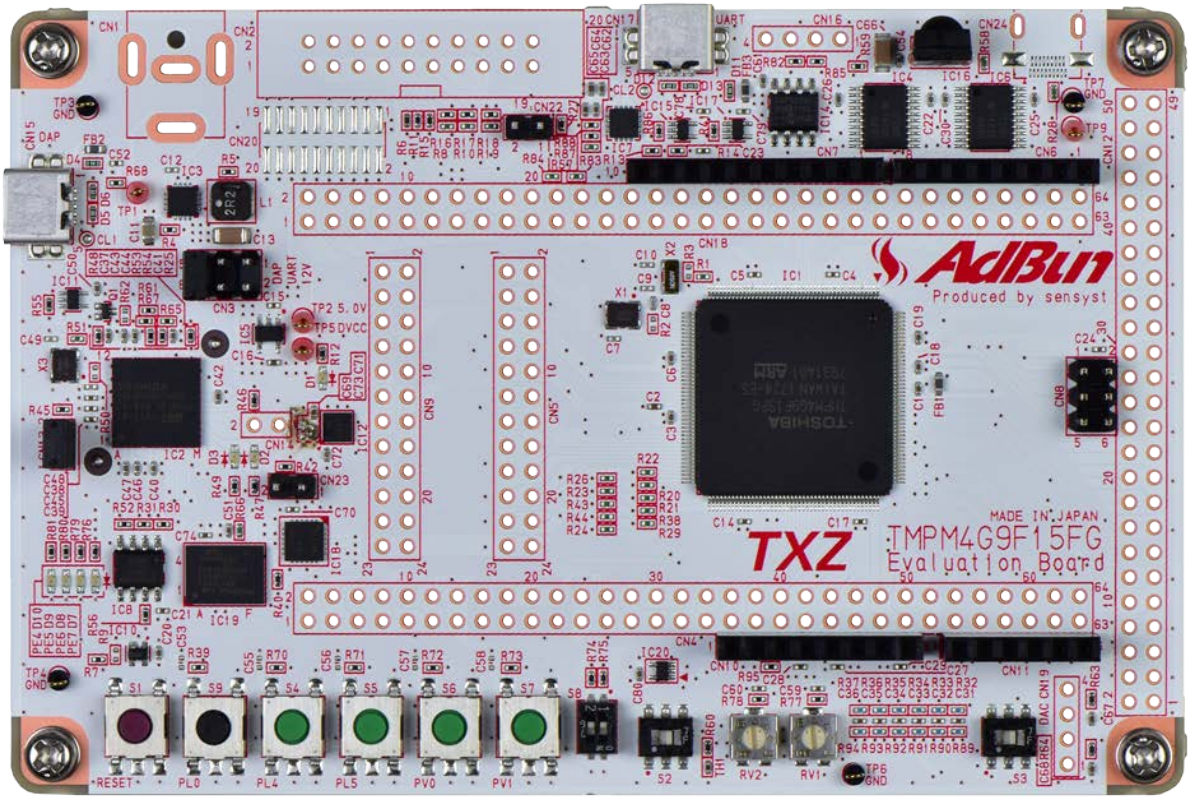
TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
	TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
	TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG

*This sample program operates on the evaluation board of TMPM4G9F15FG.
If other function than the TMPM4G9F15 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.
The BSP related file is dedicated to the evaluation board (TMPM4G9F15). If other function than the TMPM4G9F15 one is checked, the BSP related file should be changed properly.

5. Operation Confirmation Condition

Used microcontroller	TMPM4G9F15FG
Used board	TMPM4G9F15FGEvaluation Board by Sensyst
Unified development environment	IAR Embedded Workbench for ARM 8.11.2.13606
Unified development environment	µVision MDK Version 5.24.2.0
Terminal software	Tera Term V4.96
Sample program	V1000

Evaluation board (TMPM4G9F15FG Evaluation Board) Top view

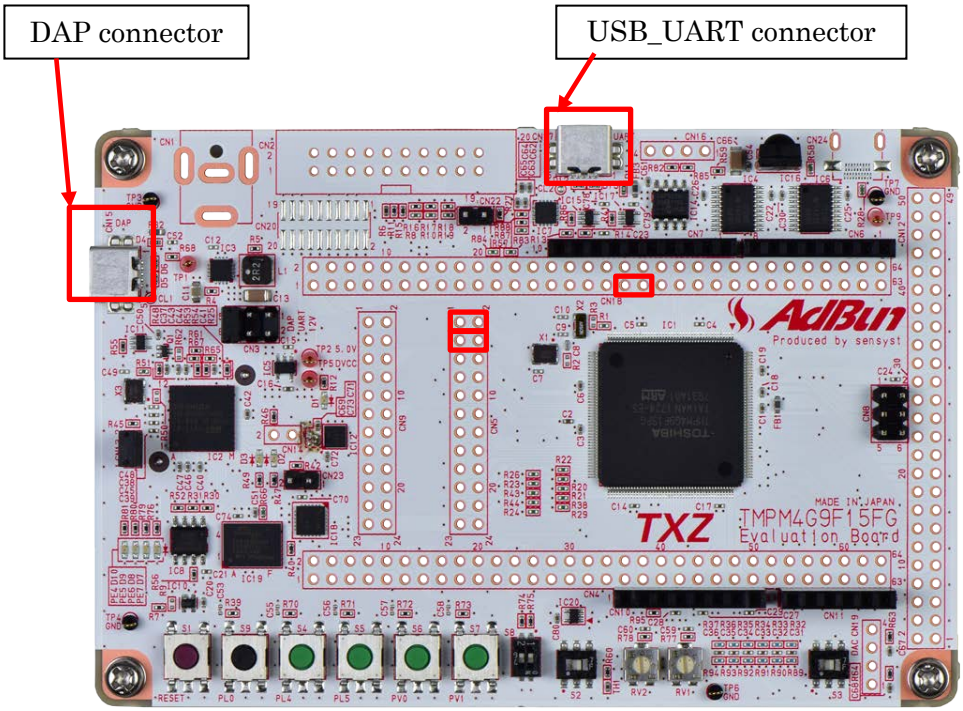


6. Evaluation Board Setting

The following pin connections should be done on the evaluation board.

CN5		
Board function	Through-hole No.	Through-hole No.
USB UART conversion	1:USB_UT_RX	2:PE2
USB UART conversion	3:USB_UT_TX	4:PE3

CN18		
Board function	Through-hole No.	Through-hole No.
TSPI (TXD-RXD)	35:PA4	37:PA5



7. Operation of Evaluation Board

PC and the USB_UART are connected for communication with the terminal software.
Enters an arbitrary character to the terminal software.
Receives the entered value via UART. The received data is transferred from memory to the TSPI, and is output to the terminal software via UART.

8. Outline of HDMAC Function

The functions of HDMAC per unit are shown in the following table.

Function category	Function	Description
Transfer request	Peripheral function	Transfer request from a peripheral device (Single transfer request/Burst transfer request)
	Software	Transfer request by software (Single transfer request/Burst transfer request)
	Request channel	16 channels (Transfer request count by peripheral devices)
Transfer mode	Single transfer	Data transfer is executed once.
	Burst transfer	Data transfer is executed once or multiple times Burst size: 1, 4, 8, 16, 32, 64, 128, and 256 beats Continuous data transfer of the specified burst count is possible without releasing the bus using the lock transfer setting.
	Chain transfer	Continuous data transfer is possible using discontinuous addresses according to Linked List Item (LLI).
Transfer type	Transfer source -> Transfer destination	Peripheral device (Register) -> Memory Peripheral device (Register) -> Peripheral device (Register) Memory -> Peripheral device (Register) Memory -> Memory (start up by only software)
Transfer control	Transfer channel	2 channels (ch 0 and ch 1)
	Transfer address	Addresses of the transfer source and destination are set. Selection of the increment of the address or fixed address for either the transfer source or destination.
	Transfer data size	8 bits, 16 bits, or 32 bits The sizes of the transfer source and destination can be set independently.
	Priority	ch 0 > ch 1 (Fixed in the unit.) Unit A > Unit B (For the integrated units, refer to “Product Information”.)
	FIFO	4 Words x 2 ch (1 Word = 32 bits)
Transfer count	Transfer count	4095 at maximum Infinite count transfers can be done using LLI.
Endian	Little endian	-
Interrupt	Transfer completion interrupt	Transfer completion interrupt (INTHDMACxTC) is generated when a transfer completes.
	Error interrupt	Error interrupt (INTHDMACxERR) is generated when a bus error or a memory protection error is detected during data transfer.

9. Sample Program

The sample program transfers the data received from the terminal software via UART to memory. The received data are transmitted from memory using the loopback of TSPI. The received data using the loopback of TSPI are transferred to memory, and it will be output from memory to the terminal software via UART. This sample program performs the transmission from memory to TSPI via HDMAC.

9.1. Initialization

The following initialization is done after power is supplied.
The initialization of each clock setting and the setting of the watchdog timer are done.

9.2. Sample Program Main Operation

The initialization of BSP is executed.
The initialization of driver is executed.
The initialization of applications is executed.
UART and TSPI are set within application initialization.

Go to main processing and make HDMAC setting within main program processing.
A message "Input =" prompting input to terminal software is output.
Wait until input comes from terminal software.
The input data is saved in memory via UART.
The DMAC transferred data is transmitted and received by TSPI.
The saved data will be displayed in the terminal software after "transdata =" via UART.
If the input character exceeds 10 byte (including a line feed code), an input error is output to the terminal software.

9.3. HDMA_TSPI_MEM Setting

The transfer channels of the sample program are changed with the following parameter(s):
Change of CFG_DMA_CH in the main.c

9.4. Output Example of Sample Program

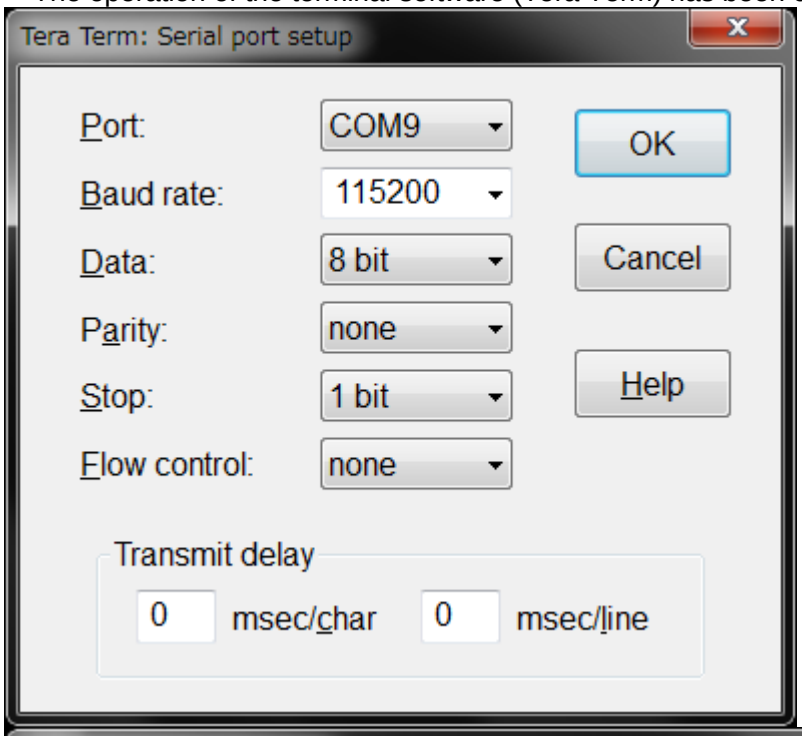
When the sample program is operated, the transferred result by HDMAC are output as follows:

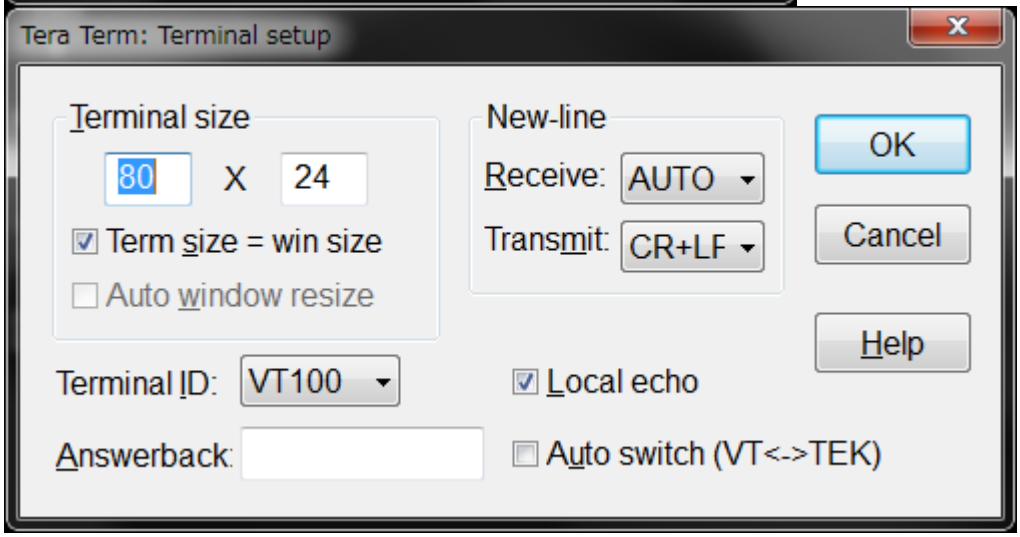
```
Input = 12345678
transdata = 12345678

Input =
```

9.4.1. Setting Example of Terminal Software

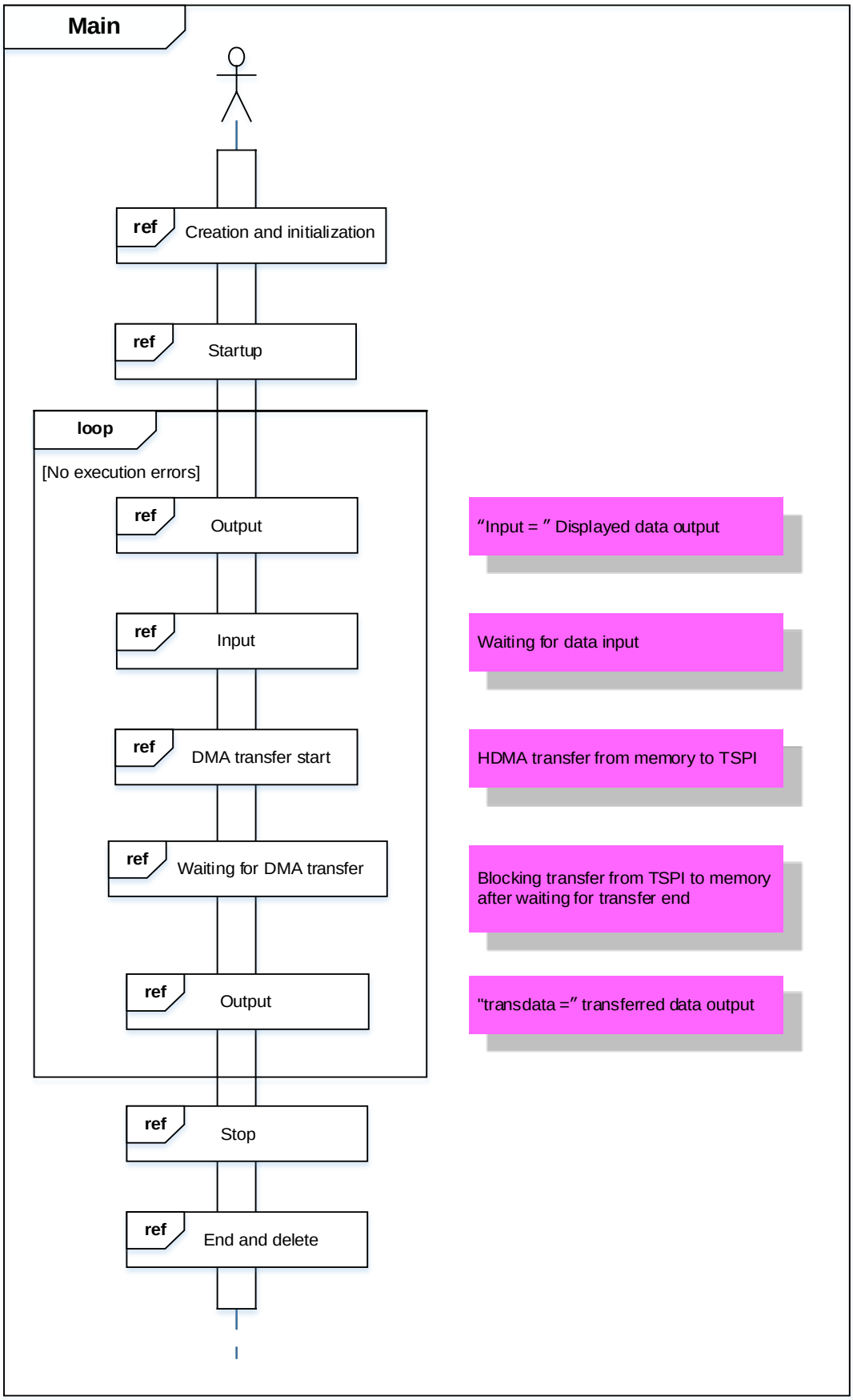
The operation of the terminal software (Tera Term) has been checked with the following settings.

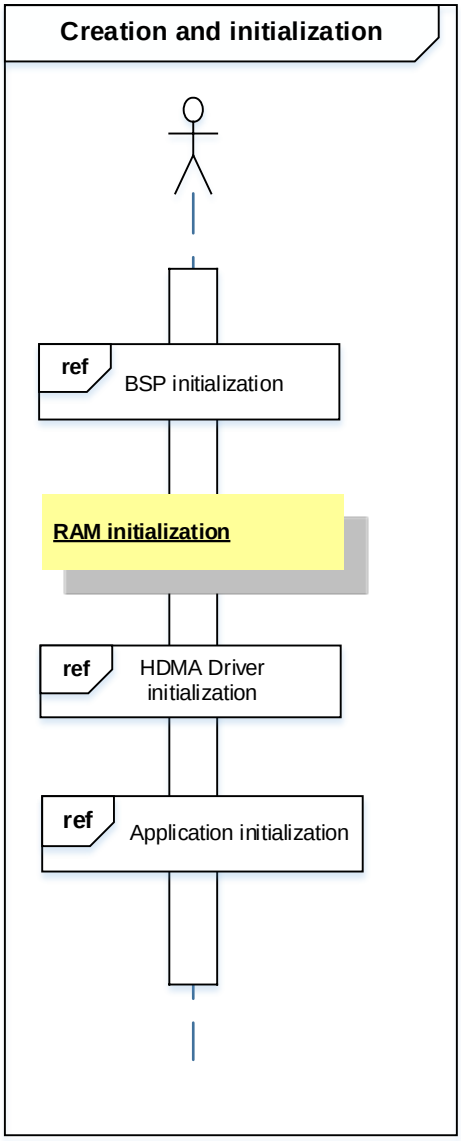


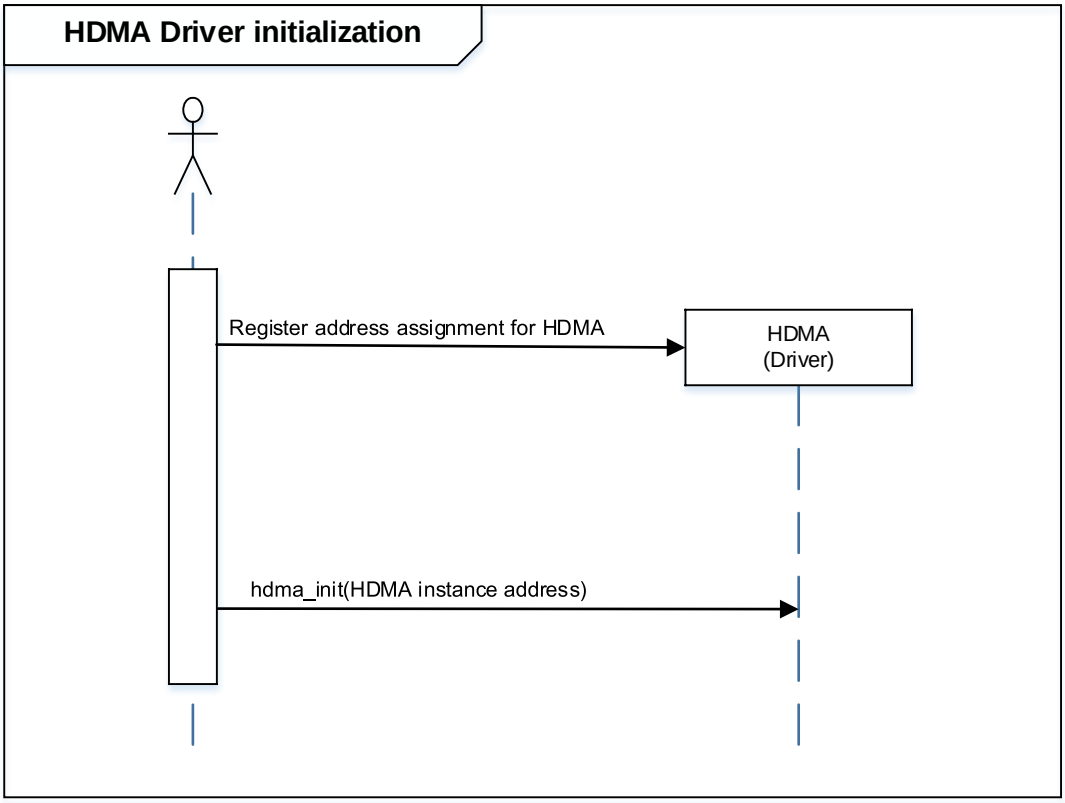


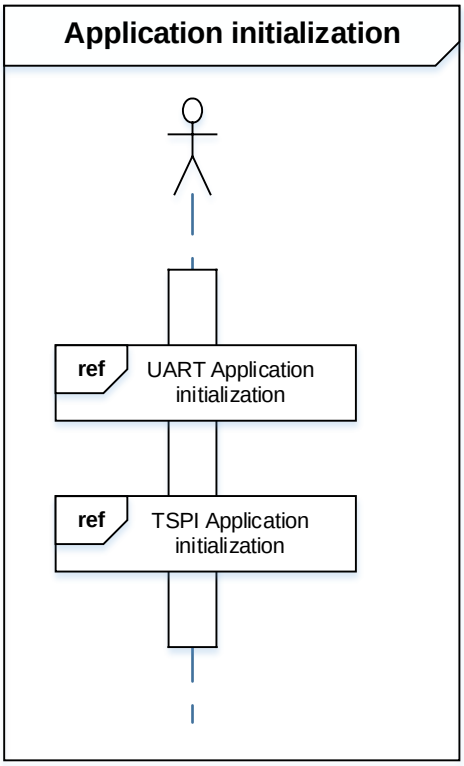
9.5. Operating Flow of Sample Program

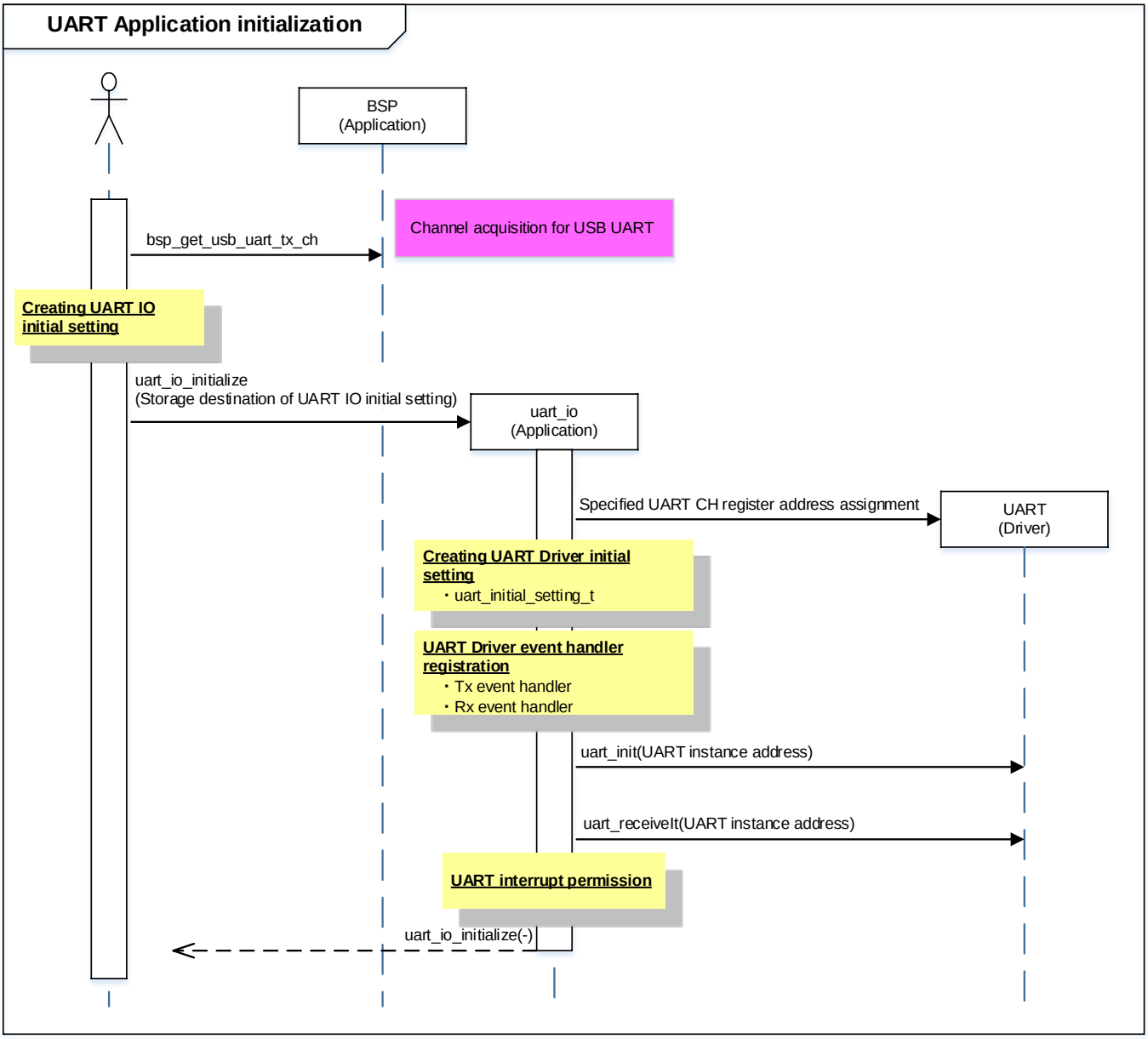
The basic operating flows of the sample program are shown in the following.

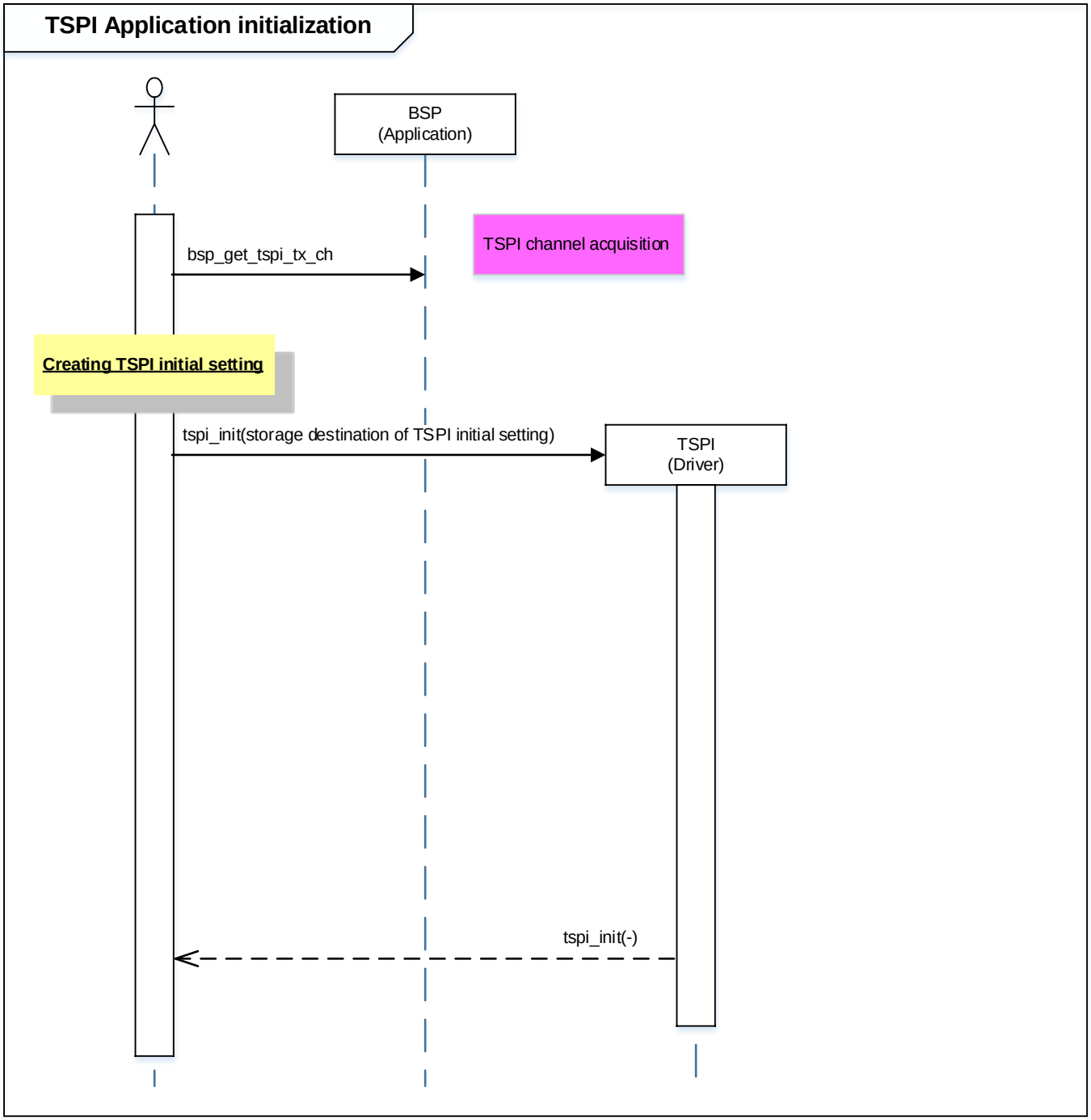


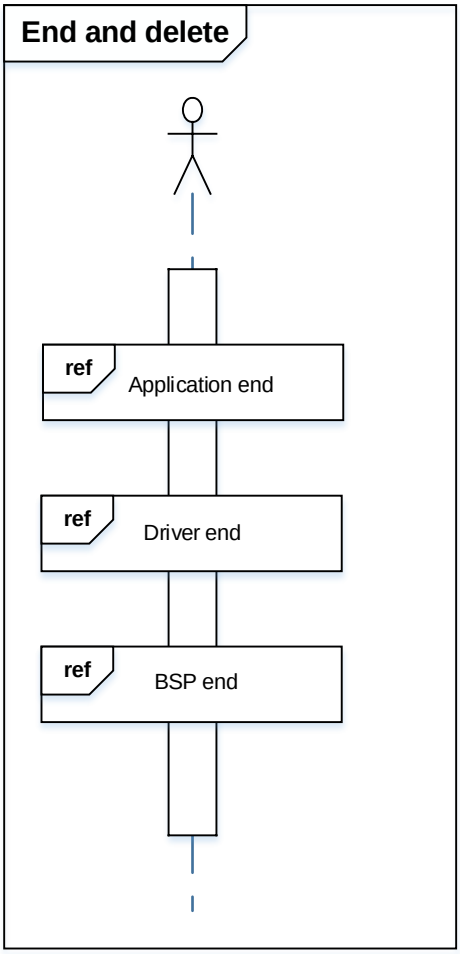

Creation and initialization
ref
BSP initialization
RAM initialization
ref
HDMA Driver initialization
ref
Application initialization

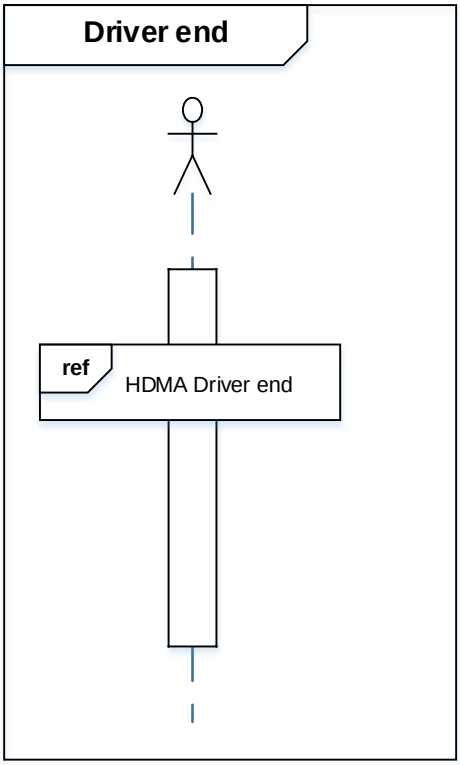

HDMA Driver initialization
Register address assignment for HDMA
HDMA
(Driver)
hdma_init(HDMA instance address)

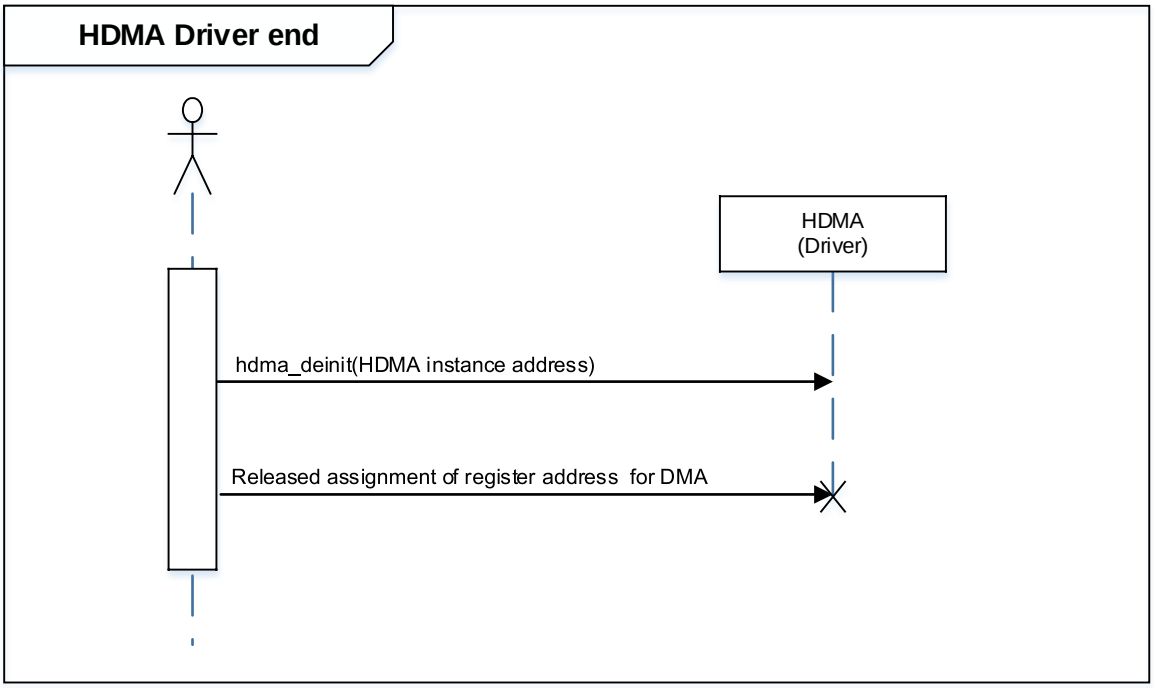

Application initialization
ref
UART Application
initialization
ref
TSPI Application
initialization

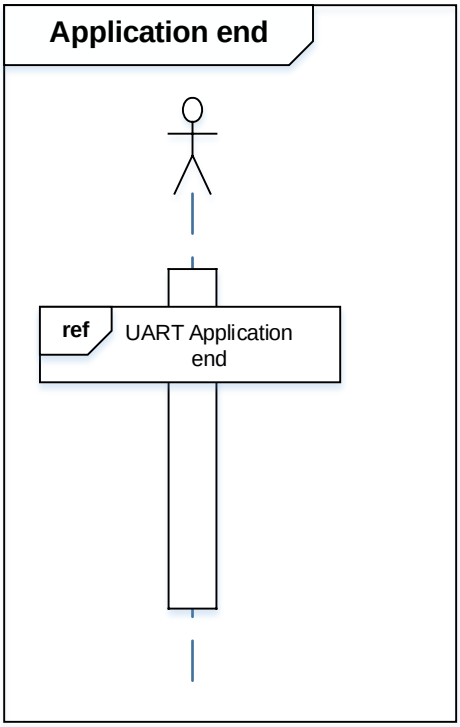

UART Application initialization
BSP
(Application)
Channel acquisition for USB UART
bsp_get_usb_uart_tx_ch
Creating UART IO initial setting
uart_io_initialize
(Storage destination of UART IO initial setting)
uart_io
(Application)
Specified UART CH register address assignment
UART
(Driver)
Creating UART Driver initial setting
・uart_initial_setting_t
UART Driver event handler registration
・Tx event handler
・Rx event handler
uart_init(UART instance address)
uart_receiveIt(UART instance address)
UART interrupt permission
uart_io_initialize(-)

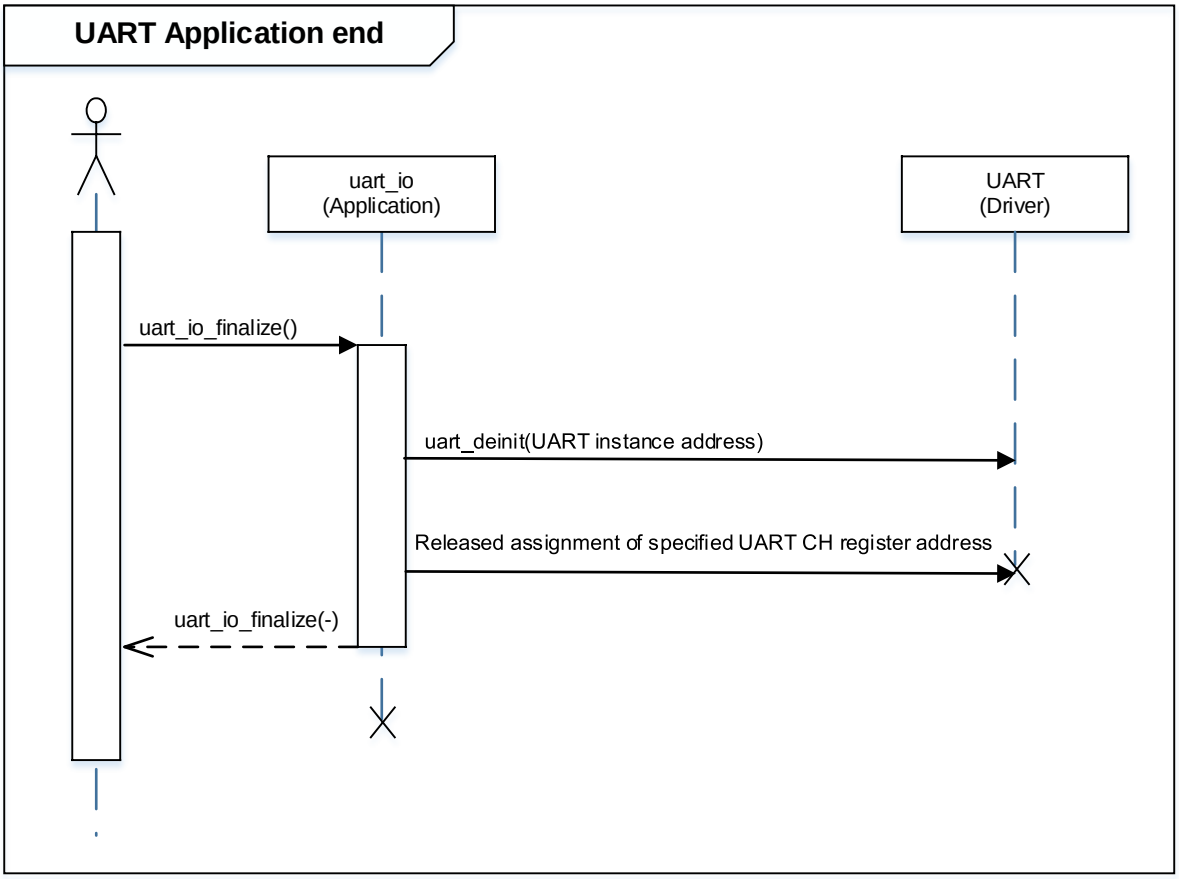

TSPI Application initialization
BSP
(Application)
TSPI channel acquisition
bsp_get_tspi_tx_ch
Creating TSPI initial setting
tspi_init(storage destination of TSPI initial setting)
TSPI
(Driver)
tspi_init(-)

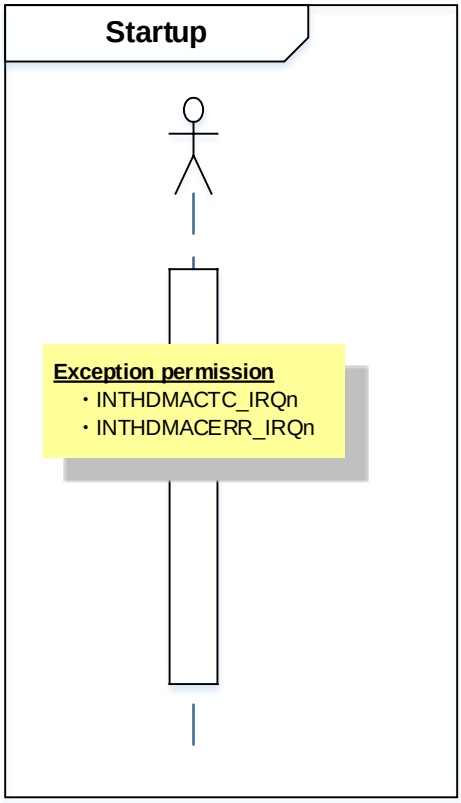

End and delete
ref
Application end
ref
Driver end
ref
BSP end

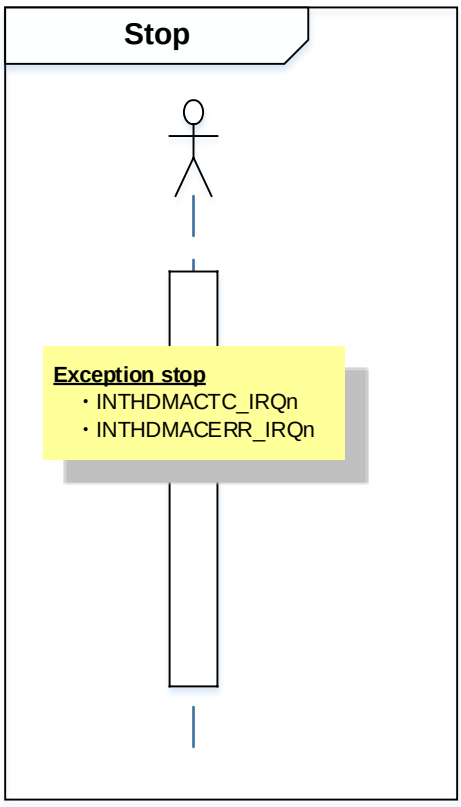

Driver end
ref
HDMA Driver end

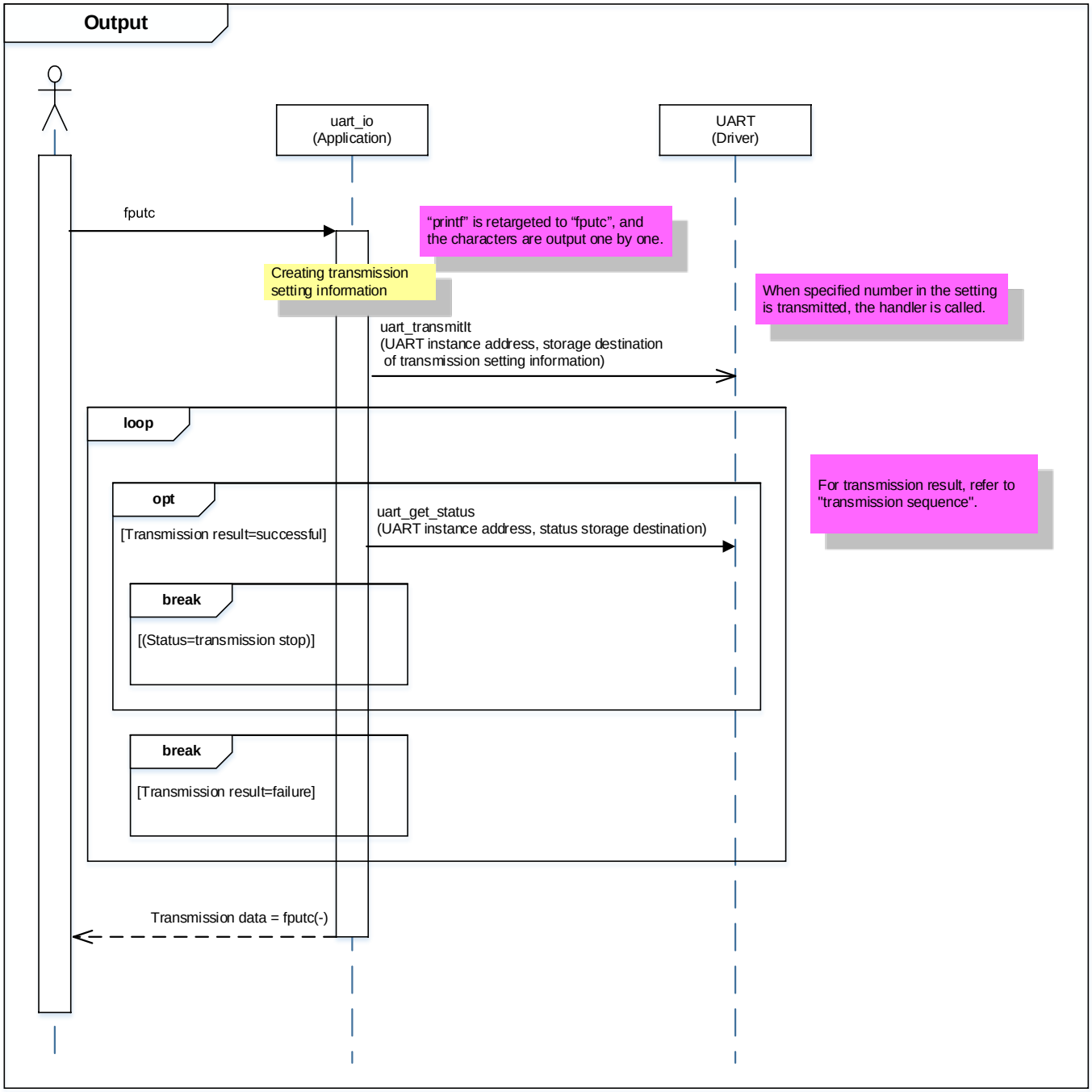

HDMA Driver end
HDMA
(Driver)
hdma_deinit(HDMA instance address)
Released assignment of register address for DMA

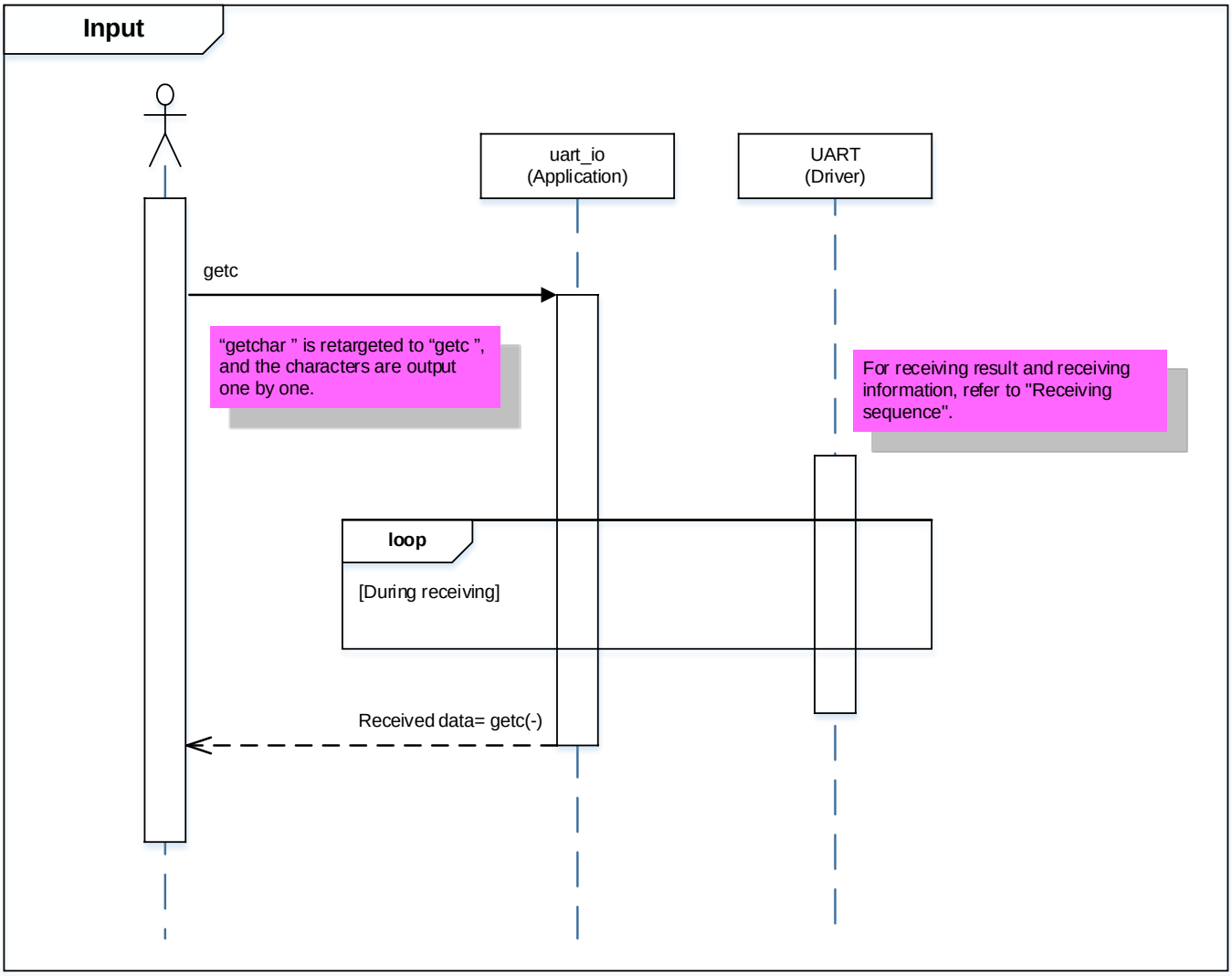

Application end
ref
UART Application
end

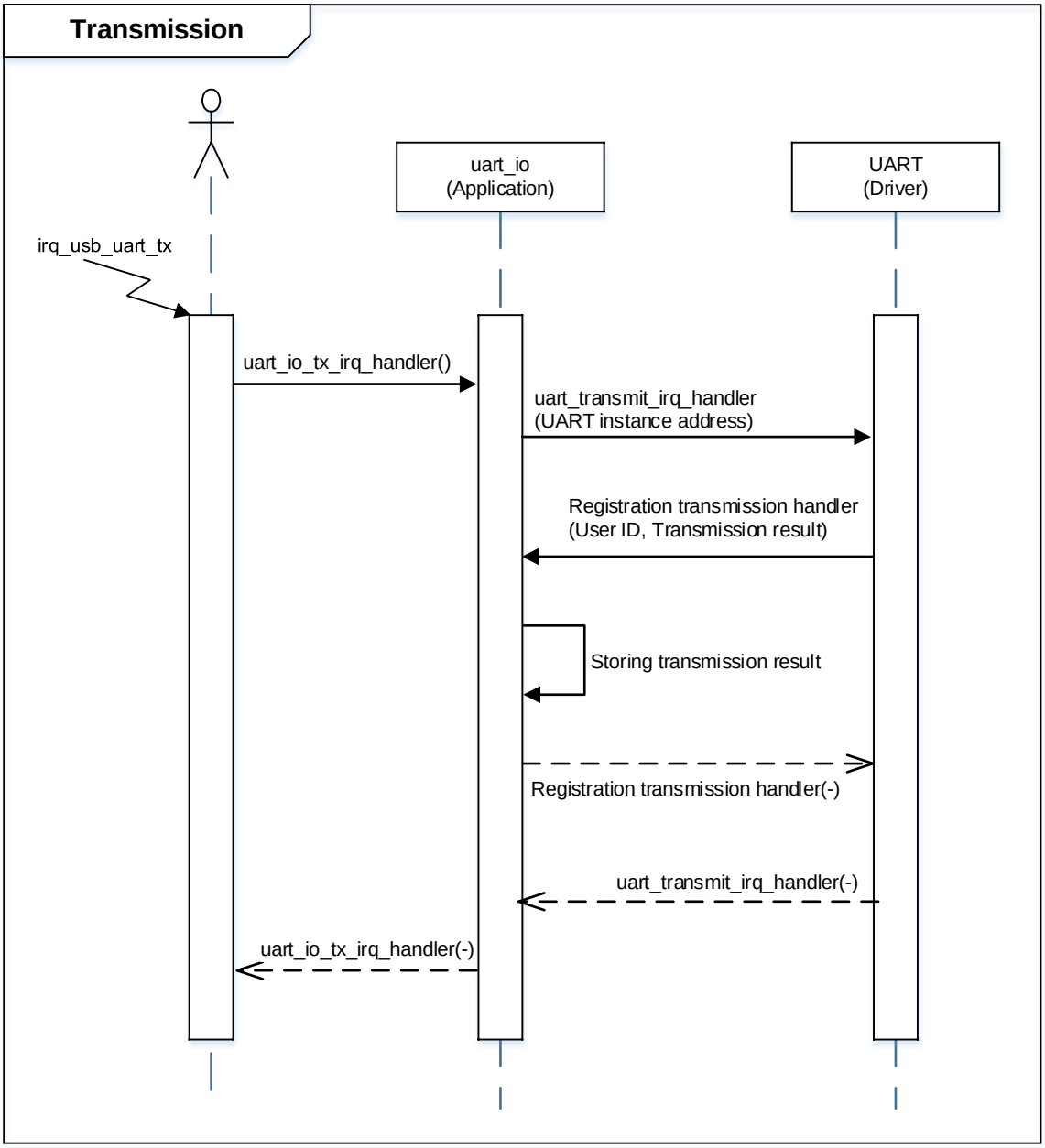

UART Application end
uart_io
(Application)
UART
(Driver)
uart_io_finalize()
uart_deinit(UART instance address)
Released assignment of specified UART CH register address
uart_io_finalize(-)

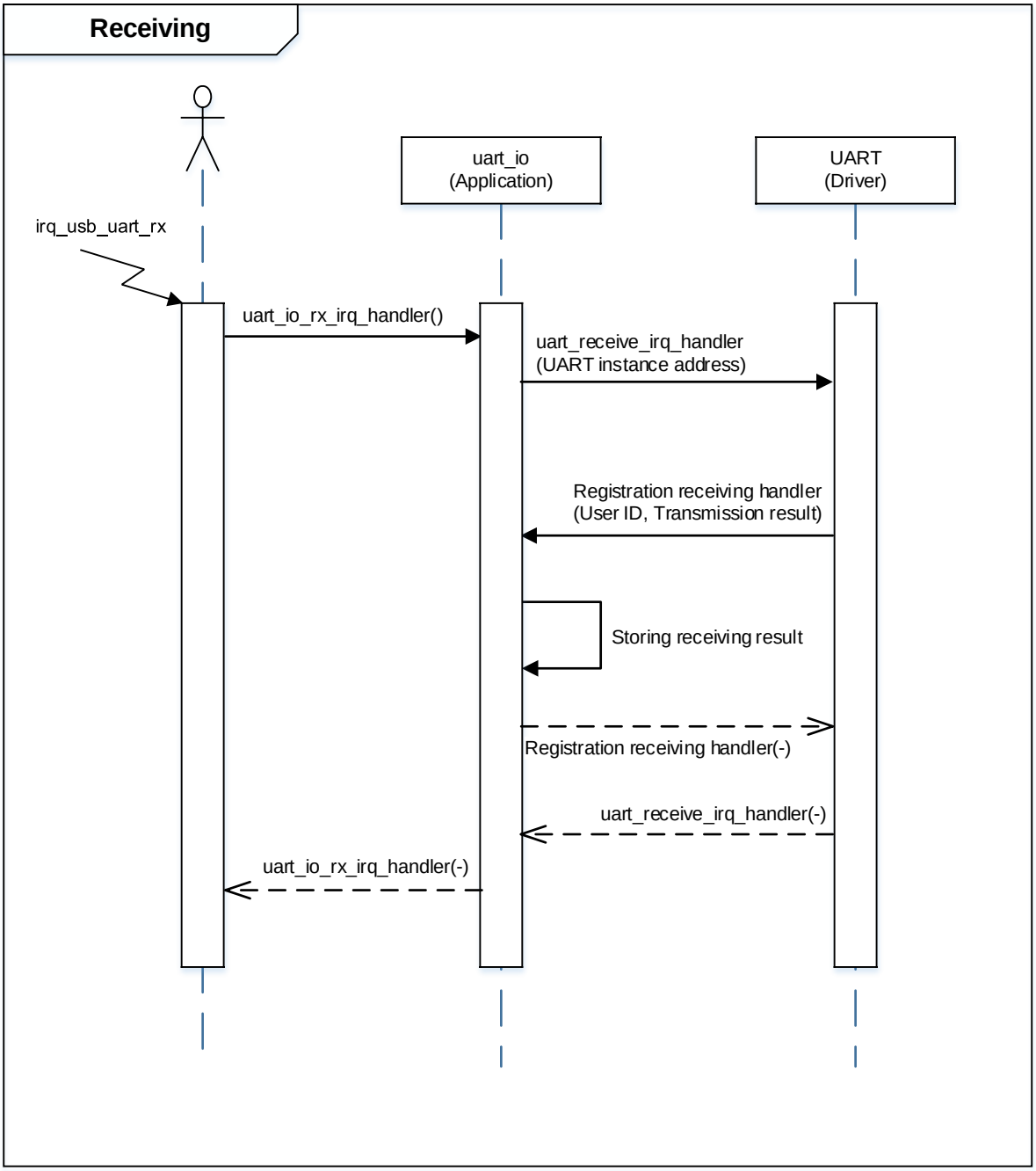

Startup
Exception permission
・INTHDMACTC_IRQn
・INTHDMACERR_IRQn

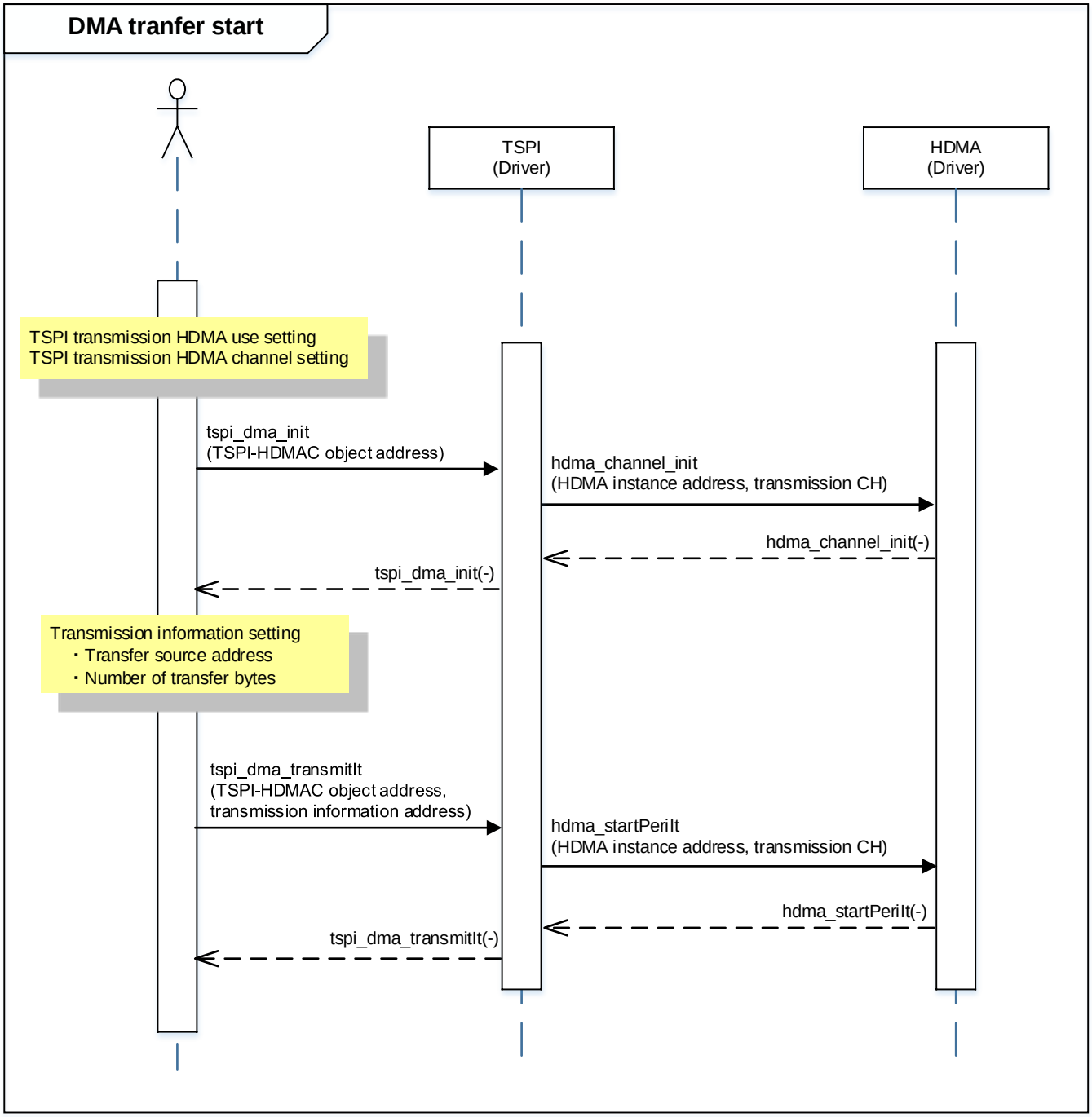

Stop
Exception stop
・INTHDMACTC_IRQn
・INTHDMACERR_IRQn

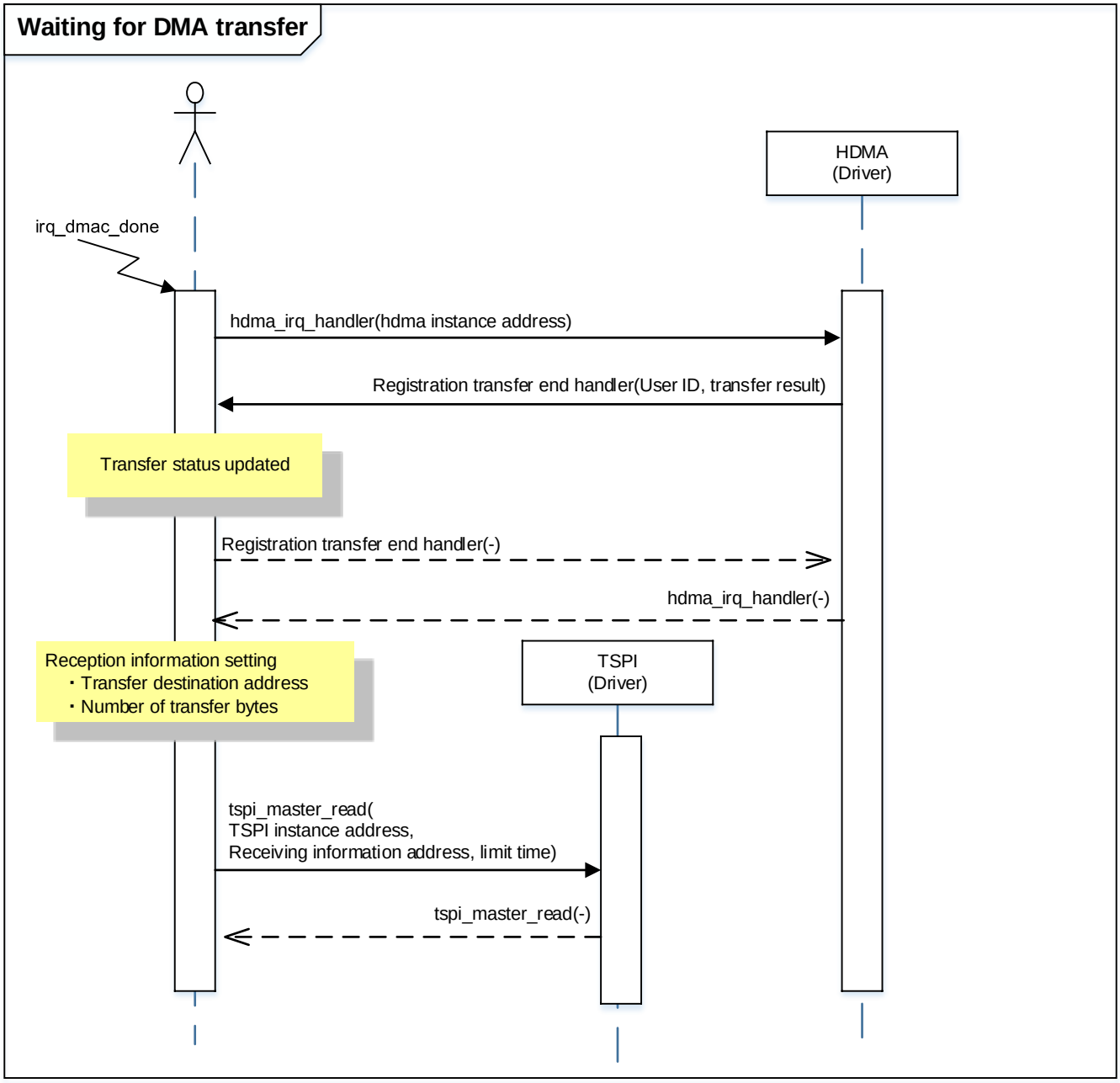

Output
uart_io
(Application)
UART
(Driver)
fputc
“printf” is retargeted to “fputc”, and
the characters are output one by one.
Creating transmission
setting information
When specified number in the setting
is transmitted, the handler is called.
uart_transmitIt
(UART instance address, storage destination
of transmission setting information)
loop
opt
[Transmission result=successful]
uart_get_status
(UART instance address, status storage destination)
For transmission result, refer to
"transmission sequence".
break
[(Status=transmission stop)]
break
[Transmission result=failure]
Transmission data = fputc(-)


Input
uart_io
(Application)
UART
(Driver)
getc
“getchar ” is retargeted to “getc ”, and the characters are output one by one.
For receiving result and receiving information, refer to "Receiving sequence".
loop
[During receiving]
Received data= getc(-)


Transmission
uart_io
(Application)
UART
(Driver)
irq_usb_uart_tx
uart_io_tx_irq_handler()
uart_transmit_irq_handler
(UART instance address)
Registration transmission handler
(User ID, Transmission result)
Storing transmission result
Registration transmission handler(-)
uart_transmit_irq_handler(-)
uart_io_tx_irq_handler(-)


Receiving
uart_io
(Application)
UART
(Driver)
irq_usb_uart_rx
uart_io_rx_irq_handler()
uart_receive_irq_handler
(UART instance address)
Registration receiving handler
(User ID, Transmission result)
Storing receiving result
Registration receiving handler(-)
uart_receive_irq_handler(-)
uart_io_rx_irq_handler(-)


DMA tranfer start
TSPI
(Driver)
HDMA
(Driver)
TSPI transmission HDMA use setting
TSPI transmission HDMA channel setting
tspi_dma_init
(TSPI-HDMAC object address)
hdma_channel_init
(HDMA instance address, transmission CH)
hdma_channel_init(-)
tspi_dma_init(-)
Transmission information setting
・Transfer source address
・Number of transfer bytes
tspi_dma_transmitIt
(TSPI-HDMAC object address,
transmission information address)
hdma_startPeriIt
(HDMA instance address, transmission CH)
hdma_startPeriIt(-)
tspi_dma_transmitIt(-)


Waiting for DMA transfer
HDMA
(Driver)
irq_dmac_done
hdma_irq_handler(hdma instance address)
Registration transfer end handler(User ID, transfer result)
Transfer status updated
Registration transfer end handler(-)
hdma_irq_handler(-)
Reception information setting
・Transfer destination address
・Number of transfer bytes
TSPI
(Driver)
tspi_master_read(
TSPI instance address,
Receiving information address, limit time)
tspi_master_read(-)

10. Precaution

When using the sample program with CPU other than TMPM4G9F15, please check operation sufficiently.

11. Revision History

Rev	Date	Description
1.0	2018-11-30	First release

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