

M4G Group (1)
Application Note
I²C Interface
(I2C-B)

Outlines

This application note is a reference material for developing products using I²C interface (I2C) function of M4G group (1).

This document helps the user check operation of the product and develop its program.

Target sample program: I2C_EEPROM

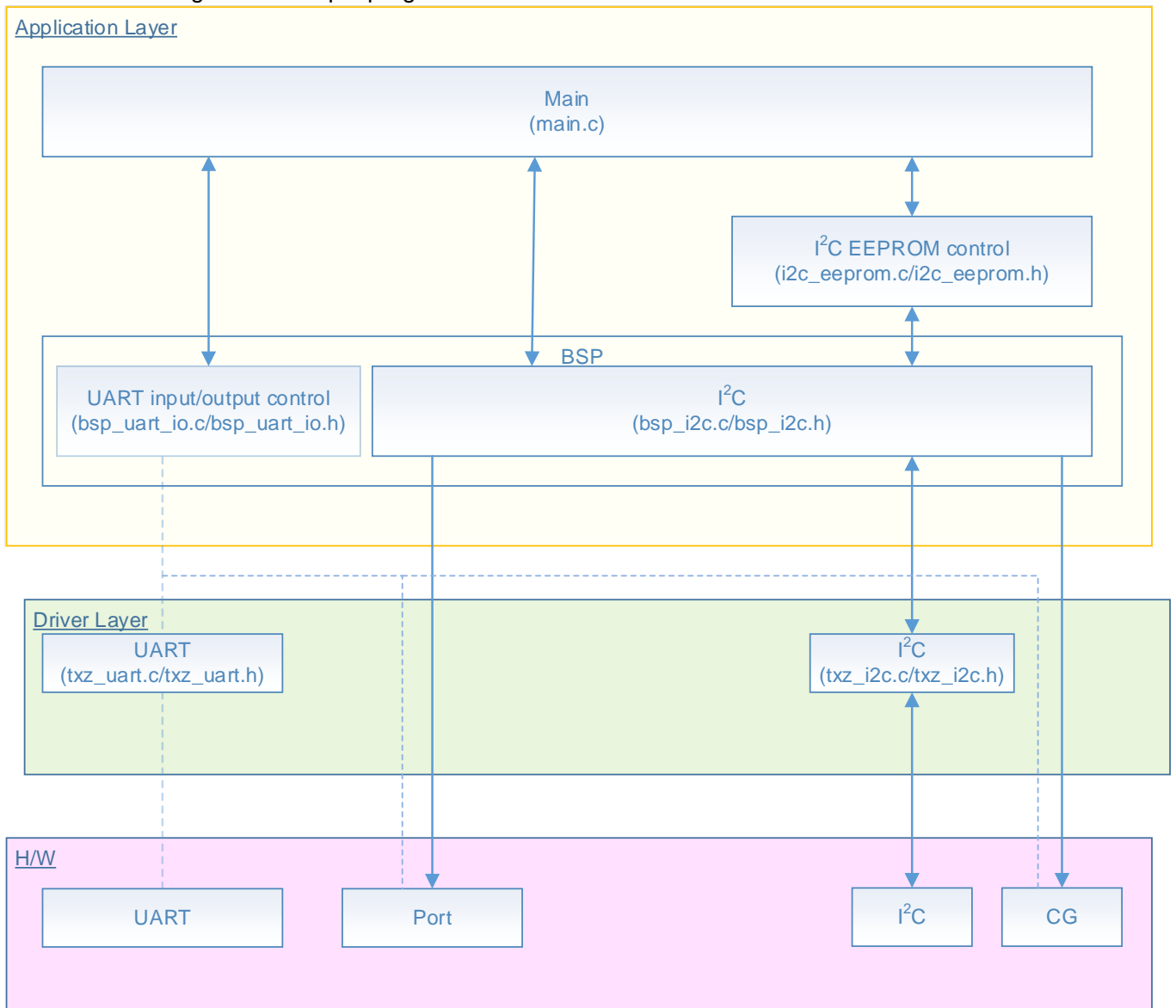
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1. Preface

This sample program should be used to check the operation of the I²C interface.
Read or write of the I²C EEPROM is done by input of a corresponding command to the terminal software.

Structure diagram of Sample program



2. Reference Document

- Datasheet
TMPM4G group (1) datasheet Rev1.0 (Japanese edition)
- Reference manual
I²C Interface (I2C-B) Rev2.1 (Japanese edition)
Asynchronous Serial Communication Circuit (UART-C) Rev3.0 (Japanese edition)
- Application note
M4G group (1) Application Note Startup (CMSIS System & Clock Configuration) Rev1.0
- Other reference document
TMPM4G (1) Group Peripheral Driver User Manual (Doxygen)

3. Function to Use

IP	Channel	Port	Function/Operation mode
Asynchronous Serial Communication Circuit	ch0	PE2 (UT0RXD) PE3 (UT0TXDA)	UART mode
I ² C Interface	ch3	PJ6 (I2C3SDA) PJ7 (I2C3SCL)	I ² C mode

4. Target Device

The target devices of this application note are as follows;

TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
	TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
	TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG

* This sample program operates on the evaluation board of TMPM4G9F15FG.

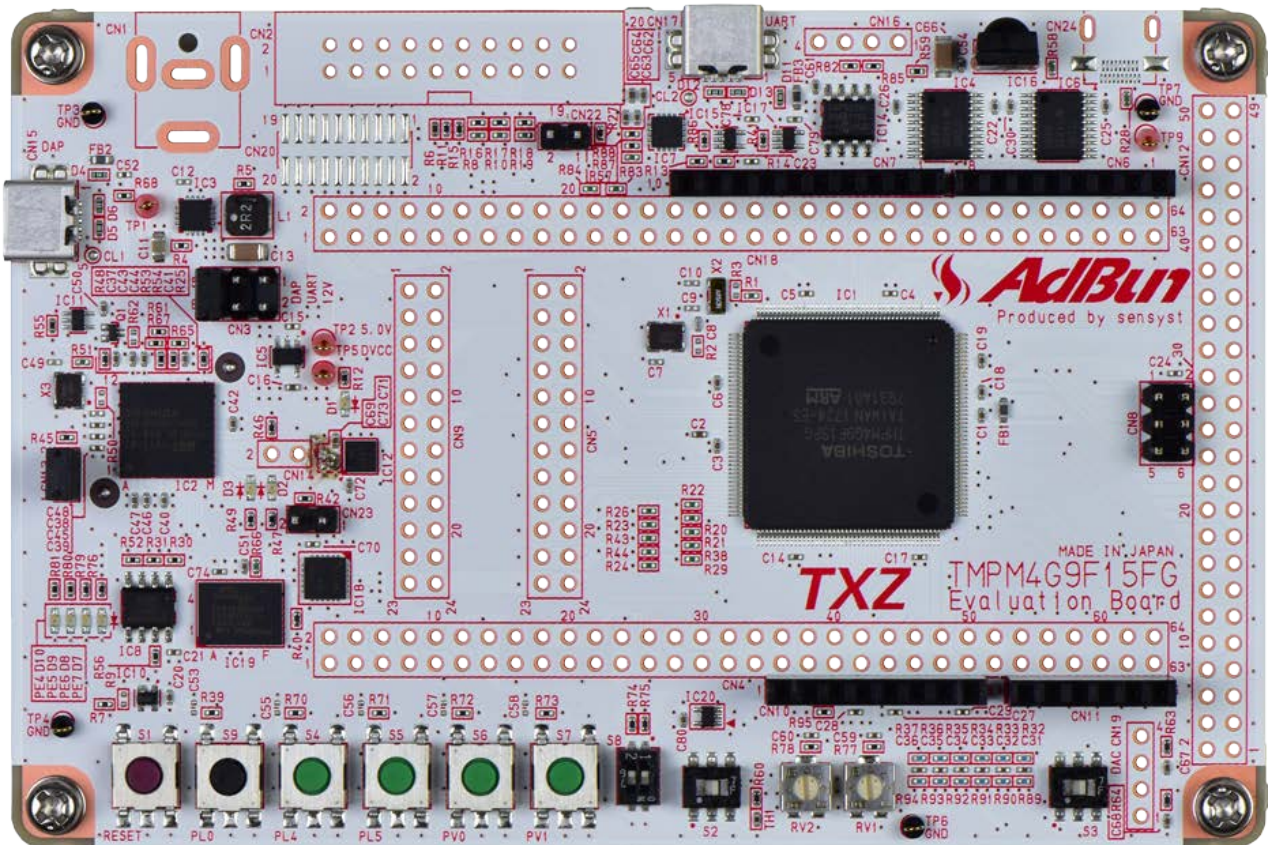
If other function than the TMPM4G9F15 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.

The BSP related file is dedicated to the evaluation board (TMPM4G9F15). If other function than the TMPM4G9F15 one is checked, the BSP related file should be changed properly.

5. Operation Confirmation Condition

Used microcontroller	TMPM4G9F15FG
Used board	TMPM4G9F15FG Evaluation Board by Sensystr
Unified development environment	IAR Embedded Workbench for ARM 8.11.2.13606
Unified development environment	µVision MDK Version 5.24.2.0
Terminal software	Tera Term V4.96
Sample program	V1000

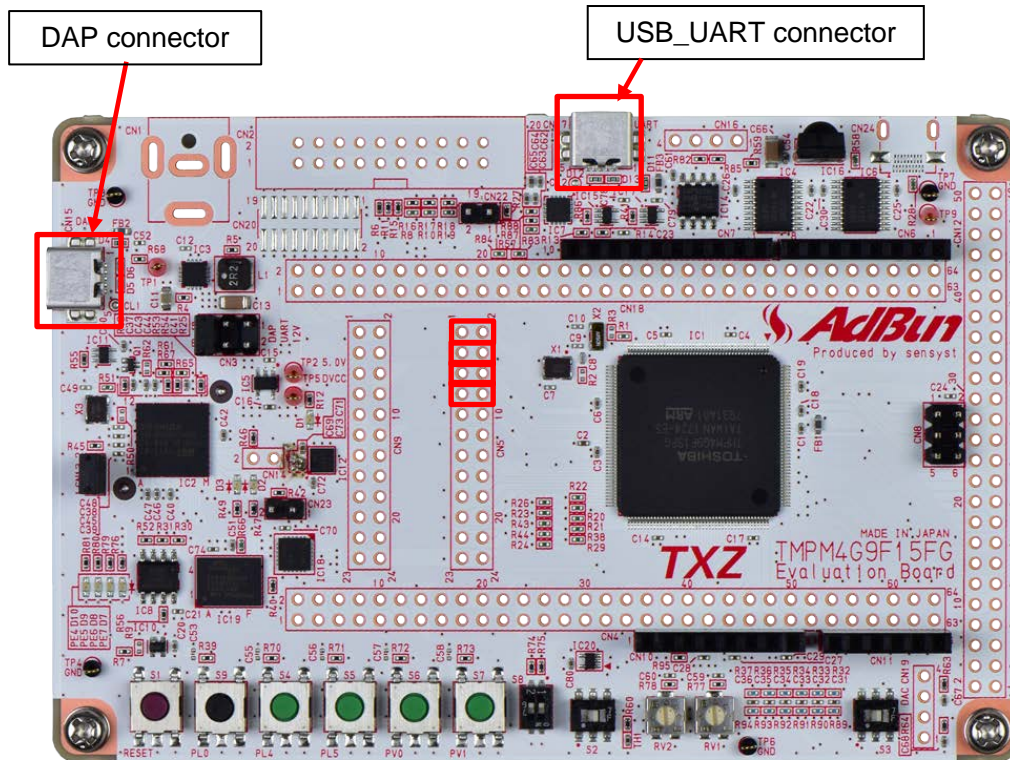
Evaluation board (TMPM4G9F15FG Evaluation Board) Top view



6. Evaluation Board Setting

The following pin connections should be done on the evaluation board.

CN5		
Board function	Through-hole No.	Through-hole No.
USB UART conversion	1: USB_UT_RX	2: PE2
USB UART conversion	3: USB_UT_TX	4: PE3
I ² C interface	5: EEPROM_I2C_SCL	6: PJ7
I ² C interface	7: EEPROM_I2C_SDA	8: PJ6



7. Operation of Evaluation Board

PC and the USB_UART are connected for communication with the terminal software. The terminal software (Tera Term) is started up, and the setting of the communication should be done. The reset button should be pushed down on the evaluation board. The communication starts according to an input command. For the details of the input operation of a command, refer to the section "Sample Program Main Operation".

8. Outline of I²C Function

The I²C can operate as a transceiver circuit of 1ch (SCL, SDA) in 1 unit circuit. The list of the functions is shown below.

Function classification (Note1)	Function	A Functional Description or the range
Transmission speed Control	prescaler dividing selection	It is dividing about a prescaler clock to 1/1, 1/2, 1/3 to 1/30, 1/31 and 1/32.
	Clock source	A selection setup of the HIGH/LOW time of SCL is possible in master mode.
	The maximum transfer rate	1Mbps (it corresponds to Fm+) (fsys = 8 to 200 MHz)
Communication Format	I ² C bus format	Selection of Addressing/Data Free Format is possible. Selection of a master/slave is possible.
	Data length	1 to 8 bits
	acknowledge	The existence of acknowledging can be chosen.
	Start/stop condition	Generating of start/stop condition is possible.
	Slave address	Only a 7-bit addressing format. 2 sets of slave addresses can be set up. (1st/2nd Slave Address)
	General call	Detection of a general call is possible in slave mode.
Transmission and reception Control	Arbitration	Multi-master Clock synchronization Existence selection of Arbitration lost detection is possible.
	Repetitive start detection, generating	Detection of a repetitive start of a bus line (at the time of slave mode) and generating (at the time of master mode) are possible.
	Noise cancellation	Digital
Ganged control	Interruption	4 kinds (The completion interruption of transmission, Arbitration lost detection interruption, Bus free detection interruption, NACK reception detection interruption)
	DMA request	A setup according to transmission and reception is possible.
	Software reset	Reset by the software of an I ² C circuit is possible.
	Bus terminal state monitor function	The level monitor of SDA and a SCL pin
	Address match Wakeup function	Slave address match detection can use the release factor for the Low power consumption mode release.

Note1: It does not support HS (High Speed) mode, 10-bit addressing, and a START byte.

Note2: There is a function in which it cannot support depending on products, such as slope control, I/O correspondence at the time of the power supply OFF, an Input voltage (VIH/VIL), and an Output voltage (VOL=0.4V, VDD>2V). Please refer to the "Product Information" of the reference manual for details.

9.3. Output Example of Sample Program

When the sample program executes, the command input and the result are displayed as shown in the following figure.

```
command > write toshiba
write data > toshiba

command > read
read data > toshiba

command > bw 1000 a
byte write data > a

command > bw 1001 b
byte write data > b

command > bw 1002 c
byte write data > c

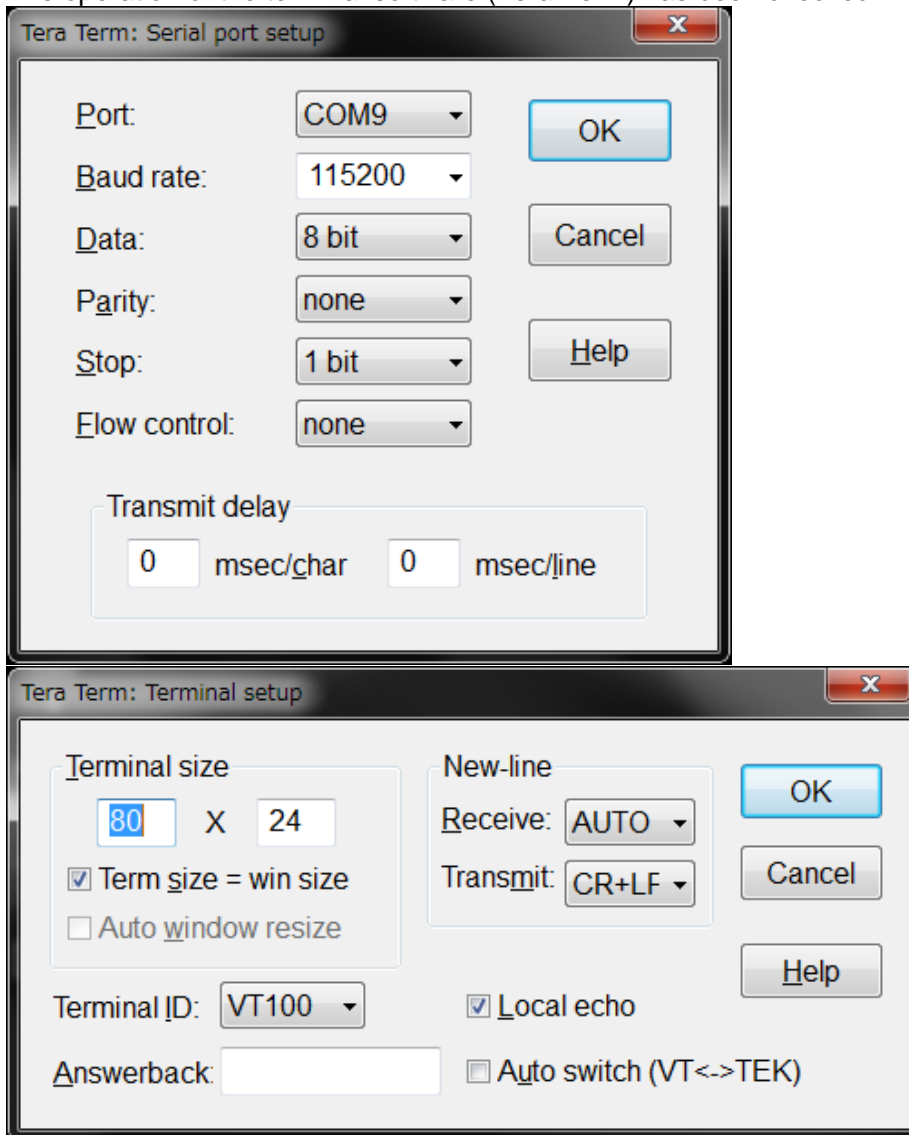
command > br 1000
byte read data > a

command > br 1001
byte read data > b

command > br 1002
byte read data > c
```

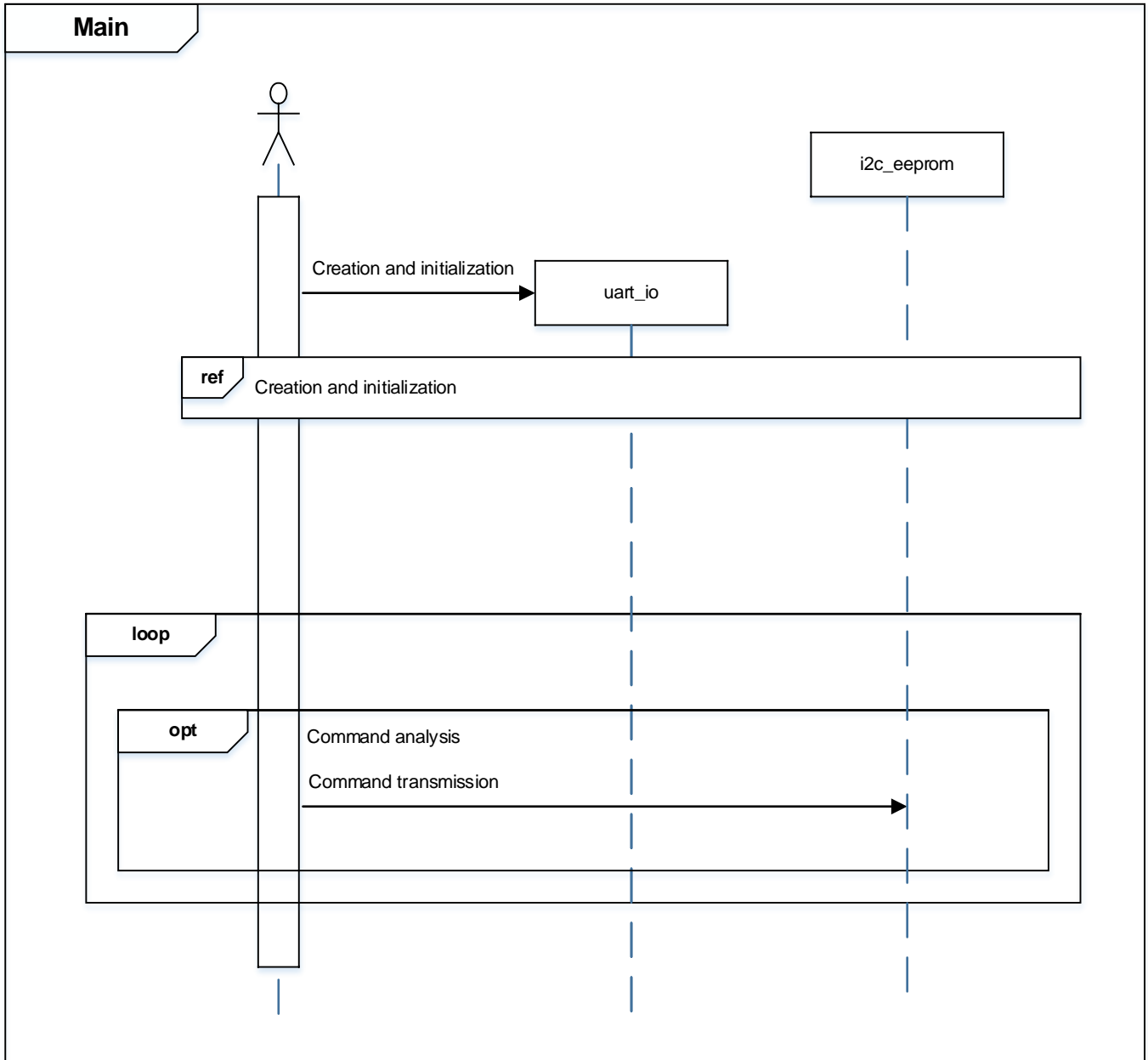
9.3.1. Setting Example of Terminal Software

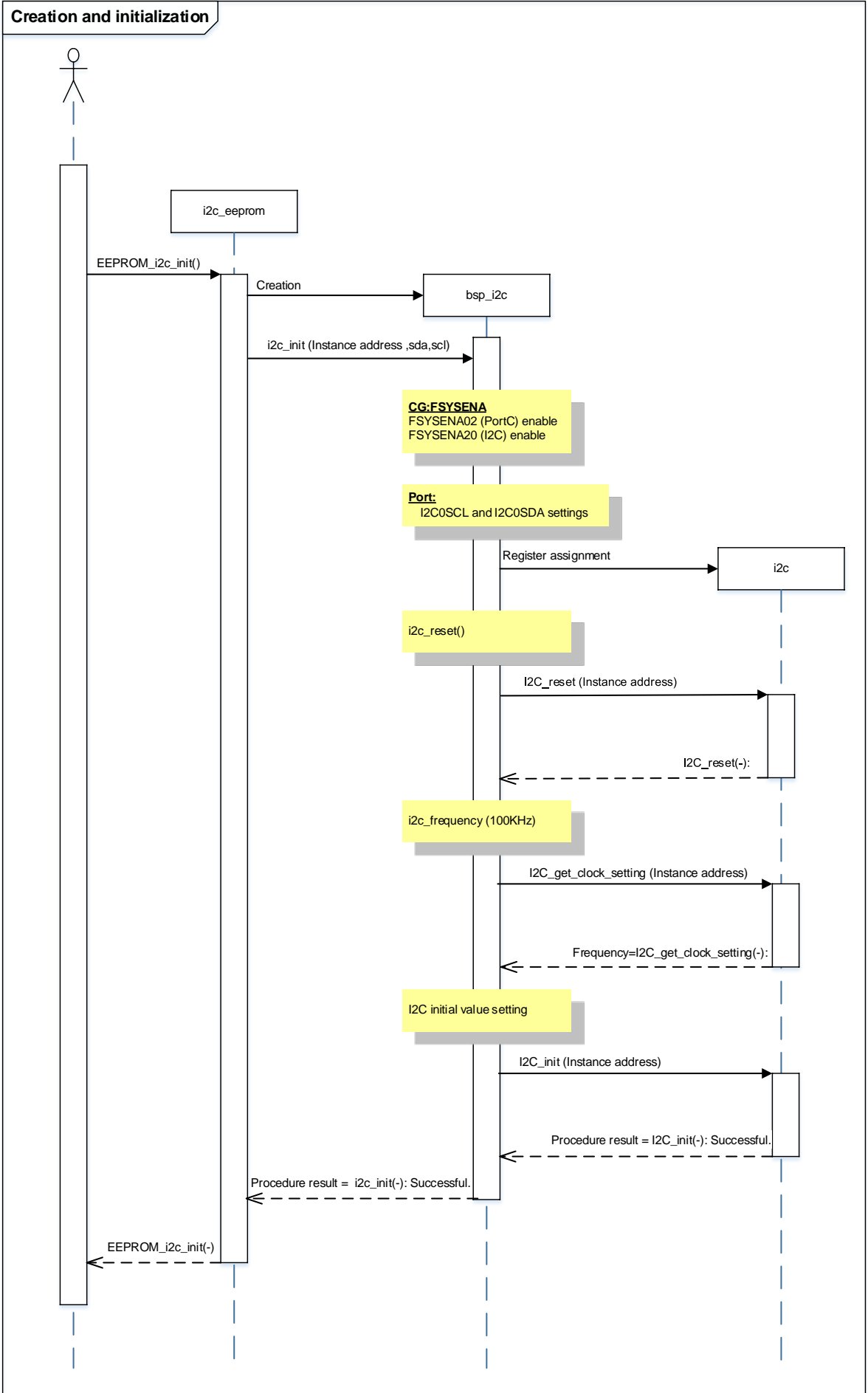
The operation of the terminal software (Tera Term) has been checked with the following settings.

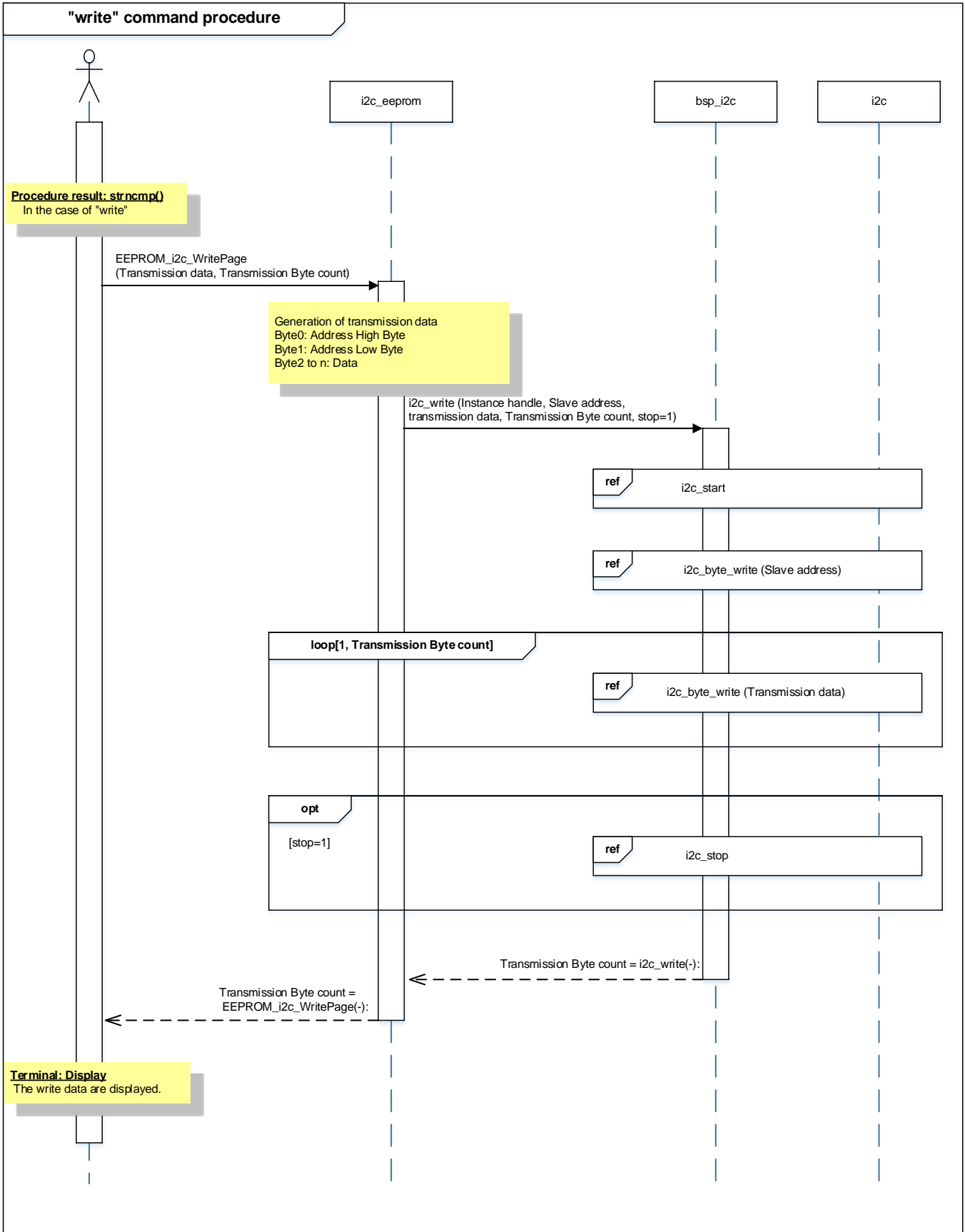


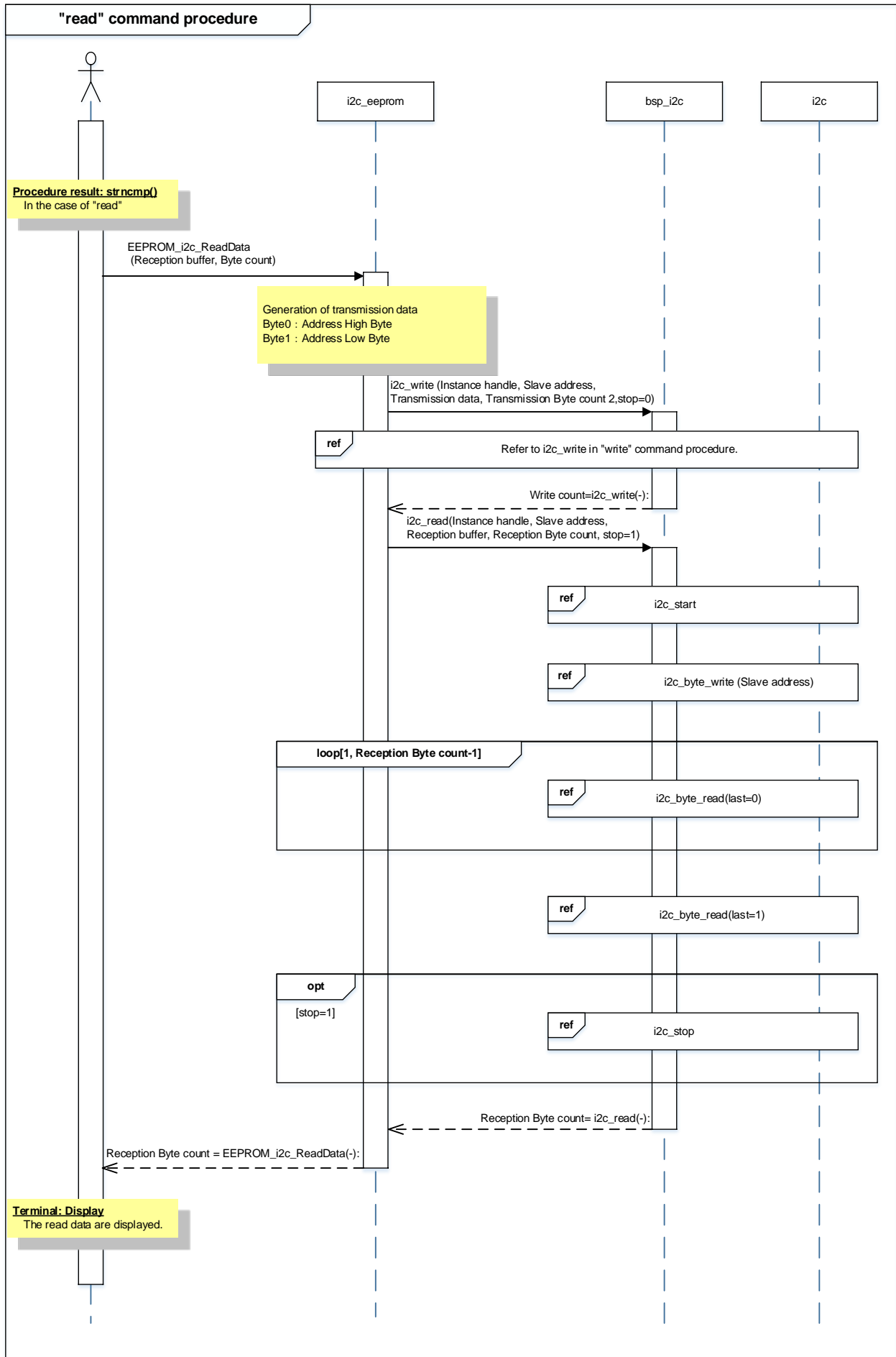
9.4. Operating Flow of Sample Program

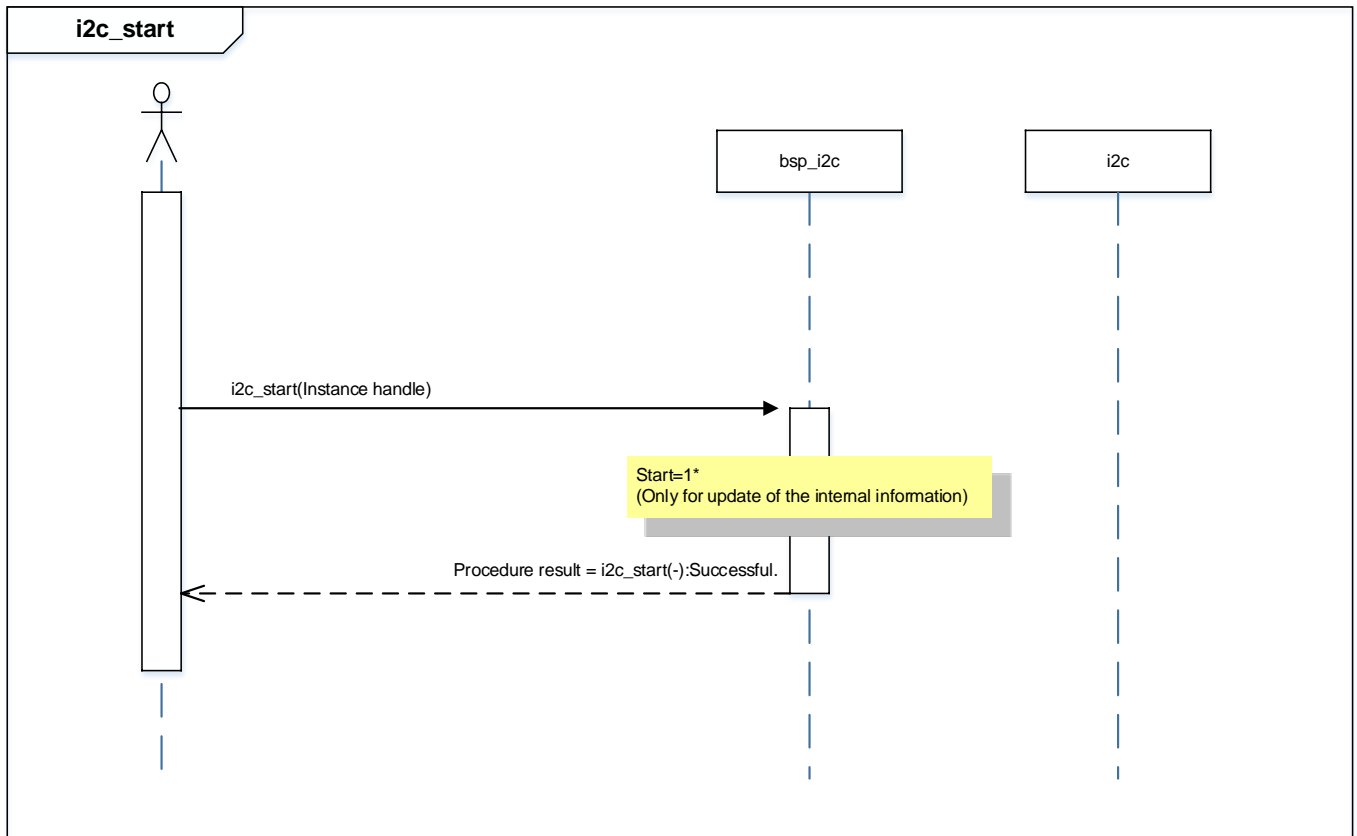
The basic operating flows of the sample program are shown in the following;

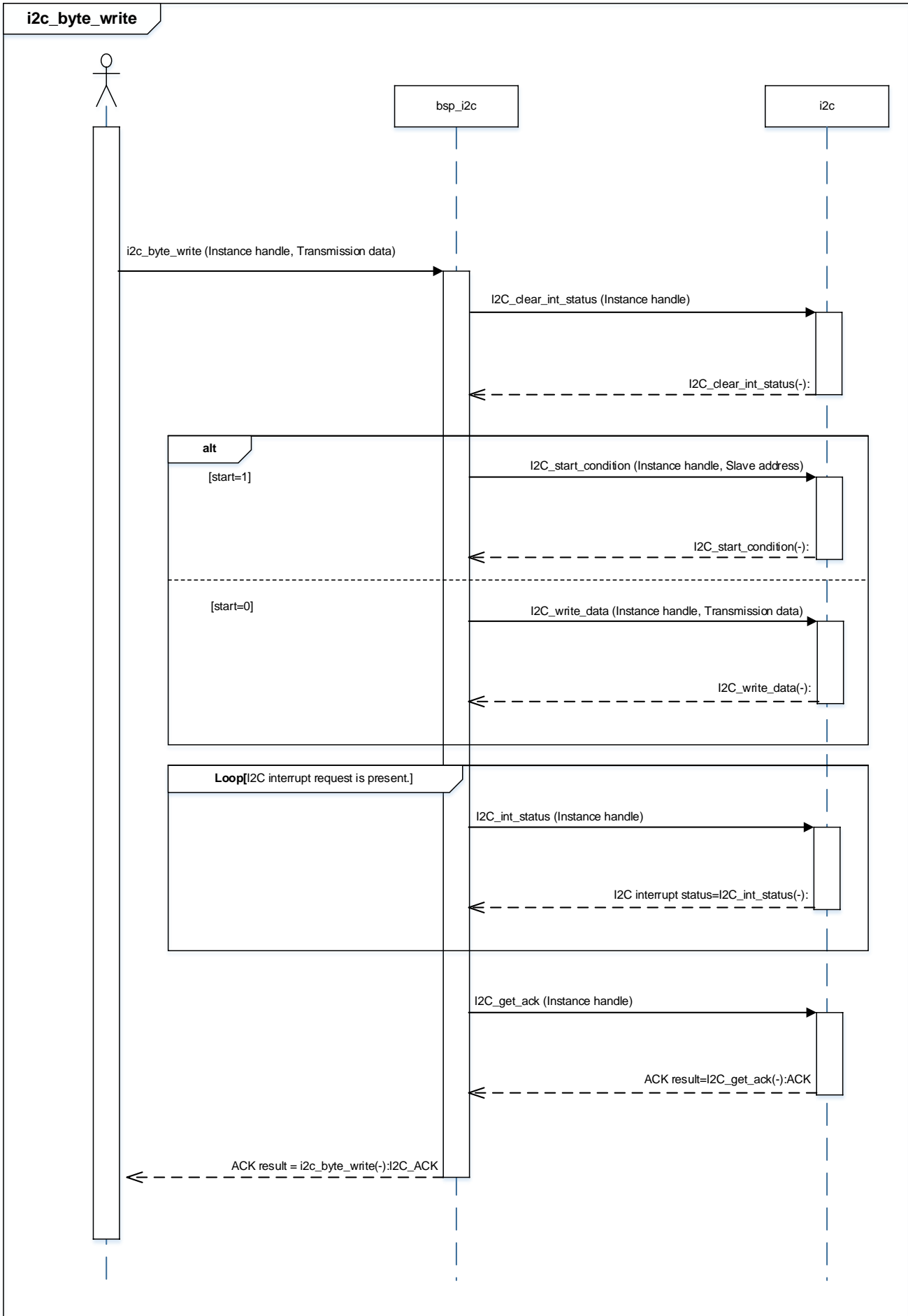


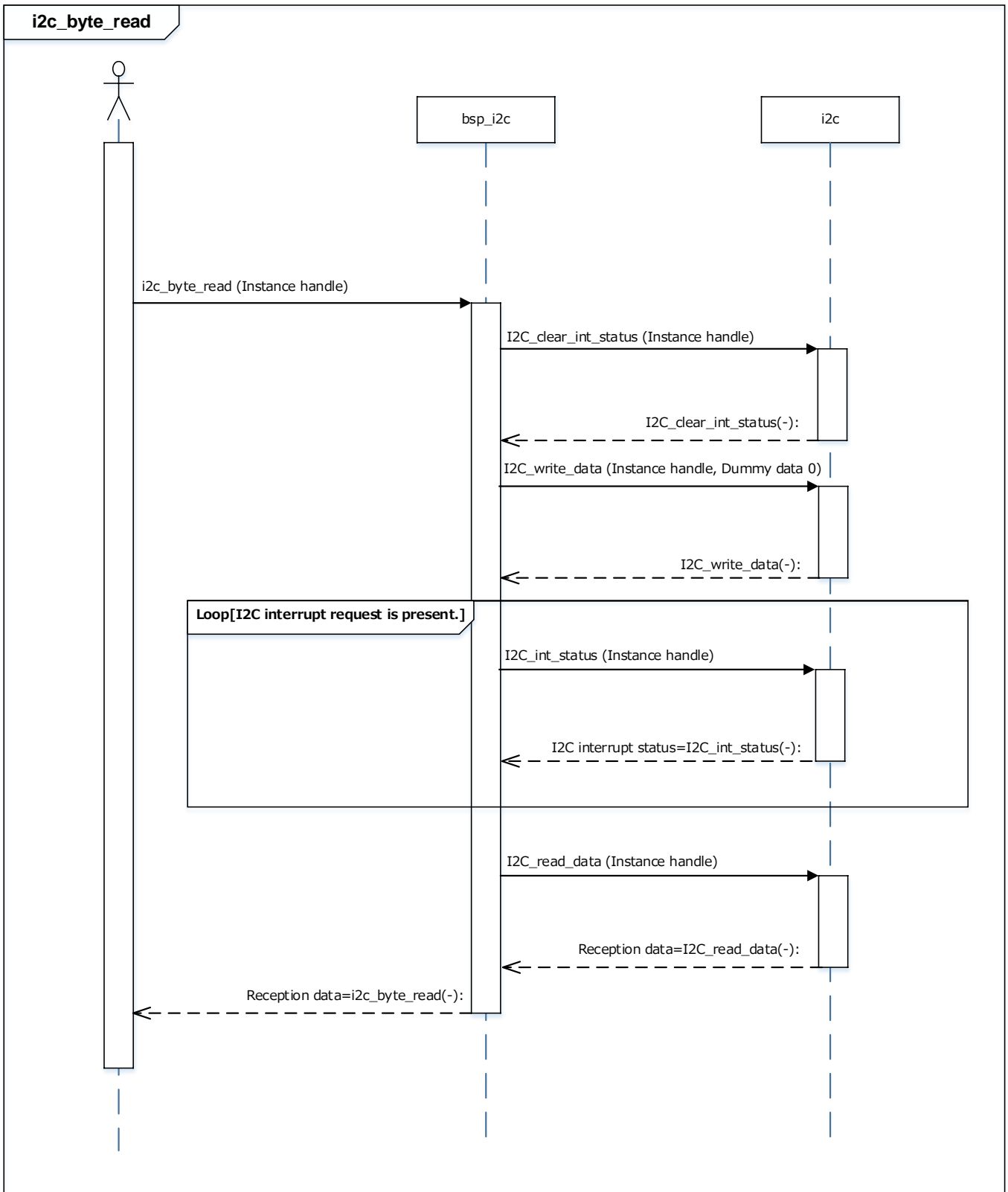


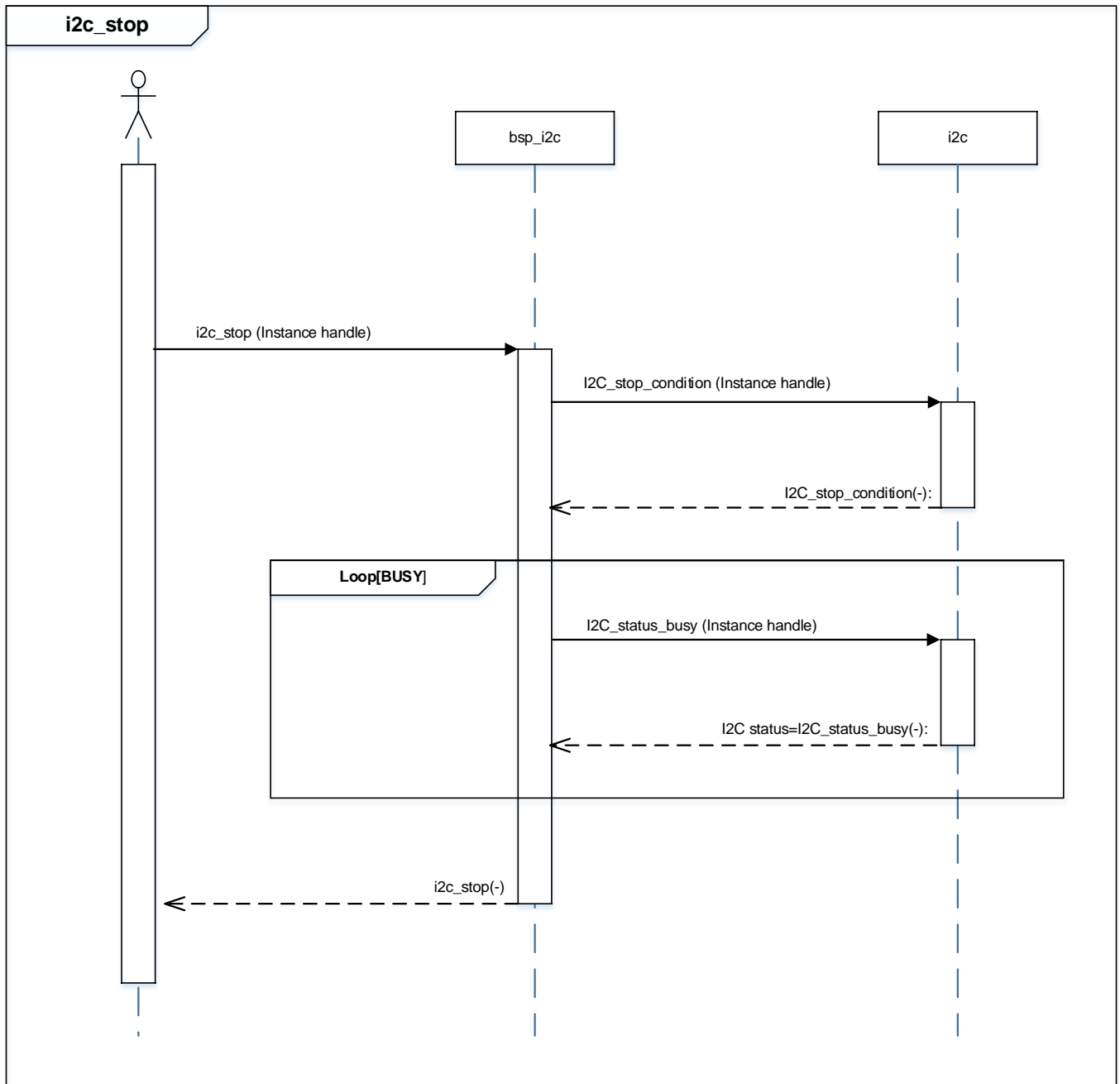












10. Precaution

When using the sample program with CPU other than TPM4G9F15, please check operation sufficiently.

11. Revision History

Rev	Date	Page	Description
1.0	2018-12-10	—	First release

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