M4G Group (1)
Application Note
Long Term Timer
(LTTMR-A)

Outlines

This application note is a reference material for developing products using Long term timer (LTTMR) function of M4G group (1).
This document helps the user check operation of the product and develop its program.

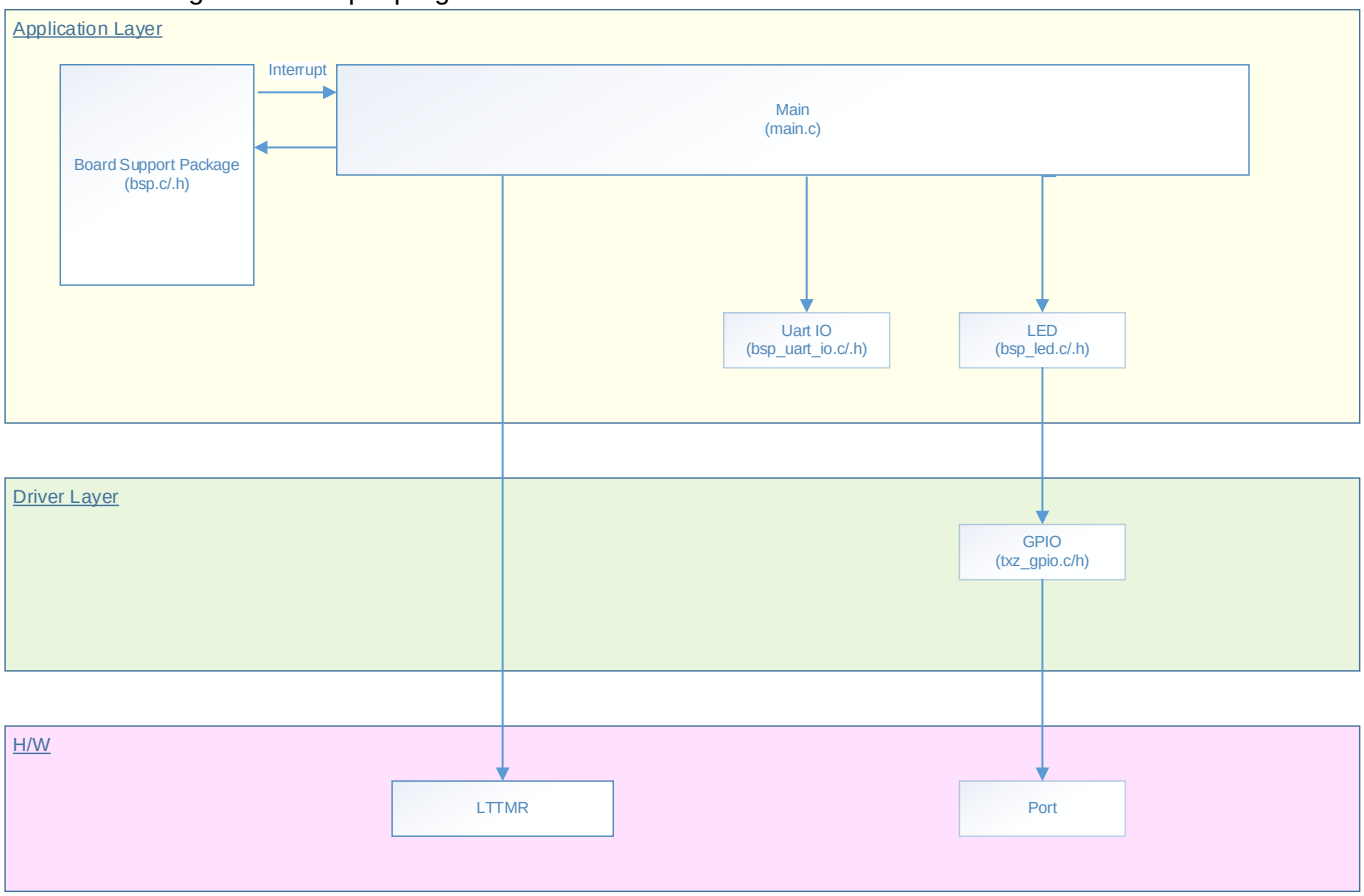
Target sample program: LTTMR32KHZ

Table of Contents

1. Preface

An interrupt of the Long term timer is used in this sample program.
A 16-kHz waveform is generated using an interrupt count value in the LTTMER, and it output from pin.

Structure diagram of Sample program



2. Reference Document

- Datasheet
  TMPM4G Group (1) datasheet Rev1.0 (Japanese edition)
- Reference manual
  Long Term Timer (LTTMR-A) Rev1.0 (Japanese edition)
  Asynchronous Serial Communication Circuit (UART-C) Rev3.0 (Japanese edition)
  Input/Output Ports (PORT-M4G (1)) Rev.1.0 (Japanese edition)
- Application note
  M4G Group (1) Application Note Startup (CMSIS System & Clock Configuration) Rev1.0
- Other reference document
  TMPM4G (1) Group Peripheral Driver User Manual (Doxygen)

3. Function to Use

IP	Channel	Port	Function/Operation mode
Long Term Timer	ch0	-	Interval timer
Asynchronous Serial Communication Circuit	ch0	PE2 (UT0RXD) PE3 (UT0TXDA)	UART mode
Input/Output Ports	-	PE4 (Output port)	Output

4. Target Device

The target devices of this application note are as follows;

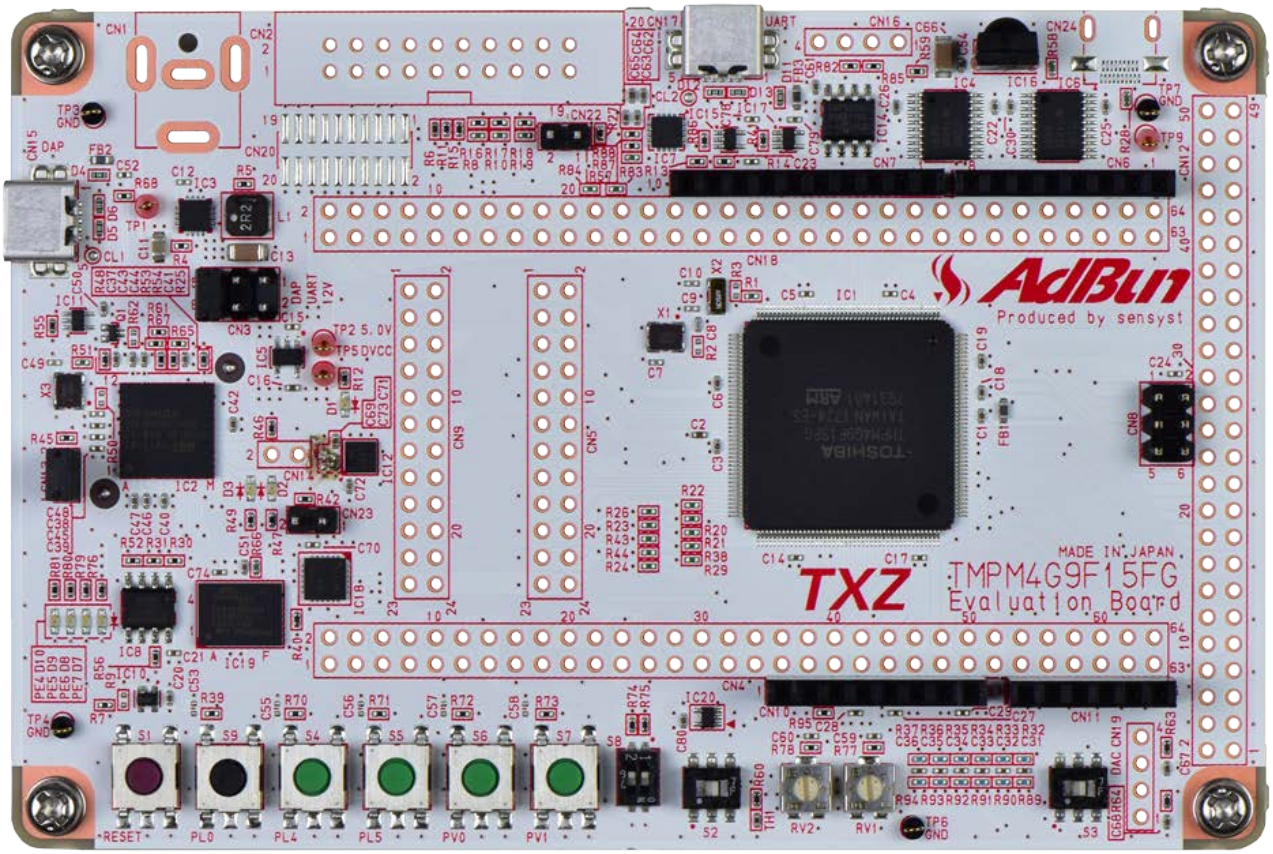
TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
	TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
	TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG

* This sample program operates on the evaluation board of TMPM4G9F15FG.
If other function than the TMPM4G9F15 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.
The BSP related file is dedicated to the evaluation board (TMPM4G9F15). If other function than the TMPM4G9F15 one is checked, the BSP related file should be changed properly.

5. Operation Confirmation Condition

Used microcontroller	TMPM4G9F15FG
Used board	TMPM4G9F15FG Evaluation Board by Sensyst
Unified development environment	IAR Embedded Workbench for ARM 8.11.2.13606
Unified development environment	µVision MDK Version 5.24.2.0
Terminal software	Tera Term V4.96
Sample program	V1000

Evaluation board (TMPM4G9F15FG Evaluation Board) Top view

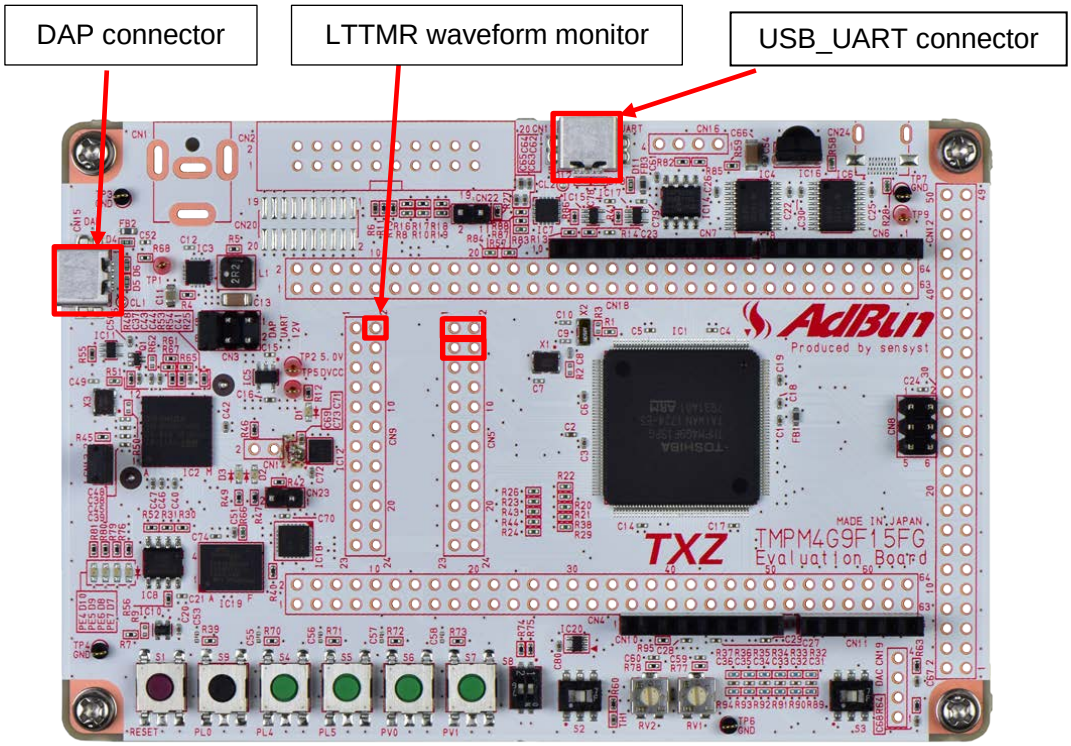


6. Evaluation Board Setting

The following pin connections should be done on the evaluation board.

CN5		
Board function	Through-hole No.	Through-hole No.
USB UART conversion	1: USB_UT_RX	2: PE2
USB UART conversion	3: USB_UT_TX	4: PE3

CN9 No2: PE4 LTTMR waveform monitor



7. Operation of Evaluation Board

PC and the USB_UART are connected for communication with the terminal software.
After the sample program starts up, ON/OFF setting of the LTTMR should be done on the terminal software.
For the details, refer to Section “Sample Program Main Operation”.

8. Outline of LTTMR Function

Long term timer (LTTMR) is a 16-bit timer which sets an interval time to start up CPU frequently.

Function category	Function	Description
Timer	Interval timer	- Clock source: Internal High speed oscillator 2 (f_{IHOSC2} = 10 MHz) - Settable time range: 0.1 µs to 6553.5 µs - Interrupt: LTTMR interrupt generation

9. Sample Program

The start and stop settings of the LTTMR can be done.
The LTTMR status (operating or stop) can be checked by monitoring the PE4.

9.1. Initialization

The following initialization is done after power is supplied.
The initialization of each clock setting and the setting of the watchdog timer are done.

9.2. Sample Program Main Operation

The initialization of BSP is executed.
The initialization of variables is executed.
The initialization of the application is executed.
The setting of internal high speed oscillator 2 is executed.

After the procedure above has been done, the LTTMR starts counting and waits for an input data to the terminal software.
After the following;
    Next Stop = (y/n)
“y” or “n” should be input.
When “y” is input, the LTTMR stops. And when “n” is input, the LTTMR is operating.

When the LTTMR interrupt count is odd, High level is output from the Port E4. And when it is even, Low level is output. An about 16-kHz waveform is output from the Port E4.

9.3. LTTMR Timer Interrupt Cycle

The LTTMR interrupt cycle is set by the long term timer data register in “main.c”.

```
#define LTTMR_VAL    ((uint16_t)304)
```

The setting value of the interrupt cycle is 304 when 32.787 kHz clock is used.
The timer interrupt cycle can be changed by modifying the value 304.

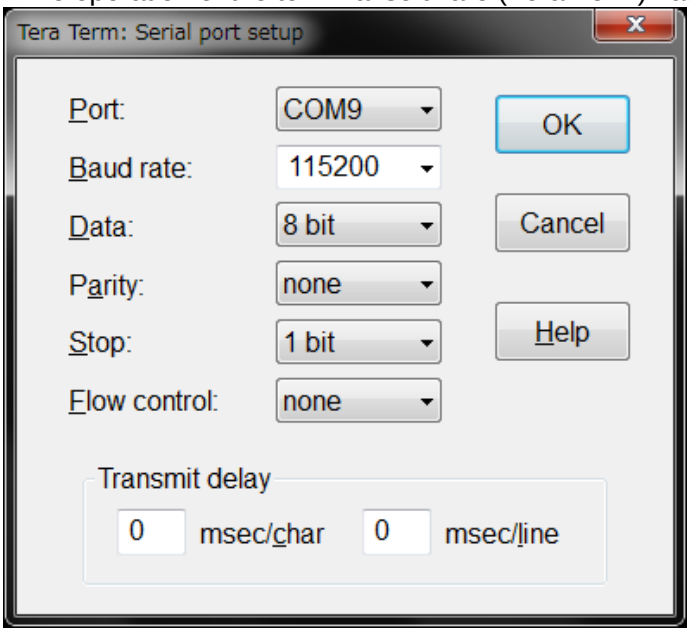
Interrupt cycle = $(1/f_{IHOSC2}\,(10\ MHz)) \times ((\textbf{\textit{[LTTxVALH]}} \times 256) + \textbf{\textit{[LTTxVALL]}} + 1)$
$= (1/f_{IHOSC2}\,(10\ MHz)) \times (LTTMR\_VAL + 1)$

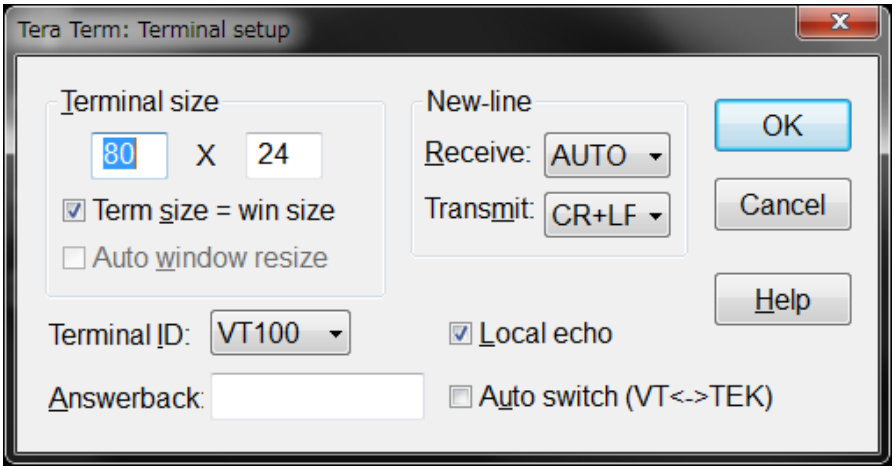
9.4. Output Example of Sample Program

When the sample program executes, the setting view of the LTTMR is displayed as shown in the following figure.

9.4.1. Setting Example of Terminal Software

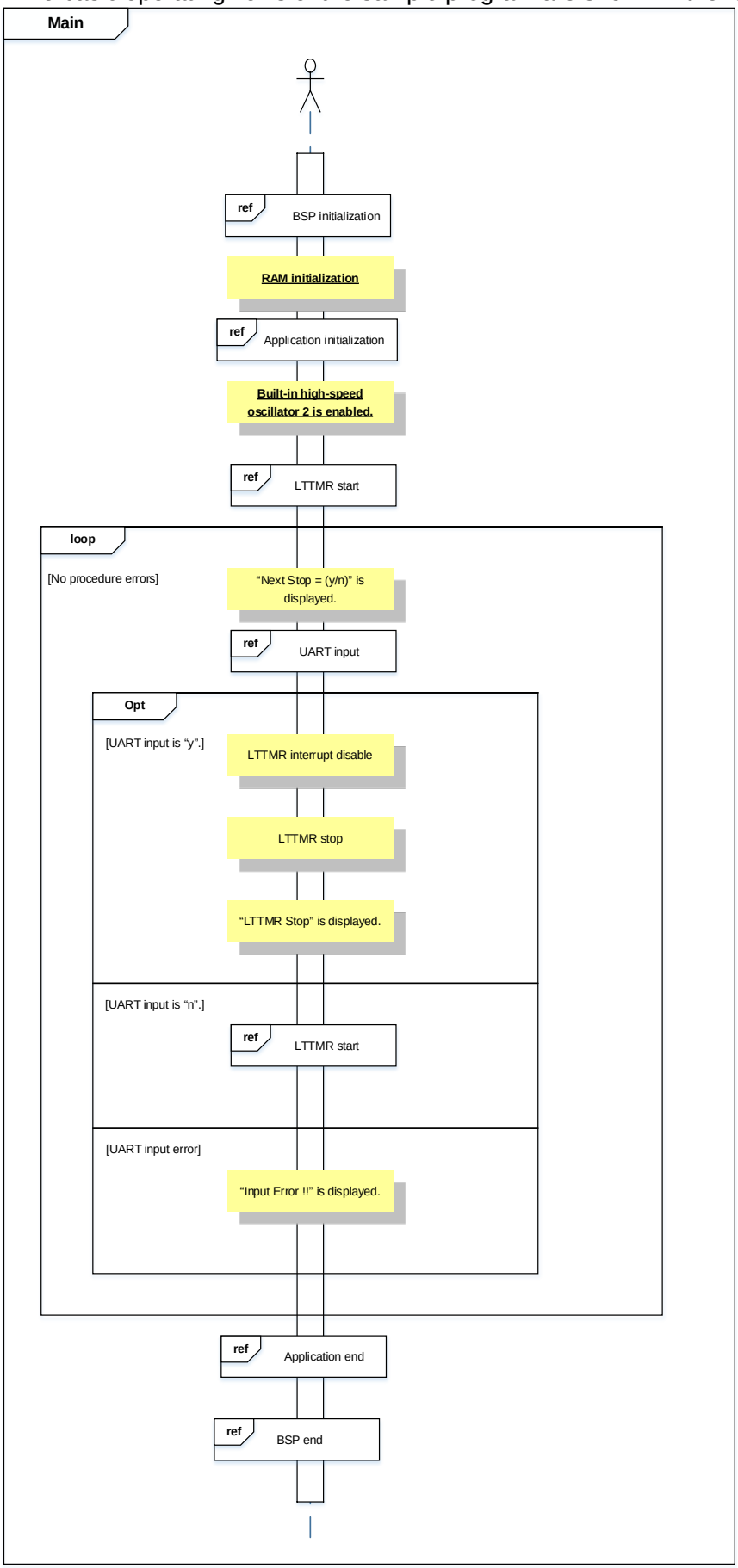
The operation of the terminal software (Tera Term) has been checked with the following settings.

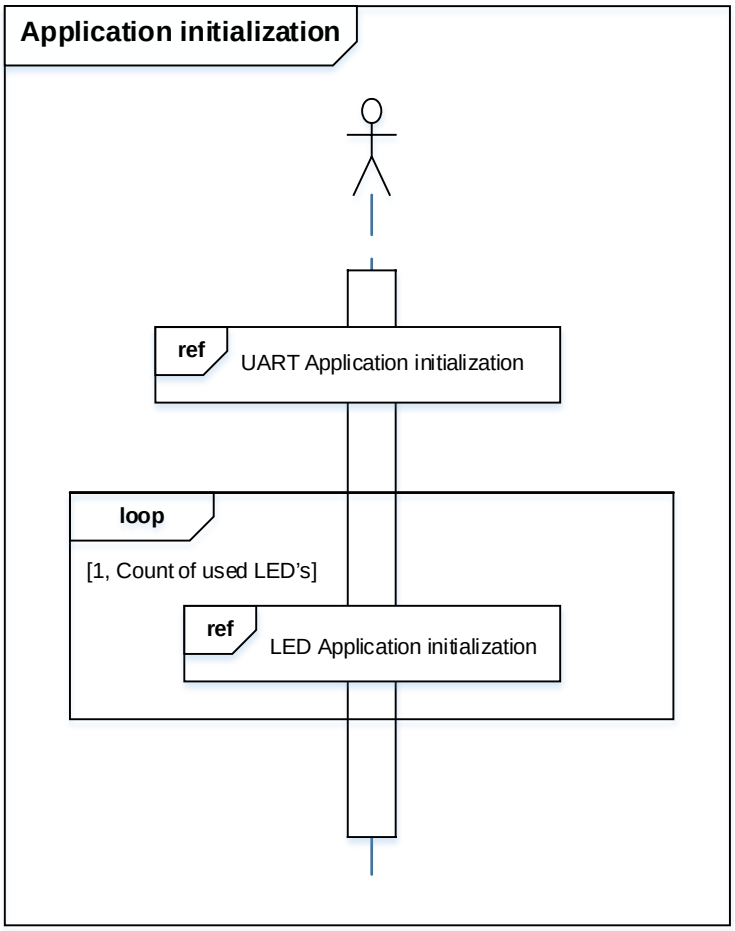


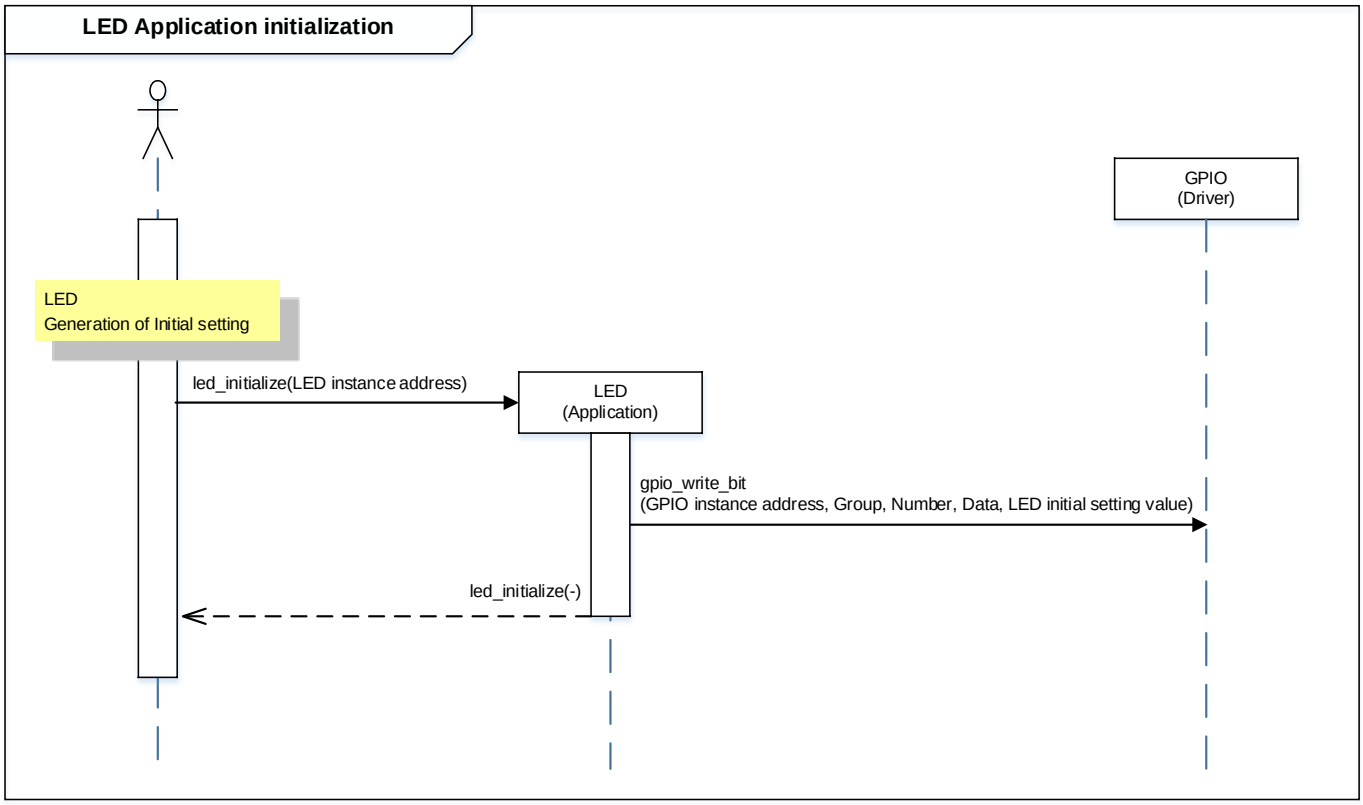


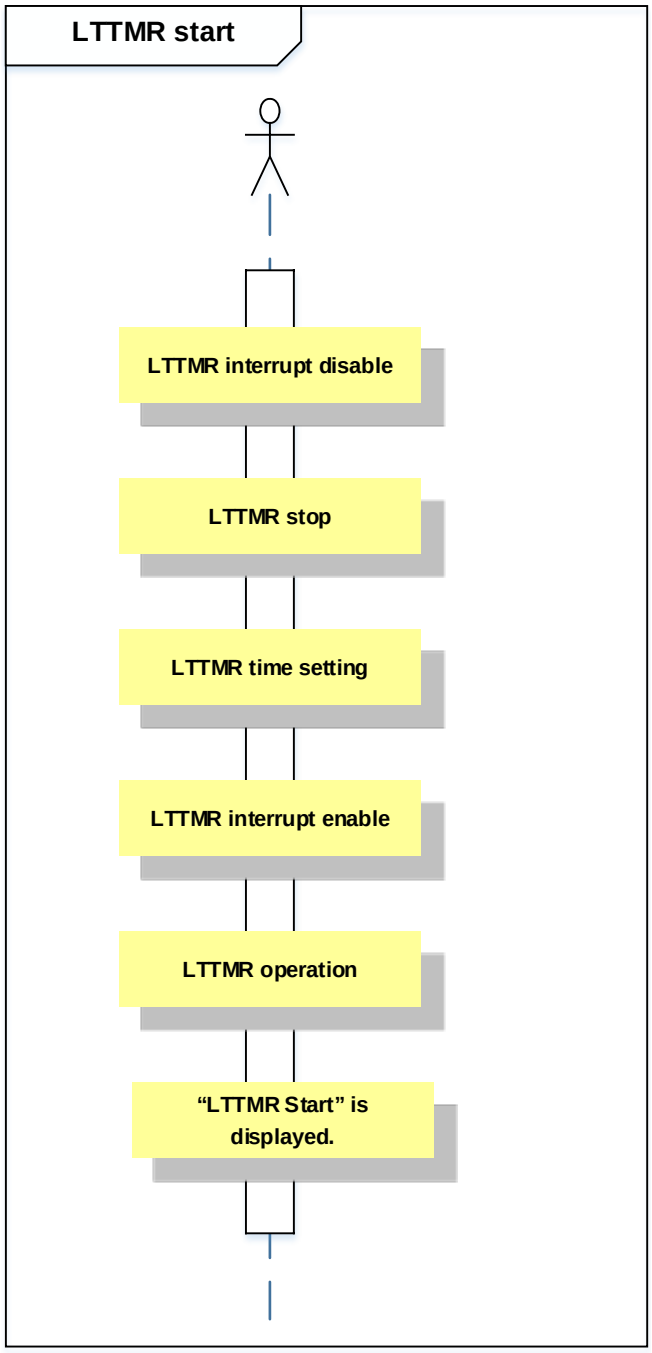
9.5. Operating Flow of Sample Program

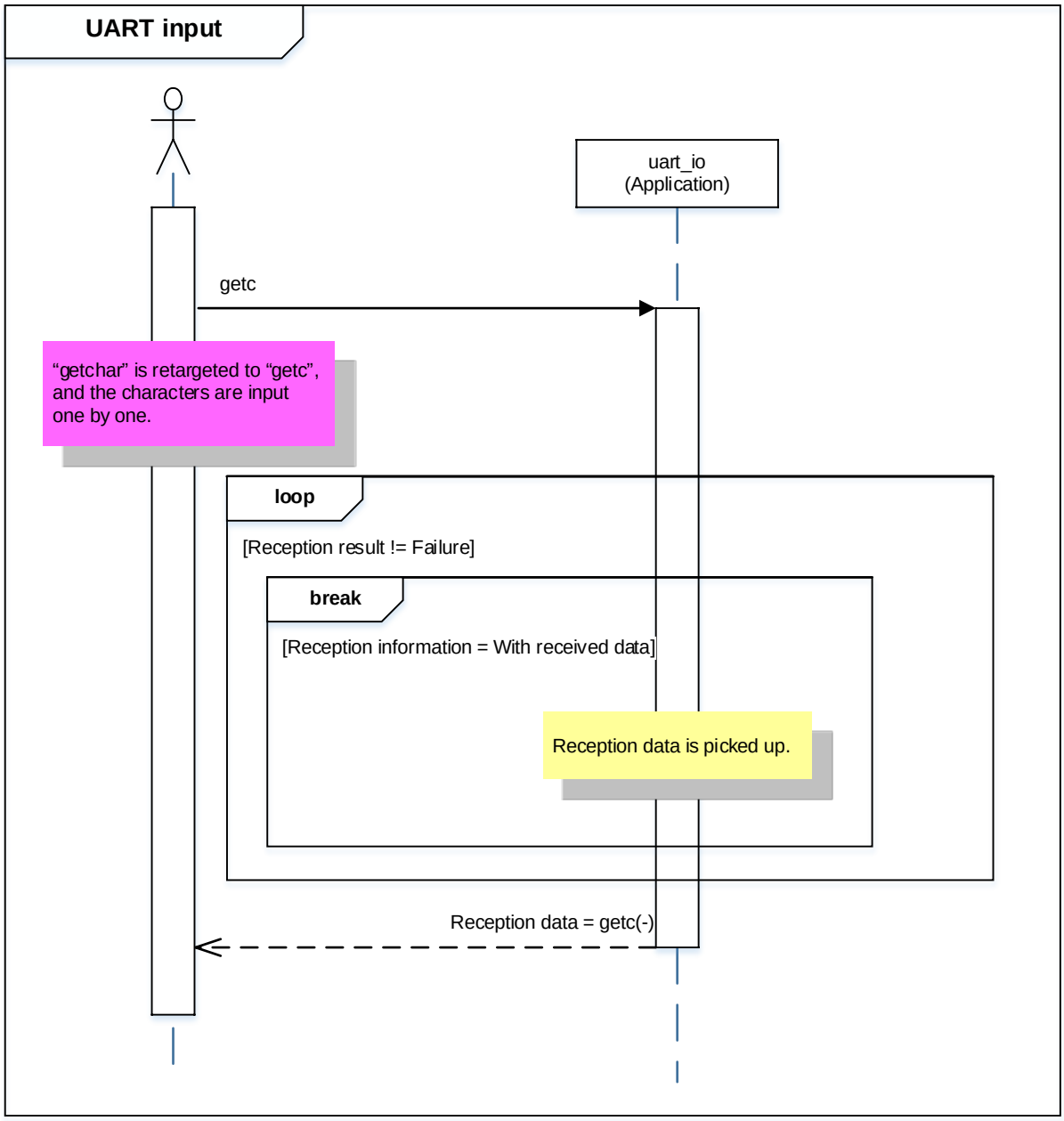
The basic operating flows of the sample program are shown in the following;

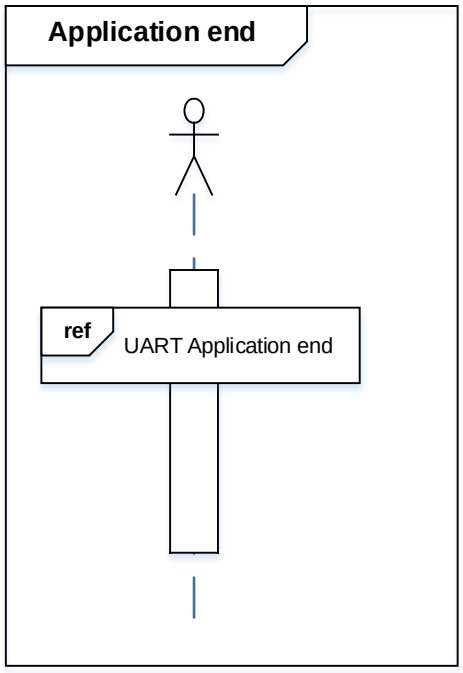


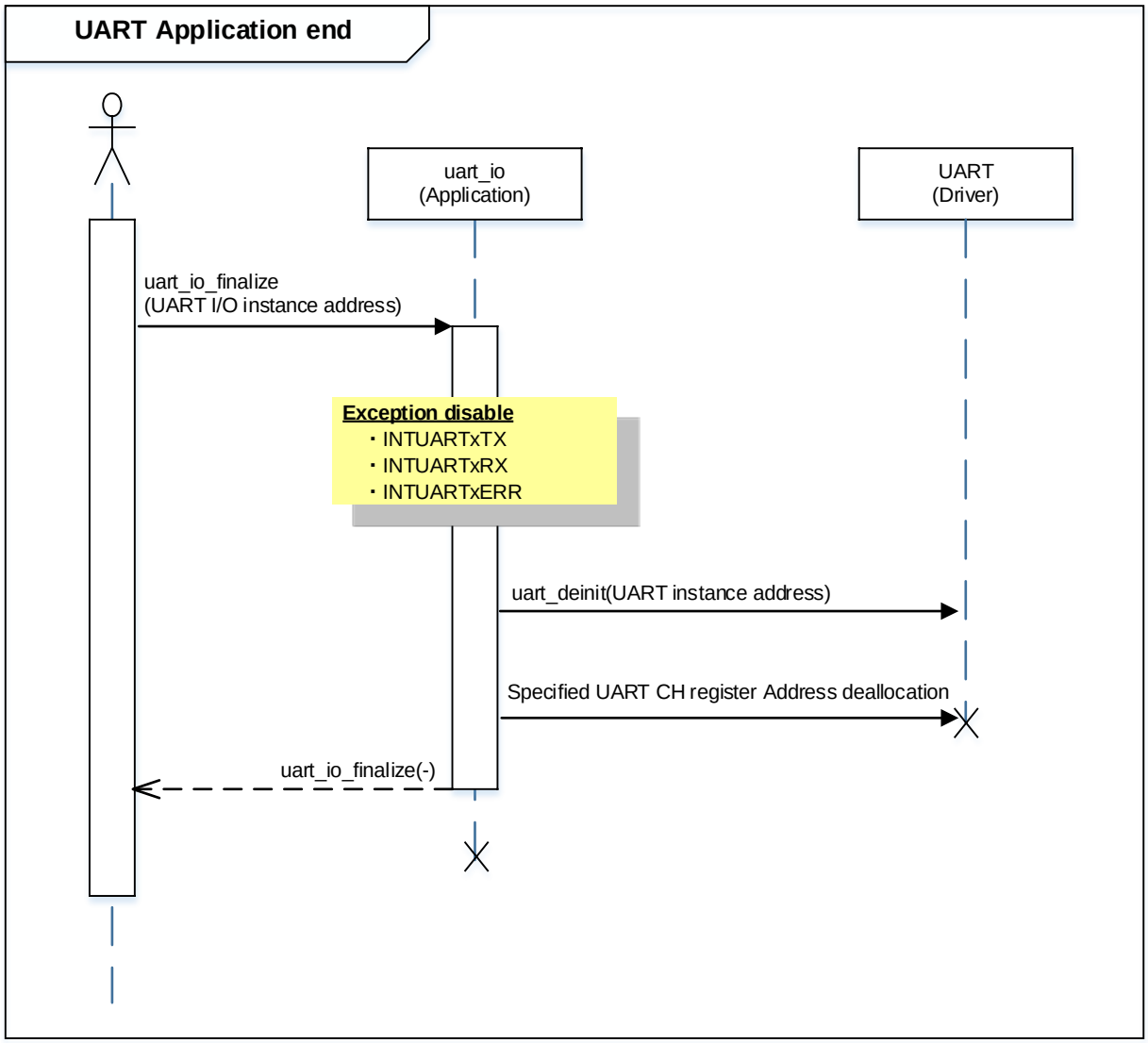

Application initialization
ref
UART Application initialization
loop
[1, Count of used LED's]
ref
LED Application initialization

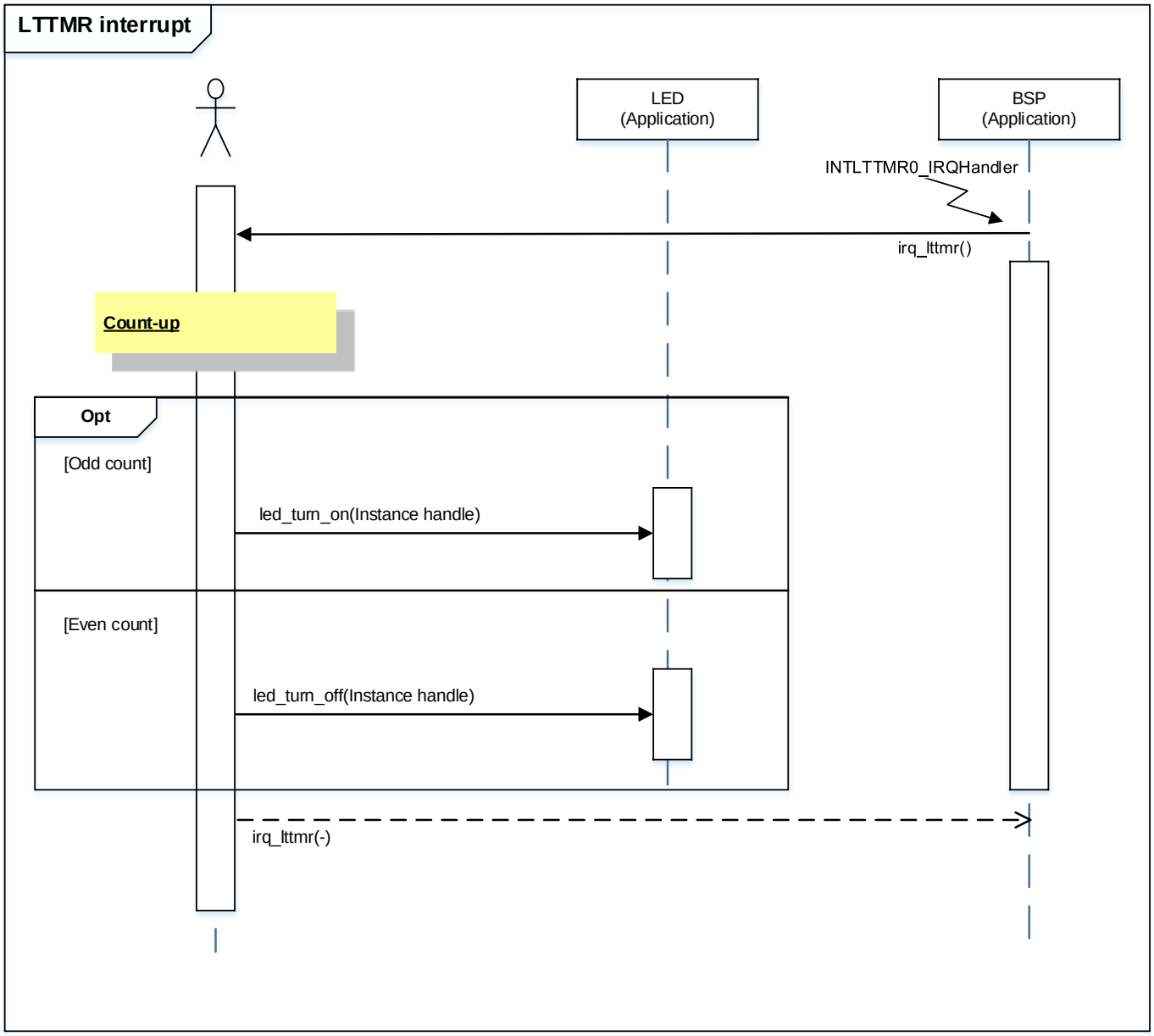

LED Application initialization
GPIO
(Driver)
LED
Generation of Initial setting
led_initialize(LED instance address)
LED
(Application)
gpio_write_bit
(GPIO instance address, Group, Number, Data, LED initial setting value)
led_initialize(-)


LTTMR start
LTTMR interrupt disable
LTTMR stop
LTTMR time setting
LTTMR interrupt enable
LTTMR operation
“LTTMR Start” is displayed.


UART input
uart_io
(Application)
getc
“getchar” is retargeted to “getc”, and the characters are input one by one.
loop
[Reception result != Failure]
break
[Reception information = With received data]
Reception data is picked up.
Reception data = getc(-)


Application end
ref
UART Application end


UART Application end
uart_io
(Application)
UART
(Driver)
uart_io_finalize
(UART I/O instance address)
Exception disable
・INTUARTxTX
・INTUARTxRX
・INTUARTxERR
uart_deinit(UART instance address)
Specified UART CH register Address deallocation
uart_io_finalize(-)


LTTMR interrupt
LED
(Application)
BSP
(Application)
INTLTTMR0_IRQHandler
irq_lttmr()
Count-up
Opt
[Odd count]
led_turn_on(Instance handle)
[Even count]
led_turn_off(Instance handle)
irq_lttmr(-)

10. Precaution

When using the sample program with CPU other than TMPM4G9F15, please check operation sufficiently.

11. Revision History

Rev	Date	Description
1.0	2018-12-11	First release

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