M4G Group (1)
Application Note
Startup
（CMSIS System & Clock Configuration)

Outlines

This application note describes the operation of the CMSIS System & Clock Configuration.
It is reference material when developing products using each function using M4G Group (1).
This document helps the user check operation of the product and develop its program.

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1. Preface

Perform the initial setting when operating the sample program.
Perform watchdog timer and clock setting.
In this sample program, the watchdog timer is disabled immediately after reset.
For the details, refer to “Clock Control and Operation Mode” and “Clock Selective Watchdog Timer” in the reference document.

2. Reference Document

- Datasheet
  TMPM4G Group (1) datasheet Rev1.0 (Japanese edition)
- Reference manual
  Clock Control and Operation Mode (CG-M4G (1)-C) Rev1.0 (Japanese edition)
  Clock Selective Watchdog Timer (SIWDT-A) Rev2.1 (Japanese edition)

3. Function to Use

IP	Channel	Port	Function/Operation mode
Watchdog Timer	-	-	Watchdog timer disable
Clock Control	-	-	External oscillator、 PLL oscillation

4. Target Device

The target devices of this application note are as follows;

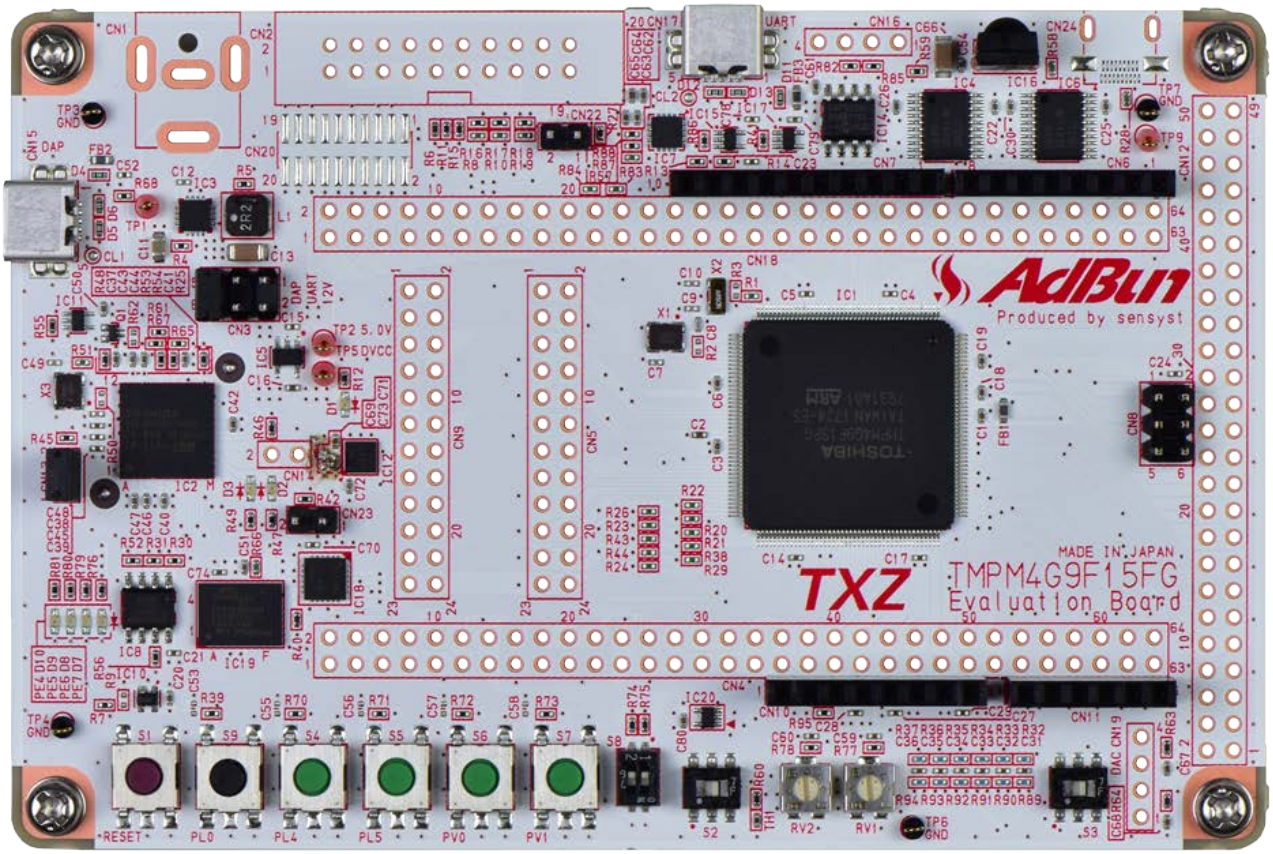
TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
	TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
	TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG

* This sample program operates on the evaluation board of TMPM4G9F15FG.
If other function than the TMPM4G9F15 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.
The BSP related file is dedicated to the evaluation board (TMPM4G9F15). If other function than the TMPM4G9F15 one is checked, the BSP related file should be changed properly.

5. Operation Confirmation Condition

Used microcontroller	TMPM4G9F15FG
Used board	TMPM4G9F15FG Evaluation Board by Sensyst
Unified development environment	IAR Embedded Workbench for ARM 8.11.2.13606
Unified development environment	µVision MDK Version 5.24.2.0
Sample program	V1000

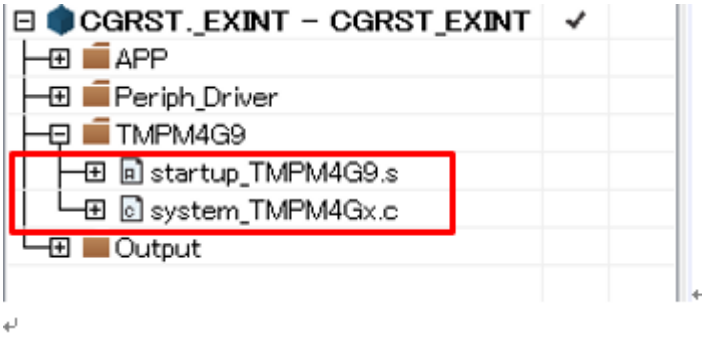
Evaluation board (TMPM4G9F15FG Evaluation Board) Top view



~~6.~~ Target files overview

The settings of the watchdog timer and the CG are done.
After the reset, execute the startup processing above and proceed to main processing.
This application note describes the following files;

- startup_TMPM4G9.s
- system_TMPM4Gx.c



6.1. Watchdog Timer Setting

The watchdog timer is set.
The sample program does not use this function (Stop state).
The control register is set to the disable code.

6.2. Clock Generator Setting

The external (f_{EHOSC}) and internal (f_{IHOSC1}) system clocks can be selected.
In addition, the division ratio of the clock for the output control and the multiplying ratio of the PLL clock can be changed.

7. Startup and system Files

The sample program is prepared for the TMPM4G9 operation.

7.1. Operation

This sample program executes the settings of each clock, the watchdog timer, the system core clock, and the PLL.
After the settings are done, the main procedure of an application program executes.

7.2. Watchdog Timer Setting

In the sample program, the watchdog timer has been set to “disable”.
SIWD_SETUP should be changed as follows to enable it.
The change is done by a macro change in “system_TMPM4Gx.c”.
SIWD_SETUP (1U) should be changed to “0U”, then the watchdog timer is set to enable.
When this sample program is used in the Enable setting, the watchdog timer starts with the initial setting value and the reset is asserted after the watchdog operation is detected.

7.3. Clock Setting

The external high speed oscillation clock or the internal high speed oscillation clock can be selected.
In the sample program, the external high speed oscillation clock is selected initially.
CLOCK_SETUP (1U)
If the (1U) is changed to (0U), the internal high speed oscillation clock is selected.

7.4. PLL Setting

The f_{PLL} clock (160 MHz) is generated by the clock multiplying circuit which multiplies properly the high-speed oscillator clock fosc (8 MHz to 20 MHz).
The sample program operates with an external 10-MHz clock.

The sample program uses the f_{PLL} setting.
The input frequency supports 8, 10, 12, 16, and 20 MHz frequencies.
The operation frequency after multiplying is as follows;

Internal frequency * (Multiplying value/Division value) = Operation frequency
8 MHz 8.00 MHz * (40.0000/2) = 160 MHz
10 MHz 10.00 MHz * (32.0000/2) = 160 MHz
12 MHz 12.00 MHz * (26.6250/2) = 159.75 MHz
16 MHz 16.00 MHz * (20.0000/2) = 160 MHz
20 MHz 20.00 MHz * (16.0000/2) = 160 MHz

In the sample program, the PLL setting value is 10-MHz selection and the multiplying rate is 16.

```
#define PLL0SEL_Ready          CG_10M_MUL_16_FPLL
```

When PLL0SEL_Ready is set to the value in system_TMPM4Gx.c, the PLL setting value is updated.

CG_8M_MUL_20_FPLL	8 MHz selection and 20 multiplying
CG_10M_MUL_16_FPLL	10 MHz selection and 16 multiplying
CG_12M_MUL_13.3125_FPLL	12 MHz selection and 13.3125 multiplying
CG_16M_MUL_10_FPLL	16 MHz selection and 10 multiplying
CG_20M_MUL_8_FPLL	20 MHz selection and 8 multiplying

7.5. Clock Frequency Setting

The system clock frequency can be divided by the clock gear in ***[CGSYSCR]***.

```
#define SYSCR_GEAR_Val          (0x00000000UL)
```

The clock selection and the system clock gear selection can be done using the setting value above.
The sample program operates with the fc setting.

The clock divided by SYSCR is used as the core clock.
The system core clock (fsys) is used for the sample program of each IP (CGRST, I2C and others).

8. Precaution

When using the sample program with CPU other than TMPM4G9F15, please check operation sufficiently.

9. Revision History

Rev	Date	Description
1.0	2018-12-14	First release

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