M4G Group (1)
Application Note
Serial Peripheral Interface
(TSPI-C)

Outlines

This application note is a reference material for developing products using Serial peripheral interface (TSPI) function of M4G group (1). This document helps the user check operation of the product and develop its program.

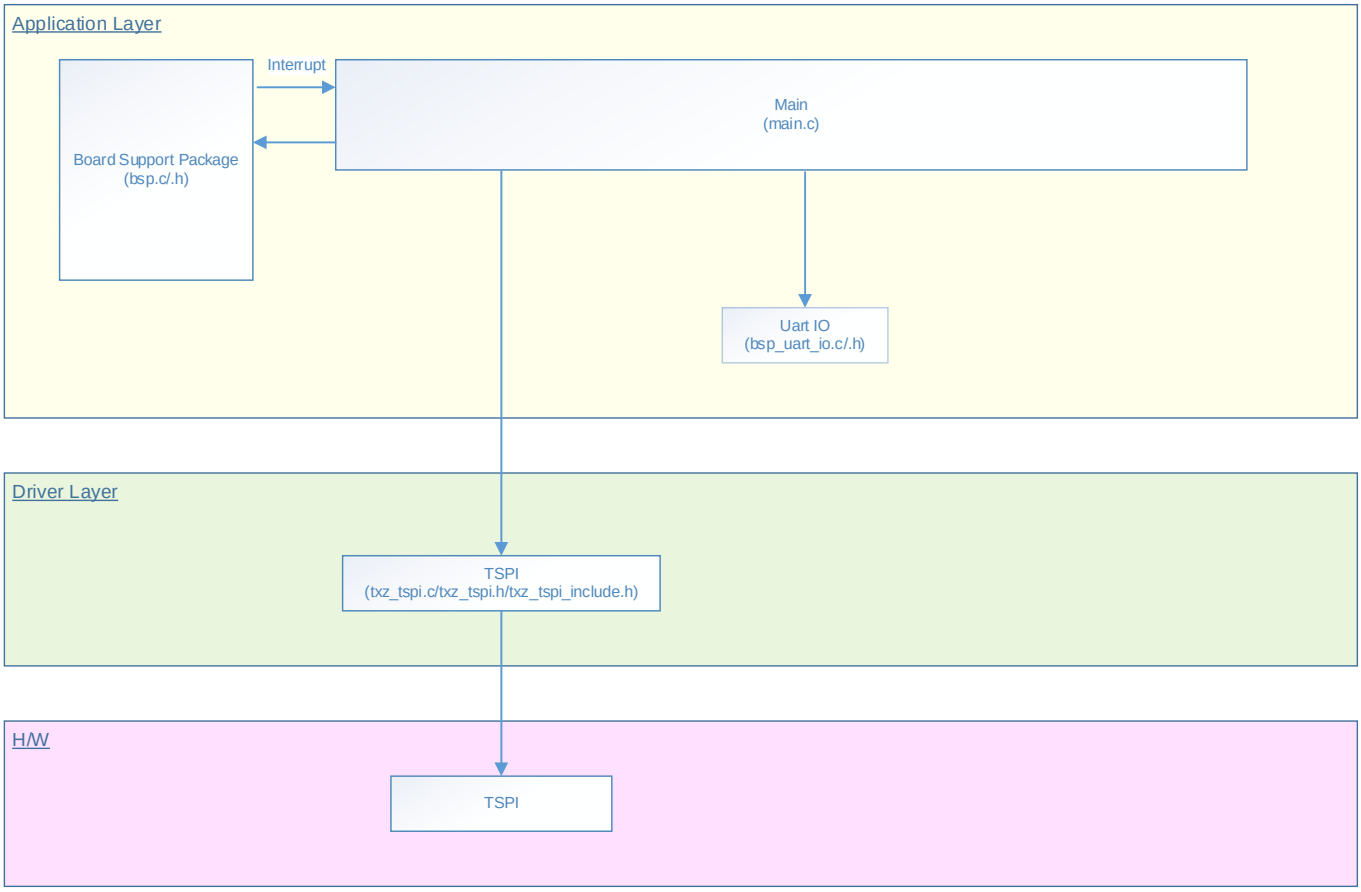
Target sample program: TSPI_ChToCh_rx_int

Table of Contents

1. Preface

This sample program should be used to check the operation of the Serial peripheral interface function. The “write” command transmits data. And the “read” command reads the reception data and outputs to the terminal software.

Structure diagram of Sample program



2. Reference Document

- Datasheet
  TMPM4G Group (1) datasheet Rev1.0 (Japanese edition)
- Reference manual
  Serial Communication (TSPI) Rev1.0 (Japanese edition)
  Asynchronous Serial Communication Circuit (UART-C) Rev3.0 (Japanese edition)
- Application note
  M4G Group (1) Application Note Startup (CMSIS System & Clock Configuration) Rev1.0
- Other reference document
  TMPM4G (1) Group Peripheral Driver User Manual (Doxygen)

3. Function to Use

IP	Channel	Port	Function/Operation mode
Serial Peripheral Interface	ch2	PA4 (TSPI2TXD) PA6 (TSPI2SCK) PA7 (TSPI2CS0)	SPI mode: Master
	ch4	PD0 (TSPI4CSIN) PD1 (TSPI4SCK) PD2 (TSPI4RXD)	SPI mode: Slave
Asynchronous Serial Communication Circuit	ch0	PE2 (UT0RXD) PE3 (UT0TXDA)	UART mode

4. Target Device

The target devices of this application note are as follows;

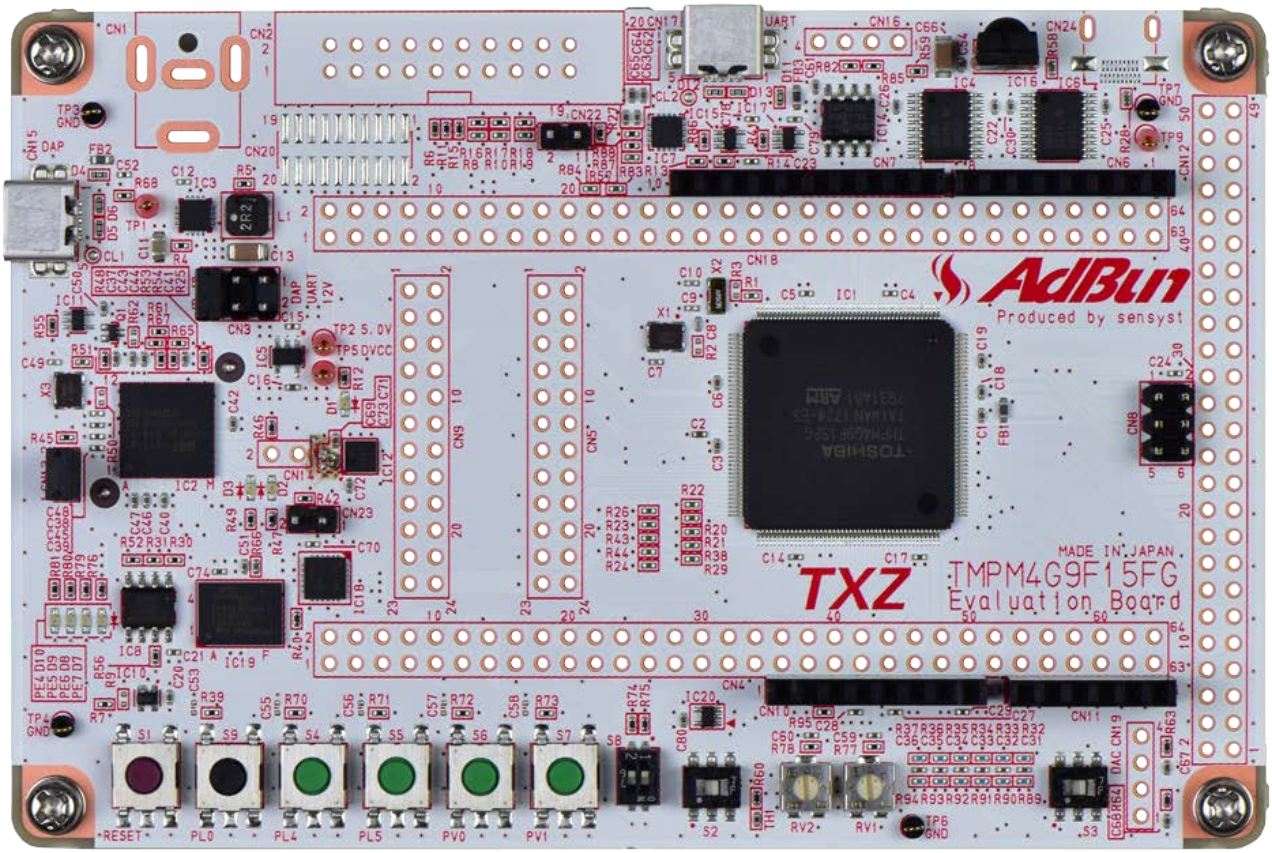
TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
	TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
	TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG

* This sample program operates on the evaluation board of TMPM4G9F15FG.
If other function than the TMPM4G9F15 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.
The BSP related file is dedicated to the evaluation board (TMPM4G9F15). If other function than the TMPM4G9F15 one is checked, the BSP related file should be changed properly.

5. Operation Confirmation Condition

Used microcontroller	TMPM4G9F15FG
Used board	TMPM4G9F15FG Evaluation Board by Sensyst
Unified development environment	IAR Embedded Workbench for ARM 8.11.2.13606
Unified development environment	µVision MDK Version 5.24.2.0
Terminal software	Tera Term V4.96
Sample program	V1000

Evaluation board (TMPM4G9F15FG Evaluation Board) Top view

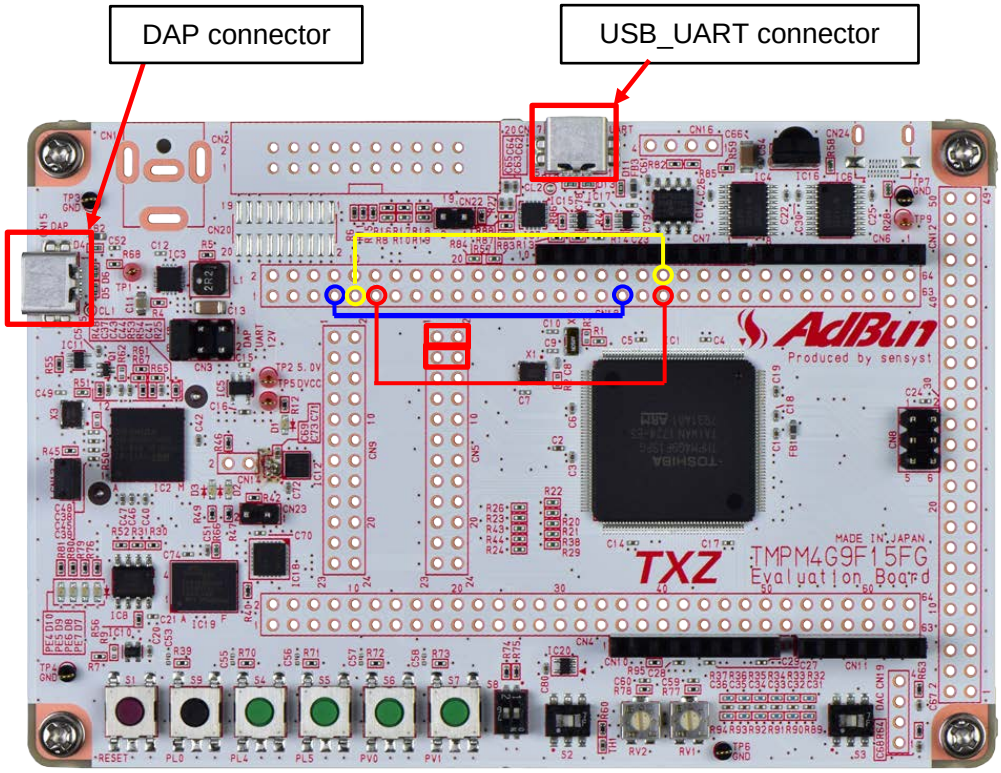


6. Evaluation Board Setting

The following pin connections should be done on the evaluation board.

CN5		
Board function	Through-hole No.	Through-hole No.
USB UART conversion	1: USB_UT_RX	2: PE2
USB UART conversion	3: USB_UT_TX	4: PE3

CN18		
Board function	Through-hole No.	Through-hole No.
SPI communication (Inter-channel)	7: PD2	35: PA4
SPI communication (Inter-channel)	9: PD1	40: PA6
SPI communication (Inter-channel)	11: PD0	39: PA7



7. Operation of Evaluation Board

PC and the USB_UART are connected for communication with the terminal software.
The sample program should be started up.
The sample program waits for data input to the terminal software.
The “write” command should be input to the terminal software. Then the “read” command should be input.
The data received by the “write” command is read and the character string “TOSHIBA” is output to the terminal software.

8. Outline of TSPI Function

TSPI (serial peripheral interface) has four operation mode as SPI/SIO mode, and the clock master/ clock slave mode. One channel/unit which is built-in TSPIxTXD, TSPIxRXD, TSPIxSCK, TSPIxCS0, TSPIxCS1, TSPIxCS2, TSPIxCS3, and TSPIxCSIN can be transmit and receive circuit. Functions are as below.

Table 8.1 Functional outline (SPI mode, master)

Function classification		Function	A Functional Description or the range
SPI mode (Master)	Transmission Speed Control	Prescaler dividing selection	The clock inputted from the prescaler can be divided 1/1,1/2,1/4..up to 1/512.
		Baud rate generator	The input clock to baud rate generator. dividing 1/N x 1/2 (N= 1 to 16)
	Data Format	Data length	The data length can be setup in a 1-bit unit. 8 to 32bits (with no parity) 7 to 31bits (with parity)
		Parity	Selection of with parity/without parity is possible. Selection of even parity/odd parity is possible.
		The direction of data transfer	Selection of the LSB first/ MSB first is possible.
	Transmission and Reception Control	FIFO number of section	Transmission: 8 steps (16bits), 4 steps (32bits) Reception: 8 steps (16bits), 4 steps (32bits)
		Communication Operation mode	Full duplexes (transmission and reception), transmission, reception
		Transfer mode	Single transfer (one burst transfer) Burst transfer (2 to 255 times transfer) Continuously transfer (No limit of transfer times specification)
		Data sampling timing	Data is sampled with 1st edge. Data is sampled with 2nd edge.
		CS control	Selection of TSPIxCS0/1/2/3 is possible. Polarity: Selection of positive logic/ negative logic is possible.
	Ganged Control	Interruption	Transmit interrupt (Transmit completion interrupt, Transmit FIFO interrupt) Receive interrupt (Receive completion interrupt, Receive FIFO interrupt) Error Interrupt (Vertical parity error interrupt, Trigger error interrupt)
		Various status detection	TSPI modify status, Transmit shift operation, Transmit completion, Transmit FIFO fill level/ empty detection, Receive operation, Receive completion, Receive FIFO fill level /full detection
		DMA request	Transmit: Single DMA request, burst DMA request Receive: Single DMA transfer, burst DMA request
		Trigger communication control	Starting communication by trigger. Refer to the "Product Information" on a reference manual for a trigger source.
	Special Control	Output level of TSPIxTXD during an idle term	High, Low, a last bit data hold, Hi-z
		Polarity of TSPIxSCK during an idle term	It is Low to during idle term. It is High to during idle term.
		Interval time between frames at the time of burst transfer.	0 x TSPIxSCK cycle to 15 x TSPIxSCK cycles
		Idle time at the time of continuously transfer.	Period of changing TSPIxCS0/1/2/3 pin to asserted, deasserted, asserted. 1 x TSPIxSCK cycle to 15 x TSPIxSCK cycles
		TSPIxSCK delay of deassert	Time of delay between from TSPIxCS0/1/2/3 is asserted to TSPIxSCK is started. 1 x TSPIxSCK cycle to 16 x TSPIxSCK cycles
		TSPIxCS0/1/2/3 deassertion delay	Time until TSPIxCS0/1/2/3 pin is deasserted from last data 1 x TSPIxSCK cycle to 16 x TSPIxSCK cycle
		Software reset	Reset by software is possible.

Table 8.2 Outline of function (SPI mode and Slave)

Function classification		Function	A Functional Description or the range
SPI mode (Slave)	Data Format	Data length	The data length can be setup in a 1-bit unit. 8 to 32bits (with no parity) 7 to 31bits (with parity)
		Parity	Selection of with parity/without parity is possible. Selection of even parity/odd parity is possible.
		The direction of data transfer	Selection of the LSB first/ MSB first is possible.
	Transmission and Reception Control	FIFO number of section	Transmission: 8 steps (16bits), 4 steps (32bits) Reception: 8 steps (16bits), 4 steps (32bits)
		Communication Operation mode	Full duplexes (transmission and reception), transmission, reception
		Transfer mode	Single transfer (one burst transfer) Burst transfer (2 to 255 times transfer) Continuously transfer (No limit of transfer times specification)
		Data sampling timing	Data is sampled with 2nd edge.
		CS control	TSPIxCSIN Polarity: Selection of positive logic/ negative logic is possible.
	Ganged Control	Interruption	Transmit interrupt (Transmit completion interrupt, Transmit FIFO interrupt) Receive interrupt (Receive completion interrupt, Receive FIFO interrupt) Error Interrupt (Vertical parity error interrupt, Overrun interrupt, Underrun interrupt)
		Various status detection	TSPI modify status, Transmit shift operation, Transmit completion, Transmit FIFO fill level/ empty detection, Receive operation, Receive completion, Receive FIFO fill level /full detection
		DMA request	Transmit: Single DMA request, burst DMA request Receive: Single DMA transfer, burst DMA request
	Special Control	Output level of TSPIxTXD during an idle term	High, Low, a last bit data hold, Hi-z
		Output level of TSPIxTXD when underrun error occurred	High, Low
		Software reset	Reset by software is possible.

Table 8.3 Outline of function (SIO mode and Master)

Function classification		Function	A Functional Description or the range
SIO mode (Master)	Transmission speed Control	Prescaler dividing selection	The clock inputted from the prescaler can be divided 1/1,1/2,1/4..up to 1/512.
		Baud rate generator	The input clock to baud rate generator. dividing 1/N x 1/2 (N= 1 to 16)
	Data Format	Data length	The data length can be setup in a 1-bit unit. 8 to 32bits (with no parity) 7 to 31bits (with parity)
		Parity	Selection of with parity/without parity is possible. Selection of even parity/odd parity is possible.
		The direction of data transfer	Selection of the LSB first/ MSB first is possible.
	Transmission and Reception Control	FIFO number of section	Transmission: 8 steps (16bits), 4 steps (32bits) Reception: 8 steps (16bits), 4 steps (32bits)
		Communication Operation mode	Full duplexes (transmission and reception), transmission, reception
		Transfer mode	Single transfer (one burst transfer) Burst transfer (2 to 255 times transfer) Continuously transfer (No limit of transfer times specification)
		Data sampling timing	Data is sampled with 1st edge. Data is sampled with 2nd edge.
	Ganged Control	Interruption	Transmit interrupt (Transmit completion interrupt, Transmit FIFO interrupt) Receive interrupt (Receive completion interrupt, Receive FIFO interrupt) Error Interrupt (Vertical parity error interrupt, Trigger error interrupt)
		Various status detection	TSPI modify status, Transmit shift operation, Transmit completion, Transmit FIFO fill level/ empty detection, Receive operation, Receive completion, Receive FIFO fill level /full detection
		DMA request	Transmit: Single DMA request, burst DMA request Receive: Single DMA transfer, burst DMA request
		Trigger communication control	Starting communication by trigger. Refer to the "Product Information" on a reference manual for a trigger source.
	Special Control	Output level of TSPIxTXD during an idle term	High, Low, a last bit data hold, Hi-z
		Polarity of TSPIxSCK during an idle term	It is Low to during idle term. It is High to during idle term.
		Interval time between frames at the time of burst transfer.	0 x TSPIxSCK cycle to 15 x TSPIxSCK cycles
		Idle time at the time of continuously transfer.	Period of changing TSPIxCS0/1/2/3 pin to asserted, deasserted, asserted.. 1 x TSPIxSCK cycle to 15 x TSPIxSCK cycles
		Software reset	Reset by software is possible.

Table 8.4 Outline of function (SIO mode and Slave)

Function classification		Function	A Functional Description or the range
SIO mode (Slave)	Data Format	Data length	The data length can be setup in a 1-bit unit. 8 to 32bits (with no parity) 7 to 31bits (with parity)
		Parity	Selection of with parity/without parity is possible. Selection of even parity/odd parity is possible.
		The direction of data transfer	Selection of the LSB first/ MSB first is possible.
	Transmission and Reception Control	FIFO number of section	Transmission: 8 steps (16bits), 4 steps (32bits) Reception: 8 steps (16bits), 4 steps (32bits)
		Communication Operation mode	Full duplexes (transmission and reception), transmission, reception
		Transfer mode	Single transfer (one burst transfer) Burst transfer (2 to 255 times transfer) Continuously transfer (No limit of transfer times specification)
		Data sampling timing	Data is sampled with 2nd edge.
	Ganged Control	Interruption	Transmit interrupt (Transmit completion interrupt, Transmit FIFO interrupt) Receive interrupt (Receive completion interrupt, Receive FIFO interrupt) Error Interrupt (Vertical parity error interrupt, Overrun interrupt, Underrun interrupt)
		Various status detection	TSPI modify status, Transmit shift operation, Transmit completion, Transmit FIFO fill level/ empty detection, Receive operation, Receive completion, Receive FIFO fill level /full detection
		DMA request	Transmit: Single DMA request, burst DMA request Receive: Single DMA transfer, burst DMA request
	Special Control	Final bit hold time of a TSPIxTXD pin	2/fsys to 128/fsys
		Output level of TSPIxTXD during an idle term	High, Low, a last bit data hold, Hi-z
		Software reset	Reset by software is possible.

9. Sample Program

The TSPI is used to communicate data. The “write” command transmits data. And the “read” command reads the reception data and outputs to the terminal software.
The UART communication is used to transfer the commands and data to the terminal software.

9.1. Initialization

The following initialization is done after power is supplied.
The initialization of each clock setting and the setting of the watchdog timer are done.

9.2. Sample Program Main Operation

The BSP (Board Support Package) is initialized.
As initialization of the application software, the initialization of the transmission and reception for the UART and the TSPI is done.

The sample program waits for the “write” or “read” command which is input with the terminal software.

The execution of each command is as follows;

- write
  After the TSPI transmission and reception interrupts are enabled, the preset character string “TOSHIBA” is transmitted. After the data is transmitted, the TSPI ch4 reception interrupt is generated, and the data is received.

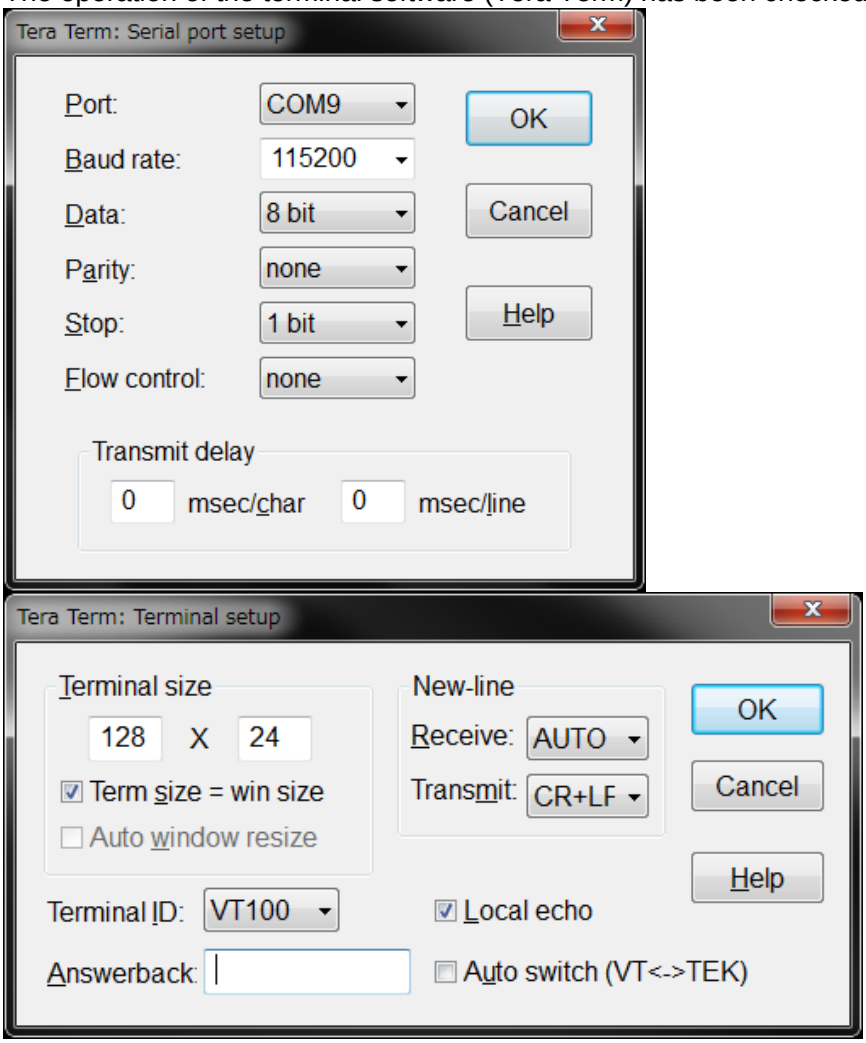
- read
  The reception data is read and output to the terminal software.

9.3. Output Example of Sample Program

When the sample program executes, the command input and its result are displayed as shown in the following figure.

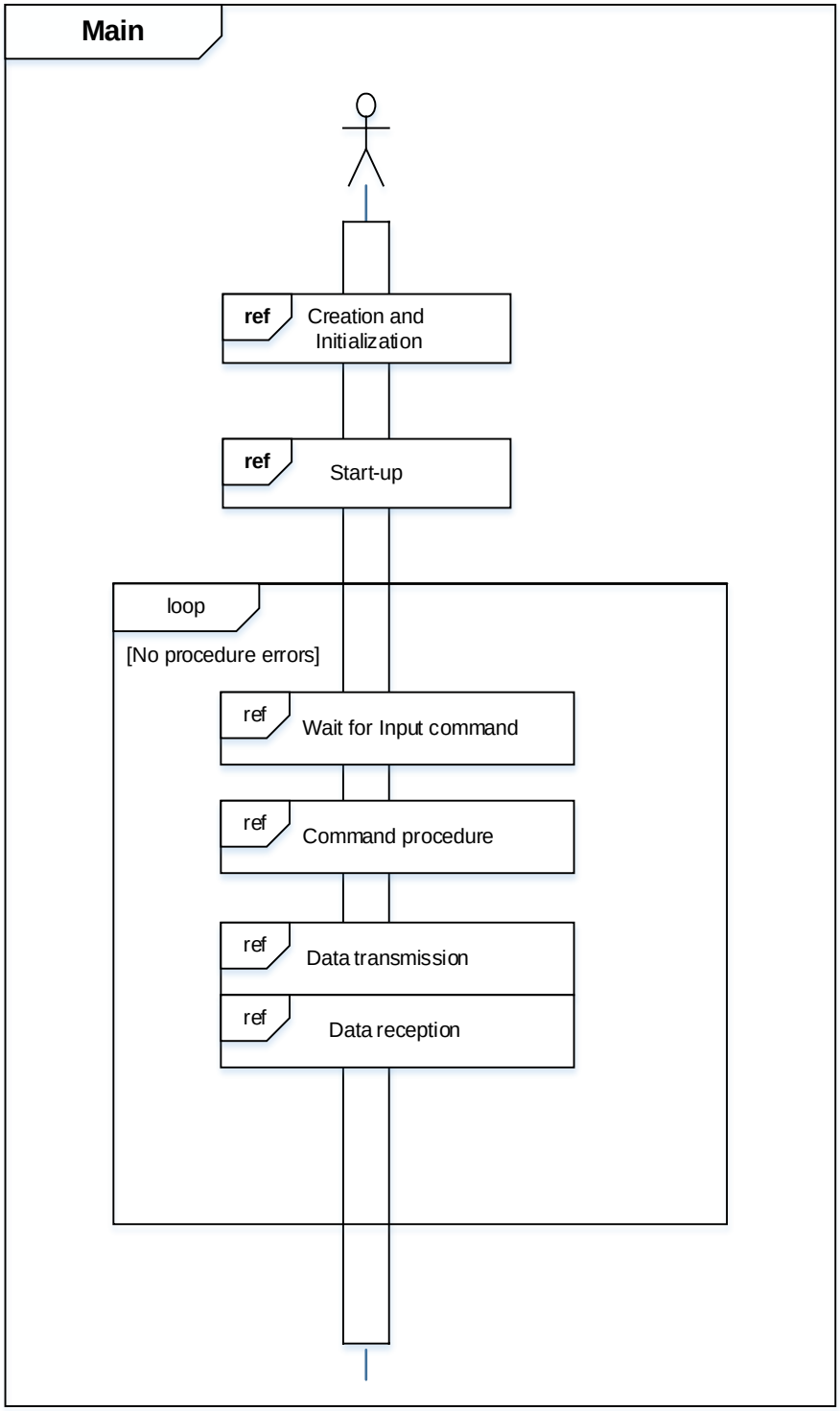
9.3.1. Setting Example of Terminal Software

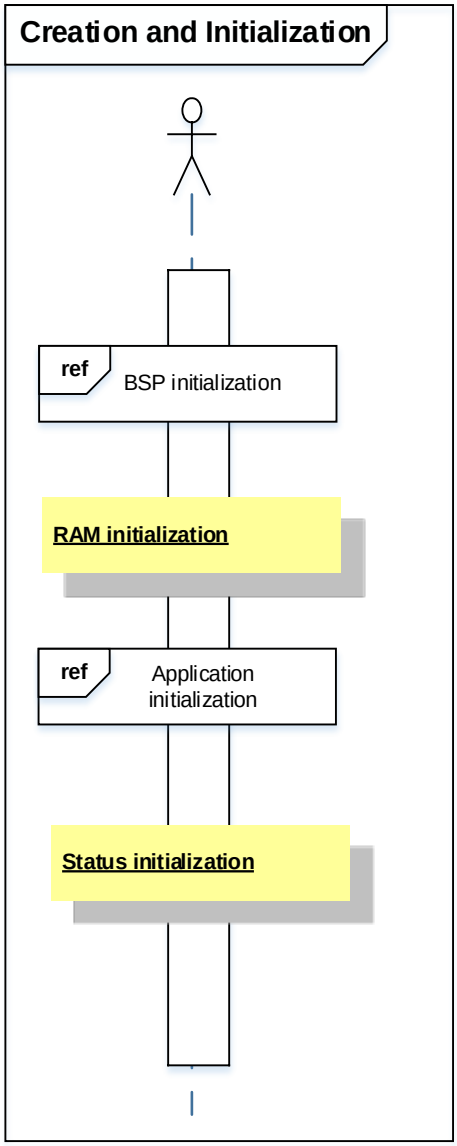
The operation of the terminal software (Tera Term) has been checked with the following settings.

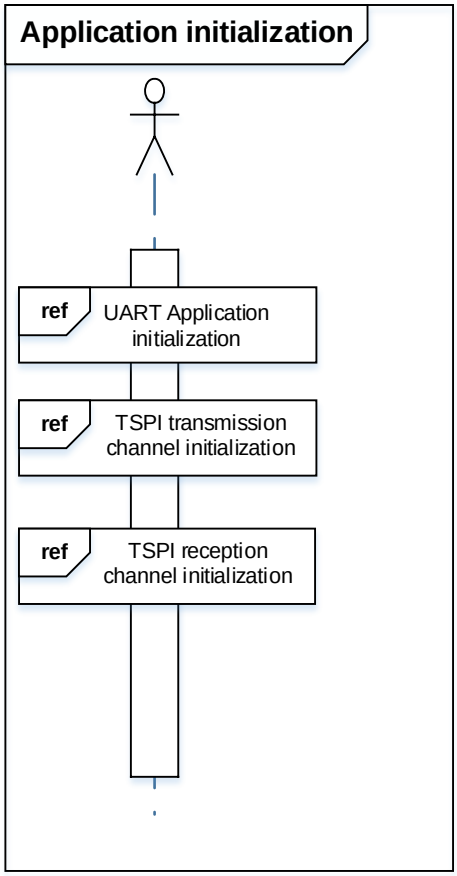


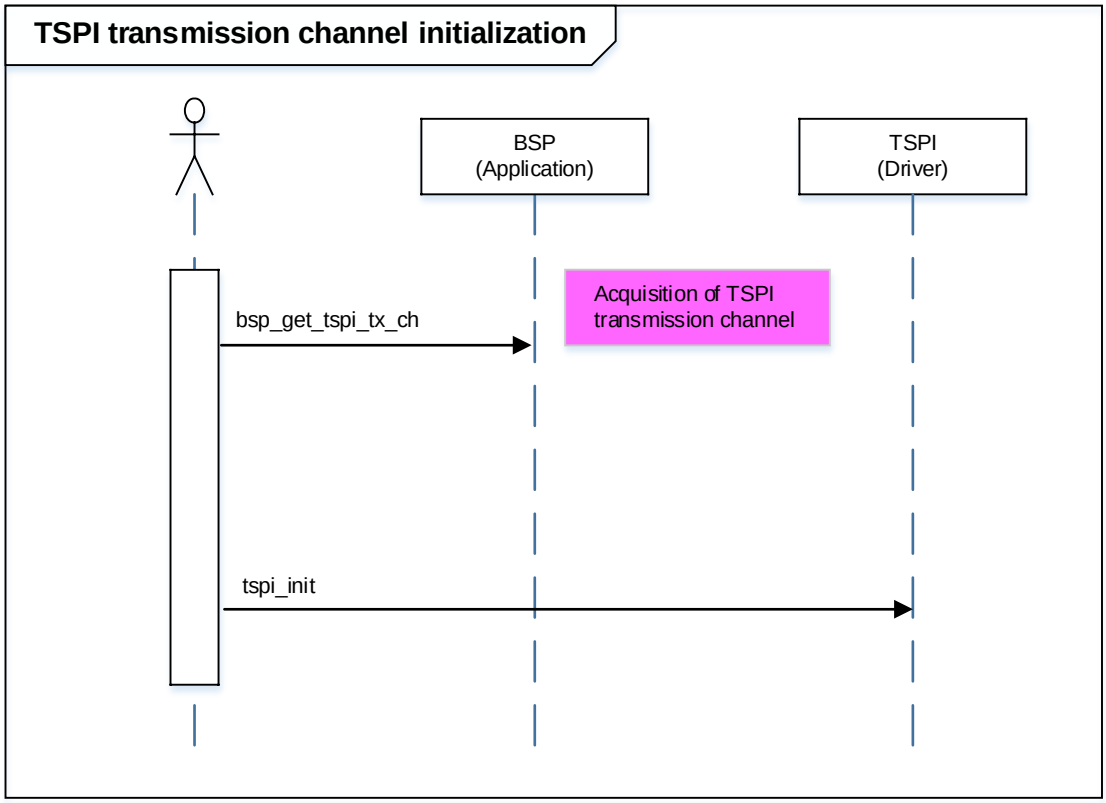
9.4. Operating Flow of Sample Program

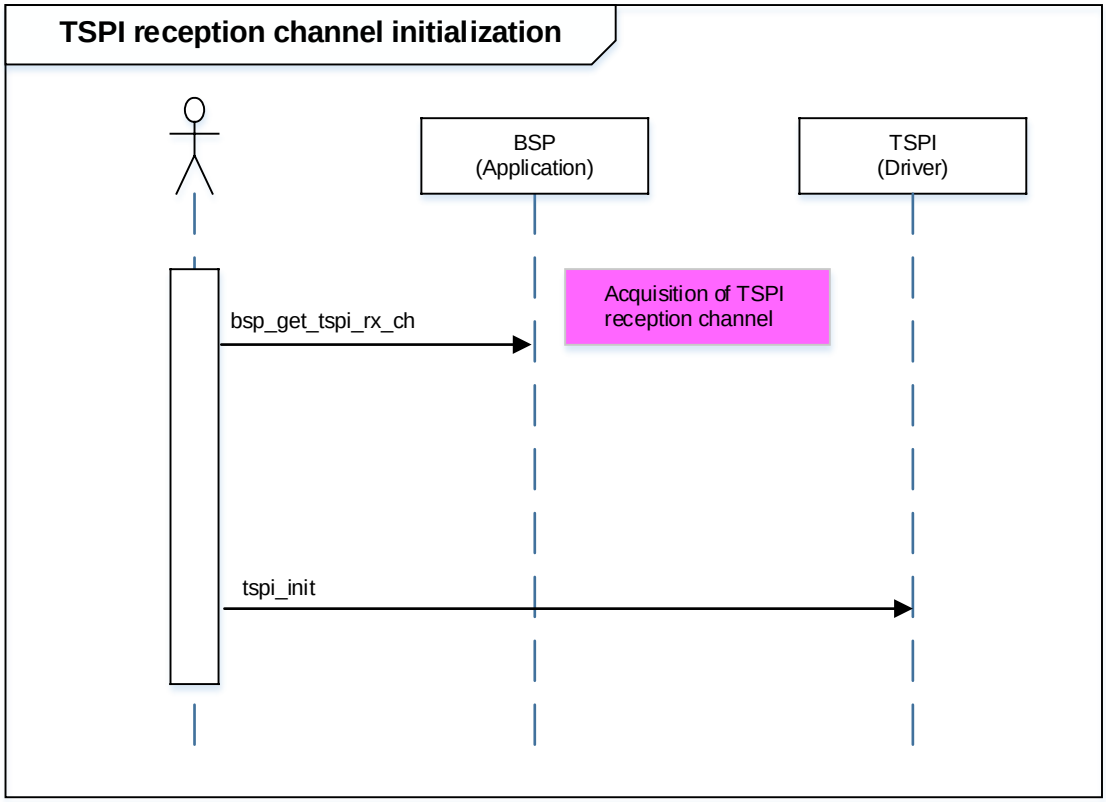
The basic operating flows of the sample program are shown in the following;

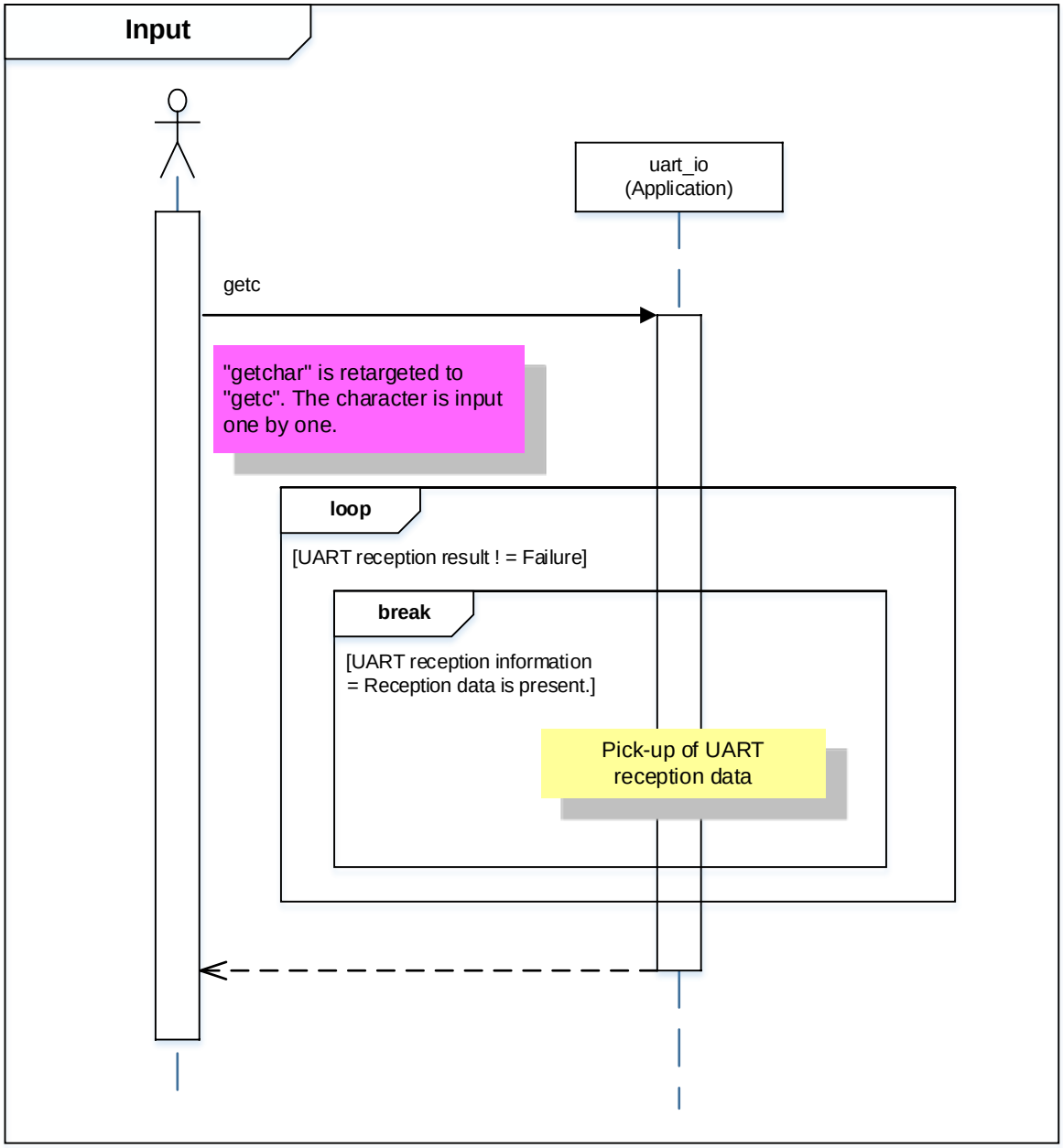


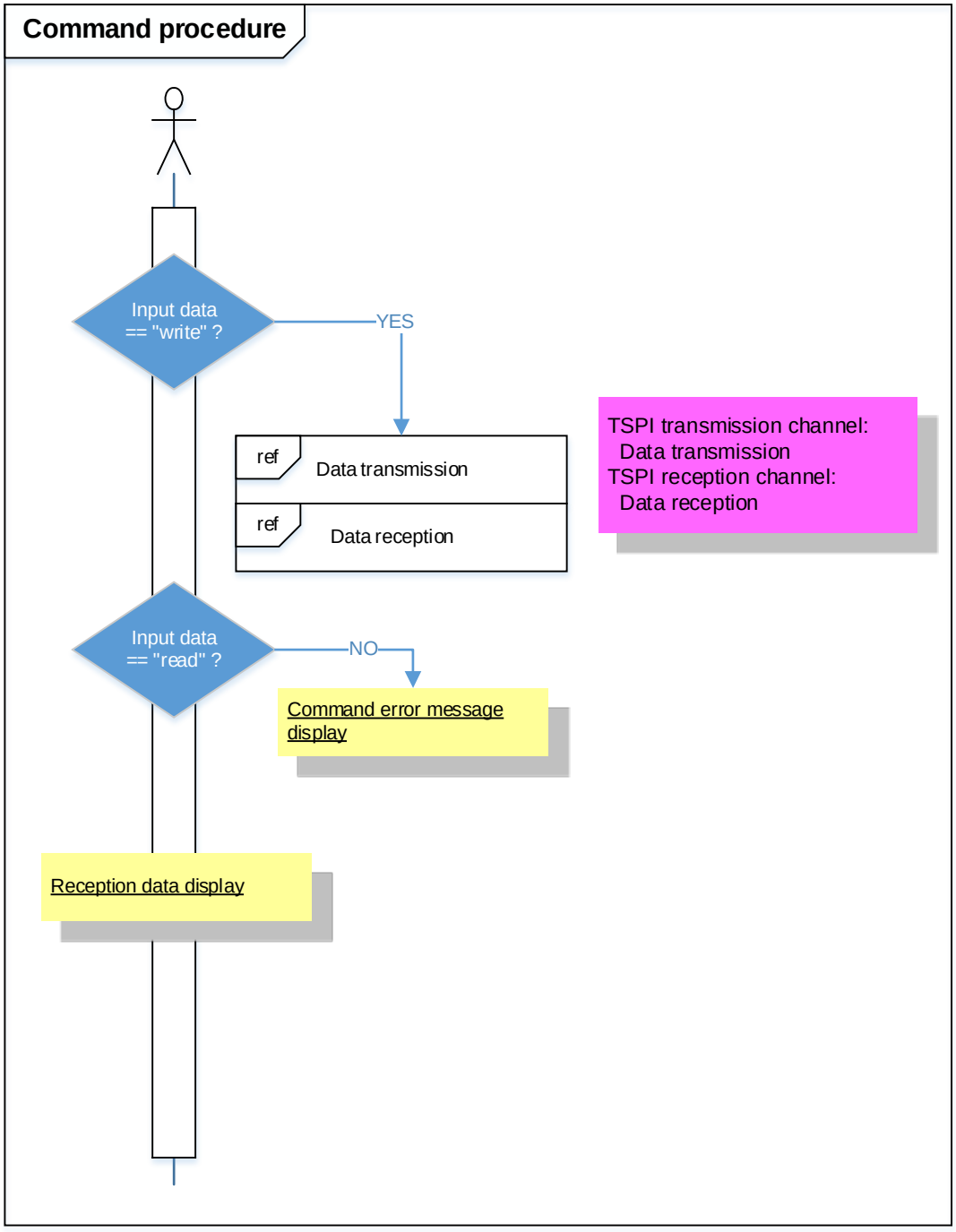

Creation and Initialization
ref
BSP initialization
RAM initialization
ref
Application initialization
Status initialization

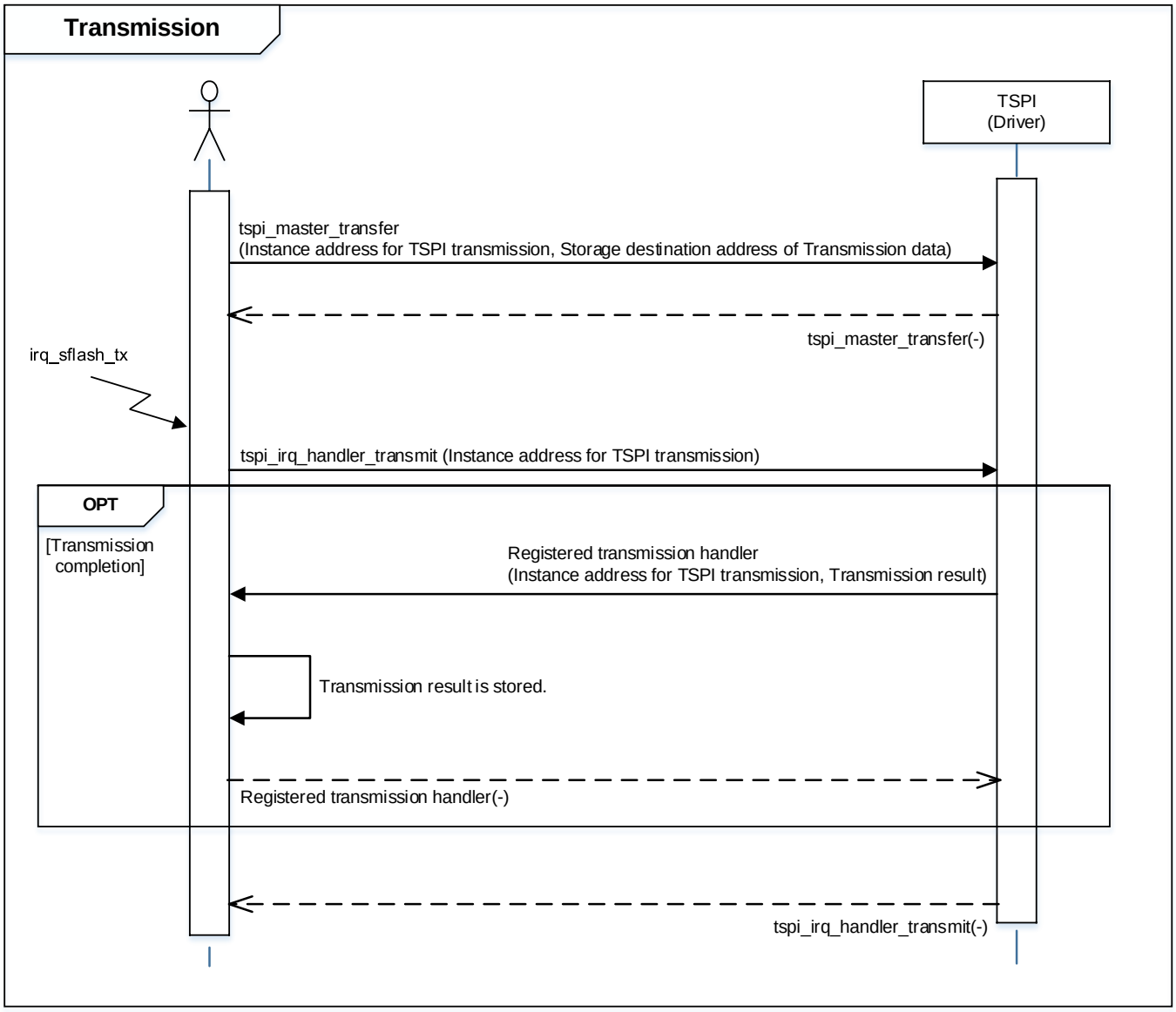

Application initialization
ref
UART Application initialization
ref
TSPI transmission channel initialization
ref
TSPI reception channel initialization

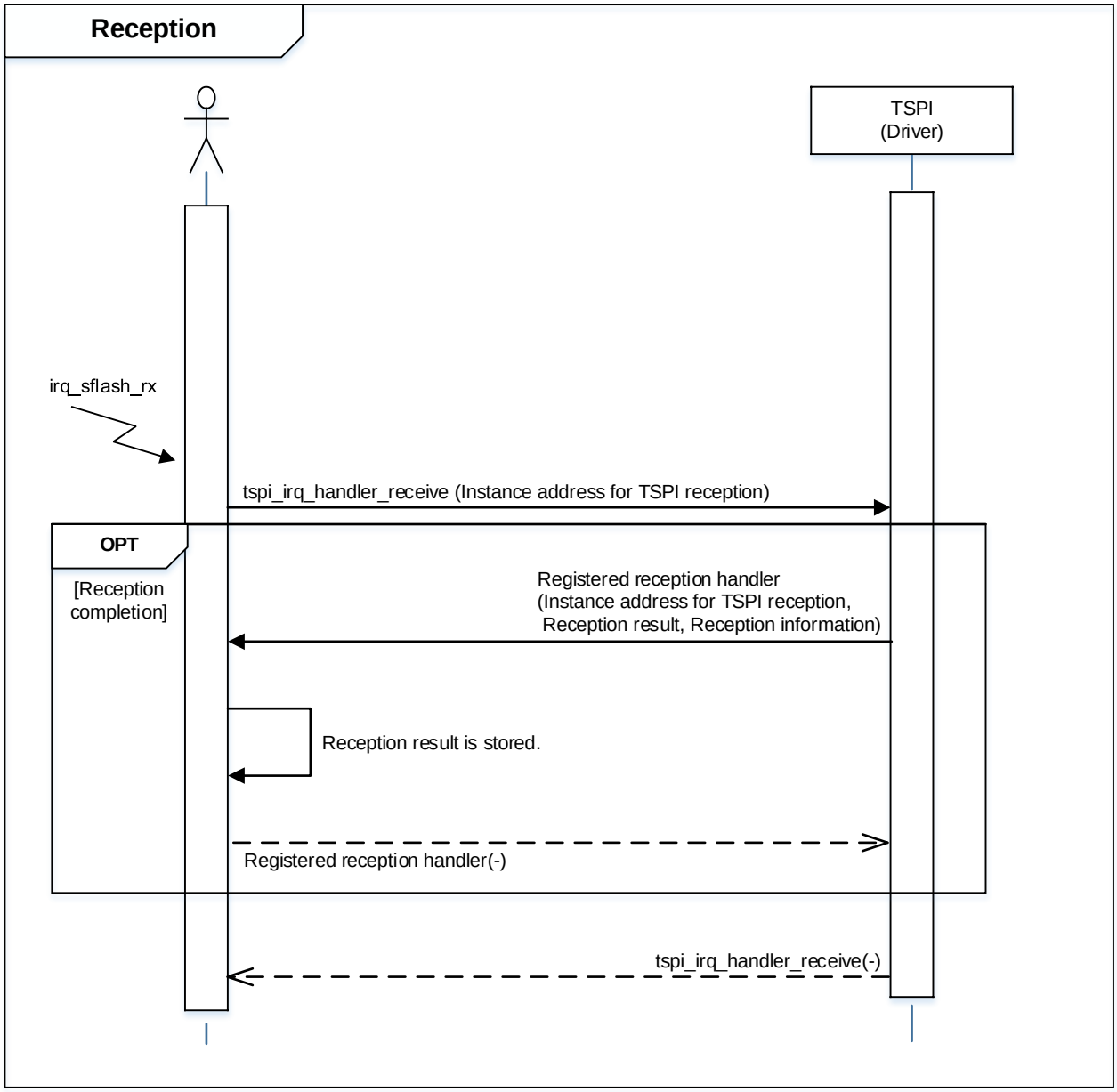

TSPI transmission channel initialization
BSP (Application)
TSPI (Driver)
Acquisition of TSPI transmission channel
bsp_get_tspi_tx_ch
tspi_init


TSPI reception channel initialization
BSP
(Application)
TSPI
(Driver)
Acquisition of TSPI
reception channel
bsp_get_tspi_rx_ch
tspi_init


Input
uart_io
(Application)
getc
"getchar" is retargeted to "getc". The character is input one by one.
loop
[UART reception result ! = Failure]
break
[UART reception information = Reception data is present.]
Pick-up of UART reception data


Command procedure
Input data
== "write" ?
YES
ref
Data transmission
ref
Data reception
TSPI transmission channel:
Data transmission
TSPI reception channel:
Data reception
Input data
== "read" ?
NO
Command error message display
Reception data display


Transmission
TSPI
(Driver)
tspi_master_transfer
(Instance address for TSPI transmission, Storage destination address of Transmission data)
tspi_master_transfer(-)
irq_sflash_tx
tspi_irq_handler_transmit (Instance address for TSPI transmission)
OPT
[Transmission completion]
Registered transmission handler
(Instance address for TSPI transmission, Transmission result)
Transmission result is stored.
Registered transmission handler(-)
tspi_irq_handler_transmit(-)


Reception
TSPI
(Driver)
irq_sflash_rx
tspi_irq_handler_receive (Instance address for TSPI reception)
OPT
[Reception
completion]
Registered reception handler
(Instance address for TSPI reception,
Reception result, Reception information)
Reception result is stored.
Registered reception handler(-)
tspi_irq_handler_receive(-)

10. Precaution

When using the sample program with CPU other than TMPM4G9F15, please check operation sufficiently.

11. Revision History

Rev	Date	Page	Description
1.0	2018-12-14	-	First release

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