

CMOS Digital Integrated Circuit Silicon Monolithic

TC358743AXBG

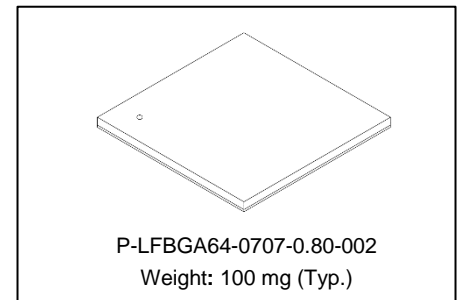
Mobile Peripheral Devices

Overview

The HDMI[®]-RX to MIPI[®] CSI-2SM-TX is a bridge device that converts HDMI stream to MIPI CSI-2 TX.

The current and next generation Application Processors and Baseband chips have been designed without video streaming input port except CSI-2 for Camcorder input. Smart Phone Processors are being used in several applications that required Video Input

TC358743AXBG takes in HDMI input and converts to CSI-2 that looks like a Camcorder input.



Features

- HDMI-RX Interface
 - ✧ HDMI 1.4
 - Video Formats Support (Up to 1080P @60fps)
 - RGB, YCbCr444: 24-bpp @60fps
 - YCbCr422 24-bpp @60fps
 - Audio Supports
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
 - 3D Support
 - Support HDCP (optional)
 - DDC Support
 - EDID Support
 - Release A, Revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
 - Embedded 1K-byte SRAM (EDID_SRAM)
 - Maximum HDMI clock speed: 165 MHz
 - ✧ Does not support Audio Return Path and HDMI Ethernet Channels
- CSI-2 TX Interface
 - ✧ MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
 - ✧ Supports up to 1 Gbps per data lane
 - Video, Audio and InfoFrame data can be transmit over MIPI CSI-2
 - ✧ Supports up to 4 data lanes
- I²C Slave Interface
 - ✧ Support for Normal-mode (100 kHz) and Fast-mode (400 kHz)
 - ✧ Support Ultra Fast-mode (2 MHz)
 - ✧ Configure all TC358743AXBG internal registers
- Audio Output Interface
 - Either I2S or TDM Audio interface available (pins are multiplexed)
 - I2S Audio Interface
 - ✧ Single data lane for stereo data
 - ✧ Support Master Clock mode only
 - ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
 - ✧ Support Left or Right-justify with MSB first
 - ✧ Support 32 bit-wide time-slot only
 - ✧ Output Audio Oversampling clock (256fs)
 - TDM (Time Division Multiplexed) Audio Interface
 - ✧ Fixed to 8 channels (depend on HDMI input stream)
 - ✧ Support 32 bit-wide time slot only
 - ✧ Support Master Clock mode only
 - ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
 - ✧ Output Audio Oversampling clock (256fs)
- InfraRed (IR)
 - ✧ Support NEC Infrared protocol.
- System
 - ✧ Internal core has two power domains (VDDC1 and VDDC2)
 - VDDC1 is always on power domain
 - VDDC2 can be shut-off during deep sleep mode
- Power supply inputs
 - ✧ Core and MIPI D-PHYSM: 1.2 V
 - ✧ I/O: 1.8V – 3.3 V
 - ✧ HDMI: 3.3 V
 - ✧ APLL: 3.3 V/2.5 V
- Power Consumption during typical operations
 - ✧ 720P: 0.48 W
 - ✧ 1080P @30fps: 0.48 W
 - ✧ 1080P @60fps: 0.54 W

Table of contents

REFERENCES.....	4
1. Overview	5
2. Features	6
3. External Pins	8
3.1. TC358743AXBG BGA64 Pin Count Summary	10
3.2. Pin Layout.....	10
4. Package	11
5. Electrical Characteristics.....	12
5.1. Absolute Maximum Ratings.....	12
5.2. Operating Condition.....	12
5.3. DC Electrical Specification	13
6. Revision History	14
RESTRICTIONS ON PRODUCT USE.....	15

List of Figures

Figure 1.1 TC358743AXBG System Overview.....	5
Figure 3.1 TC358743AXBG 64-Pin Layout (Top View).....	10
Figure 4.1 TC358743AXBG package (64 pins)	11

List of Tables

Table 2.1 TC358743AXBG Power Consumption during typical operations.....	7
Table 3.1 TC358743AXBG Functional Signal List.....	8
Table 3.2 BGA64 Pin Count Summary	10
Table 6.1 Revision History	14

- MIPI® is a registered service mark of MIPI Alliance, Inc. CSI-2SM and D-PHYSM are service marks of MIPI Alliance, Inc.
- The terms HDMI and HDMI High-Definition Multimedia Interface, and the HDMI Logo are trademarks or registered trademarks of HDMI Licensing Administrator, Inc. in the United States and other countries.
- Other company names, product names, and service names may be trademarks of their respective companies.

1 NOTICE OF DISCLAIMER

2 The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled
3 by any of the authors or developers of this material or MIPI. The material contained herein is provided on
4 an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS
5 AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all
6 other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if
7 any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of
8 accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of
9 negligence.

10 All materials contained herein are protected by copyright laws, and may not be reproduced, republished,
11 distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express
12 prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related
13 trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and
14 cannot be used without its express prior written permission.

15 ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET
16 POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD
17 TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY
18 AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR
19 MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE
20 GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL,
21 CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER
22 CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR
23 ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL,
24 WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH
25 DAMAGES.

26 Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is
27 further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the
28 contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document;
29 and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance
30 with the contents of this Document. The use or implementation of the contents of this Document may
31 involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents,
32 patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI
33 does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any
34 IPR or claims of IPR as respects the contents of this Document or otherwise.

35 Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

36 MIPI Alliance, Inc.
37 c/o IEEE-ISTO
38 445 Hoes Lane
39 Piscataway, NJ 08854
40 Attn: Board Secretary

REFERENCES

1. MIPI® D-PHYSM, "MIPI_D-PHY_specification_v01-00-00, May 14, 2009"
2. MIPI® CSI-2SM, "MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01 Revision Nov 2010"
3. VESA® Mobile Display Digital Interface Standard (Version 1.2, Type II)
4. I²C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Overview

The HDMI-RX to MIPI CSI-2-TX is a bridge device that converts HDMI stream to MIPI CSI-2 TX.

The current and next generation Application Processors and Baseband chips have been designed without video streaming input port except CSI-2 for Camcorder input. Smart Phone Processors are being used in several applications that required Video Input.

TC358743AXBG takes in HDMI input and converts to CSI-2 that looks like a Camcorder input.

TC358743AXBG System Overview block diagram is shown below.

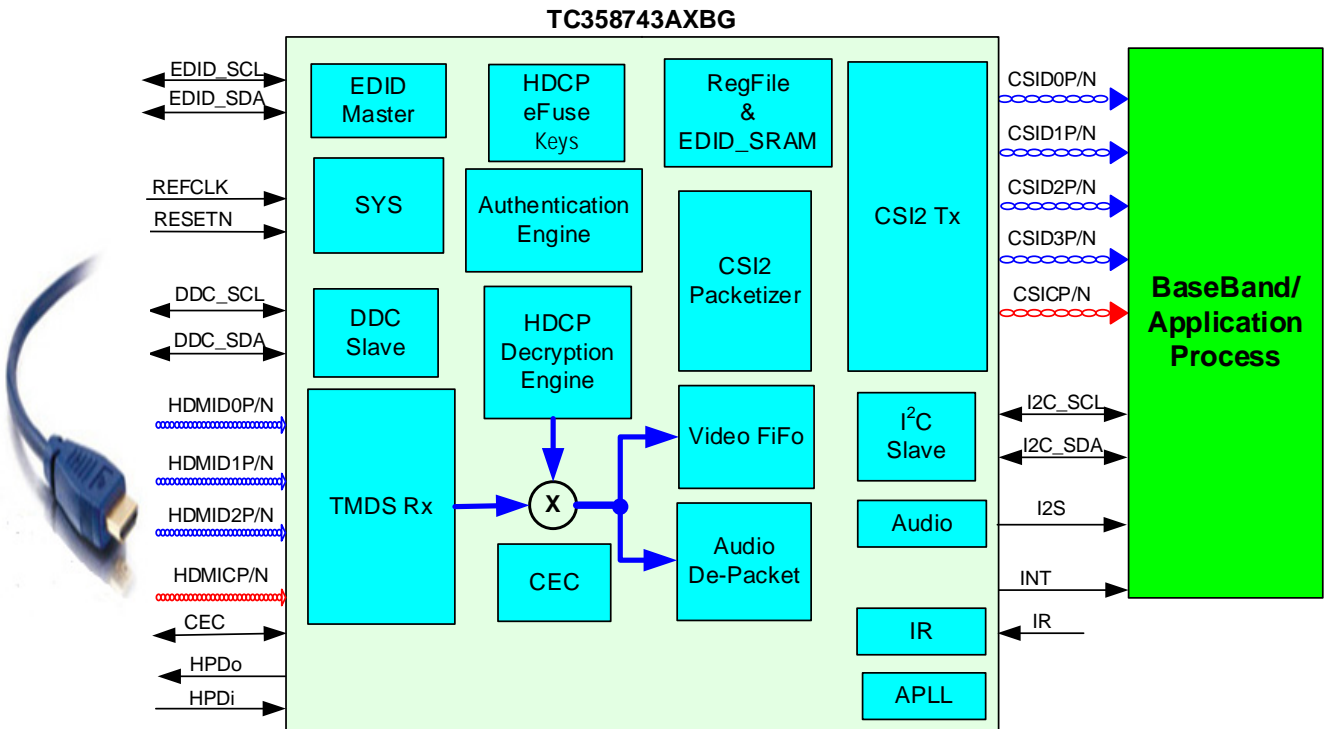


Figure 1.1 TC358743AXBG System Overview

2. Features

Below are the main features supported by TC358743AXBG.

- HDMI-RX Interface
 - ◇ HDMI 1.4
 - Video Formats Support (Up to 1080P @60fps)
 - RGB, YCbCr444: 24-bpp @60fps
 - YCbCr422 24-bpp @60fps
 - Audio Supports
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
 - 3D Support
 - Support HDCP (optional)
 - DDC Support
 - EDID Support
 - Release A, Revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
 - Embedded 1K-byte SRAM (EDID_SRAM)
 - Maximum HDMI clock speed: 165 MHz
 - ◇ Does not support Audio Return Path and HDMI Ethernet Channels
- CSI-2 TX Interface
 - ◇ MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
 - ◇ Supports up to 1 Gbps per data lane
 - Video, Audio and InfoFrame data can be transmit over MIPI CSI-2
 - ◇ Supports up to 4 data lanes
- I²C Slave Interface
 - ◇ Support for Normal-mode (100 kHz) and Fast-mode (400 kHz)
 - ◇ Support Ultra Fast-mode (2 MHz)
 - ◇ Configure all TC358743AXBG internal registers
- Audio Output Interface

Either I2S or TDM Audio interface available (pins are multiplexed)

I2S Audio Interface

 - ◇ Single data lane for stereo data
 - ◇ Support Master Clock mode only
 - ◇ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
 - ◇ Support Left or Right-justify with MSB first
 - ◇ Support 32 bit-wide time-slot only
 - ◇ Output Audio Oversampling clock (256fs)

TDM (Time Division Multiplexed) Audio Interface

 - ◇ Fixed to 8 channels (depend on HDMI input stream)
 - ◇ Support 32 bit-wide time slot only
 - ◇ Support Master Clock mode only
 - ◇ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
 - ◇ Output Audio Oversampling clock (256fs)

- InfraRed (IR)
 - ✧ Support NEC Infrared protocol
- System
 - ✧ Internal core has two power domains (VDDC1 and VDDC2)
 - VDDC1 is always on power domain
 - VDDC2 can be shut-off during deep sleep mode
- Power supply inputs
 - ✧ Core and MIPI D-PHY: 1.2 V
 - ✧ I/O: 1.8 V – 3.3 V
 - ✧ HDMI: 3.3 V
 - ✧ APLL: 3.3 V / 2.5 V
- Power Consumption during typical operations
 - ✧ 720P: 0.48 W
 - ✧ 1080P @30fps: 0.48 W
 - ✧ 1080P @60fps: 0.54 W

Table 2.1 TC358743AXBG Power Consumption during typical operations

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDD25	Total Power	Unit
		1.2	1.2	3.3	1.8	1.2	3.3	1.2	2.5		
720P @60Frames	Current (A)	0.0472		0	0.0009	0.0178	0.0879	0.0656	0.0128	480.47	mW
	Power (W)	0.05664		0	0.0017	0.0214	0.2901	0.0787	0.032		
1080P @60Frames	Current (A)	0.0766		0	0.0009	0.0228	0.0881	0.0829	0.0128	543.19	mW
	Power (W)	0.09192		0	0.0017	0.0274	0.2907	0.0995	0.032		
Sleep 0x0002 = 0x0001	Current (μA)	0.91		0.002	0.0430	0.0490	32.3700	0.3200	0.2	108.94	μW
	Power (μW)	1.092		0.0066	0.0774	0.0588	106.8210	0.3840	0.5		

Note:

- Attention about ESD. This product is weak against ESD. Please handle it carefully.
- TC358743AXBG does not perform YCbCr ↔ YUV conversion. In this document they are used interchangeably.

3. External Pins

TC358743AXBG resides in BGA64 pin packages. The following table gives the signals of TC358743AXBG and their function.

Table 3.1 TC358743AXBG Functional Signal List

Group	Pin Name	I/O	Init. (O)	Type	Function	Voltage Supply	Note
System: Reset & Clock (4)	RESETN	I	-	Sch	System reset input, active low	VDDIO2	1.8V -3.3V
	REFCLK	I	-	N	Reference clock input (27/26 MHz or 42 MHz)	VDDIO2	1.8V -3.3V
	TEST	I	-	N	TEST mode select 0: Normal mode 1: Test mode	VDDIO2	1.8V -3.3V
	INT	O	L	N	Interrupt Output signal – active high (Level)	VDDIO2	1.8V -3.3V
CSI-2 TX (10)	CSICP	-	H	MIPI-PHY	MIPI-CSI-2 clock positive	VDD_MIPI	1.2V
	CSICN	-	H	MIPI-PHY	MIPI-CSI-2 clock negative	VDD_MIPI	1.2V
	CSID0P	-	H	MIPI-PHY	MIPI-CSI-2 Data 0 positive	VDD_MIPI	1.2V
	CSID0N	-	H	MIPI-PHY	MIPI-CSI-2 Data 0 negative	VDD_MIPI	1.2V
	CSID1P	-	H	MIPI-PHY	MIPI-CSI-2 Data 1 positive	VDD_MIPI	1.2V
	CSID1N	-	H	MIPI-PHY	MIPI-CSI-2 Data 1 negative	VDD_MIPI	1.2V
	CSID2P	-	H	MIPI-PHY	MIPI-CSI-2 Data 2 positive	VDD_MIPI	1.2V
	CSID2N	-	H	MIPI-PHY	MIPI-CSI-2 Data 2 negative	VDD_MIPI	1.2V
	CSID3P	-	H	MIPI-PHY	MIPI-CSI-2 Data 3 positive	VDD_MIPI	1.2V
CSID3N	-	H	MIPI-PHY	MIPI-CSI-2 Data 3 negative	VDD_MIPI	1.2V	
HDMI-RX (8)	HDMICP	-	-	HDMI-PHY	HDMI Clock channel positive	AVDD33	3.3V
	HDMICN	-	-	HDMI-PHY	HDMI Clock channel negative	AVDD33	3.3V
	HDMID0P	-	-	HDMI-PHY	HDMI Data 0 channel positive	AVDD33	3.3V
	HDMID0N	-	-	HDMI-PHY	HDMI Data 0 channel negative	AVDD33	3.3V
	HDMID1P	-	-	HDMI-PHY	HDMI Data 1 channel positive	AVDD33	3.3V
	HDMID1N	-	-	HDMI-PHY	HDMI Data 1 channel negative	AVDD33	3.3V
	HDMID2P	-	-	HDMI-PHY	HDMI Data 2 channel positive	AVDD33	3.3V
	HDMID2N	-	-	HDMI-PHY	HDMI Data 2 channel negative	AVDD33	3.3V
DDC (2)	DDC_SCL	IO	-	N (Note2)	DDC Slave Clock	VDDIO1	3.3V (Note1)
	DDC_SDA	IO	-	N (Note2)	DDC Slave data	VDDIO1	3.3V (Note1)
EDID (2)	EDID_SCL	IO	-	N (Note2)	EDID Master Clock	VDDIO2	1.8V -3.3V
	EDID_SDA	IO	-	N (Note2)	EDID Master Data	VDDIO2	1.8V -3.3V
CEC	CEC	IO	-	N (Note2)	CEC signal	VDDIO1	3.3V
HPD (2)	HPDI	I	-	N	Hot Plug Detect Input	VDDIO1	3.3V (Note1)
	HPDO	O	L	N	Hot Plug Detect Output	VDDIO1	3.3V
Audio (4)	A_SCK	O	L	N	I2S/TDM Bit Clock signal	VDDIO2	1.8V -3.3V
	A_WFS	O	L	N	I2S Word Clock or TDM Frame Sync signal	VDDIO2	1.8V -3.3V
	A_SD	O	L	N	I2S/TDM data signal	VDDIO2	1.8V -3.3V
	A_OSCK	O	L	N	Audio Oversampling Clock	VDDIO2	1.8V -3.3V
IR	IR	I	-	Sch	Infrared signal	VDDIO2	1.8V -3.3V
I2C (2)	I2C_SCL	IO	-	N (Note2)	I2C serial clock	VDDIO2	1.8V -3.3V
	I2C_SDA	IO	-	N (Note2)	I2C serial data	VDDIO2	1.8V -3.3V
APLL (4)	BIASDA	O	L	-	BIAS signal Connect to AVSS through 0.1μF when not used	-	-
	DAOUT	O	H	-	Audio PLL clock Reference Output clock Please leave open when not used	-	-
	PCKIN	I	-	-	Audio PLL Reference Input clock Connect to AVSS through 0.1μF when not used	-	-
	PFIL	O	L	-	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1μF when not used	-	-

Group	Pin Name	I/O	Init. (O)	Type	Function	Voltage Supply	Note
POWER (12)	VDDC1, VDDC2	-	-	-	VDD for Internal Core (3)	-	1.2V
	VDDIO1	-	-	-	VDDIO1 IO power supply (1)	-	3.3V
	VDDIO2	-	-	-	VDDIO2 IO power supply (1)	-	1.8V -3.3V
	VDD_MIPI	-	-	-	VDD for the MIPI CSI-2 (2)	-	1.2V
	AVDD12	-	-	-	HDMI Phy 1.2 V power supply (2)	-	1.2V
	AVDD33	-	-	-	HDMI Phy 3.3 V power supply (2)	-	3.3V
	AVDD25	-	-	-	APLL 2.5 V power supply (1)	-	2.5V
Ground (10)	VSS	-	-	-	Ground	-	-
Misc (2)	REXT	-	-	-	External Reference Resistor, Please connect to AVDD33 with a 2 kΩ resistor (± 1%)	-	-
	VPGM	-	-	-	eFuse program power supply, please tie to ground	-	-

Total 64 pins

Note1: These IO are 5 V tolerant.

Note2: Bi-directional IO with Schmitt triggered input.

Buffer Type Abbreviation:

N: Normal IO
 N_{PD}: Normal IO with weak Internal Pull-Down
 N_{PU}: Normal IO with weak Internal Pull-Up
 FS-SOD: Failed Safe Pseudo open-drain output, Schmitt input
 FS: Failed Safe IO
 Sch: Schmitt input buffer
 MIPI-PHY: front-end analog IO for CSI-2
 HDMI-PHY: front-end analog IO for HDMI

3.1. TC358743AXBG BGA64 Pin Count Summary

Table 3.2 BGA64 Pin Count Summary

Group Name	Pin Count
System	4
CSI-2 TX	10
HDMI-RX	8
DDC	2
EDID	2
CEC	1
HPD	2
Audio	4
IR	1
I2C	2
APLL	4
POWER	12
Ground	10
Misc	2
TOTAL	64

3.2. Pin Layout

A1 REXT	A2 VSS	A3 VPGM	A4 BIASDA	A5 DAOUT	A6 PFIL	A7 CSID3N	A8 CSID3P
B1 AVDD33	B2 AVDD12	B3 INT	B4 IR	B5 AVDD25	B6 PCKIN	B7 CSID2N	B8 CSID2P
C1 HDMICP	C2 HDMICN	C3 VDDC2	C4 VSS	C5 VSS	C6 VDD_MIPI	C7 CSICN	C8 CSICP
D1 HDMID0P	D2 HDMID0N	D3 AVDD12	D4 VSS	D5 VSS	D6 VSS	D7 CSID1N	D8 CSID1P
E1 HDMID1P	E2 HDMID1N	E3 VSS	E4 VSS	E5 TEST	E6 VSS	E7 CSID0N	E8 CSID0P
F1 HDMID2P	F2 HDMID2N	F3 AVDD33	F4 VDDIO1	F5 VDDC2	F6 VDD_MIPI	F7 A_SCK	F8 A_SD
G1 CEC	G2 VDDC1	G3 DDC_SDA	G4 I2C_SDA	G5 RESETN	G6 EDID_SDA	G7 A_WFS	G8 A_OSCK
H1 HPDO	H2 HPDI	H3 DDC_SCL	H4 I2C_SCL	H5 REFCLK	H6 EDID_SCL	H7 VDDIO2	H8 VSS

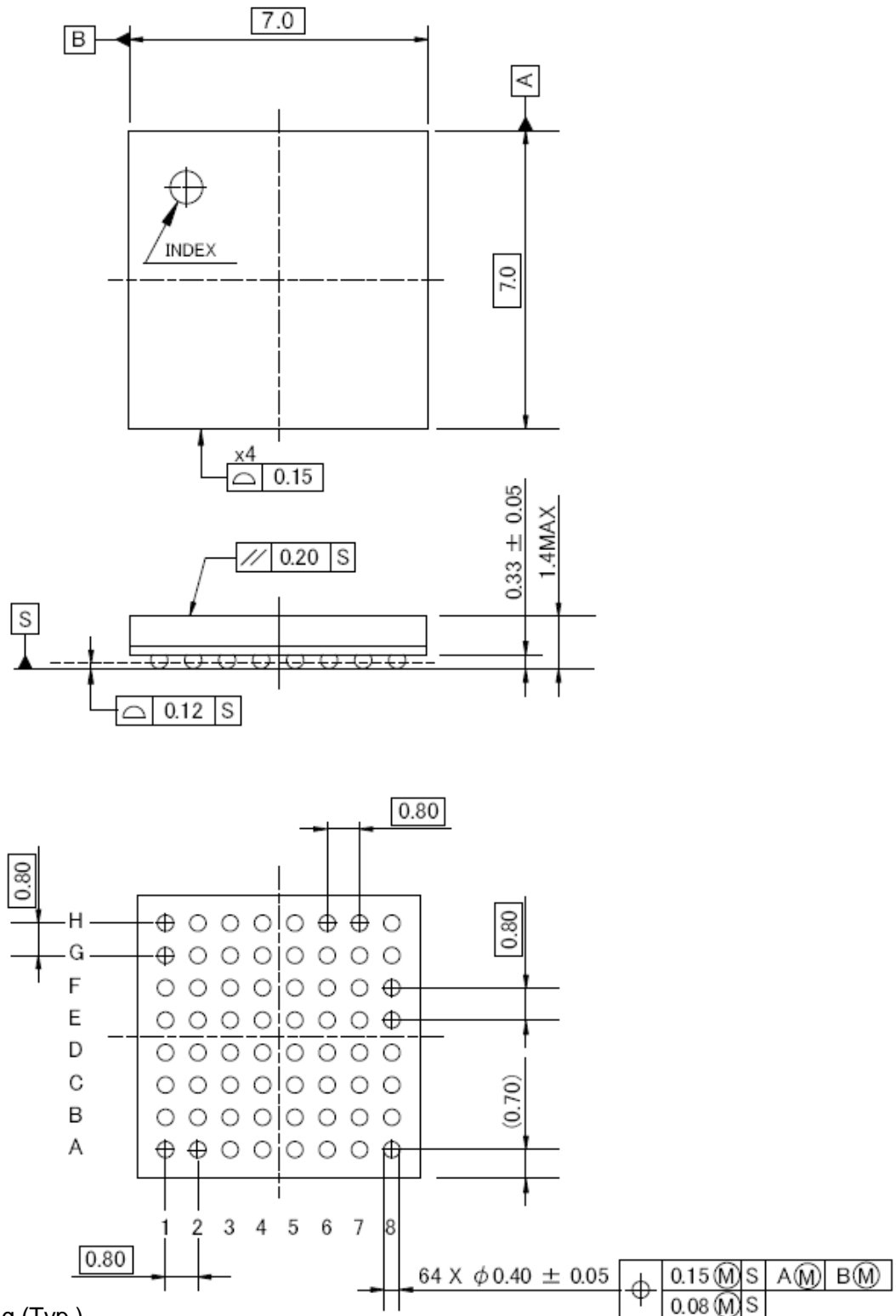
Figure 3.1 TC358743AXBG 64-Pin Layout (Top View)

4. Package

The packages for TC358743AXBG are described in the figures below.

P-LFBGA64-0707-0.80-002

(Unit: mm)



Weight: 100 mg (Typ.)

Figure 4.1 TC358743AXBG package (64 pins)

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS = 0 V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3 V – HDMI RX Phy)	AVDD33	-0.3 to +3.9	V
Supply voltage (1.2 V – HDMI RX Phy)	AVDD12	-0.3 to +1.8	V
Supply voltage (2.5 V – APLL)	AVDD25	-0.3 to +2.75	V
Input voltage (CSI IO)	V _{IN_CSI}	-0.3 to VDD_MIPI + 0.3	V
Output voltage (CSI IO)	V _{OUT_CSI}	-0.3 to VDD_MIPI + 0.3	V
Input voltage (Digital IO)	V _{IN_IO}	-0.3 to VDDIO + 0.3	V
Output voltage (Digital IO)	V _{OUT_IO}	-0.3 to VDDIO + 0.3	V
Output voltage (APLL)	V _{OUT_APLL}	-0.3 to AVDD25 + 0.3	V
Junction temperature	T _j	125	°C
Storage temperature	T _{stg}	-40 to +125	°C

5.2. Operating Condition

VSS = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8/3.3 V – Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3 V – HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2 V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Supply voltage (2.5 V – APLL)	AVDD25	2.25	2.5	2.75	V
Operating temperature (ambient temperature with voltage applied)	T _a	-30	25	85	°C
Supply Noise Voltage	V _{SN}	-	-	0.1	V _{pp}
Supply voltage (3.3 V – HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply Noise Voltage for AVDD33	V _{SN33}	-	-	0.08	V _{pp}
Supply voltage (1.2 V – HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply Noise Voltage for AVDD12	V _{SN12}	-	-	0.04	V _{pp}

5.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input ^{Note1}	V_{IH}	$0.7 \times V_{DDIO}$	-	V_{DDIO}	V
Input voltage, Low level input ^{Note1}	V_{IL}	0	-	$0.3 \times V_{DDIO}$	V
Input voltage High level CMOS Schmitt Trigger ^{Note1, Note2}	V_{IHS}	$0.7 \times V_{DDIO}$	-	V_{DDIO}	V
Input voltage Low level CMOS Schmitt Trigger ^{Note1, Note2}	V_{ILS}	0	-	$0.3 \times V_{DDIO}$	V
Output voltage High level ^{Note1, Note2}	V_{OH}	$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
Output voltage Low level ^{Note1, Note2}	V_{OL}	0	-	$0.2 \times V_{DDIO}$	V
Input leak current, High level (Condition: $V_{IN} = +V_{DDIO}$, $V_{DDIO} = 3.6 \text{ V}$)	I_{ILH1} ^(Note3)	-10	-	10	μA
Input leak current, Low level (Condition: $V_{IN} = 0 \text{ V}$, $V_{DDIO} = 3.6 \text{ V}$)	I_{ILL1} ^(Note4)	-10	-	10	μA

Note1: Each power source is operating within operating condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note3: Normal pin or Pull-up IO pin applied V_{DDIO} supply voltage to V_{in} (input voltage)

Note4: Normal pin applied V_{SS} (0 V) to V_{in} (input voltage)

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.62	2016-01-05	Newly released
1.0	2017-10-26	Added comment to HDCP in Features. Changed header, footer and the last page. Changed corporate name.
1.1	2019-01-23	Modified descriptions of service mark and trademark. Added trademarks and service marks. Modified "Note" number in section 5.3. Corrected weight. Revised the last page "RESTRICTIONS ON PRODUCT USE" and added URL.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**