32-bit RISC Microcontroller

TXZ Family

Reference Manual
Advanced Encoder Input Circuit(32-bit)
(A-ENC32-A)

Revision 1.1

2018-10

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

Related Documents

Document name
Exception
Clock Control and Operation Mode
Product Information
Advanced Programmable Motor Control Circuit
Programmable Motor Control Circuit Plus

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviation

The following words are terms or abbreviations mainly used in this Reference Manual.

A-PMD	Advanced Programmable Motor Control Circuit
ADC	Analog to Digital Converter
BLDC	Brush Less DC (Motor)
BEMF	Back Electro Motive Force
CCW	Counter Clockwise
CW	Clockwise
PMD+	Programmable Motor Control Circuit Plus
PWM	Pulse Width Modulation

1. Outlines

One unit of Advanced encoder input circuit (32-bit) (hereafter ENC) operates as one channel input circuit (ENCxA/ENCxB/ENCxZ). The list of the functions is shown in the following table.

Function category	Function	Operation
Sensor input	Encoder mode	An incremental encoder of AB or ABZ type is connected in this mode. - The rotation edge is detected and the rotation direction is judged by combination of ENCxA and ENCxB inputs. - The counter counts up or down depending on the rotation direction. - The maximum count number per cycle is 2^{32}. - ENCxZ input logic is selectable.
	Sensor mode (Event count)	2-phase or 3-phase hall IC (U, V, or W) is connected in this mode. - The rotation edge is detected and the rotation direction is judged by combination of 2-phase or 3-phase signals. - The counter counts up or down depending on the rotation direction. - The maximum count number is 2^{32}.
	Sensor mode (Timer count)	2-phase or 3-phase hall IC (U, V, or W) is connected in this mode. - The rotation edge is detected and the rotation direction is judged by combination of 2-phase or 3-phase signals. - The interval of the rotation edge detection can be measured by the 32-bit counter. - Comparison function: Commutation trigger of PMD circuit synchronous with the edge detection can be generated. - Sensor-less control of a pulse driven brushless DC (BLDC) motor is supported by PWM synchronous sampling.
	Sensor mode (Phase count)	2-phase or 3-phase hall IC (U, V, or W) is connected in this mode. - The rotation edge is detected and the rotation direction is judged by combination of 2-phase or 3-phase signals. - The interval of the rotation edge detection can be measured by the 32-bit counter. - The counter operates with any frequency clock and the count-up and count-down can be selected.
General purpose timer	Timer mode	This circuit is used as a 32-bit timer operating with the system clock (fsys) in this mode. - ENCxZ input edge detection can be done. - The interval of the rotation edge detection can be measured by the 32-bit counter. - An interrupt can be generated by the comparison function.
Phase counter	Phase counter mode (Phase measurement)	This circuit is used as a 32-bit counter operating with any frequency clock in this mode. - ENCxZ input edge detection can be done. - The interval of the rotation edge detection can be measured by the 32-bit counter. - An interrupt can be generated by the comparison function.
	Phase counter mode (Phase difference measurement)	This circuit is used as a 32-bit counter operating with any frequency clock in this mode. The phase difference between the general purpose timer output and ENCxZ input can be measured.
Noise cancellation	Input circuit	The sampling by fsys division clock or a signal synchronous with PWM signal can be done. - The interval of the noise cancellation can be selected.

Table 1.1 Signal input pin

Signal name		Encoder A, B, or Z	Hall sensor U, V, or W
Connection pin	ENCxA	A	U
	ENCxB	B	V
	ENCxZ	Z	W

2. Configuration

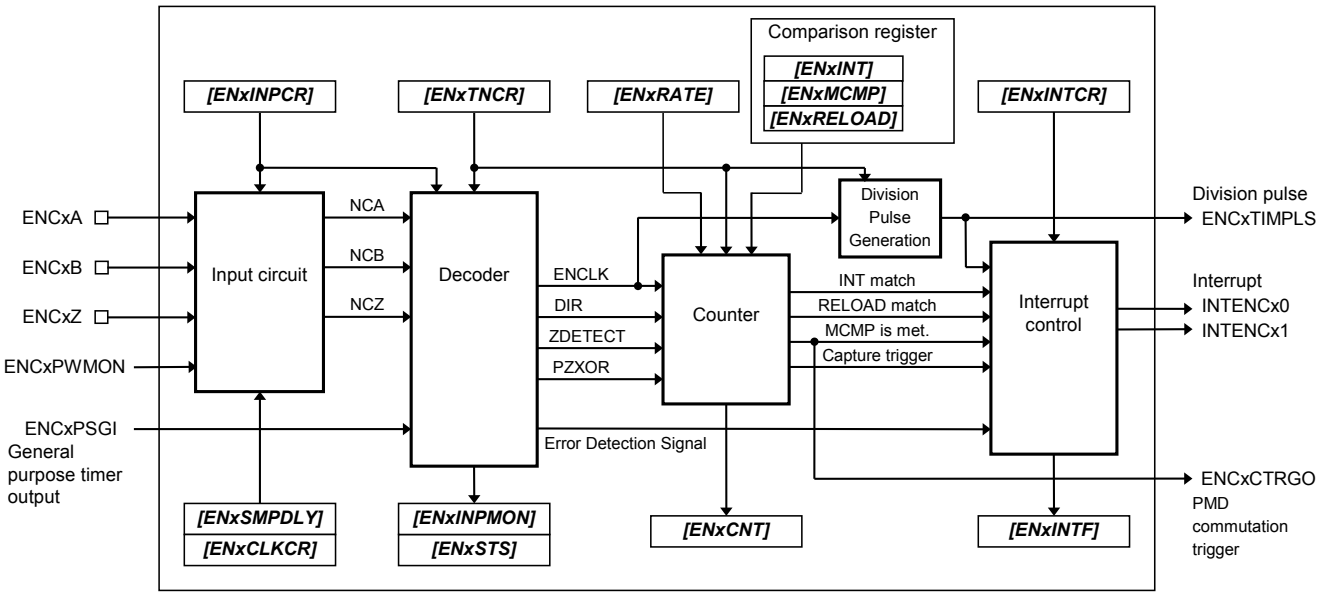

Figure 2.1 Block diagram of ENC

Table 2.1 List of signals

No	Symbol	Signal name	I/O	Reference manual
1	ENCxA	Encoder input A pin	Input	Product Information
2	ENCxB	Encoder input B pin	Input	Product Information
3	ENCxZ	Encoder input Z pin	Input	Product Information
4	ENCxPWMON	PWM signal for sampling	Input	Product Information
5	ENCxCTRGO	Commutation trigger for PMD	Output	Product Information
6	ENCxPSGI	General purpose timer output signal	Input	Product Information
7	ENCxTIMPLS	Division pulse signal	Output	Product Information
8	INTENCx0	Encoder input interrupt 0	Output	Exception
9	INTENCx1	Encoder input interrupt 1	Output	Exception, Product Information

3. Function and Operation

3.1. Clock Supply

When ENC is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB]***), and fc supply stop register (***[CGFCEN]***). The registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock control and operation mode" in Reference manual.

3.2. Operation Mode

There are 13 operation modes in ENC. The mode is determined by the setting of ***[ENxTNCR]***<MODE>, <P3EN>, and <ZEN>. The operation modes are shown in the following table.

The other combinations should not be set.

Table 3.1 Operation modes

[ENxTNCR]			Input pin	Mode
<MODE>	<ZEN>	<P3EN>		
000	0	0	ENCxA and ENCxB	Encoder mode (without ENCxZ signal)
	1		ENCxA, ENCxB, and ENCxZ	Encoder mode (with ENCxZ signal)
001	0	0	ENCxA and ENCxB	Sensor mode (Event count: 2-pahse input)
		1	ENCxA, ENCxB, and ENCxZ	Sensor mode (Event count: 3-phase input)
010	0	0	ENCxA and ENCxB	Sensor mode (Timer count: 2-phase input)
		1	ENCxA, ENCxB, and ENCxZ	Sensor mode (Timer count: 3-phase input)
011	0	0	-	Timer mode
	1		ENCxZ	Timer mode (with Capture input)
110	0	0	ENCxA and ENCxB	Sensor mode (Phase count: 2-phase input)
		1	ENCxA, ENCxB, and ENCxZ	Sensor mode (Phase count: 3-phase input)
111	0	0	-	Phase counter mode (Phase count)
	1		ENCxZ	Phase counter mode (Phase count: with Capture input)
	1	1	ENCxZ	Phase counter mode (Phase difference measurement)

3.2.1. Encoder Mode

This mode supports High-speed position sensor (Phase judgment). The incremental encoder (AB and ABZ) should be used.

- Using the rotation edge detection, a division pulse and an interrupt can be generated.
- Using the rotation edge pulse count, an interrupt can be generated at any counter value.
- Rotation direction judgment
- 32-bit up- and down-count (controlled by the rotation direction judgment)
- The setting of the counter value is available.
- The setting of the detected rotation direction is available.
- Abnormal state detection flag

(1) ENCxZ input is valid. Positive logic input: (***[ENxTNCR]***<ZEN>=1 and ***[ENxTNCR]***<ZEACT>=0)
In the case of ***[ENxRELOAD]***=0x00000380 and ***[ENxINT]***=0x00000002;

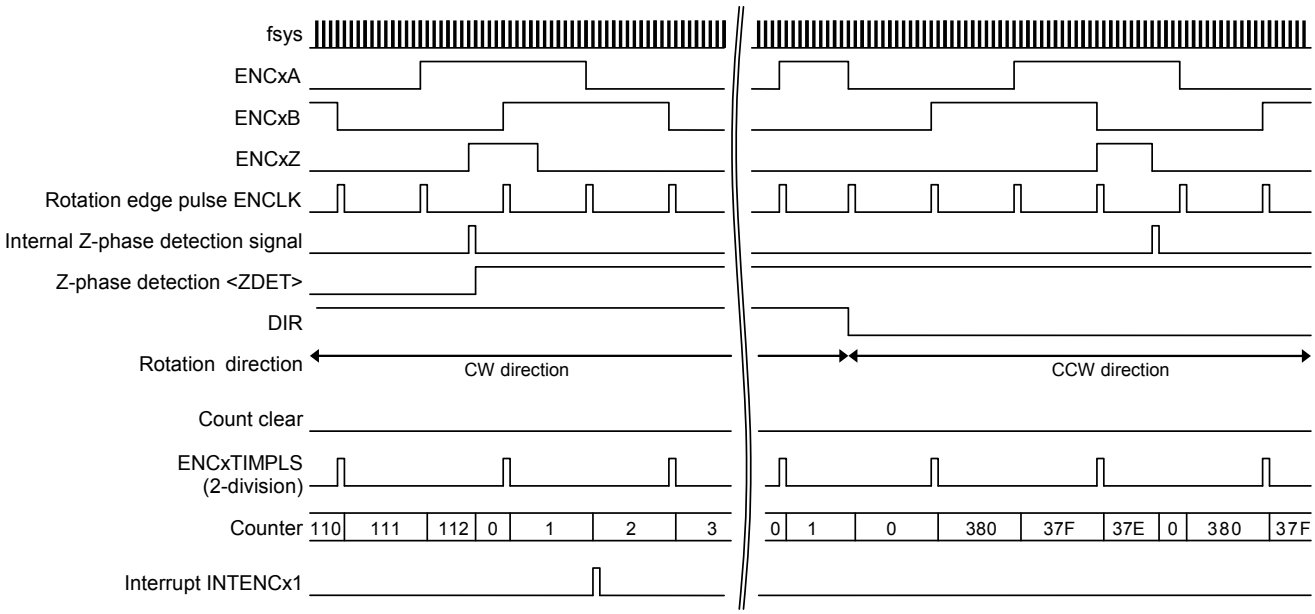

Figure 3.1 ENCxZ input is valid (*[ENxTNCR]*<ZEN>=1).

(2) ENCxZ input is invalid (***[ENxTNCR]***<ZEN>=0).

In the case of ***[ENxRELOAD]***=0x00000380 and ***[ENxINT]***=0x00000002;

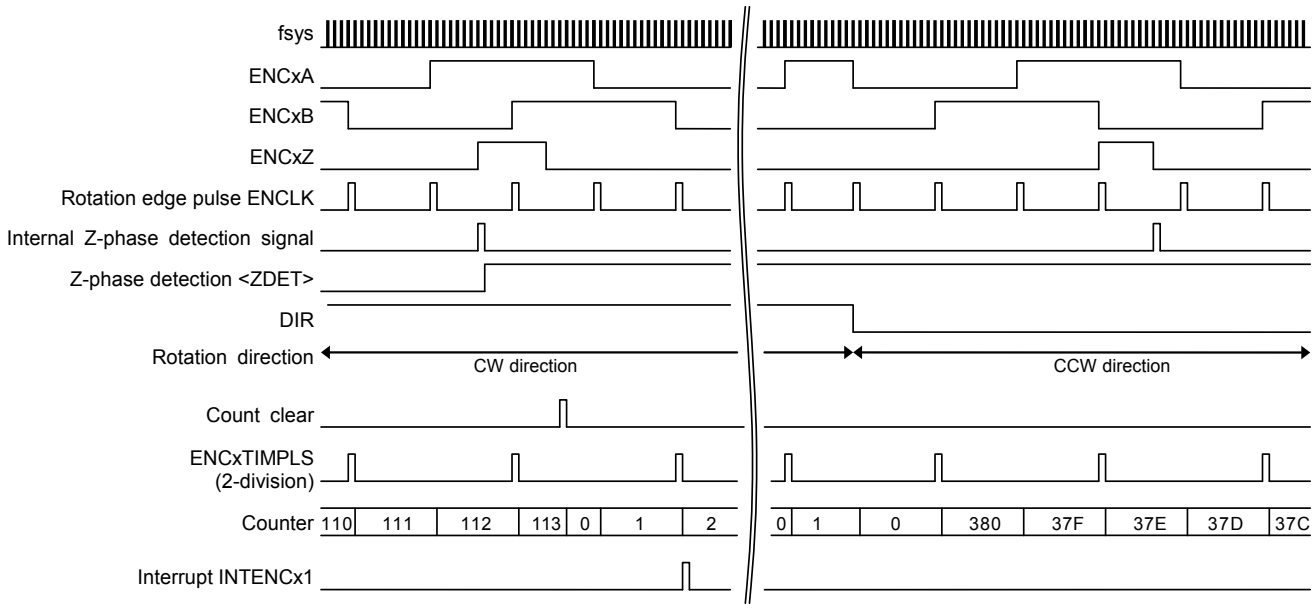

Figure 3.2 ENCxZ input is invalid (*[ENxTNCR]*<ZEN>=0).

In the encoder mode, incremental encoder signals should be connected to ENCxA, ENCxB, and ENCxZ pins. The frequencies of ENCxA and ENCxB signals are multiplied by 4. Then, the rotation edge pulses are counted.

When the rotation is done in CW direction (ENCxA is 90 degrees ahead comparing with ENCxB), the counter value increments. After the counter value matches the value in ***[ENxRELOAD]***, the counter is cleared to "0" at the next ENCLK.

When the rotation is done in CCW direction (ENCxA is 90 degrees late comparing with ENCxB), the counter value decrements. After the counter value equals to "0x00000000", the counter value is set to the value in ***[ENxRELOAD]*** at the next ENCLK.

When <ZEN> is set to "1", ENCxZ pin input is valid.

When <ZEN>=1 and <ZEACT>=0 (Input positive logic), the counter is cleared to "0" by the rising edge of ENCxZ in the CW-direction rotation, and by the falling edge of ENCxZ in the CCW-direction rotation.

When <ZEN>=1 and <ZEACT>=1 (Input negative logic), the counter is cleared to "0" by the falling edge of ENCxZ in the CW-direction rotation, and by the rising edge of ENCxZ in the CCW-direction rotation.

If ENCLK timing coincides with ENCxZ detection timing, the counter is cleared to "0" without counting.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0".

When the rotation direction is detected as CW, ***[ENxSTS]***<UD> is set to "1", and detected as CCW, set to "0".

[ENxTNCR]<DECMD> can set the detecting direction to CW only or CCW only. And, when <DECMD> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

The signal dividing ENCLK (ENCxTIMPLS) is output.

When ***[ENxINTCR]***<CMPIE>=1 and the counter value becomes ***[ENxINT]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<MCMPIE>=1 and the counter value becomes ***[ENxMCMP]*** value, INTENCx1 interrupt can be generated.

When <ZEN>=1, however, the coincidence interrupt is not generated during the interval of ***[ENxSTS]***<ZDET>=0.
<ZDET> is set to "1" when the first ENCxZ signal is detected after the encoder input is enabled.
<ZDET> and ***[ENxSTS]***<UD> are cleared to "0" when ***[ENxTNCR]***<ENRUN>=0.

3.2.2. Sensor Mode

The low-speed position sensor (Zero-cross judgment) is supported to use 2-phase hall sensor input and 3-phase hall sensor input. There are three sensor modes, Event count mode, Timer count mode, and Phase count mode.

In the timer count mode and the phase count mode, when PMD circuit drives BLDC motor with the pulse signal, the zero cross detection of the induced voltage can be supported using PWM synchronous sampling. (BEMF detection control)

3.2.2.1. Event Counter

The count is done by the rotation edge detection.

- Using the rotation edge detection, a division pulse and an interrupt can be generated.
- Using the rotation edge pulse count, an interrupt can be generated at any counter value.
- Rotation direction judgment
- 32-bit up- and down-count (controlled by the rotation direction judgment)
- The setting of the detected rotation direction is available.
- Abnormal state detection flag

(1) 3-phase decode (***[ENxTNCR]***<P3EN>=1)
In the case of ***[ENxINT]***=0x00000002;

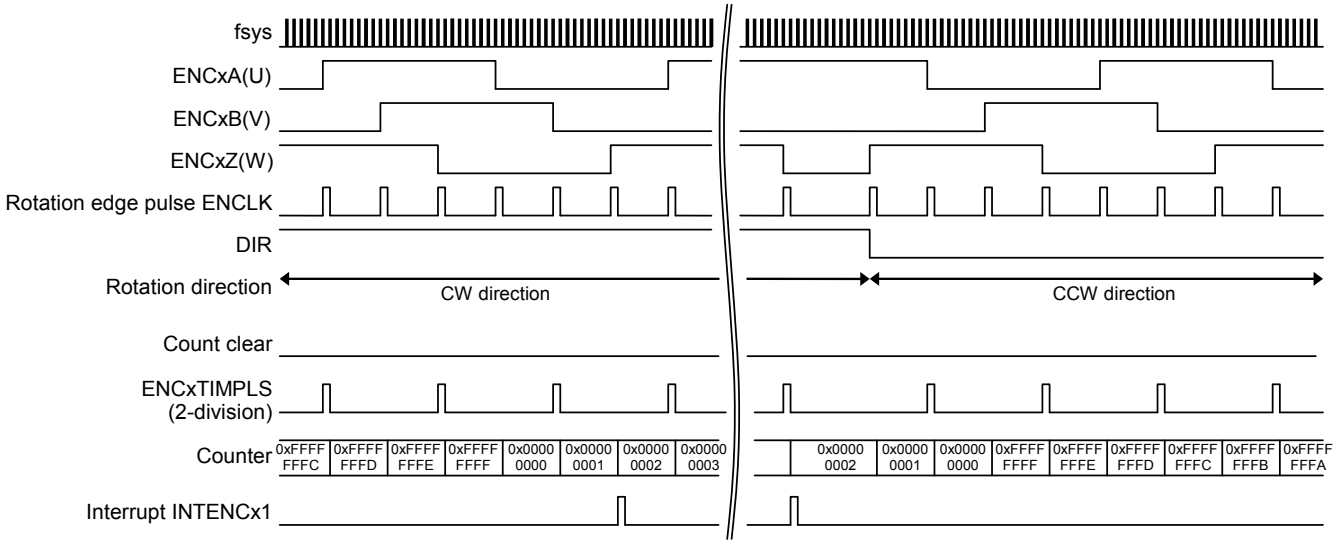

Figure 3.3 3-phase decode (*[ENxTNCR]*<P3EN>=1)

(2) 2-phase decode (***[ENxTNCR]***<P3EN>=0)

In the case of ***[ENxINT]***=0x00000002;

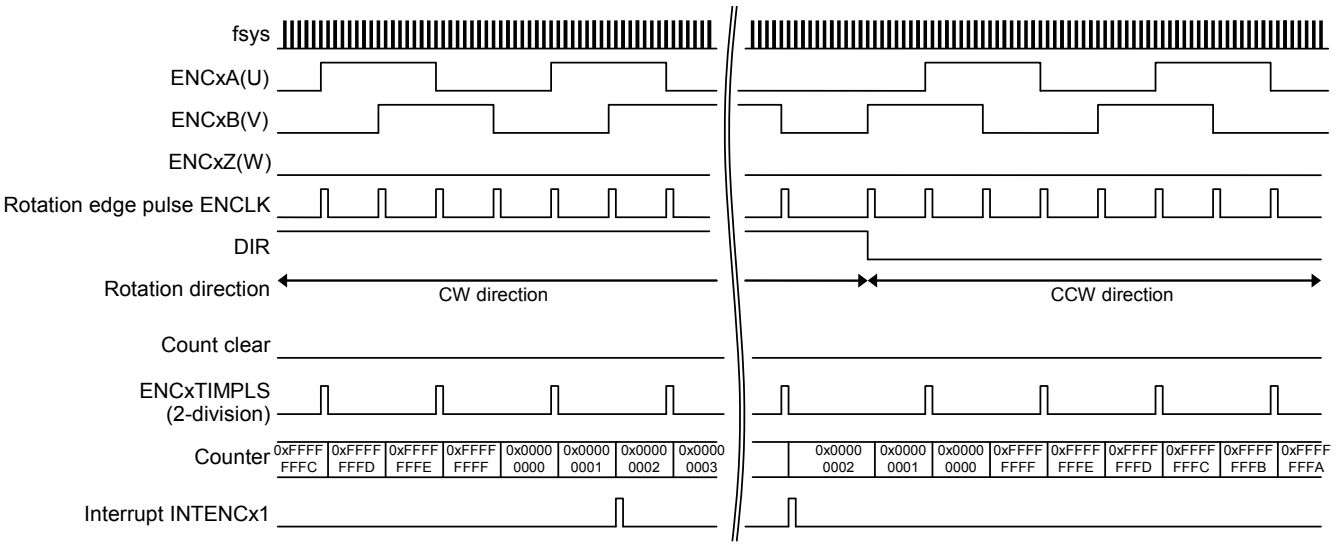

Figure 3.4 2-phase decode (*[ENxTNCR]*<P3EN>=0)

The hall sensor inputs (U, V, and W) are connected to ENCxA, ENCxB, and ENCxZ, respectively. When <P3EN>=0, the frequency of 2-phase inputs (ENCxA and ENCxB) is multiplied by 4, and when <P3EN>=1, the frequency of 3-phase inputs (ENCxA, ENCxB, and ENCxZ) is multiplied by 6. Then, the rotation edge pulses are counted.

When the rotation is done in CW direction (ENCxA is 90 degrees ahead comparing with ENCxB), the counter value increments. After the counter value matches the value "0xFFFFFFFF", the counter is cleared to "0" at the next ENCLK.

When the rotation is done in CCW direction (ENCxA is 90 degrees late comparing with ENCxB), the counter value decrements. After the counter value equals to "0x00000000", the counter value is set to the value "0xFFFFFFFF" at the next ENCLK.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0".

When the rotation direction is detected as CW, ***[ENxSTS]***<UD> is set to "1", and detected as CCW, set to "0". <UD> is cleared to "0" when ***[ENxTNCR]***<ENRUN>=0.

[ENxTNCR]<DECMD> can set the rotation direction to CW only or CCW only. When <DECMD> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

The signal dividing ENCLK (ENCxTIMPLS) is output.

When ***[ENxINTCR]***<CMPIE>=1 and the counter value becomes ***[ENxINT]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<MCMPIE>=1 and the counter value becomes ***[ENxMCMP]*** value, INTENCx1 interrupt can be generated.

3.2.2.2. Timer Count

(1) 3-phase decode (***[ENxTNCR]***<P3EN>=1)
In the case of ***[ENxINT]***=0x00000002;

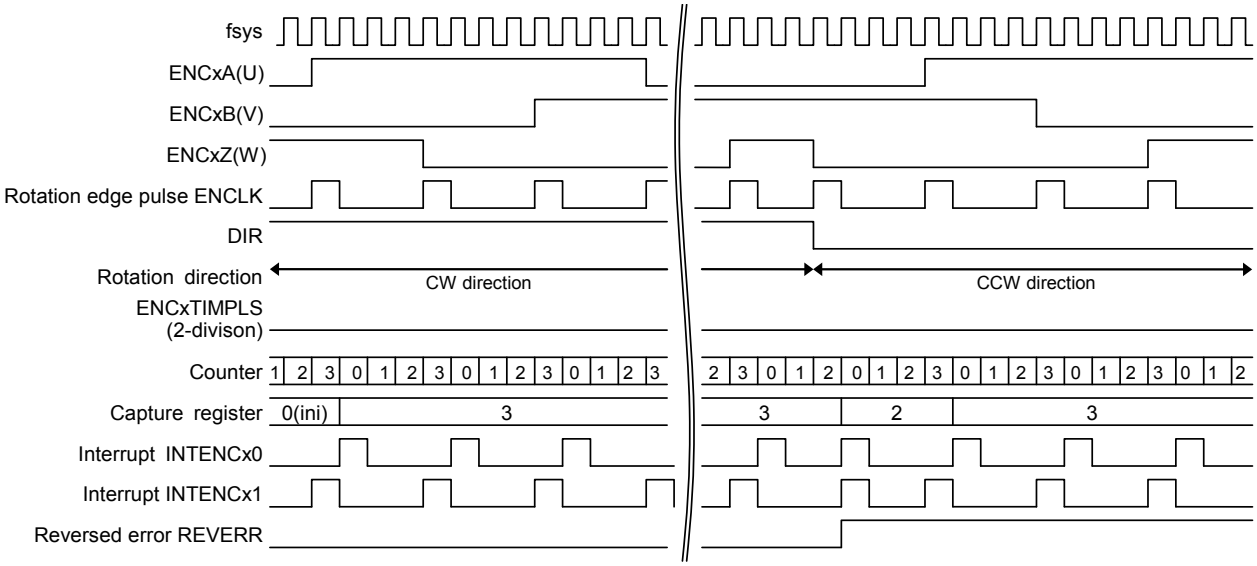

Figure 3.5 3-phase decode (*[ENxTNCR]*<P3EN>=1)

(2) 2-phase decode (***[ENxTNCR]***<P3EN>=0)
In the case of ***[ENxINT]***=0x00000002;

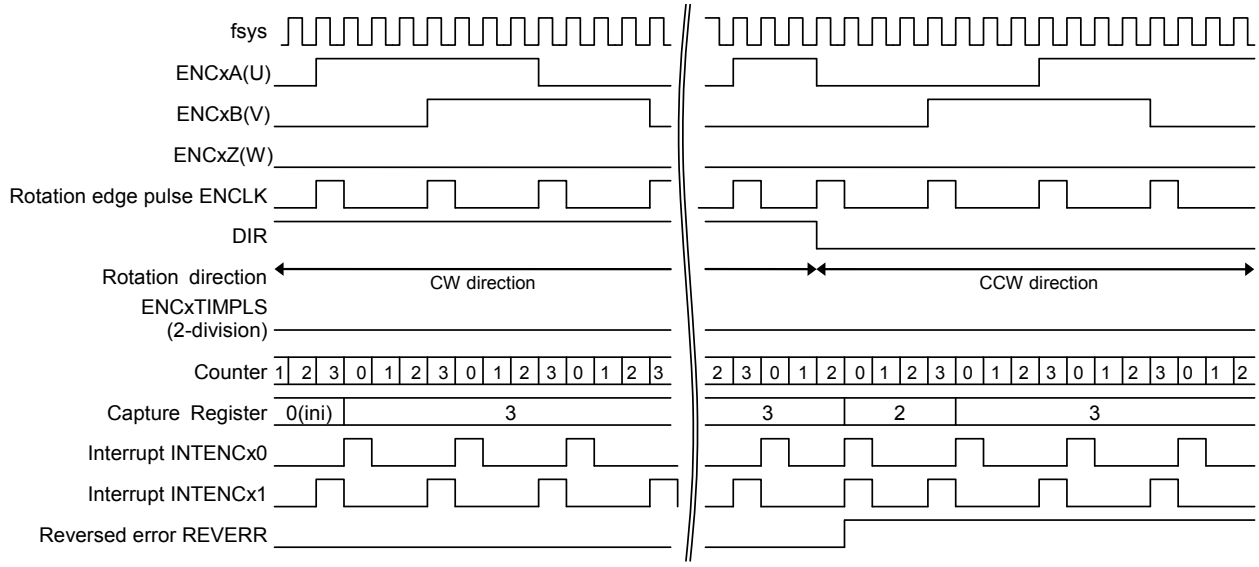

Figure 3.6 2-phase decode (*[ENxTNCR]*<P3EN>=0)

The hall sensor inputs (U, V, and W) are connected to ENCxA, ENCxB, and ENCxZ, respectively. When <P3EN>=0, the frequency of 2-phase inputs (ENCxA and ENCxB) are multiplied by 4, and when <P3EN>=1, the frequency of 3-phase inputs (ENCxA, ENCxB, and ENCxZ) are multiplied by 6. Then, the rotation edge pulses (ENCLK) are generated.

The counter always increments. It is cleared to "0" by ENCLK. When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0".

The counter value is captured by ENCLK. The captured value can be read through ***[ENxCNT]*** register.

When ***[ENxTNCR]***<SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing. The captured value can be read through ***[ENxCNT]*** register.

The value in ***[ENxCNT]*** register (the captured value) is kept regardless of the value of ***[ENxTNCR]***<ENRUN>.

When the rotation direction is detected as CW, ***[ENxSTS]***<UD> is set to "1", and detected as CCW, set to "0". <UD> is cleared to "0" when <ENRUN>=0. When the rotation direction changes, ***[ENxSTS]***<REVERR>=1 is set. The flag is cleared by reading itself.

[ENxTNCR]<DECMD> can set the rotation direction to CW only or CCW only. When <DECMD> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

When ***[ENxINTCR]***<RLDIE>=1 and the counter value becomes ***[ENxRELOAD]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<CMPIE>=1 and the counter value becomes ***[ENxINT]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<MCMPIE>=1 and the counter value becomes ***[ENxMCMP]*** value, INTENCx1 interrupt can be generated. When ***[ENxTNCR]***<MCMPMD>=1 is set and the counter value becomes ***[ENxMCMP]*** value or more, INTENCx1 interrupt can be generated.

3.2.2.3. Phase Count

(1) 3-phase decode (***[ENxTNCR]***<P3EN>=1)

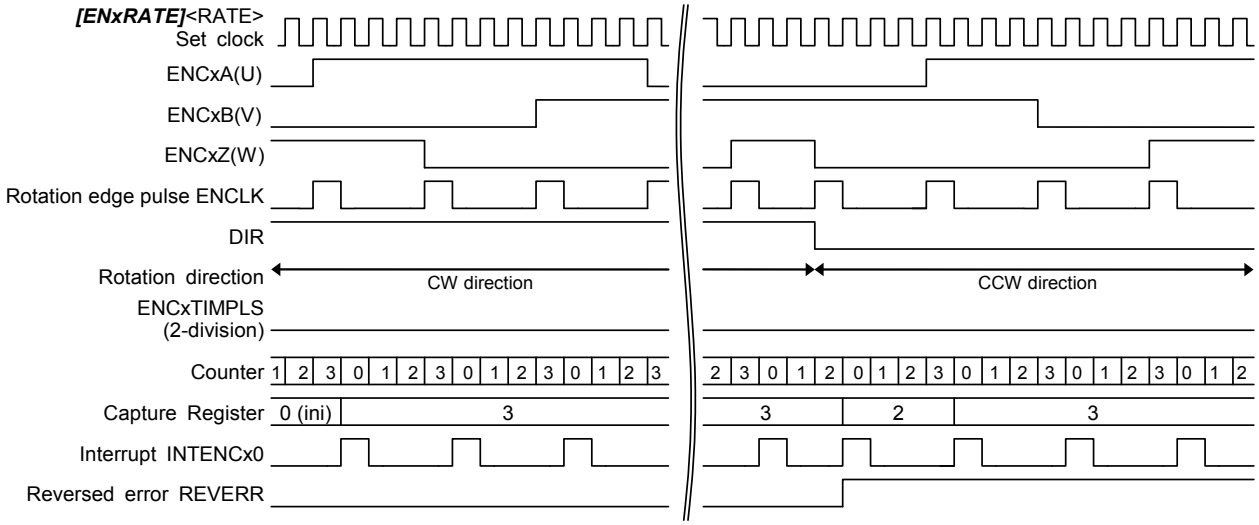

Figure 3.7 3-phase decode (*[ENxTNCR]*<P3EN>=1)

(2) 2-phase decode (***[ENxTNCR]***<P3EN>=0)

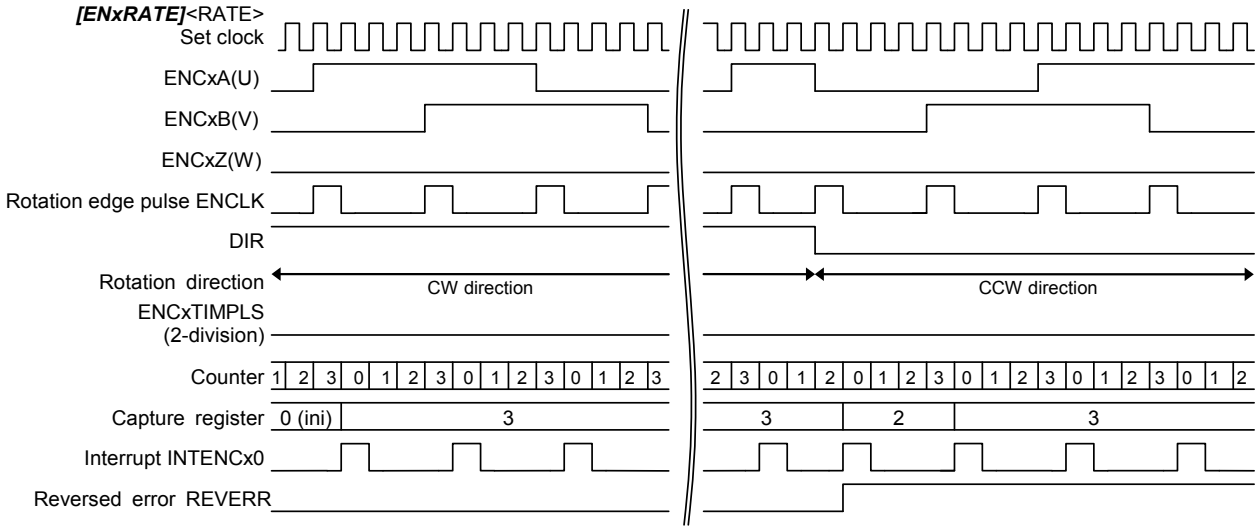

Figure 3.8 2-phase decode (*[ENxTNCR]*<P3EN>=0)

The hall sensor inputs (U, V, and W) are connected to ENCxA, ENCxB, and ENCxZ, respectively. When <P3EN>=0, the frequency of 2-phase inputs (ENCxA and ENCxB) are multiplied by 4, and when <P3EN>=1, the frequency of 3-phase inputs (ENCxA, ENCxB, and ENCxZ) are multiplied by 6. Then, the rotation edge pulses (ENCLK) are generated.

Using <UDMD> setting and ***[ENxRATE]*** register setting, the up-count of the counter or the down-count is controlled. The counter operates with any frequency. At up-count, when the counter value becomes ***[ENxRELOAD]*** value, the counter is cleared to "0". At down-count, when the counter value becomes

"0x00000000", the counter value is set to ***[ENxRELOAD]*** value.

When <ENCLR> is set to "1", the counter is cleared to "0x00000000".

When <TOVMD>=1 is set, the counter stops at the value in ***[ENxRELOAD]***.

The counter value is captured by ENCLK. The captured value can be read through ***[ENxCNT]*** register.

When <SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing. The captured value can be read through ***[ENxCNT]*** register.

The value in ***[ENxCNT]*** register (the captured value) is kept regardless of the value of <ENRUN>.

When the rotation direction is detected as CW, <UD> is set to "1", and detected as CCW, set to "0". <UD> is cleared to "0" when <ENRUN>=0.
When the rotation direction changes, <REVERR>=1 is set. The flag is cleared by reading itself.

[ENxTNCR]<DECMD> can set the rotation direction to CW only or CCW only. When <DECMD> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

When ***[ENxINTCR]***<CMPIE>=1 and the counter value becomes ***[ENxINT]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<MCMPIE>=1 and the counter value becomes ***[ENxMCMP]*** value, INTENCx1 interrupt can be generated.

3.2.3. Timer Mode

This circuit can be used as a general purpose 32-bit timer.

- 32-bit up-counter (fsys clock for counting)
- Counter clear control (Software clear, Comparison match clear, and External trigger)
- A match interrupt is generated by the comparison function.
- Capture function: External trigger capture (an interrupt generation available), and Software capture

(1) ENCxZ input is valid (***[ENxTNCR]***<ZEN>=1).
[ENxINT]=0x00000006

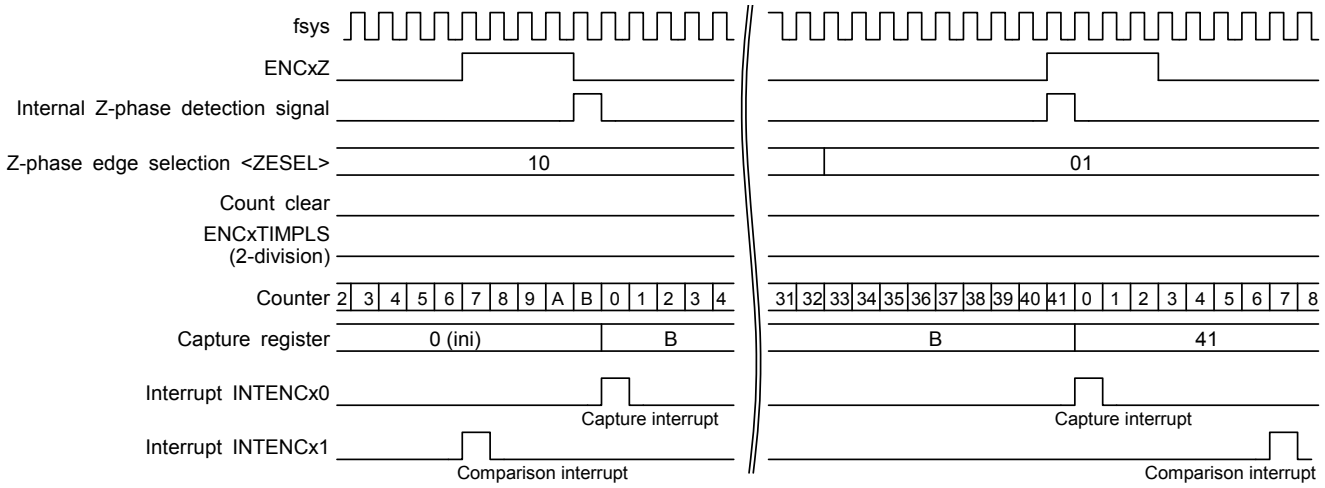

Figure 3.9 ENCxZ input is valid (*[ENxTNCR]*<ZEN>=1).

(2) ENCxZ input is invalid (***[ENxTNCR]***<ZEN>=0).
[ENxINT]=0x00000006

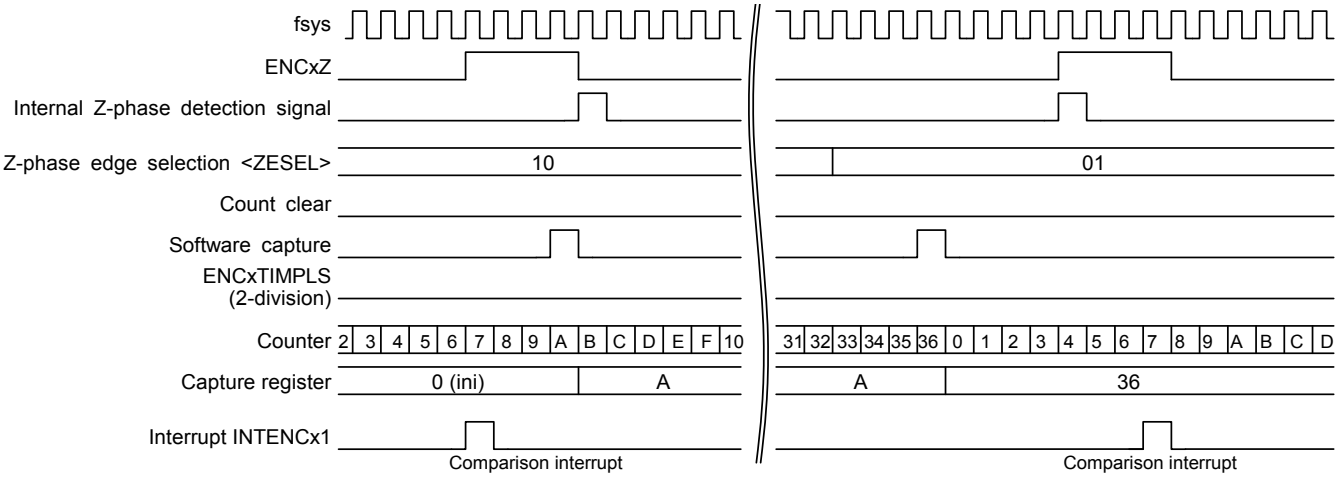

Figure 3.10 ENCxZ input is invalid (*[ENxTNCR]*<ZEN>=0).

When <ZEN>=1, ENCxZ input is used as an external trigger. When <ZEN>=0, no external triggers are used. The counter always increments.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0".

When <ZEN>=1 and ***[ENxTNCR]***<ZESEL>=01, the counter is cleared to "0" by ENCxZ rising edge. And when <ZESEL>=10, it cleared by ENCxZ falling edge, and, when <ZESEL>=11, cleared by both edges.

The counter value is captured by the edge detection of ENCxZ. The captured value can be read through ***[ENxCNT]*** register.

When ***[ENxTNCR]***<SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing. The captured value can be read through ***[ENxCNT]*** register.

The value in ***[ENxCNT]*** register (the captured value) is kept regardless of the value of ***[ENxTNCR]***<ENRUN>. The capture value is cleared only by the reset.

When ***[ENxINTCR]***<RLDIE>=1 and the counter value becomes ***[ENxRELOAD]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<CMPIE>=1 and the counter value becomes ***[ENxINT]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<MCMPIE>=1 and the counter value becomes ***[ENxMCMP]*** value, INTENCx1 interrupt can be generated.

When ***[ENxTNCR]***<MCMPMD>=1 is set and the counter value becomes ***[ENxMCMP]*** value or more, INTENCx1 interrupt can be generated.

3.2.4. Phase Counter Mode

3.2.4.1. Phase Measurement

The counter is 32-bit one which is controlled by any frequency clock.

- Up- and down-count are available.
- Comparison function is available and a match interrupt can be generated.
- ENCxZ input can capture the counter value, clear the counter, and generate an interrupt.

(1) ENCxZ input is valid (***[ENxTNCR]***<ZEN>=1).
[ENxINT]=0x00000006

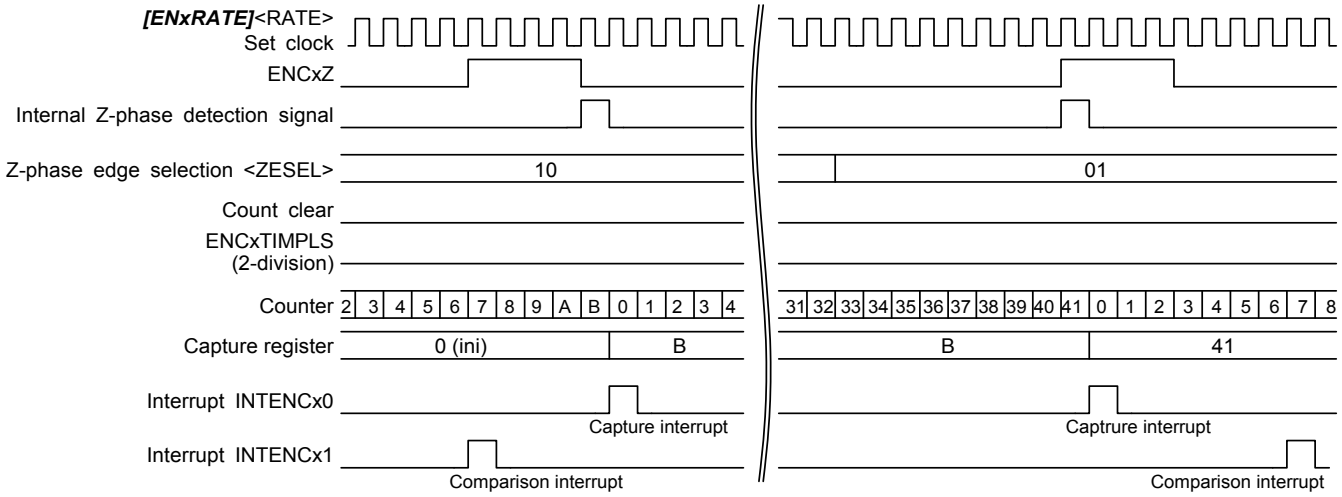

Figure 3.11 ENCxZ input is valid (*[ENxTNCR]*<ZEN>=1).

(2) ENCxZ input is invalid (***[ENxTNCR]***<ZEN>=0).
[ENxINT]=0x00000006

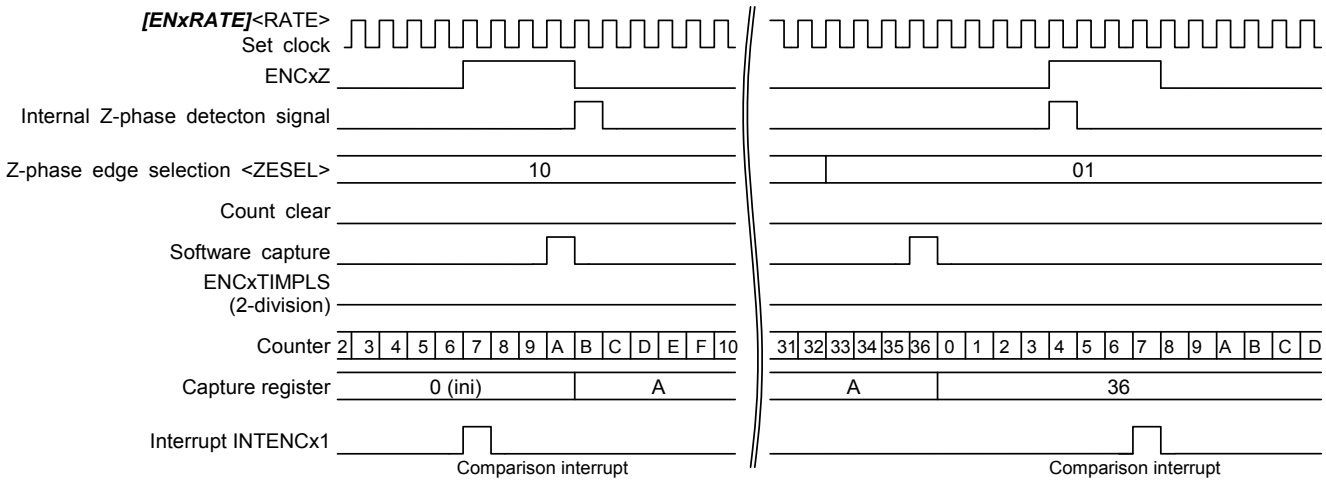

Figure 3.12 ENCxZ input is invalid (*[ENxTNCR]*<ZEN>=0).

When <ZEN>=1, ENCxZ input is used as an external trigger. When <ZEN>=0, no external triggers are used.
Using ***[ENxTNCR]***<UDMD> setting and ***[ENxRATE]*** register setting, the up-count and the down-count of the counter are controlled with any frequency clock.

At up-count, when the counter value becomes ***[ENxRELOAD]*** value, the counter is cleared to "0".

At down-count, when the counter value becomes "0x00000000", the counter value is set to ***[ENxRELOAD]*** value.

When ***[ENxTNCR]***<TOVMD>=1 is set, the counter stops at the value in ***[ENxRELOAD]***.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0".

When <ZEN>=1 and ***[ENxTNCR]***<ZESEL>=01, the counter is cleared to "0" by ENCxZ rising edge. And when <ZESEL>=10, it cleared by ENCxZ falling edge, and, when <ZESEL>=11, cleared by both edges.

The counter value is captured by the edge detection of ENCxZ. The captured value can be read through ***[ENxCNT]*** register.

When ***[ENxTNCR]***<SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing. The captured value can be read through ***[ENxCNT]*** register.

The value in ***[ENxCNT]*** register (the captured value) is kept regardless of the value of ***[ENxTNCR]***<ENRUN>. The capture value is cleared only by the reset.

When ***[ENxINTCR]***<CMPIE>=1 and the counter value becomes ***[ENxINT]*** value, INTENCx1 interrupt can be generated.

When ***[ENxINTCR]***<MCMPIE>=1 and the counter value becomes ***[ENxMCMP]*** value, INTENCx1 interrupt can be generated.

3.2.4.2. Phase Difference Measurement

The phase difference can be measured in the phase counter mode with setting <P3EN>=<ZEN>=1.

The up- and down-counter is controlled by the output of the general purpose timer (ENCxPSGI) and ENCxZ input.

・When the output of the general purpose timer and the value of ENCxZ input are the same, up-count is done. When they are different, down-count is done.

・The output edge of the general timer can capture the counter value, clear the counter, and generate an interrupt.

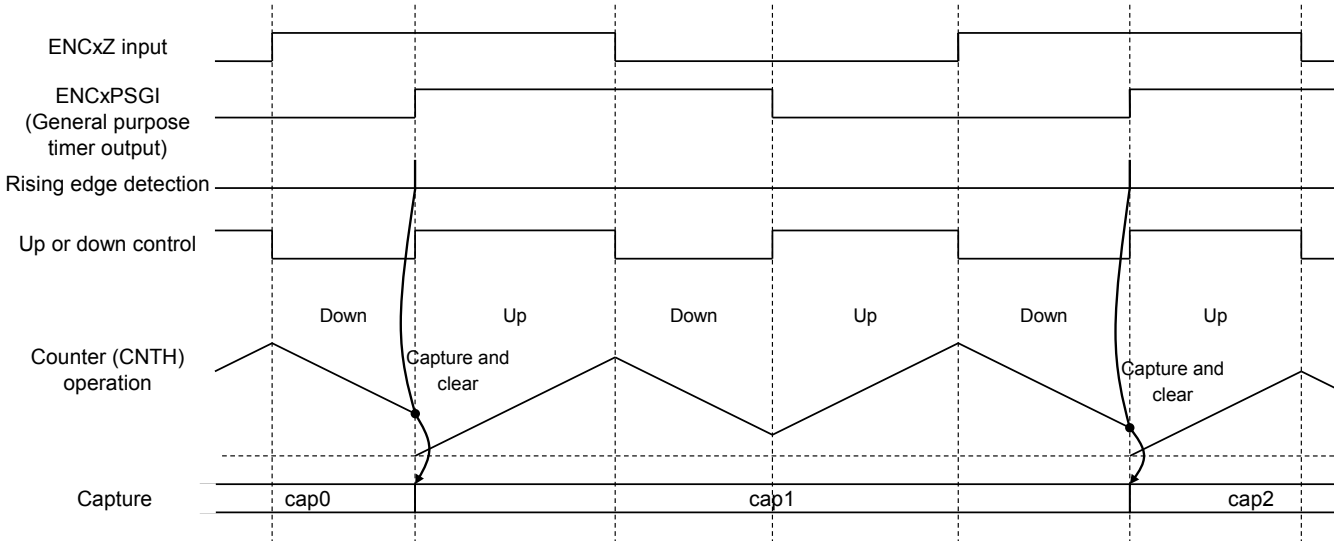

Figure 3.13 Operation of Phase counter mode (Phase difference)

The output edge of the general purpose timer (ENCxPSGI) is detected, then the counter value is captured and the counter is cleared. The detection edge should be selected by ***[ENxTNCR]***<ZESEL>. When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0".

The captured value represents the phase difference between ENCxZ input and the output of the general purpose timer (ENCxPSGI). The origin (the captured value is "0") of the phase difference between them is 1/4 cycles.

3.3. Function Outline of Each Circuit

3.3.1. Input Circuit

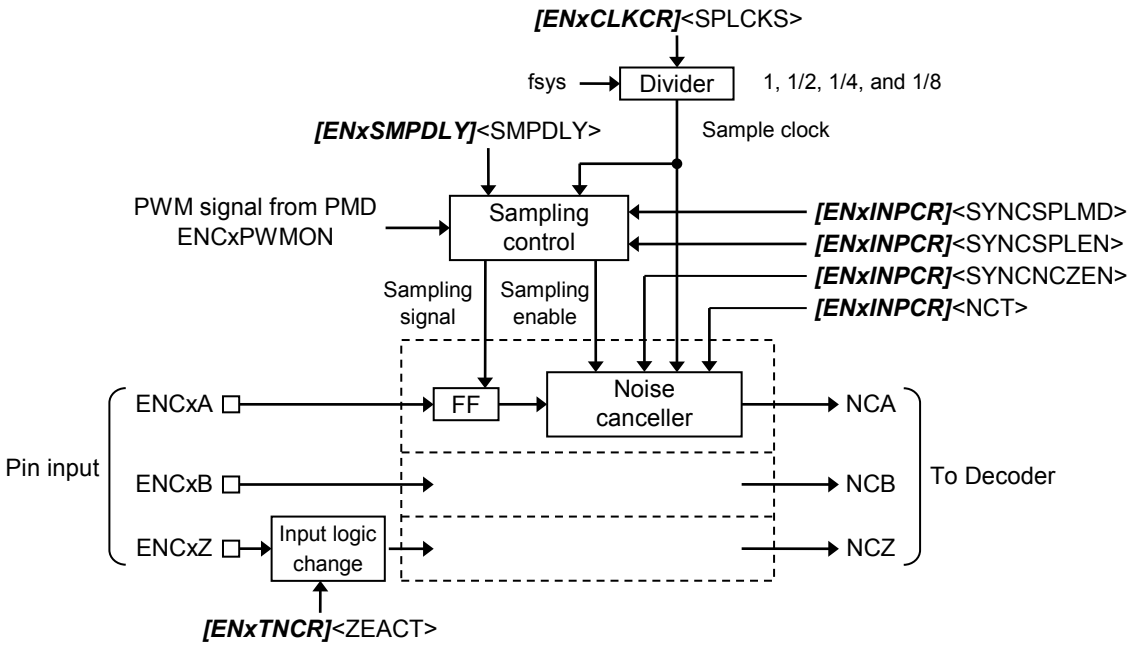

Figure 3.14 Input circuit configuration

The pin inputs (ENCxA, ENCxB, and ENCxZ) are sampled by a suitable sampling signal, and noises are reduced by the digital noise filter in the input circuit.

The input logic change circuit of ENCxZ pin input is valid only in the encoder mode (***[ENxTNCR]*** <MODE>=000).

3.3.1.1. Sample Clock

The sample clock can be selected from among fsys, fsys/2, fsys/4, and fsys/8 by ***[ENxCLKCR]***<SPLCKS>.

3.3.1.2. Sampling Mode

(1) Continuous sampling (***[ENxINPCR]***<SYNCSPLEN>=0)
The input signals are sampled by the sampling clock which is selected by ***[ENxCLKCR]***<SPLCKS>.

(2) PWM synchronous sampling (***[ENxINPCR]***<SYNCSPLEN>=1)
The sampling is done at the timing synchronous with PWM signal (ENCxPWMON) from PMD.

- PWM-On interval sampling (***[ENxINPCR]***<SYNCSPLMD>=0)
  Only in the interval when PWM signal is On, the sampling is done by the clock selected by ***[ENxCLKCR]***<SPLCKS>.
  An On-delay time can be set by ***[ENxSMPDLY]***<SMPDLY> in PWM-On interval sampling.

  Delay time: <SMPDLY> × Sample clock cycle

  Note: After ENC is enabled (after changing ***[ENxTNCR]***<ENRUN> from "0" to "1"), the first delay time may be different from the <SMPDLY> setting value.

- PWM-Off edge sampling (***[ENxINPCR]***<SYNCSPLMD>=1)
  The sampling signal is ENCxPWMON. The sampling is done at the Off edge of ENCxPWMON.

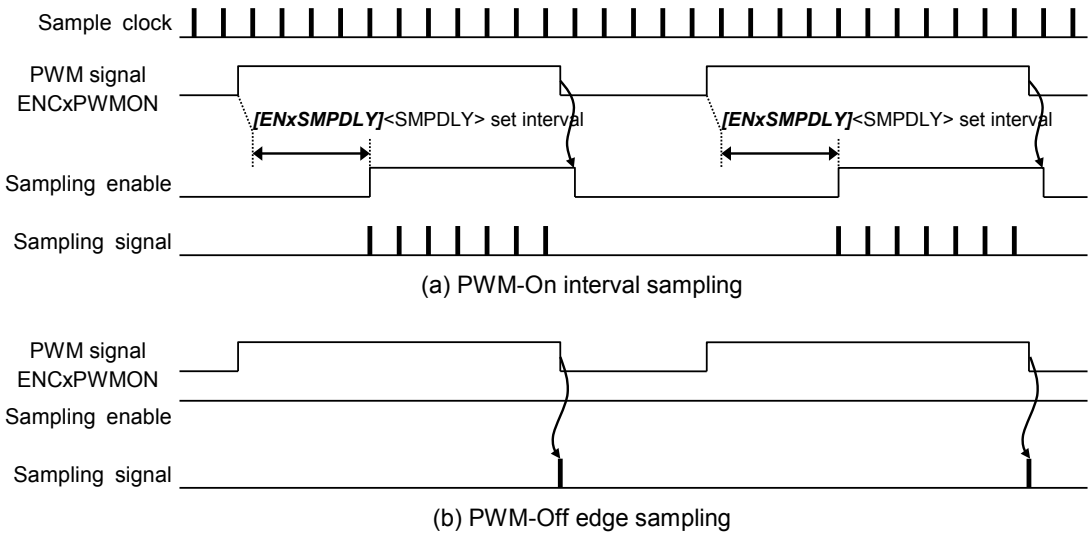

Figure 3.15 PWM synchronous sampling

3.3.1.3. Noise Cancellation

(1) Continuous sampling (***[ENxINPCR]***<SYNCSPLEN>=0)

The noise cancellation time should be set to ***[ENxINPCR]***<NCT>. The real noise cancellation time is calculated by the following formula.

Noise cancellation time: <NCT> × Sample clock cycle

Note: When <NCT> is set to "0", the noise cancellation is invalid.

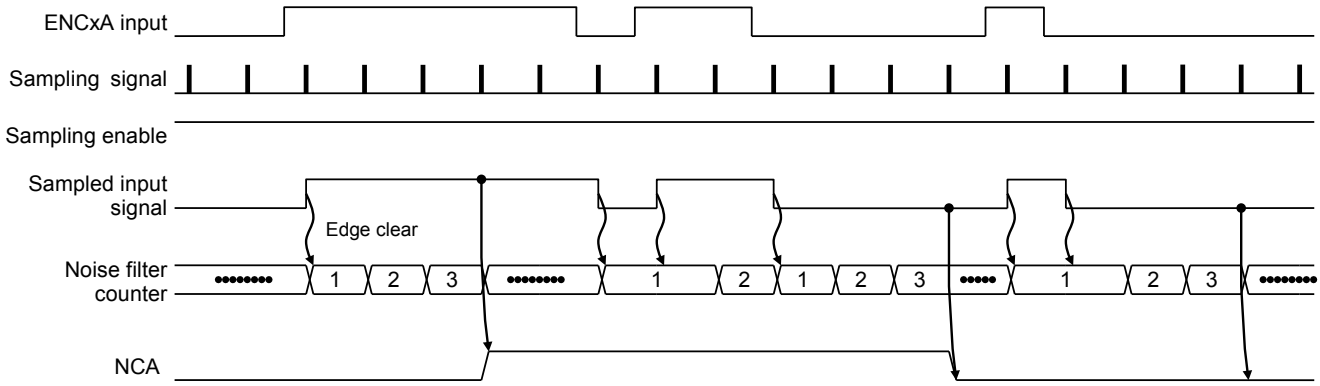

Figure 3.16 Noise cancellation (Continuous sampling: <NCT>=3)

(2) PWM-On interval sampling (***[ENxINPCR]***<SYNCSPLEN>=1)

- The noise cancellation timer stops during "Low" interval of the sampling enable signal (***[ENxINPCR]***<SYNCNCZEN>=0).
- The noise cancellation timer is cleared during "Low" interval of the sampling enable signal (***[ENxINPCR]***<SYNCNCZEN>=1).

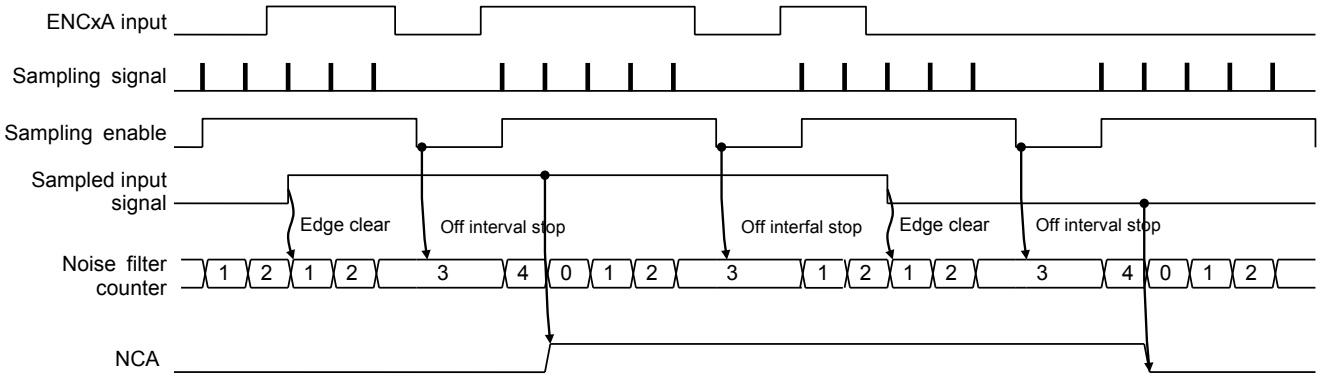

Figure 3.17 Noise cancellation (PWM-On interval sampling and PWM-Off interval stop: <NCT>=4)

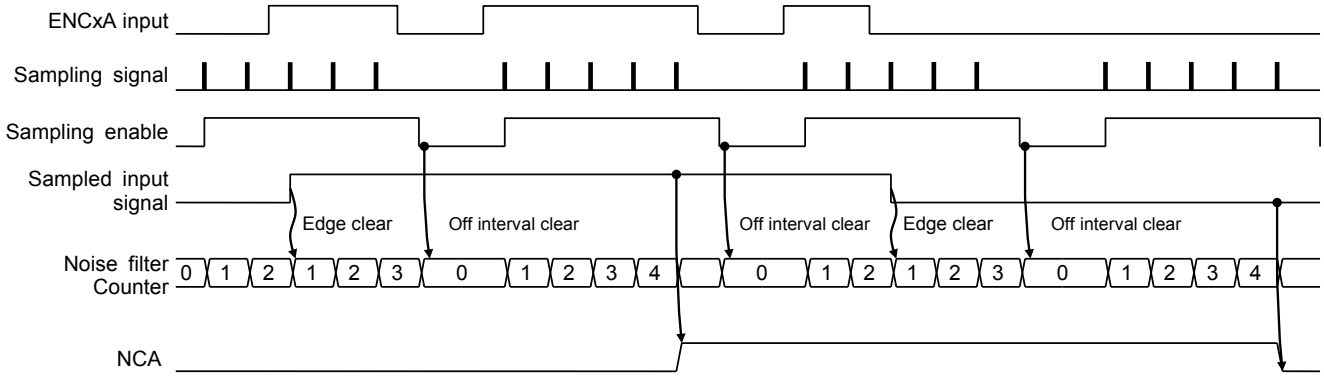

Figure 3.18 Noise cancellation (PWM-On interval sampling and PWM-Off interval clear: <NCT>=4)

3.3.2. Decoder

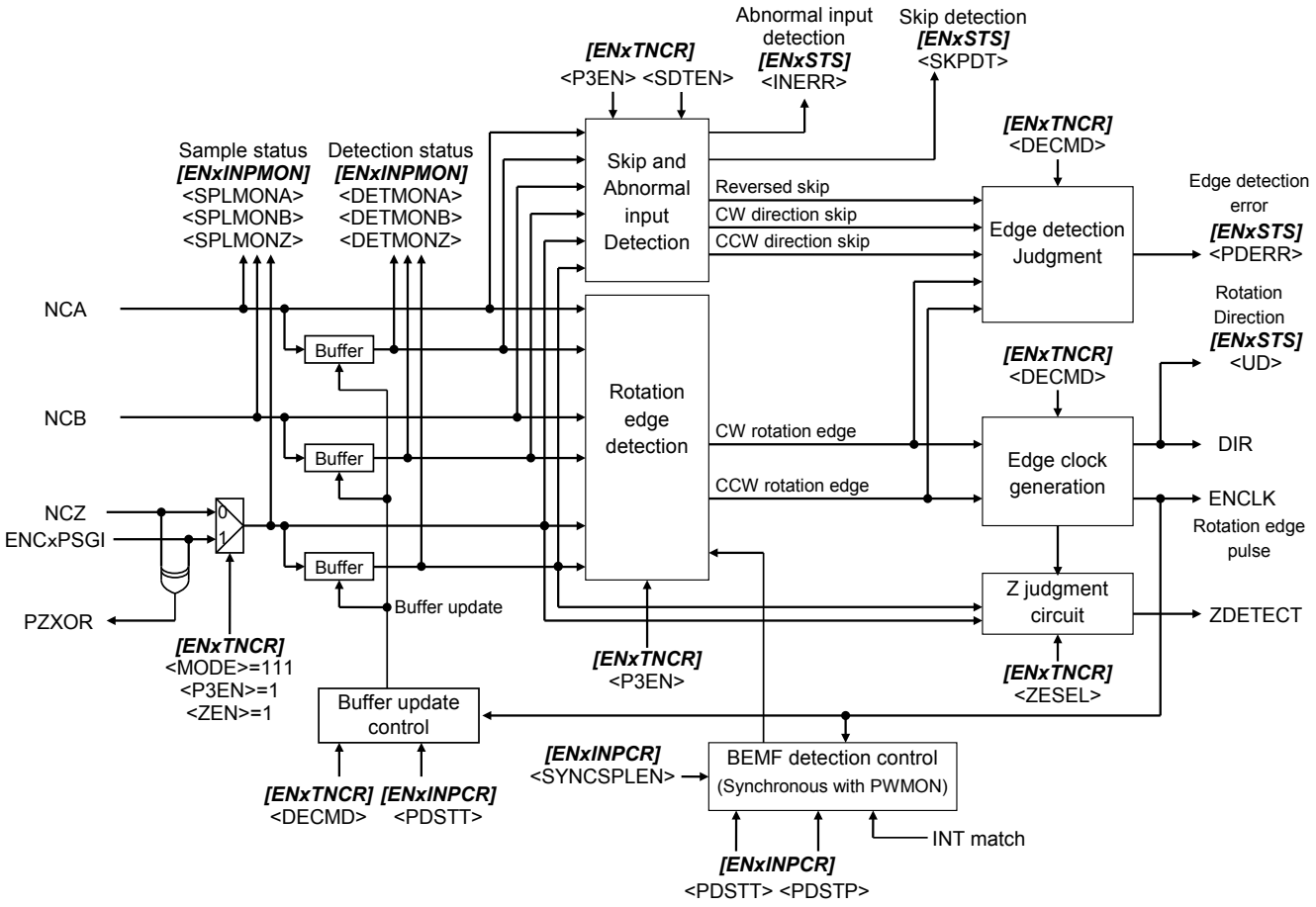

Figure 3.19 Decoder circuit

The decoder detects the rotation edge and judges the rotation direction using the noise-canceled 2-phase or 3-phase input signals. It also detects ENCxZ in the encoder mode, and the edge of ENCxZ signal in the timer mode and the phase counter mode.

3.3.2.1. Rotation Edge Detection and Direction Signal Generation

(1) 2-phase decode (***[ENxTNCR]***<P3EN>=0)

The encoder mode and the sensor mode (2-phase input) are supported.

A change of input patterns (a rotation edge) among 4 patterns is detected in 2-phase decode.

CW direction input: The rotation edges of (1)→(2), (2)→(3), (3)→(4), and (4)→(1) are detected. Then ***[ENxSTS]***<UD> is set to "1".

CCW direction input: The rotation edges of (4)→(3), (3)→(2), (2)→(1), and (1)→(4) are detected. Then ***[ENxSTS]***<UD> is set to "0".

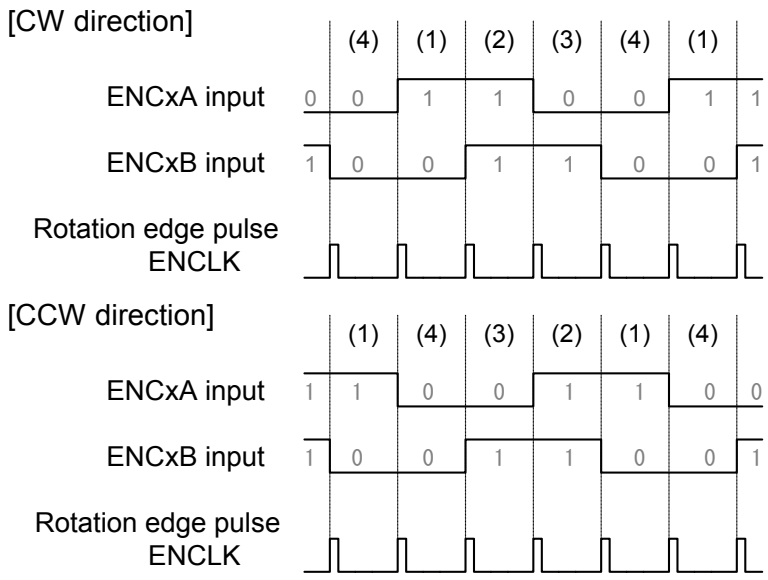

Figure 3.20 2-phase decoder waveform

(2) 3-phase decode (***[ENxTNCR]***<P3EN>=1)

The sensor mode (3-phase input) is supported.

A change of input patterns (a rotation edge) among 6 patterns is detected in 3-phase decode.

CW direction input: The rotation edges of (1)→(2), (2)→(3), (3)→(4), (4)→(5), (5)→(6), and (6)→(1) are detected. Then ***[ENxSTS]***<UD> is set to "1".

CCW direction input: The rotation edges of (6)→(5), (5)→(4), (4)→(3), (3)→(2), (2)→(1), and (1)→(6) are detected. Then ***[ENxSTS]***<UD> is set to "0".

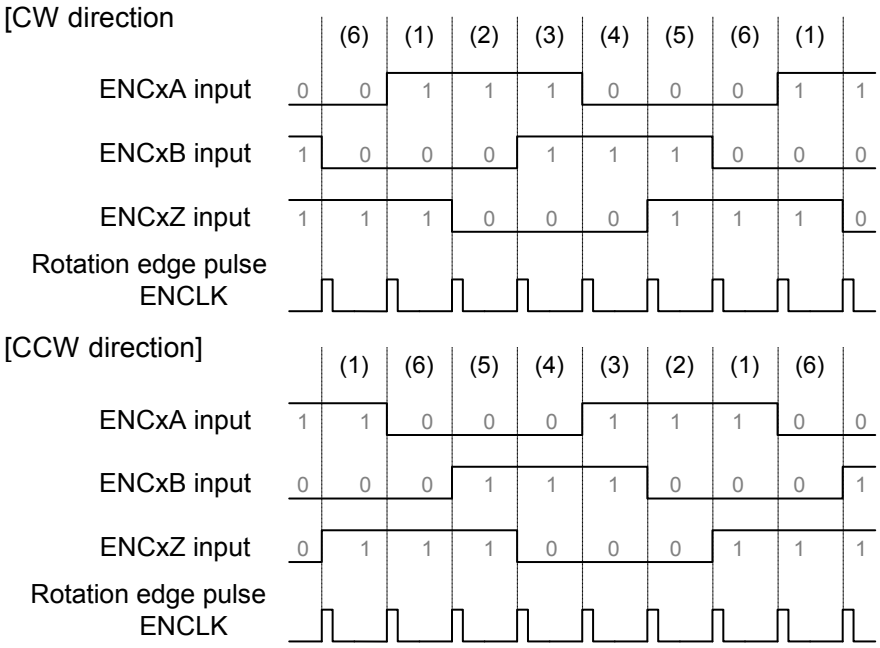

Figure 3.21 3-phase decoder waveform

3.3.2.2. Z Judgment Circuit

This circuit detects the edge of ENCxZ input signal.

- Encoder mode

  A rising edge is detected when ENCxA/ENCxB input is CW direction, and a falling edge is detected when the input is CCW direction.

  The input logic of the ENCxZ input can be selected with ***[ENxTNCR]***<ZACT>.

- Timer mode and Phase counter mode

  The rising edge detection, the falling edge detection, and both edge detection can be selected by ***[ENxTNCR]***<ZESEL>.

3.3.2.3. Skip Judgment and Abnormal Input Judgment

(1) Skip judgment

This function is valid when ***[ENxTNCR]***<SDTEN>=1.
When a skip is detected, <SKPDT> is set to "1".

- Skip detection in 2-phase decode (***[ENxTNCR]***<P3EN>=0)

Reversed skip detection: (1)→(3), (2)→(4), (3)→(1), and (4)→(2)

- Skip detection in 3-phase decode (***[ENxTNCR]***<P3EN>=1)

CW direction skip detection: (1)→(3), (2)→(4), (3)→(5), (4)→(6), (5)→(1), and (6)→(2)
CCW direction skip detection: (1)→(5), (2)→(6), (3)→(1), (4)→(2), (5)→(3), and (6)→(4)
Reversed skip detection: (1)→(4), (4)→(1), (2)→(5), (5)→(2), (3)→(6), and (6)→(3)

(2) Abnormal input judgment

In the sensor mode (the event count, the timer count, or the phase count), when all 3 inputs change to "0" or "1" for 3-phase decode, the detected edges are judged as the abnormal input. Then ***[ENxSTS]***<INERR> is set to "1".

3.3.2.4. Edge Detection Error Judgment

When ***[ENxTNCR]***<DECMD> sets a direction and an unset direction is detected, the detected direction is judged as an error. The error judgment can generate an interrupt.

- Skip detection disable (***[ENxTNCR]***<SDTEN>=0)

CW rotation edge detection (***[ENxTNCR]***<DECMD>=01): CCW rotation edge is an error.
CCW rotation edge detection (***[ENxTNCR]***<DECMD>=10): CW rotation edge is an error.

- Skip detection enable (***[ENxTNCR]***<SDTEN>=1)

CW rotation edge detection (***[ENxTNCR]***<DECMD>=01): CCW direction skip, Reversed skip, and CCW rotation edge are errors.
CCW rotation edge detection (***[ENxTNCR]***<DECMD>=10): CW direction skip, Reversed skip, and CW rotation edge are errors.

3.3.2.5. Buffer Update Control

When the selection of the decoder detection direction (***[ENxTNCR]***<DECMD>) is set to "00", the buffer is always valid. The rotation edge judgment and the skip judgment are done by the change of the input signals.

When <DECMD> is not "00", the buffer is updated only at the rotation edge detection. So, the edge judgment and the skip judgment are done by using the data at the previous rotation edge detection in the buffer (***[ENxINPMON]*** <DETMONA>, <DETMONB>, and <DETMONZ>) and the current input data (***[ENxINPMON]***<SPLMONA>, <SPLMONB>, and <SPLMONZ>).

3.3.2.6. BEMF Detection Control

In the sensor mode (the timer count and the phase count), this circuit is valid when PWM synchronous sampling is enabled (***[ENxINPCR]***<SYNCSPLEN>=1). Then the rotation edge detection can be stopped (suspended) and started (re-started).

This control is used when the position detection (the position sensor-less control) is done using the induced voltage of BLDC motor (BEMF) which is driven with the pulse wave of a motor control circuit (PMD).

(1) Rotation edge detection start

- Command operation: ***[ENxINPCR]***<PDSTT> should be set to "1".
- Event operation: At match of INT comparison by a counter circuit

(2) Rotation edge detection stop

- Command operation: ***[ENxINPCR]***<PDSTP> should be set to "1".
- Event operation: At the rotation edge detection

3.3.3. Counter

The counter circuit consists of a clock generator, a counter, a comparison function, a capture function, and others. The used internal circuits depend on an operation mode.

3.3.3.1. Encoder Mode and Sensor Mode (Event Count)

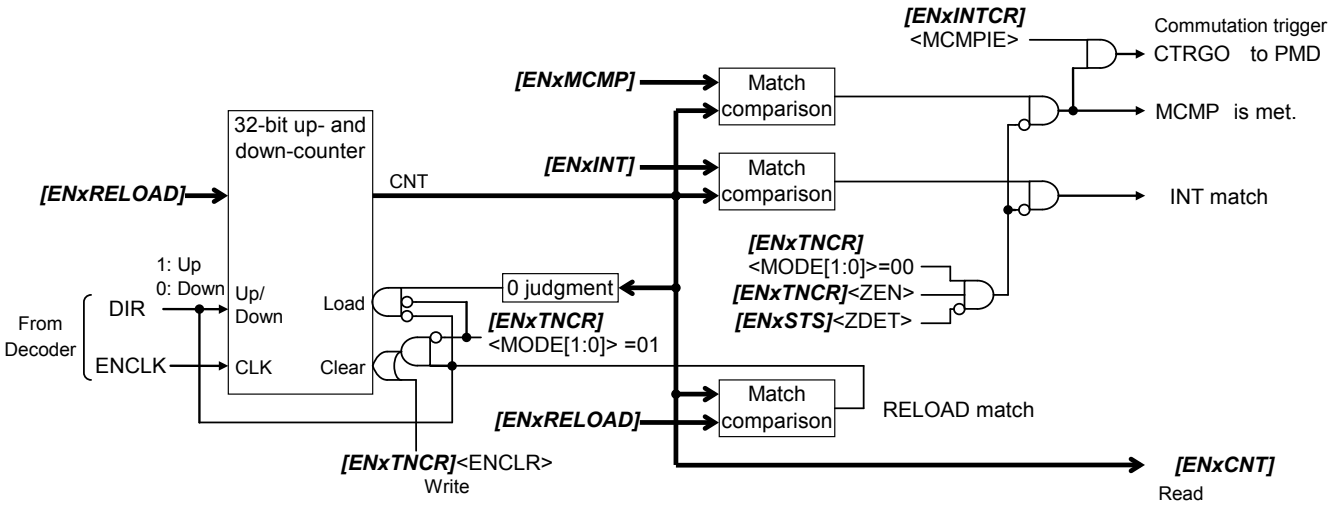

Figure 3.22 Counter circuit (Encoder mode and Sensor mode (Event count))

This circuit consists of 32-bit up- and down-counter which is driven by the rotation edge pulse (ENCLK) and the rotation direction signal (DIR) from the decoder, and 3 comparison functions (***[ENxRELOAD]***, ***[ENxINT]***, and ***[ENxMCMP]***).

In the encoder mode, the counter is cleared at the match with ***[ENxRELOAD]*** at CW rotation. And ***[ENxRELOAD]*** value is loaded to the counter when the counter value becomes "0" at CCW rotation.

In the encoder mode, when Z detection enable (***[ENxTNCR]***<ZEN>=1) is set, the matches with ***[ENxINT]*** and ***[ENxMCMP]*** are ignored till the first ENCxZ edge detection after the encoder input enable (***[ENxTNCR]***<ENRUN>=1) is set.

The up- and down-counter value can be acquired by reading the counter register (***[ENxCNT]***).

When ***[ENxINTCR]***<MCMPIE>=1 is set, MCMP comparison match signal can be used as the commutation trigger for PMD circuit.

3.3.3.2. Sensor Mode (Timer Count) and Timer Mode

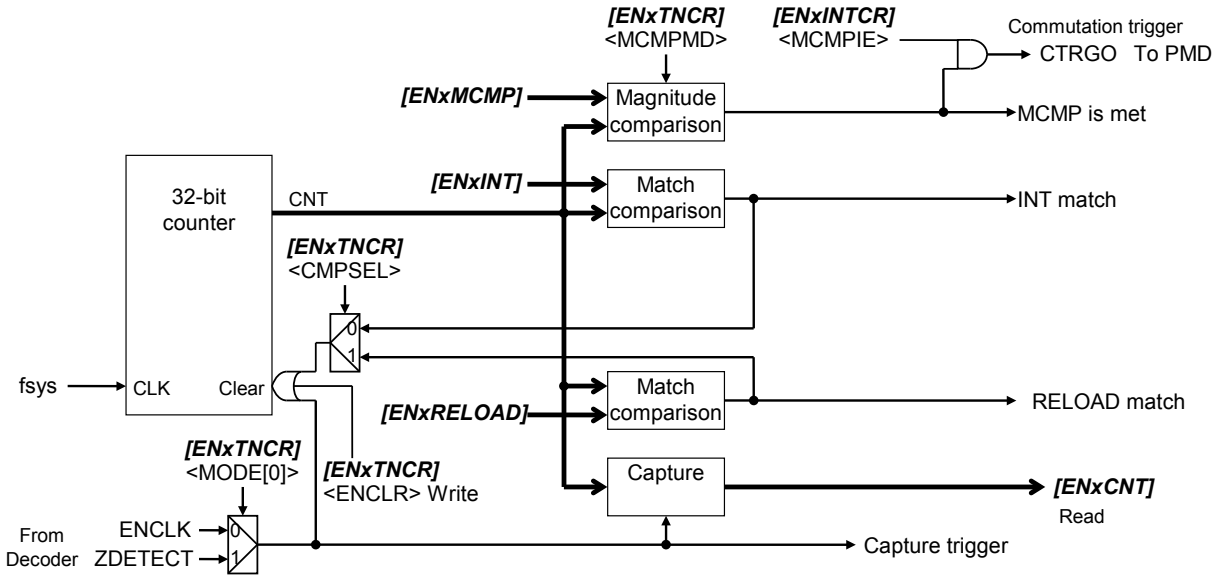

Figure 3.23 Counter configuration (Sensor mode (Timer count) and Timer mode)

This circuit consists of a 32-bit counter operating with the system clock (fsys), 3 comparison function circuits (***[ENxRELOAD]***, ***[ENxINT]***, and ***[ENxMCMP]***), and a capture function circuit.

A match comparison and a magnitude comparison can be selected in MCMP comparison function. In the magnitude comparison (***[ENxTNCR]***<MCMPMD>=1), the comparison starts at the setting of ***[ENxMCMP]*** register and finishes when the condition is met and the MCMP met signal is generated.

In the timer mode, INT comparison or RELOAD comparison can clear the counter.

In the sensor mode (Timer count), the rotation edge detection (ENCLK) captures the counter value and clears the counter. In the timer mode, Z edge detection (ZDETECT) can capture the counter value and clear the counter. The captured value can be acquired by reading the counter register (***[ENxCNT]***).

When ***[ENxINTCR]***<MCMPIE>=1 is set, MCMP comparison match signal can be used as the commutation trigger for PMD circuit.

3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode

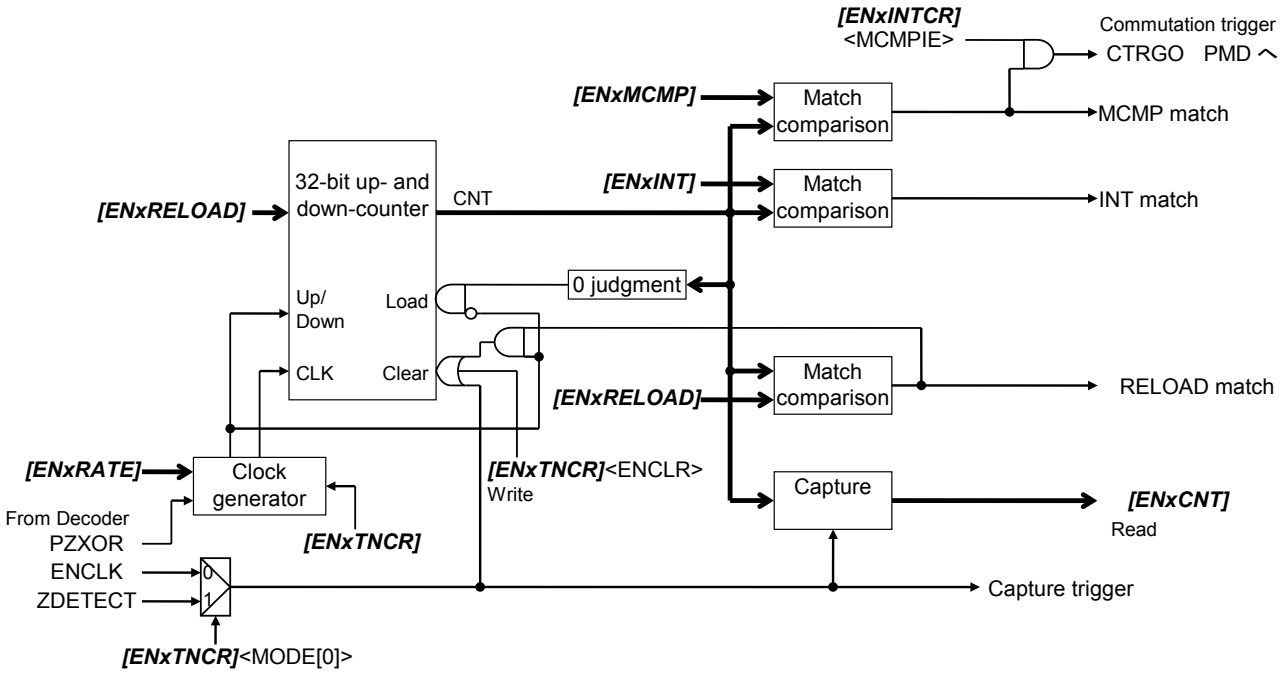

Figure 3.24 Counter configuration (Sensor mode (Phase count) and Phase counter mode)

This circuit consists of a clock generator which generates the counter clock controlled by ***[ENxRATE]*** setting, a 16-bit up- and down-counter which operates with the clock signal and the direction signal from the clock generator, 3 match comparators (***[ENxRELOAD]***, ***[ENxINT]***, and ***[ENxMCMP]***), and a capture function circuit.

The counter clock settings are done in ***[ENxRATE]*** register.

The settings of the up- and down-counter are done in ***[ENxTNCR]***<UDMD>. In the phase counter mode (Phase difference measurement) (***[ENxTNCR]***<MODE>=111, <ZEN>=1, and <P3EN>=1), PZXOR signal controls the up- and down-counter.

When the up-count is set, RELOAD comparison match clears the counter, and when the down-count is set, "0" match loads the ***[ENxRELOAD]*** value to the counter.

In the sensor mode (Phase count), the rotation edge detection (ENCLK) captures the counter value and clears the counter. In the phase counter mode, Z edge detection (ZDETECT) can capture the counter value and clear the counter. The captured value can be acquired by reading the counter register (***[ENxCNT]***).

When ***[ENxINTCR]***<MCMPIE>=1 is set, MCMP comparison match signal can be used as the commutation trigger for PMD circuit.

3.3.4. Interrupt Control

There are 6 interrupt factors and 2 interrupt outputs. The output of the interrupt of each factor is enabled by Interrupt control register (***[ENxINTCR]***) individually. The factor generating the current interrupt can be checked in Interrupt flag register (***[ENxINTF]***).

A bit in Interrupt flag register (***[ENxINTF]***) is set by occurrence of the corresponding interrupt factor, and cleared by reading its register.

Table 3.2 List of the interrupt factors

Interrupt factor	Description	Mode	Interrupt enable *[ENxINTCR]*	Factor flag *[ENxINTF]*	Interrupt output
Division pulse	The frequency of the rotation edge pulse is divided by 1 to 128 according to ***[ENxTNCR]***<ENDEV> setting. And the result pulse generation is notified.	Encoder mode Sensor mode (Event count)	<TPLSIE>	<TPLSF>	INTENCx0
Capture	This notifies that a capture is done by an external trigger (ENCxZ input).	Timer mode Phase counter mode	<CAPIE>	<CAPF>	INTENCx0
	This notifies that a capture is done by a rotation edge pulse (ENCLK).	Sensor mode (Timer count and Phase count)			
Detection error	This notifies of occurrence of an edge detection error (***[ENxSTS]*** <PDERR>) or a skip detection (***[ENxSTS]***<SKPDT>).	Encoder mode Sensor mode (Event count, Timer count and Phase count)	<ERRIE>	<ERRF>	INTENCx0
INT match	This notifies that the counter value matches ***[ENxINT]*** register value.	All modes	<CMPIE>	<INTCPF>	INTENCx1
RELOAD match	This notifies that the counter value matches ***[ENxRELOAD]*** register value.	Sensor mode (Timer count and Phase count) Timer mode Phase counter mode (Phase difference measurement)	<RLDIE>	<RLDCPF>	INTENCx1
MCMP is met	When ***[ENxTNCR]***<MCMPMD>=0, this notifies that the counter value matches ***[ENxMCMP]*** register value. When <MCMPMD>=1, this notifies the counter value becomes ***[ENxMCMP]*** register value or more.	Sensor mode (Timer count) Timer mode	<MCMPIE>	<MCMPF>	INTENCx1
	This notifies that the counter value matches ***[ENxMCMP]*** register value.	Encoder mode Sensor mode (Event count and Phase count) Phase counter mode			

Table 3.3 List of interrupt factors in each mode

Mode	Interrupt factor
Encoder mode	Division pulse, Detection error, INT match, and MCMP met condition.
Sensor mode (Event count)	Division pulse, Detection error, INT match, and MCMP met condition
Sensor mode (Timer count)	Capture, Detection error, INT match, RELOAD match, and MCMP met condition
Sensor mode (Phase count)	Capture, Detection error, INT match, RELOAD match, and MCMP met condition
Timer mode	Capture, INT match, RELOAD match, and MCMP met condition
Phase counter mode	Capture, INT match, RELOAD match, and MCMP met condition

4. Registers

4.1. List of Registers

The control registers and their addresses are shown in the following tables.

Peripheral function		Channel/Unit	Base address		
			TYPE1	TYPE2	TYPE3
Advanced Encoder Input Circuit (32-bit)	A-ENC32	ch0	0x400F7000	0x400EA000	0x4008A000
		ch1	-	0x400EA400	0x4008A400
		ch2	-	0x400EA800	0x4008A800
		ch3	-	0x400EAC00	0x4008AC00

Note: The channel/unit and base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Address (Base+)
ENC Control Register	***[ENxTNCR]***	0x0000
RELOAD Comparison Register	***[ENxRELOAD]***	0x0004
INT Comparison Register	***[ENxINT]***	0x0008
Counter Register	***[ENxCNT]***	0x000C
MCMP Comparison Register	***[ENxMCMP]***	0x0010
Phase Count Rate Register	***[ENxRATE]***	0x0014
Status Register	***[ENxSTS]***	0x0018
Input Procedure Control Register	***[ENxINPCR]***	0x001C
Sample Delay Register	***[ENxSMPDLY]***	0x0020
Input Monitor Register	***[ENxINPMON]***	0x0024
Sample Clock Control Register	***[ENxCLKCR]***	0x0028
Interrupt Control Register	***[ENxINTCR]***	0x002C
Interrupt Flag Register	***[ENxINTF]***	0x0030

Note: The registers which can be updated in operation are ***[ENxTNCR]***<SFTCAP>, <ENRUN>, and <ENCLR>, and ***[ENxINPCR]***<PDSTP> and <PDSTT>.
The other registers should not be updated in operation.

4.2. Details of Registers

For a special description in an operation mode is shown separately after **[xx mode]** ("xx mode" means the corresponding operation mode).

4.2.1. *[ENxTNCR]* (ENC Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:29	-	0	R	Read as "0".
28	CMPSEL	0	R/W	**[Timer mode]** Counter clear condition 0: ***[ENxINT]*** register match 1: ***[ENxRELOAD]*** register match When <CMPSEL>=<TOVMD>=1, the counter is not cleared. **[Encoder mode, Sensor mode (Phase count), and Phase counter mode]** ***[ENxRELOAD]*** register match at CW rotation, regardless of the setting of this bit **[Sensor mode (Event count and Timer count)]** The counter is not cleared by any comparison matches.
27:26	UDMD[1:0]	00	R/W	**[Sensor mode (Phase count), Phase counter mode (Phase measurement)]** Up-count or Down-count control 00: Up-count 01: Down-count 10, 11: Up- and down-count are controlled by ***[ENxRATE]*** register. When this field is set to "10" or "11", the setting value in ***[ENxRATE]*** becomes 2-complementary. The value in ***[ENxRATE]*** < 0 makes down-count, and ***[ENxRATE]*** ≥ 0, up-count. **[Encoder mode, Sensor mode (Event count) and Phase counter mode (Phase difference measurement)]** Auto judgment is done (refer to "3.3.2.1 Rotation Edge Detection and Direction Signal Generation"). **[Sensor mode (Timer count) and Timer mode]** Up-count is done.

Bit	Bit Symbol	After Reset	Type	Description
25	TOVMD	0	R/W	Operation setting at RELOAD match **[Sensor mode (Timer count)]** 0: Count continues. 1: Count stops. If the counter should be operated from the stop state, the match state should be released by the software clear. **[Timer mode, Sensor mode (Phase count), and Phase counter mode (Phase measurement)]** 0: Counter is cleared and continues the count. 1: Counter stops. If the counter should be operated from the stop state, the match state should be released by the software clear. **[Encoder mode, Sensor mode (Event count) and Phase counter mode (Phase difference measurement)]** This bit can not be used. In Encoder mode, regardless of <TOVMD> setting, CW direction: Counter is cleared and continues the count. CCW direction: Counter continues the count. In Sensor mode (Event count), RELOAD match cannot be used.
24	MCMPMD	0	R/W	**[Sensor mode (Timer count) and Timer mode]** Comparison mode of ***[ENxMCMP]*** register 0: Match comparison (***[ENxMCMP]*** = Counter value) 1: Magnitude comparison (***[ENxMCMP]*** ≤ Counter value) The magnitude comparison is available only for the up-counter. **[Encoder mode, Sensor mode (Event count and Phase count), and Phase counter mode]** The MCMP comparison is a match comparison regardless of the setting.
23:22	DECMD[1:0]	00	R/W	**[Encoder mode and Sensor mode (Event count, Timer count and Phase count)]** Selection of Decoder detection direction 00: CW or CCW rotation edge detection The changes of the input signals (ENCxA, ENCxB, and ENCxZ) are detected. 01: CW Rotation edge detection Changes of the input signals from the previous rotation edge detection are detected. (The detected result is kept.) 10: CCW rotation edge detection Changes of the input signals from the previous rotation edge detection are detected. (The detected result is kept.) 11: CW or CCW rotation edge detection Changes of the input signals from the previous rotation edge detection are detected. (The detection result is kept.) **[Timer mode and Phase counter mode]** <DECMD>=00 should be set.
21	SDTEN	0	R/W	**[Encoder mode and Sensor mode (Event count, Timer count and Phase count)]** Skip detection 0: Detection disable 1: Detection enable When the skip is detected, the error flag (***[ENxSTS]***<SKPDT>) is set. Set it to "0" in other mode.
20	-	0	R	Read as "0".

Bit	Bit Symbol	After Reset	Type	Description
19:17	MODE[2:0]	000	R/W	Operation mode setting 000: Encoder mode 001: Sensor mode (Event counter) 010: Sensor mode (Timer count) 011: Timer mode 100: Reserved. 101: Reserved. 110: Sensor mode (Phase count) 111: Phase counter mode In Phase counter mode, when <ZEN>=<P3EN>=1, the operation mode becomes "Phase difference measurement ". There are 13 operation modes. The operation mode is determined by <MODE>, <P3EN>, and <ZEN> (Refer to "Table 3.1 Operation modes").
16	P3EN	0	R/W	**[Sensor mode (Event count, Timer count and Phase count)]** Decode mode setting (2-phase/3-phase input selection) 0: 2-phase decode 1: 3-phase decode **[Phase counter mode (Phase difference measurement)]** Set <ZEN> and <P3EN> to "1". **[Encoder mode, Timer mode and** Phase counter mode (Phase measurement)**]** Set <P3EN> to "0". (Refer to "Table 3.1 Operation modes").
15:13	-	0	R	Read as "0".
12	TRGCAPMD	0	R/W	**[Sensor mode (Timer count and Phase count), Timer mode, and Phase counter mode]** Trigger capture operation selection Operation selection for the capture by the rotation edge pulse and ENCxZ input 0: Capture and counter clear 1: Only capture This bit selects the trigger capture operation at the rotation edge detection in the sensor mode (Timer count and Phase count), and at ENCxZ input enable in Timer mode and Phase counter mode. The counter is not cleared by the software capture. **[Encoder mode and Sensor mode (Event count)]** Capture is not performed.
11	SFTCAP	0	W	**[Sensor mode (Timer count and Phase count), Timer mode, and Phase counter mode]** Software capture execution 1: The counter value is captured. When this bit is set to "1", the counter value is captured. ***[ENxCNT]*** should be read to acquire the captured value. Writing "0" means nothing. Read as "0". **[Encoder mode and Sensor mode (Event count)]** Write as "0".
10	ENCLR	0	W	Counter clear 1: Clear When this bit is set to "1", the counter is cleared to "0". The counter operates after the clear. Writing "0" means nothing. Read as "0". <SFTCAP> and <ENCLR> should not be set to "1" at the same time.

Bit	Bit Symbol	After Reset	Type	Description
9:8	ZESEL[1:0]	00	R/W	**[Timer mode and Phase counter mode]** This field selects the detection edge in ENCxZ input enable (<ZEN>=1). (ENCxZ input/ENCxPSGI input) 00: Reserved. 01: Rising edge detection 10: Falling edge detection 11: Both edge detection The detection target is ENCxPSGI input in the phase difference measurement. **[Encoder mode and Sensor mode (Event count, Timer count and Phase count)]** Set it to "00".
7	ZEN	0	R/W	**[Encoder mode, Timer mode, and Phase counter mode (Phase measurement)]** ENCxZ input enable 0: ENCxZ input disable 1: ENCxZ input enable **[Phase counter mode (Phase difference measurement)]** Set <P3EN> and <ZEN> to "1". **[Sensor mode (Event count and Timer count and Phase count)]** Set <ZEN> to "0". (Refer to "Table 3.1 Operation modes").
6	ENRUN	0	R/W	Encoder input circuit enable 0: Disable 1: Enable When <ENRUN>=1 is set, <ZDET> is cleared to "0" and the encoder input circuit is enabled. When <ENRUN>=0 is set, the encoder input circuit is disabled.
5	ZEACT	0	R/W	**[Encoder mode]** ENCxZ active level selection 0: H active input (Positive logic) 1: L active input (Negative logic) This bit is valid when ENCxZ input is enabled (<ZEN>=1) in Encoder mode. **[Sensor mode (Event count, Timer count, and Phase count), Timer mode, and Phase counter mode]** High active input is selected regardless of the setting.
4:3	-	0	R	Read as "0".
2:0	ENDEV[2:0]	000	R/W	**[Encoder mode and Sensor mode (Event count)]** The division ratio of the division signal of the rotation edge pulse (ENCxTIMPLS) is set. The frequency of the rotation edge pulse is divided according to the setting and the output signal is used as an interrupt factor. 000: 1-division 100: 16-division 001: 2-division 101: 32-division 010: 4-division 110: 64-division 011: 8-division 111: 128-division **[Sensor mode (Timer count and Phase count), Timer mode, and Phase counter mode]** There is no division output.

Note: When setting <ENRUN> = 1, do not change other bits at the same time. Operation settings other than <ENRUN> must be set before setting <ENRUN> = 1.

4.2.2. *[ENxRELOAD]* (RELOAD Comparison Register)

Bit	Bit Symbol	After Reset	Type	Description
31:0	RELOAD[31:0]	0x00000000	R/W	**[Encoder mode]** The maximum value of the counter is set. (Input pulse count per rotation) x 4 – 1 is set. **[Sensor mode (Phase count) and Phase counter mode(Phase measurement)]** The maximum value of the counter (the count region per rotation) is set. When ***[ENxINTCR]***<RLDIE>=1, an interrupt (INTENCx1) is generated with a RELOAD match. **[Sensor mode (Timer count) and Timer mode]** This register can be used as a comparison register with the counter value. When ***[ENxINTCR]***<RLDIE>=1, an interrupt (INTENCx1) is generated with a RELOAD match. **[Sensor mode (Event count) and Phase counter mode(Phase difference measurement)]** Unused.

4.2.3. *[ENxINT]* (INT Comparison Register)

Bit	Bit Symbol	After Reset	Type	Description
31:0	INT[31:0]	0x00000000	R/W	**[Encoder mode]** When the counter value matches this value, ***[ENxINTF]***<INTCPF> is set to "1". When ***[ENxINTCR]***<CMPIE>=1, an interrupt (INTENCx1) is generated with an INT match. When ***[ENxTNCR]***<ZEN>=1, however, no interrupt is generated at INT matchbefore ***[ENxSTS]***<ZDET> becomes "1". **[Sensor mode (Event count)]** When the counter value matches this value, <INTCPF> is set to "1". When <CMPIE>=1, an interrupt (INTENCx1) is generated with an INT match. **[Sensor mode (Timer count)]** When the counter value matches this value, it is judged that the rotation edge pulse un-detection interval error occurs. Then, <INTCPF> is set to "1". When <CMPIE>=1, an interrupt (INTENCx1) is generated with an INT match. **[Timer mode]** When the counter value matches this value, <INTCPF> is set to "1". When <CMPIE>=1, an interrupt (INTENCx1) is generated with an INT match. **[Sensor mode (Phase count) and Phase counter mode]** When the counter value matches this value, <INTCPF> is set to "1" at the next count. When <CMPIE>=1, an interrupt (INTENCx1) is generated. When ***[ENxTNCR]***<TOVMD>=1, which stops the counter at RELOAD match, the interrupt (INTENCx1) will not be generated if this value is the same as the ***[ENxRELOAD]*** value.

4.2.4. *[ENxCNT]* (Counter Register)

Bit	Bit Symbol	After Reset	Type	Description
31:0	CNT[31:0]	0x00000000	R	**[Encoder mode and Sensor mode (Event count)]** The counter value of the rotation edge pulses can be read. **[Sensor mode (Timer count and Phase count)]** The captured value of the internal counter by the rotation edge pulse (ENCLK) can be read. Or the captured value of the internal counter by writing ***[ENxTNCR]***<SFTCAP> to "1" in software can be read. **[Timer mode and Phase counter mode (Phase measurement)]** <SFTCAP> should be set to "1" to read the software-captured value of the internal counter. When ***[ENxTNCR]***<ZEN>=1, the capture is also done by the edge of ENCxZ (ZDETECT timing) set by ***[ENxTNCR]***<ZESEL>. **[Phase counter mode(Phase difference measurement)]** The software-captured value of the internal counter by writing <SFTCAP> to "1" can be read. When <ZEN>=<P3EN>=1, the capture is also done by the edge of ENCxPSGI (ZDETECT timing) set by <ZESEL>.

4.2.5. *[ENxMCMP]* (MCMP Comparison Register)

Bit	Bit Symbol	After Reset	Type	Description
31:0	MCMP[31:0]	0x00000000	R/W	**[Sensor mode (Timer count) and Timer mode]** When the comparison condition with the counter value is met, ***[ENxINTF]***<MCMPF> is set to "1".When ***[ENxINTCR]*** <MCMPIE>=1, an interrupt (INTENCx1) is generated. Magnitude comparison mode (***[ENxTNCR]***<MCMPMD>=1) When ***<MCMP> ≥ counter value*** is met, one pulse is generated. * Only one pulse is generated per writing to the register. Match comparison mode (***[ENxTNCR]***<MCMPMD>=0) When the counter value matches this value, the match signal is generated. **[Encoder mode and Sensor mode (Event count)** When the comparison condition with the counter value is met, ***[ENxINTF]***<MCMPF> is set to "1".When ***[ENxINTCR]*** <MCMPIE>=1, an interrupt (INTENCx1) is generated. **[Sensor mode (Phase count) and Phase counter mode]** When the comparison condition with the counter value is met, ***[ENxINTF]***<MCMPF> is set to "1".When ***[ENxINTCR]*** <MCMPIE>=1, an interrupt (INTENCx1) is generated. When it is set that RELOAD match counter stops at ***[ENxTNCR]***<TOVMD>=1, do not set to <MCMP>=***[ENxRELOAD]***.

Note: In Sensor mode (Timer count) or Timer counter mode, the comparison mode of ***[ENxTNCR]register*** <MCMPMD> is set to the magnitude comparison, and ***[ENxMCMP]*** value is updated at the same time when MCMP comparison is met, MCMP comparison met interrupt is not generated by the updated ***[ENxMCMP]*** value. MCMP comparison met flag ***[ENxINTF]***<MCMPIF> is not set, either.

4.2.6. *[ENxRATE]* (Phase Count Rate Register)

Bit	Bit Symbol	After Reset	Type	Description
31:16	-	0	R	Read as "0".
15:0	RATE[15:0]	0x0000	R/W	**[Sensor mode (Phase count) and Phase counter mode]** The count frequency of the counter is set. Generated clock frequency: fsys × <RATE> /2^{16} By ***[ENxTNCR]***<UDMD> setting, the sign of <RATE> setting value can be selected. When the value is negative, the counter decrements. <UDMD>=0x: Without a sign. 0 and more/Less than 1.0 (0x0000 to 0xFFFF) <UDMD>=1x: With a sign. -0.5 and more/Less than 0.5 (0x8000 to 0x7FFF, two's complement) When <RATE>=0x0000, ***[ENxCNT]*** does not count. **[Encoder mode, Sensor mode (Event count and Timer count), and Timer mode]** Unused.

4.2.7. *[ENxSTS]* (Status Register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0".
14	REVERR	0	R	**[Sensor mode (Timer count and Phase count)]** The reversed <UD> flag at both direction detection (Note1) (Note2) 0: - 1: Reversed <UD> is generated. When ***[ENxTNCR]***<ENRUN>=0, "0" is always set. In Encoder mode, Sensor mode (Event count), Timer mode and Phase counter mode, this bit means nothing.
13	UD	0	R	**[Encoder mode, Sensor mode (Event count, Timer count, and Phase count)]** Rotation direction judgment 0: CCW (Counter-clockwise) 1: CW (Clockwise) When a motor rotates in CW direction, this bit is set to "1", and, in CCW direction, set to "0". When ***[ENxTNCR]***<ENRUN>=0, "0" is always set.
12	ZDET	0	R	**[Encoder mode]** ENCxZ input pass detection 0: Z input has not been detected after the encoder input is enabled. 1: Z input has been detected. This bit is cleared by ***[ENxTNCR]***<ENRUN>=0.
11:3	-	0	R	Read as "0".
2	SKPDT	0	R	**[Sensor mode (Event count, Timer count, and Phase count)]** Skip detection flag at Skip detection enable (Note1) 0: No detection. 1: Skip is detected.
1	PDERR	0	R	**[Encoder mode, Sensor mode (Event count, Timer count, and Phase count)]** Edge detection error flag (Note1) 0: No detection. 1: Error is detected.
0	INERR	0	R	**[Sensor mode (Event count, Timer count, and Phase count)]** Abnormal input detection (Note1) 0: Abnormal input has not been detected. 1: Abnormal input has been detected. In 3-phase decode operation, 3 phase inputs are detected as all Low or all High, this bit is set to "1".

Note1: When the register is read, the flag is cleared.

Note2: After an operation mode (***[ENxTNCR]***<MODE>) is updated, this register should be read to clear the flags to "0" at first.

4.2.8. *[ENxINPCR]* (Input Procedure Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:15	-	0	R	Read as "0".
14:8	NCT[6:0]	0x00	R/W	Noise cancellation time (Note1) Setting range: 0 to 127 (0x00 to 0x7F) Cancellation time: Setting value × Sample clock cycle (by ***[ENxCLKCR]***<SPLCKS> setting) When "0" is set, the noise cancellation does not operate (the circuit is bypassed). The sampling clock is PWM signal (ENCxPWMON) in PWM-Off edge sample mode.
7	PDSTP	0	W	**[Sensor mode (Timer count and Phase count)]** The rotation edge detection stop command (BEMF detection control) at PWM synchronous sampling. 0: - 1: Rotation edge detection stop When "1" is set, the rotation edge detection stops. Writing "0" means nothing. Read as "0". <PDSTP> and <PDSTT> should not be set to "1" at the same time.
6	PDSTT	0	W	**[Sensor mode (Timer count and Phase count)]** The rotation edge detection start command (BEMF detection control) at PWM synchronous sampling. 0: - 1: Rotation edge detection start When "1" is set, the rotation edge detection starts. Writing "0" means nothing. Read as "0". <PDSTP> and <PDSTT> should not be set to "1" at the same time.
5:3	-	0	R	Read as "0".
2	SYNCNCZEN	0	R/W	Noise cancellation counter control at PWM-On interval sampling 0: PWM-Off interval counter stop 1: PWM-Off interval counter stop and clear This bit is valid at PWM-On interval sampling selection (<SYNCSPLMD>=0) in PWM synchronous sampling enable (<SYNCSPLEN>=1).
1	SYNCSPLMD	0	R/W	PWM synchronous sampling selection 0: PWM-On interval sampling 1: PWM-Off edge sampling This bit is valid at PWM synchronous sampling enable (<SYNCSPLEN>=1).
0	SYNCSPLEN	0	R/W	PWM synchronous sampling enable 0: Continuous sampling 1: PWM synchronous sampling (Note1) The sampling synchronous with PWM signal in PMD circuit (ENCxPWMON) is done. (Note2) When <SYNCSPLEN>=1 is set in Sensor mode (Timer count and Phase count), BEMF detection control is valid in the decode operation.

Note1: When PWM synchronous sampling (<SYNCSPLEN>=1), <NCT> should be set to "1" or more.

Note2: For the details of PMD circuit, refer to "Programmable Motor Control Circuit Plus" or "Advanced Programmable Motor Control Circuit" in Reference manual.

4.2.9. *[ENxSMPDLY]* (Sample Delay Register)

Bit	Bit Symbol	After Reset	Type	Description
31:8	-	0	R	Read as "0".
7:0	SMPDLY[7:0]	0x00	R/W	Sampling disable interval Setting range: 0 to 255 (0x00 to 0xFF) Disable interval: <SMPDLY> value x Sampling cycle (by ***[ENxCLKCR]***<SPLCKS> setting) This field sets the sampling disable interval after PWM is On in the PWM-On interval sampling mode (***[ENxINPCR]*** <SYNCSPLEN>=1 and ***[ENxINPCR]***<SYNCSPLMD>=0).

Note: After ENC is enabled (after changing ***[ENxTNCR]***<ENRUN> from "0" to "1"), the first delay time may be different from the <SMPDLY> setting value.

4.2.10. *[ENxINPMON]* (Input Monitor Register)

Bit	Bit Symbol	After Reset	Type	Description
31:7	-	0	R	Read as "0".
6	DETMONZ	0	R	Monitor of NCZ rotation edge detection status (Note1) (Note2) NCZ value at the rotation edge detection is stored.
5	DETMONB	0	R	Monitor of NCB rotation edge detection status (Note1) (Note2) NCB value at the rotation edge detection is stored.
4	DETMONA	0	R	Monitor of NCA rotation edge detection status (Note1) (Note2) NCA value at the rotation edge detection is stored.
3	-	0	R	Read as "0".
2	SPLMONZ	0	R	ENCxZ status after the noise cancellation Status of the signal of the noise-cancelled ENCxZ input (NCZ)
1	SPLMONB	0	R	ENCxB status after the noise cancellation Status of the signal of the noise-cancelled ENCxB input (NCB)
0	SPLMONA	0	R	ENCxA status after the noise cancellation Status of the signal of the noise-cancelled ENCxA input (NCA)

Note1: This bit is valid when ***[ENxTNCR]***<DECMD> is not "00". When <DECMD>=00, this bit shows <SPLMONn> value (n = A, B, or Z) in the previous cycle.

Note2: Even when ***[ENxTNCR]***<ENRUN> is updated to "1" or ***[ENxINPCR]***<PDSTT> is set to "1", this bit shows <SPLMONn> value (n = A, B, or Z) in the previous cycle until the first rotation edge is detected.

4.2.11. *[ENxCLKCR]* (Sample Clock Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:2	-	0	R	Read as "0".
1:0	SPLCKS[1:0]	00	R/W	Sampling frequency 00: fsys 01: fsys/2 10: fsys/4 11: fsys/8 The sampling frequency is selected for ENCxA, ENCxB, and ENCxZ inputs. This field is not valid when Off edge sampling (***[ENxINPCR]*** <SYNCSPLEN>=1 and ***[ENxINPCR]***<SYNCSPLMD>=1) in PWM synchronous sampling.

4.2.12. *[ENxINTCR]* (Interrupt Control Register)

Bit	Bit Symbol	After Reset	Type	Description
31:6	-	0	R	Read as "0".
5	MCMPIE	0	R/W	MCMP met interrupt enable 0: Disable 1: Enable When "1" is set to this bit and MCMP is met, INTENCx1 is generated.
4	RLDIE	0	R/W	RELOAD match interrupt enable 0: Disable 1: Enable When "1" is set to this bit and RELOAD matches, INTENCx1 is generated. In Encoder mode and Sensor mode (Event count), the interrupt is not generated.
3	CMPIE	0	R/W	INT match interrupt enable 0: Disable 1: Enable When "1" is set to this bit and INT matches, INTENCx1 is generated.
2	ERRIE	0	R/W	Detection error interrupt enable 0: Disable 1: Enable When "1" is set to this bit and the edge detection error (***[ENxSTS]*** <PDERR>) occurs or the skip detection (***[ENxSTS]***<SKPDT>) is done, INTENCx0 is generated. In Timer mode and Phase counter mode, the interrupt is not generated.
1	CAPIE	0	R/W	Capture trigger interrupt enable 0: Disable 1: Enable When "1" is set to this bit and the external trigger (ENCxZ input) or the rotation edge pulse (ENCLK) captures the counter value, INTENCx0 is generated. In Encoder mode and Sensor mode (Event count), the interrupt is not generated.
0	TPLSIE	0	R/W	Rotation edge division interrupt enable 0: Disable 1: Enable When "1" is set to this bit, INTENCx0 is generated by a rotation edge division pulse. In the other modes than Encoder mode and Sensor mode (Event count), the interrupt is not generated.

4.2.13. *[ENxINTF]* (Interrupt Flag Register)

Bit	Bit Symbol	After Reset	Type	Description
31:6	-	0	R	Read as "0".
5	MCMPF	0	R	MCMP comparison met flag 0: Not generated. 1: Generated.
4	RLDCPF	0	R	RELOAD match flag 0: Not generated 1: Generated In Encoder mode and Sensor mode (Event count), this bit is not set.
3	INTCPF	0	R	INT match flag 0: Not generated. 1: Generated.
2	ERRF	0	R	Detection error flag 0: Not generated. 1: Generated. In Timer mode and Phase counter mode, this bit is not set.
1	CAPF	0	R	Capture flag 0: Not generated. 1: Generated. This bit is not set by the software capture. In Encoder mode and Sensor mode (Event count), this bit is not set.
0	TPLSF	0	R	Rotation edge division pulse flag 0: Not generated. 1: Generated. This bit is valid in Encoder mode and Sensor mode (Event count).

Note: Each flag is set by the occurrence of the enabled factor, and cleared by reading ***[ENxINTF]*** register. When ***[ENxTNCR]***<ENRUN>=0, the flags are set to "0".

5. Precaution for Usage

- Before the clock supply is shut down, it should be checked that ENC has stopped. And, before the operation mode is changed to the stop mode, it should be checked that ENC has stopped.

6. Revision History

Table 6.1 Revision history

Revision	Date	Description
1.0	2018-06-18	First release
1.1	2018-10-11	- Conventions Modified explanation of trademark - 2. Configuration Figure 2.1: "Encoder input circuit"→"ENC" - 3.2.1. Encoder Mode "incremental encoder input" →"incremental encoder" - 3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode Corrected Figure 3.24 " ***[ENxRATE]***<RATE> " → " ***[ENxRATE]*** " - 3.3.4. Interrupt Control Corrected Table 3.2. " PDERR " → " ***[ENxSTS]***<PDERR> " " SKPDT " → " ***[ENxSTS]***<SKPDT>" - 4.2.1. ***[ENxTNCR]*** (ENC Control Register) Changed the expression of "Note:". - RESTRICTIONS ON PRODUCT USE Replaced

RESTRICTIONS ON PRODUCT USE

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