32-bit RISC Microcontroller

TMPM4L Group(1)

Reference Manual
Input/Output Ports
(PORT-M4L(1))

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

JTAG	Joint Test Action Group
SW	Serial Wire

1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

Function Classification	Function	Description
Port	-	Programmable pull-up/Programmable pull-down/open-drain output are possible.
Peripheral Function pins	External Interrupt	Interrupt pin has a noise filter(Filter width 30ns Typ.).
	32-bit Timer Event Counter	Input capture input pin. Timer output pin.
	Serial Peripheral Interface	Data input pin, Data output pin, Clock input/output pin
	Asynchronous Serial Communication Circuit	Data input pin, Data output pin, Clear to send signal pin.
	Analog Digital Convertor	Analog input pin
	Programmable Motor Control Circuit Plus	X/Y/Z phase output pins, U/V/W phase output pins, EMG detection input pin, Overvoltage detection input pin.
	Advanced Encoder Input Circuit(32-bit)	Encoder input pin
Debug pins	JTAG	Test select input pin, Serial clock input pin, Serial data output pin, Serial data input pin
	SW	Serial wire data input/output pin, Serial wire clock input pin, Serial wire viewer output pin
Control pins	High speed clock	High speed resonator connection pin / External Clock signal input pin
	BOOT mode control	BOOT mode control pin

2. Function

2.1. Clock supply

When you use Port, please set an applicable clock enable bit to 1 (clock supply) in fsys supply stop registers A (***[CGFSYSENA]***). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to “Clock Control and Operation Mode” in Reference manual.

3. Signal connection list

This table is sorted the function pins by the signal name of the block diagram which is described each reference manual. Register setting of the peripherals function is being explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal connection list (1/3)

Related Reference Manual	Function pin name	Port name	M4L2 (LQFP48)	M4L1 (LQFP44)
Asynchronous Serial Communication Circuit	UT0RXD	PC1	18	17
		PC0	17	16
	UT0TXDA	PC0	17	16
		PC1	18	17
	UT0CTS_N	PC2	19	18
	UT1RXD	PD3	23	22
		PD2	22	21
	UT1TXDA	PD2	22	21
		PD3	23	22
	UT1CTS_N	PD1	21	20
	UT2RXD	PA1	47	43
		PA2	46	42
	UT2TXDA	PA2	46	42
		PA1	47	43
	UT2CTS_N	PA0	48	44
Serial Peripheral Interface	TSPI0RXD	PC1	18	17
	TSPI0TXD	PC0	17	16
	TSPI0SCK	PC2	19	18
	TSPI1RXD	PD3	23	22
	TSPI1TXD	PD2	22	21
	TSPI1SCK	PD1	21	20
	TSPI2RXD	PA2	46	42
	TSPI2TXD	PA1	47	43
	TSPI2SCK	PA0	48	44

Table 3.2 Signal connection list (2/3)

Related Reference Manual	Function pin name	Port name	M4L2 (LQFP48)	M4L1 (LQFP44)
32-bit Timer Event Counter	T32A00INA0	PD0	12	11
	T32A00OUTA	PD0	12	11
	T32A00INB0	PD4	24	-
	T32A00OUTB	PD4	24	-
	T32A00INC0	PD0	12	11
	T32A00OUTC	PD0	12	11
	T32A01INA0	PC3	20	19
	T32A01OUTA	PC3	20	19
	T32A01INB0	PA3	25	-
	T32A01OUTB	PA3	25	-
	T32A01INC0	PC3	20	19
	T32A01OUTC	PC3	20	19
	T32A02INA0	PC4	45	41
	T32A02OUTA	PC5	44	40
	T32A02INB0	PC5	44	40
	T32A02OUTB	PC4	45	41
	T32A02INC0	PC4	45	41
	T32A02OUTC	PC5	44	40
	T32A03INA0	PA2	46	42
	T32A03OUTA	PA1	47	43
	T32A03INB0	PA1	47	43
	T32A03OUTB	PA2	46	42
	T32A03INC0	PA1	47	43
	T32A03OUTC	PA2	46	42
12-bit Analog to Digital Convertor	AINA00	PF0	35	32
	AINA01	PG0	36	33
	AINA02	PG3	37	-
	AINA03	PG1	38	34
	AINA04	PG2	39	35
	AINA05	PH0	40	36
	AINA06	PH1	41	37

Table 3.3 Signal connection list (3/3)

Related Reference Manual	Function pin name	Port name	M4L2 (LQFP48)	M4L1 (LQFP44)
Exception	INT00	PC3	20	19
	INT01	PG1	38	34
	INT02	PG2	39	35
	INT03	PH0	40	36
	INT04	PH1	41	37
	INT05	PC5	44	40
	INT06	PC4	45	41
	INT07	PA3	25	-
Programmable Motor Control Circuit Plus	EMG0_N	PE6	8	7
	OVV0_N	PE7	9	8
	UO0	PE0	2	1
	VO0	PE2	4	3
	WO0	PE4	6	5
	XO0	PE1	3	2
	YO0	PE3	5	4
	ZO0	PE5	7	6
Advanced Encoder Input Circuit(32-bis)	ENC0A	PD1	21	20
	ENC0B	PD2	22	21
	ENC0Z	PD3	23	22
Debug Interface	TMS	PB0	16	15
	TCK	PB1	15	14
	TDO	PB2	14	13
	TDI	PB3	13	12
	SWDIO	PB0	16	15
	SWCLK	PB1	15	14
	SWV	PB2	14	13
Clock Control and Operation Mode	X1	PJ0	27	24
	X2	PJ1	29	26
FLASH Memory	BOOT_N	PD0	12	11

4. Registers

The following registers should be set appropriately to use the ports.
Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.
"x" and "n" in the following table show a port name and a function number, respectively.

Register Name		Type	Setting Value	Description
[PxDATA]	Data Register	R/W	0 or 1	Read from and write to a port.
[PxCR]	Output Control Register	R/W	0: Output disabled 1: Output enabled	Output control.
[PxFRn]	Function register n	R/W	0: PORT 1: Function	Function setting. When “1” is set, the assigned function becomes available. Each function assigned to a port has its own function register. If multiple functions are assigned to one port, only one function should be enabled.
[PxOD]	Open-drain Control Register	R/W	0: CMOS 1: Open-drain	Programmable open-drain control. The programmable open-drain is a pseudo open-drain. An output buffer is disabled when the output data is 1, which is set by ***[PxOD]*** = 1.
[PxPUP]	Pull-up Control Register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up control.
[PxPDN]	Pull-down Control Register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down control.
[PxIE]	Input Control Register	R/W	0: Input disabled 1: Input enabled	Input control. It takes 100ns time(Max) that an external data is reflected on ***[PxDATA]*** after the ***[PxIE]*** is enabled.

4.1. List of Register

When the bit which is assigned to no functions is read, "0" is returned. The write to the bit is ignored.

Table 4.1 Ports base address

Peripheral function		Channel/Unit	Base address
Input/output ports	PA	—	0x40080000
	PB	—	0x40080100
	PC	—	0x40080200
	PD	—	0x40080300
	PE	—	0x40080400
	PF	—	0x40080500
	PG	—	0x40080600
	PH	—	0x40080700
	PJ	—	0x40080800
	PK	—	0x40080900

Table 4.2 Register List

Register Name	Address (Base+)	Port A	Port B	Port C	Port D	Port E	Port F
Data Register	0x0000	*[PADATA]*	*[PBDATA]*	*[PCDATA]*	*[PDDATA]*	*[PEDATA]*	*[PFDATA]*
Output Control Register	0x0004	*[PACR]*	*[PBCR]*	*[PCCR]*	*[PDCR]*	*[PECR]*	*[PFCR]*
Function Register 1	0x0008	*[PAFR1]*	*[PBFR1]*	*[PCFR1]*	*[PDFR1]*	*[PEFR1]*	—
Function Register 2	0x000C	*[PAFR2]*	—	*[PCFR2]*	*[PDFR2]*	—	—
Function Register 3	0x0010	*[PAFR3]*	—	*[PCFR3]*	*[PDFR3]*	—	—
Function Register 4	0x0014	*[PAFR4]*	—	*[PCFR4]*	*[PDFR4]*	—	—
Function Register 5	0x0018	*[PAFR5]*	—	—	—	—	—
Function Register 6	0x001C	*[PAFR6]*	—	—	—	—	—
Open Drain Control Register	0x0028	*[PAOD]*	*[PBOD]*	*[PCOD]*	*[PDOD]*	*[PEOD]*	*[PFOD]*
Pull-up Control Register	0x002C	*[PAPUP]*	*[PBPUP]*	*[PCPUP]*	*[PDPUP]*	*[PEPUP]*	*[PFPUP]*
Pull-down Control Register	0x0030	*[PAPDN]*	*[PBPDN]*	*[PCPDN]*	*[PDPDN]*	*[PEPDN]*	*[PFPDN]*
Input Control Register	0x0038	*[PAIE]*	*[PBIE]*	*[PCIE]*	*[PDIE]*	*[PEIE]*	*[PFIE]*

Register Name	Address (Base+)	PORT G	PORT H	PORT J	PORT K
Data Register	0x0000	*[PGDATA]*	*[PHDATA]*	*[PJDATA]*	*[PKDATA]*
Output Control Register	0x0004	*[PGCR]*	*[PHCR]*	—	*[PKCR]*
Function Register 1	0x0008	—	—	—	—
Function Register 2	0x000C	—	—	—	—
Function Register 3	0x0010	—	—	—	—
Function Register 4	0x0014	—	—	—	—
Function Register 5	0x0018	—	—	—	—
Function Register 6	0x001C	—	—	—	—
Open Drain Control Register	0x0028	*[PGOD]*	*[PHOD]*	—	*[PKOD]*
Pull-up Control Register	0x002C	*[PGPUP]*	*[PHPUP]*	—	*[PKPUP]*
Pull-down Control Register	0x0030	*[PGPDN]*	*[PHPDN]*	*[PJPDN]*	*[PKPDN]*
Input Control Register	0x0038	*[PGIE]*	*[PHIE]*	*[PJIE]*	*[PKIE]*

Note: Do not access the addresses described as "—".

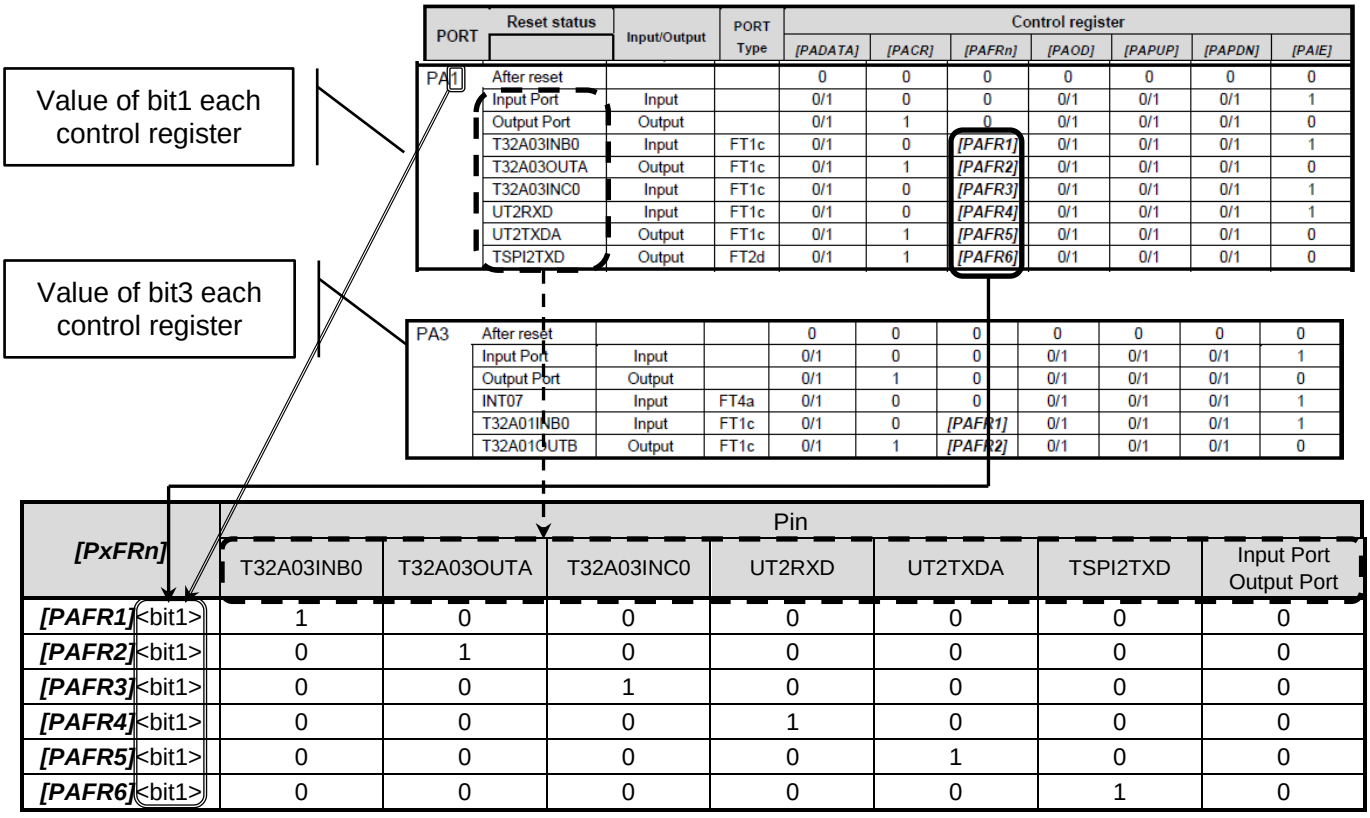
4.2. List of Port Functions and Settings

It is explained about viewpoint of a port register setting table.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit in the "N/A" in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the value which should be set. "0/1" means either value can be set.



PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	[PACR]	[PAFRn]	[PAOD]	[PAPUP]	[PAPDN]	[PAIE]
PA1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03INB0	Input	FT1c	0/1	0	[PAFR1]	0/1	0/1	0/1	1
	T32A03OUTA	Output	FT1c	0/1	1	[PAFR2]	0/1	0/1	0/1	0
	T32A03INC0	Input	FT1c	0/1	0	[PAFR3]	0/1	0/1	0/1	1
	UT2RXD	Input	FT1c	0/1	0	[PAFR4]	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1c	0/1	1	[PAFR5]	0/1	0/1	0/1	0
	TSPI2TXD	Output	FT2d	0/1	1	[PAFR6]	0/1	0/1	0/1	0

PA3										
	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A01INB0	Input	FT1c	0/1	0	[PAFR1]	0/1	0/1	0/1	1
	T32A01OUTB	Output	FT1c	0/1	1	[PAFR2]	0/1	0/1	0/1	0

[PxFRn]	Pin						
	T32A03INB0	T32A03OUTA	T32A03INC0	UT2RXD	UT2TXDA	TSPI2TXD	Input Port Output Port
[PAFR1]<bit1>	1	0	0	0	0	0	0
[PAFR2]<bit1>	0	1	0	0	0	0	0
[PAFR3]<bit1>	0	0	1	0	0	0	0
[PAFR4]<bit1>	0	0	0	1	0	0	0
[PAFR5]<bit1>	0	0	0	0	1	0	0
[PAFR6]<bit1>	0	0	0	0	0	1	0

4.2.1. Setting of using the function pin

To use the alternated pins as peripheral function output pins, set the peripheral function (***[PxFRn]***<bit m>=1) that uses the function register and then enable output control register (***[PxCR]***<bit m>=1). If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register of the port (***[PxIE]***<bit m>=1) and set the peripheral function that uses the function register (***[PxFRn]***<bit m>=1), then set the peripheral functions.

To use peripheral functions such as SWDIO, set the input control register of the port (***[PxIE]***<bit m>=1), set the peripheral function (***[PxFRn]***<bit m>=1) and set the output control register to output enable (***[PxCR]***<bit m>=1), then set the peripheral function.

- When plural functions are assigned to the same pin, please use a function pin exclusively.
- When the same function is assigned to plural ports, please use a pin exclusively.

4.2.2. PORT A

Table 4.3 Port A register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UT2CTS_N	Input	FT1c	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	TSPI2SCK	Input	FT1c	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
		Output	FT1c	0/1	1		0/1	0/1	0/1	0
PA1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03INB0	Input	FT1c	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	T32A03OUTA	Output	FT1c	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	T32A03INC0	Input	FT1c	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	UT2RXD	Input	FT1c	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	UT2TXDA	Output	FT1c	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
	TSPI2TXD	Output	FT2d	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A03INA0	Input	FT1c	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	T32A03OUTB	Output	FT1c	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FT1c	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	UT2TXDA	Output	FT1c	0/1	1	***[PAFR4]***	0/1	0/1	0/1	0
	UT2RXD	Input	FT1c	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	TSPI2RXD	Input	FT1c	0/1	0	***[PAFR6]***	0/1	0/1	0/1	1
PA3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A01INB0	Input	FT1c	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	T32A01OUTB	Output	FT1c	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0

4.2.3. PORT B

Table 4.4 Port B register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBPUP]*	*[PBPDN]*	*[PBIE]*
PB0	After reset (TMS/SWDIO)	I/O	FT2d	0	1 (Note)	***[PBFR1]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PB1	After reset (TCK/SWCLK)	Input	FT2d	0	0	***[PBFR1]***	0	0	1	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PB2	After reset (TDO/SWV)	Output	FT2d	0	1 (Note)	***[PBFR1]***	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
PB3	After reset (TDI)	Input	FT2d	0/1	0	***[PBFR1]***	0	1	0	1
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0

Note: When receive the command from TOOL, it becomes output.

4.2.4. PORT C

Table 4.5 Port C register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0TXD	Output	FT2d	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT0TXDA	Output	FT1c	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	UT0RXD	Input	FT1c	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
PC1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0RXD	Input	FT1c	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT0RXD	Input	FT1c	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FT1c	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
PC2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI0SCK	Input	FT1c	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
		Output	FT1c	0/1	1		0/1	0/1	0/1	0
	UT0CTS_N	Input	FT1c	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
PC3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT00	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A01INA0	Input	FT1c	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	T32A01OUTA	Output	FT1c	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	T32A01INC0	Input	FT1c	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A01OUTC	Output	FT1c	0/1	1	***[PCFR4]***	0/1	0/1	0/1	0
PC4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT06	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A02INA0	Input	FT1a	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	T32A02OUTB	Output	FT1a	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	T32A02INC0	Input	FT1a	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
PC5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT05	Input	FT4a	0/1	0	0	0/1	0/1	0/1	1
	T32A02INB0	Input	FT1c	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	T32A02OUTA	Output	FT1c	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FT1c	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0

4.2.5. PORT D

Table 4.6 Port D register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD0	During reset (BOOT_N)	Input	FT16a	0	0	0	0	1(Note)	0	1(Note)
	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A00INA0	Input	FT1c	0/1	0	***[PDFR1]***	0/1	0	0	1
	T32A00OUTA	Output	FT1c	0/1	0	***[PDFR2]***	0/1	0	0	0
	T32A00INC0	Input	FT1c	0/1	0	***[PDFR3]***	0/1	0	0	1
	T32A00OUTC	Output	FT1c	0/1	0	***[PDFR4]***	0/1	0	0	0
PD1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ENC0A	Input	FT1c	0/1	0	***[PDFR1]***	0/1	0	0	1
	TSPI1SCK	Input	FT1c	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
		Output	FT1c	0/1	1		0/1	0/1	0/1	0
	UT1CTS_N	Input	FT1c	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
PD2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ENC0B	Input	FT1c	0/1	0	***[PDFR1]***	0/1	0	0	1
	TSPI1TXD	Output	FT2d	0/1	1	***[PDFR2]***	0/1	0/1	0/1	0
	UT1TXDA	Output	FT1c	0/1	1	***[PDFR3]***	0/1	0/1	0/1	0
	UT1RXD	Input	FT1c	0/1	0	***[PDFR4]***	0/1	0/1	0/1	1
PD3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ENC0Z	Input	FT1c	0/1	0	***[PDFR1]***	0/1	0	0	1
	TSPI1RXD	Input	FT1c	0/1	0	***[PDFR2]***	0/1	0/1	0/1	1
	UT1RXD	Input	FT1c	0/1	0	***[PDFR3]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FT1c	0/1	1	***[PDFR4]***	0/1	0/1	0/1	0
PD4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	T32A00INB0	Input	FT1c	0/1	0	***[PDFR1]***	0/1	0/1	0/1	1
	T32A00OUTB	Output	FT1c	0/1	0	***[PDFR2]***	0/1	0	0	0

Note: PD0 can input the BOOT_N signal while ***[PDPUP]*** is enabled ("1") and ***[PDIE]*** is also enabled ("1") during the reset period by the reset pin (RESET_N).

4.2.6. PORT E

Table 4.7 Port E register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	UO0	Output	FT2d	0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
PE1	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	XO0	Output	FT2d	0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
PE2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	VO0	Output	FT2d	0/1	0	***[PEFR1]***	0/1	0/1	0/1	0
PE3	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	YO0	Output	FT2d	0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
PE4	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	WO0	Output	FT2d	0/1	0	***[PEFR1]***	0/1	0/1	0/1	0
PE5	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	ZO0	Output	FT2d	0/1	1	***[PEFR1]***	0/1	0/1	0/1	0
PE6	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	EMG0_N	Input	FT1c	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1
PE7	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	OVV0_N	Input	FT1c	0/1	0	***[PEFR1]***	0/1	0/1	0/1	1

4.2.7. PORT F

Table 4.8 Port F register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA00	Input	FT5a	0/1	0	N/A	0/1	0/1	0/1	0

4.2.8. PORT G

Table 4.9 Port G register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA01	Input	FT5a	0/1	0	N/A	0/1	0/1	0/1	0
PG1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT01	Input	FT4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINA03	Input	FT5a	0/1	0	N/A	0/1	0/1	0/1	0
PG2	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT02	Input	FT4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINA04	Input	FT5a	0/1	0	N/A	0/1	0/1	0/1	0
PG3	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	AINA02	Input	FT5a	0/1	0	N/A	0/1	0/1	0/1	0

Note: When using analog input(AINAx), ***[PGCR]*** should be output disable”0”, ***[PGIE]*** should be input disable"0", ***[PGPUP]*** should be pull-up disable"0", and ***[PGPDN]*** should be pull-down disable"0".

4.2.9. PORT H

Table 4.10 Port H register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PHDATA]	*[PHCR]*	*[PHFRn]*	*[PHOD]*	*[PHPUP]*	*[PHPDN]*	*[PHIE]*
PH0	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT03	Input	FT4a	0/1	0	N/A	0/1	0/1	0/1	1
	AINA05	Input	FT5a	0/1	0	N/A	0/1	0/1	0/1	0
PH1	After reset			0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0
	INT04	Input	FT4a	0/1	1	N/A	0/1	0/1	0/1	0
	AINA06	Input	FT5a	0/1	0	N/A	0/1	0/1	0/1	0

Note: When using analog input(AINAx), ***[PHCR]*** should be output disable”0”, ***[PHIE]*** should be input disable"0", ***[PHPUP]*** should be pull-up disable"0", and ***[PHPDN]*** should be pull-down disable"0".

4.2.10. PORT J

Table 4.11 Port J register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PJDATA]	*[PJCR]*	*[PJFRn]*	*[PJOD]*	*[PJPUP]*	*[PJPDN]*	*[PJIE]*
PJ0	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X1	Input	FT11a	0/1	N/A	N/A	N/A	N/A	0/1	0
	EHCLKIN	input	FT11a	0/1	N/A	N/A	N/A	N/A	0/1	0
PJ1	After reset			0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input		0/1	N/A	N/A	N/A	N/A	0/1	1
	X2	Output	FT11a	0/1	N/A	N/A	N/A	N/A	0/1	0

4.2.11. PORT K

Table 4.12 Port K register setting

PORT	Reset status	Input/Output	PORT Type	Control register						
				[PKDATA]	*[PKCR]*	*[PKFRn]*	*[PKOD]*	*[PKPUP]*	*[PKPDN]*	*[PKIE]*
PK0	After reset	Input		0	0	N/A	0	0	0	0
	Input Port	Input		0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	N/A	0/1	0/1	0/1	0

5. Port Circuit Diagram

The port has 6 types of circuits, FT1c to FT2d, FT4a, FT5a, FT11a and FT16a. Each circuit diagram is shown in the following page and after. The dot line block shows "Equivalent Circuit" which is described in "Datasheet".

The "I/O Reset" shown in the circuit diagram is described the power on reset (POR) or the reset pin(RESET_N). Although, “I/O Reset” of debug pins(TMS/SWDIO.TDI,TDO/SWV,TCK/SWCLK) is the power on reset(POR) only.

5.1. Type FT1c

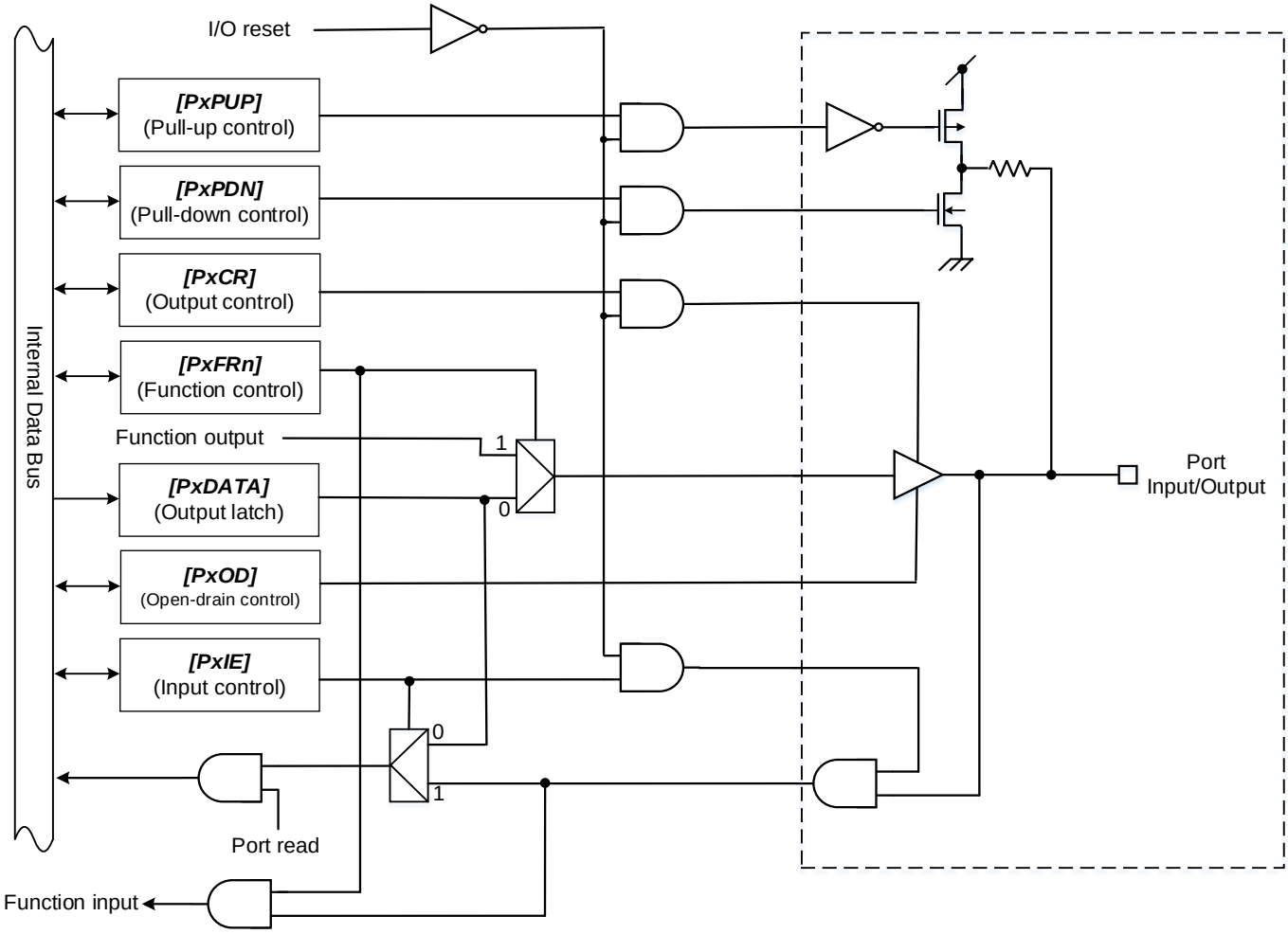


Figure 5.1 Port Type FT1c

5.2. Type FT2d

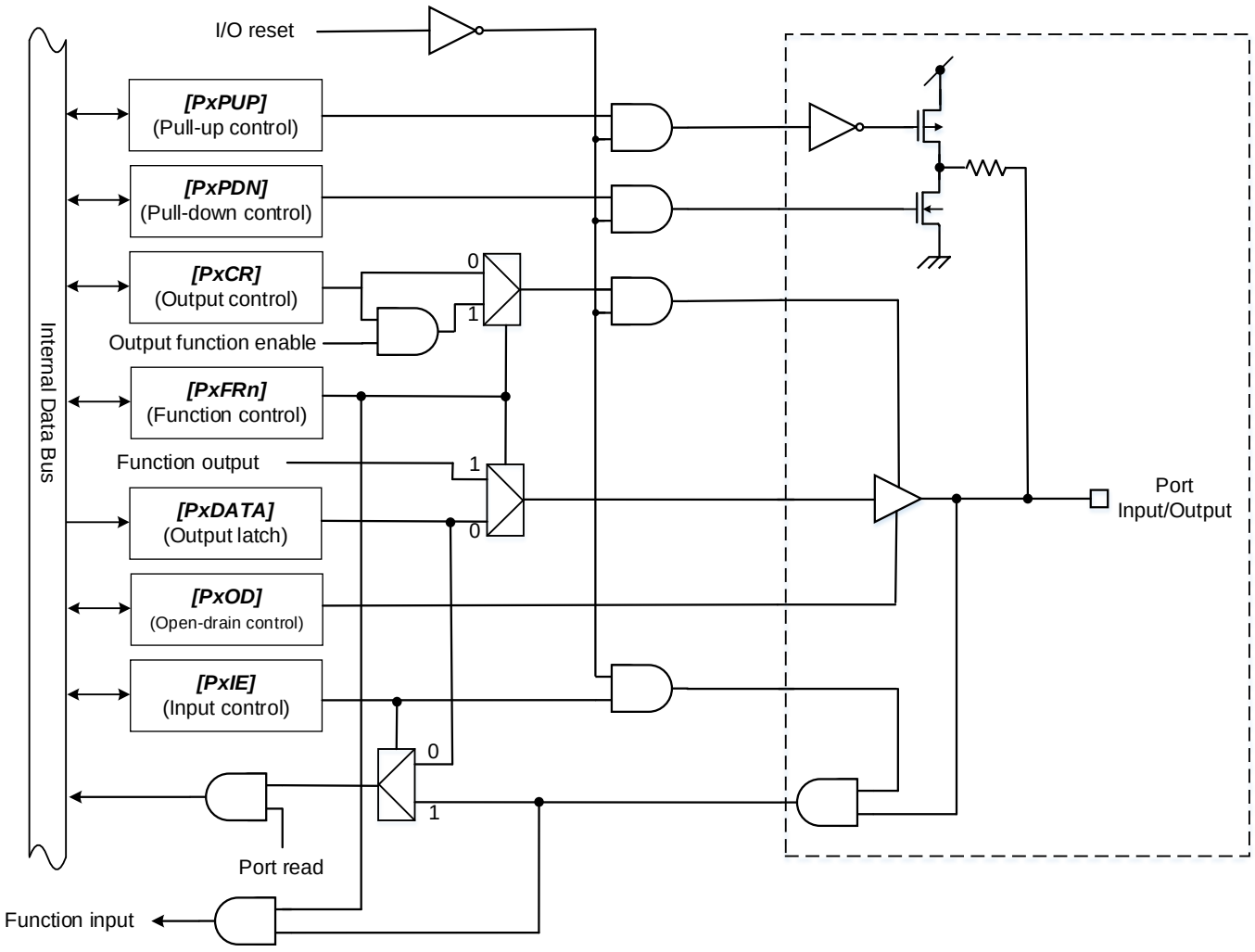


Figure 5.2 Port Type FT2d

5.3. Type FT4a

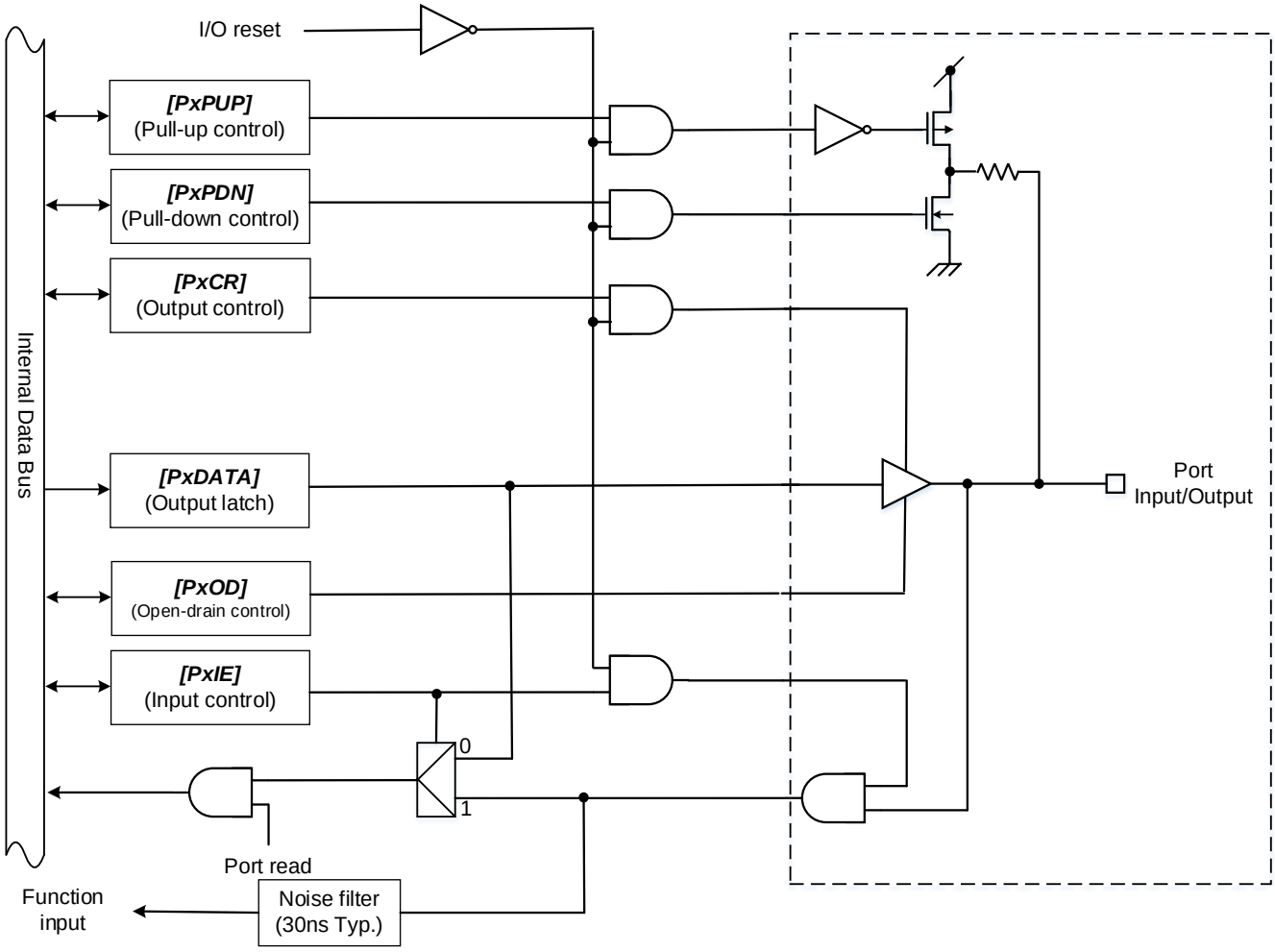


Figure 5.3 Port Type FT4a

5.4. Type FT5a

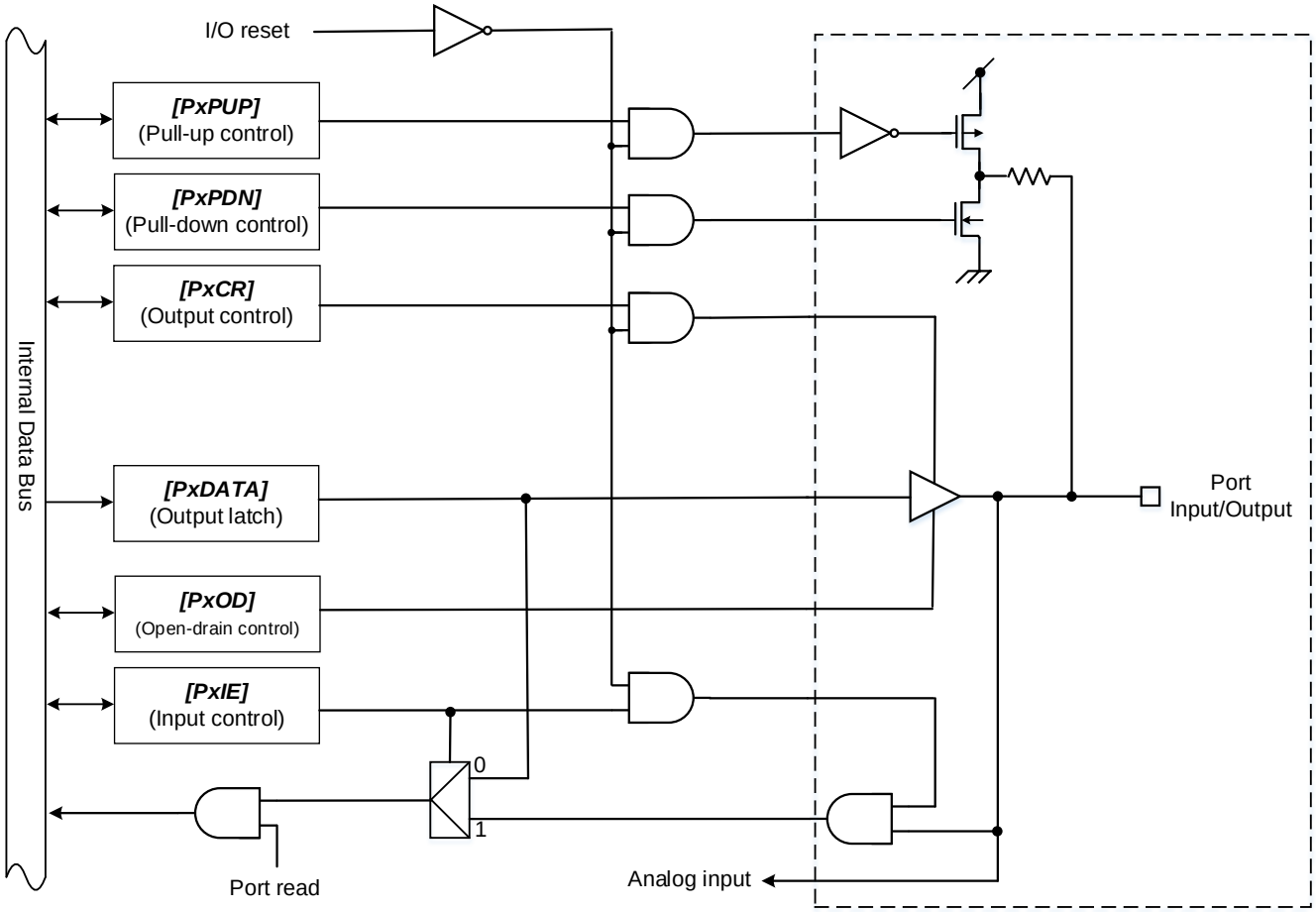


Figure 5.4 Port Type FT5a

5.5. Type FT11a

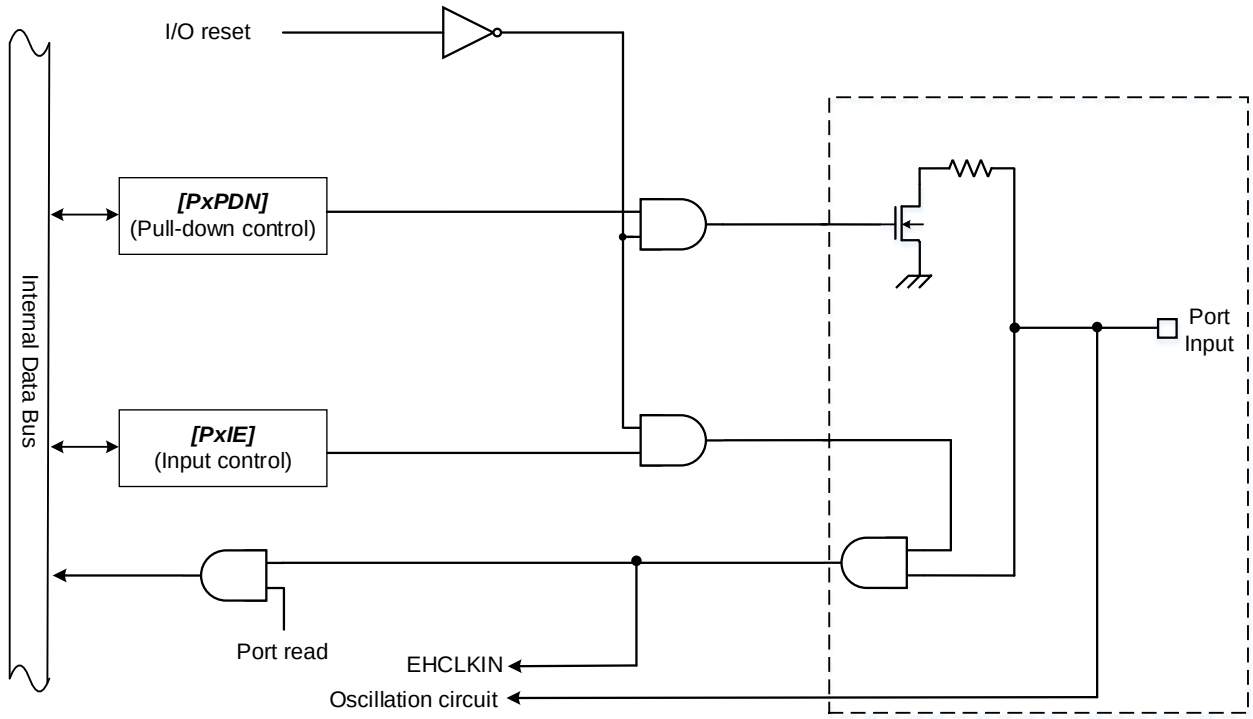


Figure 5.5 Port Type FT11a

5.6. Type FT16a

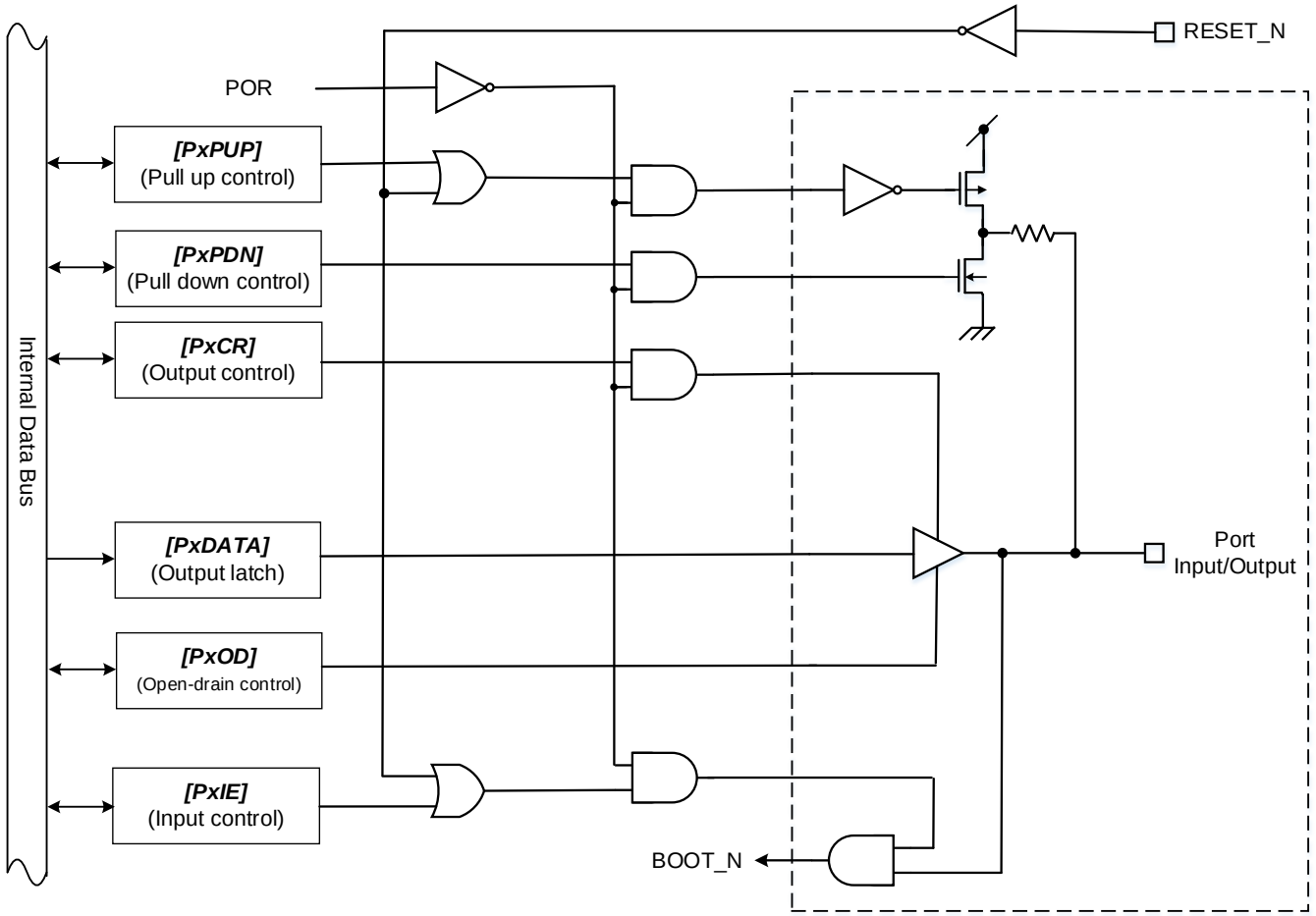


Figure 5.6 Port Type FT16a

6. Precaution

6.1. pin status during a reset period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is invalid.

- The debug interface alternate pins(PB0 to PB3) are debug pin status.
- PD0(BOOT_N) works as a BOOT function. It is enabled to be input and pulled-up during pin reset period. At the rising edge of the reset signal, if PD0 is "High", the device enters single chip mode and boots from the on chip flash memory. If PD0 is "Low", the device enters single BOOT mode and boots from the internal BOOT program.

6.2. Unused pins

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important points of using debug interface pins used as general-purpose ports

After releasing reset, If the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected

If the debug tool cannot be connected, it can recover debug connection to erase the flash memory using UART connection set as single BOOT mode from external. For details, please refer "Flash Memory" of reference manual.

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2018-09-20	- First release
1.1	2019-06-06	-1. Outlines Corrected Function Classification : “Debug pin” to “Debug pins”, “Control pin” to “Control pins” -4.2.4 PORT C revised as follows. PC0(UT0TXD → UT0TXDA ,input to output, ***[PCCR]***:0 → 1, ***[PCIE]***:1 → 0 UT0RXD: Ouput to Input, ***[PCCR]***:1 → 0, ***[PCIE]***: 0 → 1) PC1(UT0RXD:output → inputt, ***[PCCR]***:1 → 0, ***[PCIE]***:0 → 1 UT0TXD → UT0TXDA: Input → output, ***[PCCR]***:0 → 1, ***[PCIE]***: 1 → 0) -4.2.5 PORT D revised as follows. PD2(UT1TXDA: input → output, ***[PDCR]***:0 → 1, ***[PDIE]***:1 → 0 UT1RXD: Ouput → Input, ***[PDCR]***:1 → 0, ***[PDIE]***: 0 → 1) PD3(UT1RXD:output → inputt, ***[PDCR]***:1 → 0, ***[PDIE]***:0 → 1 UT1TXDA : Input → output, ***[PDCR]***:0 → 1, ***[PDIE]***: 1 → 0) -5. Block Diagrams of Ports Added description

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