32-Bit RISC Microcontroller

TMPM4L Group(1)

Reference Manual
Memory Map
(MMAP-M4L(1))

Revision 1.0

2018-09

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

Related documents

Document name
Arm documentation set for the Arm Cortex-M4

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "—", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder input Circuit (32-bit)
AO	Constant energization region (8bit Bus)
APB	Advanced Peripheral Bus
PMD+	Advanced Programmable Motor Control Circuit Plus
A-VE	Advanced Vector Engine
CG	Clock Control and Operation Mode
CRC	Cyclic Redundancy Check
DNF	Digital Noise Filter
IA(INTIF)	Interrupt control register A
IB(INTIF)	Interrupt control register B
IMN(INTIF)	Interrupt Monitor
IO	IO Bus(32bit Peripheral Bus)
LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
RAMP	RAM Parity
RLM	Low-speed oscillation / power supply control / reset
SIWDT	Clock Selective Watchdog timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event counter
UART	Universal Asynchronous Receiver Transmitter

1. Memory Map

The memory maps for TMPM4L Group(1) are based on the Arm® Cortex®-M4(with FPU) processor core memory map.

The internal ROM, internal RAM and special function registers (SFR) of TMPM4L Group(1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4(with FPU) respectively. The special function register (SFR) means the control registers of all input/output ports and peripheral functions.

The CPU register area is the processor core's internal register region.

For more information on each region, see the "Arm documentation set for the Arm Cortex-M4".

Note that access to regions indicated as "Fault" causes a memory fault if memory faults are enabled, or causes a hard fault if memory faults are disabled. Also, do not access the vendor-specific region.

1.1. TMPM4LxFW

- Code Flash : 128KB
- RAM : 6KB
- Product : TMPM4L2FWDUG, TMPM4L1FWUG

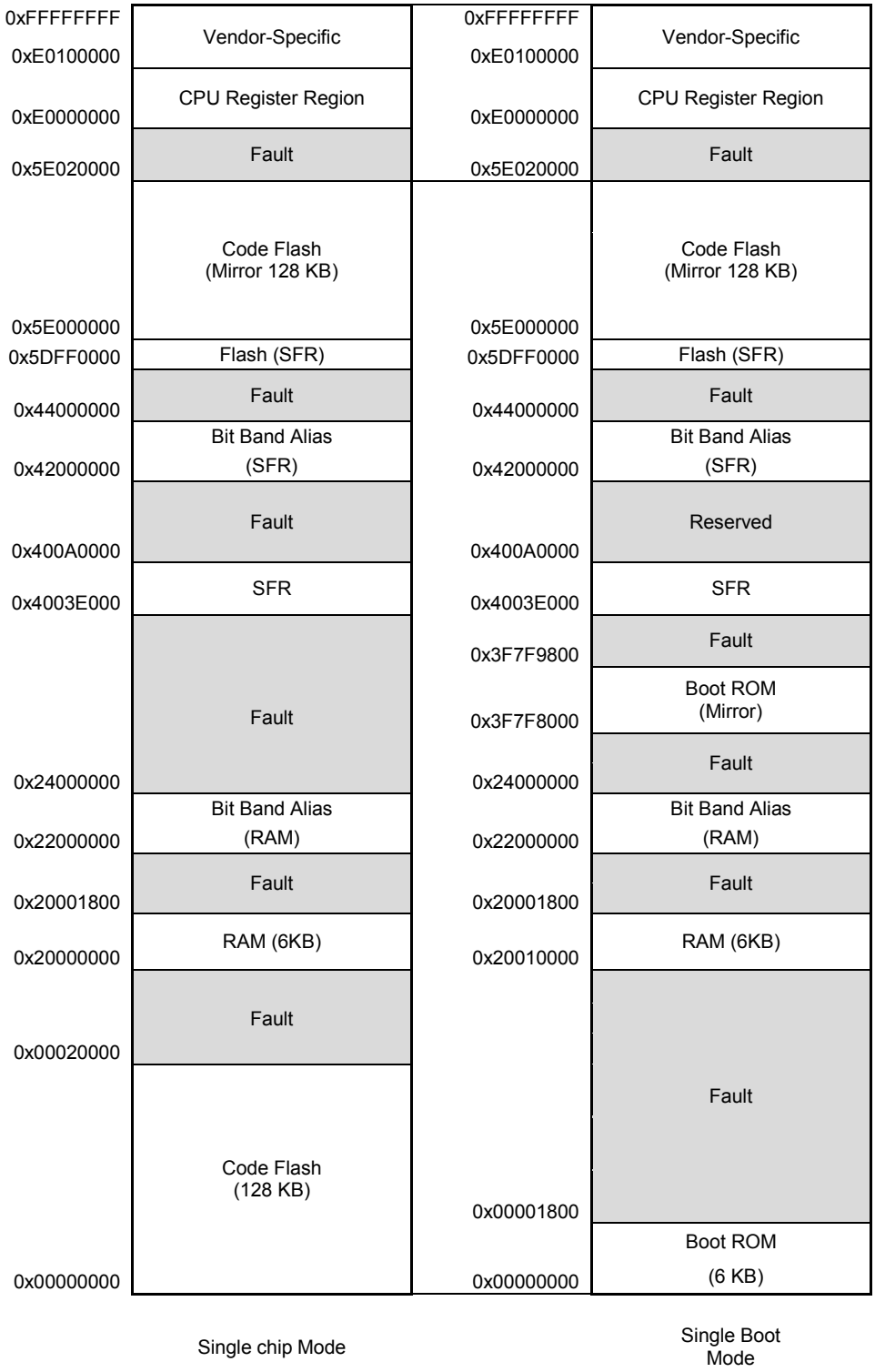

Figure 1.1 TMPM4LxFW

2. Bus Matrix

TMPM4L Group(1) contains one bus masters such as a CPU core.

Bus masters connect to slave ports (S0 to S2) of Bus Matrix. In the bus matrix, master ports (M0 to M7) connect to peripheral functions via connections described as (○) or (●) in the following figure. (●) shows a connection to a mirror area.

While multiple slaves are connected to the same bus master line in the Bus Matrix, if multiple slave accesses are generated at the same time, a priority is given to access from a master with the smallest slave number.

2.1. Structure

2.1.1. Single chip mode

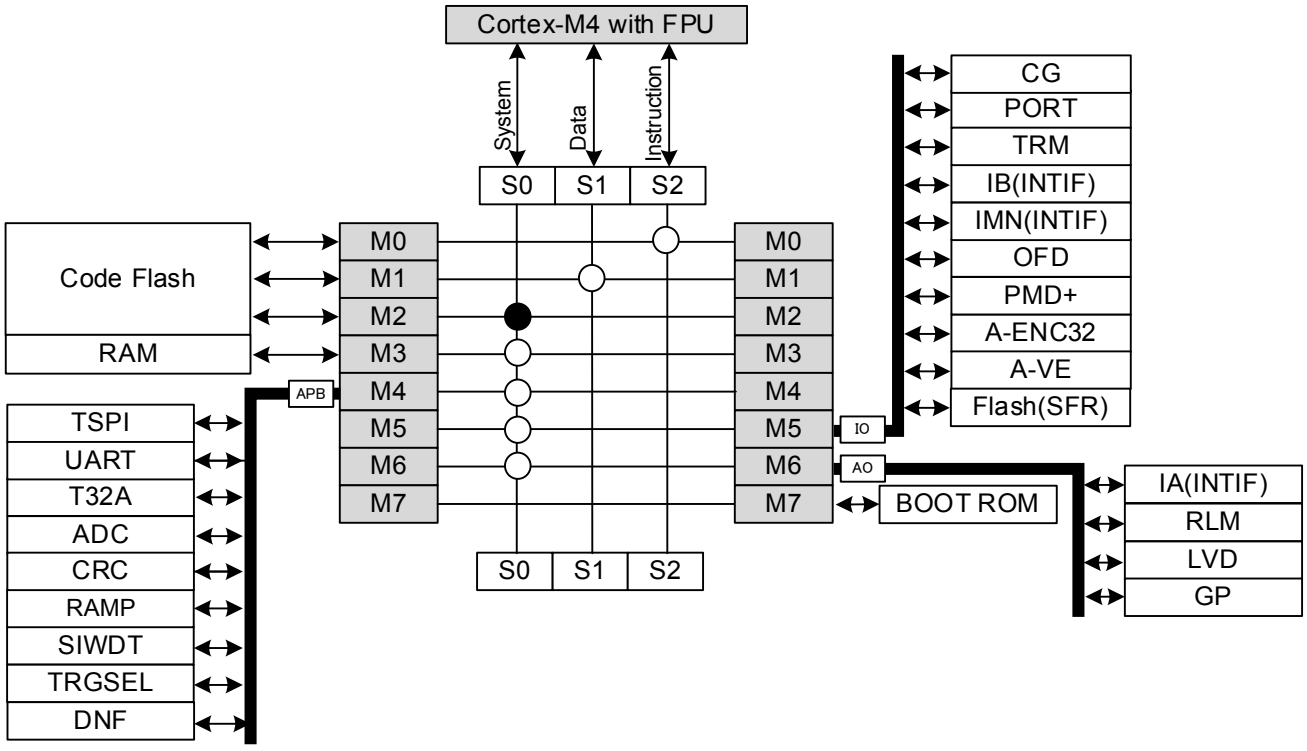

Figure 2.1 Single chip mode

2.1.2. Single boot mode

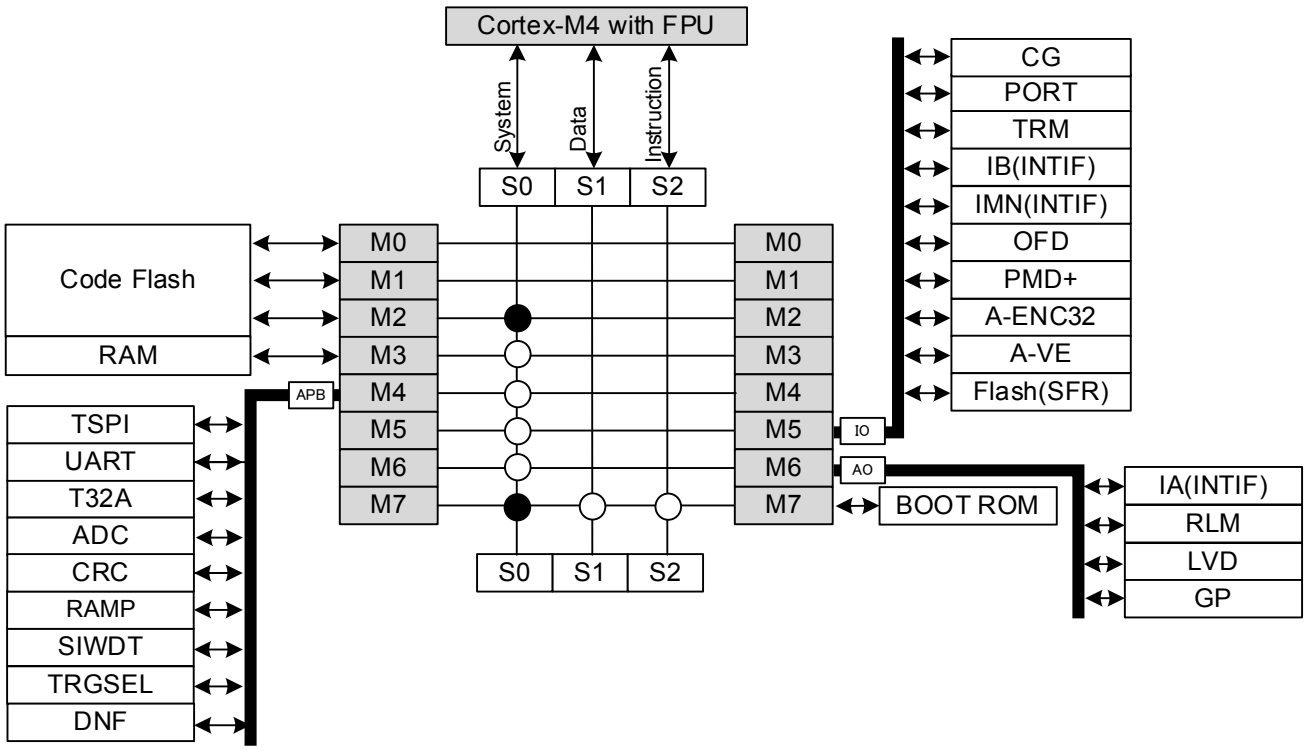

Figure 2.2 Single boot mode

2.2. Connection table

2.2.1. Code area / SRAM area

(1) Single chip mode

Table 2.1 Single chip mode

Start Address	Slave		Master		
			Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2
0x00000000	Code Flash	M0	—	—	✓
		M1	—	✓	—
0x00020000	Fault	—	—	Fault	Fault
0x20000000	RAM	M3	✓	—	—
0x20001800	Fault	—	Fault	—	—
0x22000000	Bit band alias	—	✓	—	—
0x24000000	Fault	—	Fault	—	—
For the address of this area, refer to "2.2.2 Peripheral area / External bus area"					
0x5E000000	Code Flash (Mirror)	M2	✓	—	—

✓: Accessible , —: Not accessible, Fault: Bus error

(2) Single boot mode

Table 2.2 Single boot mode

Start Address	Slave		Master		
			Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2
0x00000000	Boot ROM	M7	—	✓	✓
0x00001800	Fault	—	—	Fault	Fault
0x20000000	RAM	M3	✓	—	—
0x20001800	Fault	—	Fault	—	—
0x22000000	Bit band alias	—	✓	—	—
0x24000000	Fault	—	Fault	—	—
0x3F7F8000	Boot ROM(Mirror)	M7	✓	—	—
For the address of this area, refer to "2.2.2 Peripheral area / External bus area"					
0x5E000000	Code Flash (Mirror)	M2	✓	—	—

✓: Accessible , —: Not accessible, Fault: Bus error

2.2.2. Peripheral area / External bus area

Table 2.3 Peripheral area / External bus area

Start Address	Slave		Master		
			Core S-Bus	Core D-Bus	Core I-Bus
			S0	S1	S2
0x40000000	Fault	—	Fault	—	—
0x4003E000	IA(INTIF)	M6	✓	—	—
0x4003E400	RLM		✓	—	—
0x4003EC00	LVD		✓	—	—
0x4003FF00	AGPREG		✓	—	—
0x40040200	DNF	M4	✓	—	—
0x40040400	TRGSEL		✓	—	—
0x40040600	SIWDT		✓	—	—
0x40043000	RAMP		✓	—	—
0x40043100	CRC		✓	—	—
0x4005A000	ADC		✓	—	—
0x40061000	T32A		✓	—	—
0x4006A000	TSPI		✓	—	—
0x4006E000	UART		✓	—	—
0x40080000	PORT	M5	✓	—	—
0x40083000	CG		✓	—	—
0x40083100	TRM		✓	—	—
0x40083200	IB(INTIF)		✓	—	—
0x40083300	IMN(INTIF)		✓	—	—
0x40084000	OFD		✓	—	—
0x40089000	PMD+		✓	—	—
0x4008A000	A-ENC32		✓	—	—
0x4008B000	A-VE		✓	—	—
0x42000000	Bit Band Alias	—	✓	—	—
0x44000000	Fault	—	Fault	—	—
0x5DFF0000	Flash(SFR)	M5	✓	—	—

✓: Accessible , —: Not accessible, Fault: Bus error

3. Revision History

Table 3.1 Revision History

Revision	Date	Description
1.0	2018-09-11	- First release

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