32-Bit RISC Microcontroller

TMPM4L Group(1)

Reference Manual
Product Information
(PINFO-M4L(1))

Revision 1.1

2019-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

List of Figures

List of Tables

Preface

Related Document

Document name	IP Symbol
Input/output ports (TMPM4L Group(1))	PORT-M4L(1)
Clock Control and Operation Mode (TMPM4L Group(1))	CG-M4L(1)-A
Power Supply and Reset Operation (TMPM4L Group(1))	RESET-M4L(1)
Exception (TMPM4L Group(1))	EXCEPT-M4L(1)
Flash Memory	FLASH256-B
32-bit Timer Event Counter	T32A-B
Asynchronous Serial Communication Circuit	UART-C
Serial Peripheral Interface	TSPI-C
12-bit Analog to Digital Converter	ADC-D
Programmable Motor Control Circuit Plus	PMD+-B
32-bit Advanced Encoder Input Circuit	A-ENC32-A
Advanced Vector Engine	A-VE-A
Clock Selective Watchdog Timer	SIWDT-A
Oscillation Frequency Detector	OFD-A
Debug Interface	DEBUG-A
Digital Noise Filter Circuit	DNF-A
Trimming Circuit	TRM-A
Voltage Detection Circuit	LVD-B
CRC calculation circuit	CRC-A
RAM PARITY	RAMP-B

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, "x" means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] →[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, in the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—" , follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

The Flash memory uses the Super Flash® technology under license from Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviation

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder input Circuit(32-bit)
A-VE	Advanced Vector Engine
CRC	Cyclic Redundancy Check
DNF	Digital Noise Filter
EHOSC	External High Speed Oscillator
IHOSC	Internal High Speed Oscillator
INT	Interrupt
LVD	Voltage Detection Circuit
OFD	Oscillation Frequency Detector
PMD+	Programmable Motor Control Circuit Plus
RAMP	RAM parity
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

This chapter describes the information which relates to peripheral functions about the channel or unit count, the pin information, and the product specific function. Use this document together with Reference manuals for peripheral functions.

2. Information of Peripheral Function

2.1. Register Base Address

The register base address type of TMPM4L group(1) is shown below.

Table 2.1 Type of the register base address

Peripheral function			Base address type (✓: Available, —: N/A)			Base Address
			TYPE1	TYPE2	TYPE3	
Voltage Detection Circuit	LVD	—	✓	—	—	0x4003EC00
Digital Noise Filter Circuit	DNF	unit A	—	—	✓	0x40040200
Clock Selective Watchdog Timer	SIWDT	ch0	—	—	✓	0x40040600
RAM Parity	RAMP	ch0	—	—	✓	0x40043000
CRC	CRC	—	—	—	✓	0x40043100
12-bit Analog to Digital Converter	ADC	unit A	—	—	✓	0x4005A000
32-bit Timer Event Counter	T32A (ch0 to 3)	ch0	—	—	✓	0x40061000
		ch1				0x40061400
		ch2				0x40061800
		ch3				0x40061C00
Serial Peripheral Interface	TSPI (ch0 to 2)	ch0	—	—	✓	0x4006A000
		ch1				0x4006A400
		ch2				0x4006A800
Asynchronous Serial Communication	UART (ch0 to 2)	ch0	—	—	✓	0x4006E000
		ch1				0x4006E400
		ch2				0x4006E800
Trimming Circuit	TRM	—	—	—	✓	0x40083100
Oscillation Frequency Detector	OFD	—	—	—	✓	0x40084000
Programmable Motor Control Circuit Plus	PMD+	ch0	—	—	✓	0x40089000
Advanced Encoder input Circuit(32-bit)	A-ENC32	ch0	—	—	✓	0x4008A000
Advanced Vector Engine	A-VE	ch0	—	—	✓	0x4008B000
Flash Memory	Flash	—	✓	—	—	0x5DFF0000

Each peripheral function should be developed using the type of the base address.

2.2. Trigger Selector (TRGSEL)

The trigger selector is the circuit which chooses the one trigger from two or more triggers inputted from the peripheral function, and outputs the trigger signal to the peripheral function.

The trigger selected from eight triggers by ***[TSEL0CRn]*** <INSELm> is outputted to the peripheral function of a connection destination.

"Figure 2.1 Example of Trigger Selector Connection" shows an example of which the trigger signal outputted from 32-bit timer event counter (T32A ch1) connects to TSPI(ch0)/UART(ch0) via trigger selector. The input trigger selection and trigger output control is performed by ***[TSEL0CR3]***.

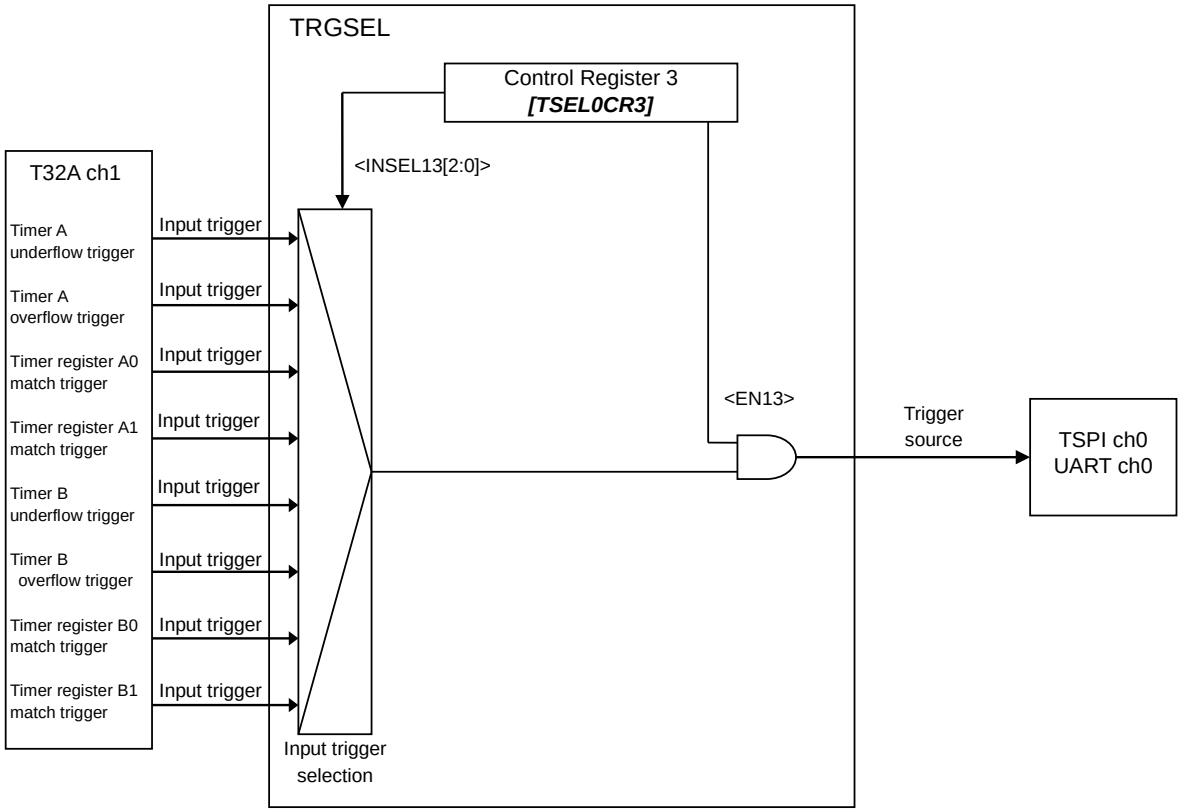

Figure 2.1 Example of the trigger selector connection

2.2.1. Trigger Selector per Product

TMPM4L group(1) trigger group selector consists of 4 control registers (***[TSEL0CR0-3]***), and can control 16 triggers.

The control register, the connection destination, and correspondence products are shown in the following table.

Table 2.2 List of the trigger selectors per product (1/2)

Register	Bit Symbol	Trigger source	Input trigger	Product table (✓: Available, —: N/A) M4L2	M4L1
[TSEL0CR0]	INSEL0[2:0]	T32A ch0 Timer A	T32A ch0 Timer B underflow trigger T32A ch0 Timer B overflow trigger T32A ch0 Timer register B0 match trigger T32A ch0 Timer register B1 match trigger	✓	✓
	INSEL1[2:0]	T32A ch0 Timer B	T32A ch0 Timer A underflow trigger T32A ch0 Timer A overflow trigger T32A ch0 Timer register A0 match trigger T32A ch0 Timer register A1 match trigger	✓	✓
			ADC unit A General purpose trigger interrupt / Single conversion interrupt / Continuous conversion interrupt / Monitor function 0 interrupt / Monitor function 1 interrupt	✓	✓
	INSEL2[2:0]	T32A ch1 Timer A	T32A ch1 Timer B underflow trigger T32A ch1 Timer B overflow trigger T32A ch1 Timer register B0 match trigger T32A ch1 Timer register B1 match trigger	✓	✓
			UART ch0 Reception completion trigger UART ch0 Transmission completion trigger	✓	✓
			TSPI ch0 Receive Completion TSPI ch0 Transmit Completion	✓	✓
	INSEL3[2:0]	T32A ch1 Timer B	T32A ch1 Timer A underflow trigger T32A ch1 Timer A overflow trigger T32A ch1 Timer register A0 match trigger T32A ch1 Timer register A1 match trigger	✓	✓
[TSEL0CR1]	INSEL4[2:0]	T32A ch2 Timer A	T32A ch2 Timer B underflow trigger T32A ch2 Timer B overflow trigger T32A ch2 Timer register B0 match trigger T32A ch2 Timer register B1 match trigger	✓	✓
			UART ch1 Reception completion trigger UART ch1 Transmission completion trigger	✓	✓
			TSPI ch1 Receive Completion TSPI ch1 Transmit Completion	✓	✓
	INSEL5[2:0]	T32A ch2 Timer B	T32A ch2 Timer A underflow trigger T32A ch2 Timer A overflow trigger T32A ch2 Timer register A0 match trigger T32A ch2 Timer register A1 match trigger	✓	✓
			A-ENC32 ch0 Divided pulse signal	✓	✓
	INSEL6[2:0]	T32A ch3 Timer A	T32A ch3 Timer B underflow trigger T32A ch3 Timer B overflow trigger T32A ch3 Timer register B0 match trigger T32A ch3 Timer register B1 match trigger	✓	✓
			UART ch2 Reception completion trigger UART ch2 Transmission completion trigger	✓	✓
			TSPI ch2 Receive Completion TSPI ch2 Transmit Completion	✓	✓
	INSEL7[2:0]	T32A ch3 Timer B	T32A ch3 Timer A underflow trigger T32A ch3 Timer A overflow trigger T32A ch3 Timer register A0 match trigger T32A ch3 Timer register A1 match trigger	✓	✓

Table 2.3 List of the trigger selectors per product (2/2)

Register	Bit Symbol	Trigger source	Input trigger	Product table (✓: Available, —: N/A) M4L2	M4L1
[TSEL0CR2]	INSEL8[2:0]	T32A ch1 Timer C	T32A ch3 Timer C underflow trigger T32A ch3 Timer C overflow trigger T32A ch3 Timer register C0 match trigger T32A ch3 Timer register C1 match trigger	✓	✓
	INSEL9[2:0]	T32A ch0 Timer C	T32A ch2 Timer C underflow trigger T32A ch2 Timer C overflow trigger T32A ch2 Timer register C0 match trigger T32A ch2 Timer register C1 match trigger	✓	✓
	INSEL10[2:0]	T32A ch3 Timer C	T32A ch1 Timer C underflow trigger T32A ch1 Timer C overflow trigger T32A ch1 Timer register C0 match trigger T32A ch1 Timer register C1 match trigger	✓	✓
	INSEL11[2:0]	T32A ch2 Timer C	T32A ch0 Timer C underflow trigger T32A ch0 Timer C overflow trigger T32A ch0 Timer register C0 match trigger T32A ch0 Timer register C1 match trigger	✓	✓
[TSEL0CR3]	INSEL12[2:0]	ADC unit A	T32A ch0 Timer B underflow trigger T32A ch0 Timer B overflow trigger T32A ch0 Timer register B0 match trigger T32A ch0 Timer register B1 match trigger	✓	✓
	INSEL13[2:0]	TSPI ch0 UART ch0	T32A ch1 Timer A underflow trigger T32A ch1 Timer A overflow trigger T32A ch1 Timer register A0 match trigger T32A ch1 Timer register A1 match trigger T32A ch1 Timer B underflow trigger T32A ch1 Timer B overflow trigger T32A ch1 Timer register B0 match trigger T32A ch1 Timer register B1 match trigger	✓	✓
	INSEL14[2:0]	TSPI ch1 UART ch1	T32A ch2 Timer A underflow trigger T32A ch2 Timer A overflow trigger T32A ch2 Timer register A0 match trigger T32A ch2 Timer register A1 match trigger T32A ch2 Timer B underflow trigger T32A ch2 Timer B overflow trigger T32A ch2 Timer register B0 match trigger T32A ch2 Timer register B1 match trigger	✓	✓
	INSEL15[2:0]	TSPI ch2 UART ch2	T32A ch3 Timer A underflow trigger T32A ch3 Timer A overflow trigger T32A ch3 Timer register A0 match trigger T32A ch3 Timer register A1 match trigger T32A ch3 Timer B underflow trigger T32A ch3 Timer B overflow trigger T32A ch3 Timer register B0 match trigger T32A ch3 Timer register B1 match trigger	✓	✓

2.2.2. Operation and setting

When using TRGSEL, please set an applicable clock enable bit to "1" (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***, ***[CGFSYSMENB]***), and fc supply stop registers (***[CGFCEN]***).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

Setting procedure of trigger selector is as following.

(1) Selection of an input trigger (***[TSEL0CRn]*** <INSELm>)

Selection of the input trigger used for the trigger source is performed.

Please set up selection of the input trigger by the input trigger subdevice bit (***[TSEL0CRn]*** <INSELm>) of the control register. (n: register number, m: trigger number)

(2) Output enable (***[TSEL0CRn]***<ENm>)

The output (enable/disable) of the selected trigger signal is chosen.

Please set up selection of output (enable/disable) in the setting bit (***[TSEL0CRn]***<ENm>) of a control register. A trigger output will be enabled if ***[TSEL0CRn]***<ENm> is set as "1".

2.2.3. List of Registers

The control registers and their addresses are shown in the following tables.

Peripheral function		Channel/Unit	Base address
Trigger Selector	TRGSEL	ch0	0x40040400

Register name		Address (Base+)
Control Register 0	***[TSEL0CR0]***	0x0000
Control Register 1	***[TSEL0CR1]***	0x0004
Control Register 2	***[TSEL0CR2]***	0x0008
Control Register 3	***[TSEL0CR3]***	0x000C

2.2.4. Details of Registers

The following chapters show the details of a register.

The corresponding signal name is shown in parentheses in the column "Description".

2.2.4.1. *[TSEL0CR0]* (Control Register 0)

Bit	Bit Symbol	After Reset	Type	Description
31	—	0	R	Read as "0".
30:28	INSEL3[2:0]	000	R/W	Input trigger selection (T32A ch1 Timer B internal trigger input) 000: T32A ch1 Timer A underflow trigger (T32A01TRGOUTUFA) 001: T32A ch1 Timer A overflow trigger (T32A01TRGOUTOFA) 010: T32A ch1 Timer register A0 match trigger (T32A01TRGOUTCMPA0) 011: T32A ch1 Timer register A1 match trigger (T32A01TRGOUTCMPA1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	—	0	R	Read as "0".
26:25	—	00	R/W	Write as "00".
24	EN3	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	—	0	R	Read as "0".
22:20	INSEL2[2:0]	000	R/W	Input trigger selection (T32A ch1 Timer A internal trigger input) 000: T32A ch1 Timer B underflow trigger (T32A01TRGOUTUFB) 001: T32A ch1 Timer B overflow trigger (T32A01TRGOUTOFB) 010: T32A ch1 Timer register B0 match trigger (T32A01TRGOUTCMPB0) 011: T32A ch1 Timer register B1 match trigger (T32A01TRGOUTCMPB1) 100: UART ch0 Reception completion trigger (UART0RXTRG) 101: UART ch0 Transmission completion trigger (UART0TXTRG) 110: TSPI ch0 Receive Completion (TSPI0RXEND) 111: TSPI ch0 Transmit Completion (TSPI0TXEND)
19	—	0	R	Read as "0".
18:17	—	00	R/W	Write as "00".
16	EN2	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	—	0	R	Read as "0".

Bit	Bit Symbol	After Reset	Type	Description
14:12	INSEL1[2:0]	000	R/W	Input trigger selection (T32A ch0 Timer B internal trigger input) 000: T32A ch0 Timer A underflow trigger (T32A00TRGOUTUFA) 001: T32A ch0 Timer A overflow trigger (T32A00TRGOUTOFA) 010: T32A ch0 Timer register A0 match trigger (T32A00TRGOUTCMPA0) 011: T32A ch0 Timer register A1 match trigger (T32A00TRGOUTCMPA1) 100: ADC unit A General purpose trigger interrupt (INTADATRG) Single conversion interrupt (INTADASGL) Continuous conversion interrupt (INTADACNT) Monitor function 0 interrupt (INTADACP0) Monitor function 1 interrupt (INTADACP1) 101: Reserved 110: Reserved 111: Reserved
11	—	0	R	Read as "0".
10:9	—	00	R/W	Write as "00".
8	EN1	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	—	0	R	Read as "0".
6:4	INSEL0[2:0]	000	R/W	Input trigger selection (T32A ch0 Timer A internal trigger input) 000: T32A ch0 Timer B underflow trigger (T32A00TRGOUTUFB) 001: T32A ch0 Timer B overflow trigger (T32A00TRGOUTOFB) 010: T32A ch0 Timer register B0 match trigger (T32A00TRGOUTCMPB0) 011: T32A ch0 Timer register B1 match trigger (T32A00TRGOUTCMPB1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	—	0	R	Read as "0".
2:1	—	00	R/W	Write as "00".
0	EN0	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.2. *[TSEL0CR1]* (Control Register 1)

Bit	Bit Symbol	After Reset	Type	Description
31	—	0	R	Read as "0".
30:28	INSEL7[2:0]	000	R/W	Input trigger selection (T32A ch3 Timer B internal trigger input) 000: T32A ch3 Timer A underflow trigger (T32A03TRGOUTUFA) 001: T32A ch3 Timer A overflow trigger (T32A03TRGOUTOFA) 010: T32A ch3 Timer register A0 match trigger (T32A03TRGOUTCMPA0) 011: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	—	0	R	Read as "0".
26:25	—	00	R/W	Write as "00".
24	EN7	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	—	0	R	Read as "0".
22:20	INSEL6[2:0]	000	R/W	Input trigger selection (T32A ch3 Timer A internal trigger input) 000: T32A ch3 Timer B underflow trigger (T32A03TRGOUTUFB) 001: T32A ch3 Timer B overflow trigger (T32A03TRGOUTOFB) 010: T32A ch3 Timer register B0 match trigger (T32A03TRGOUTCMPB0) 011: T32A ch3 Timer register B1 match trigger (T32A03TRGOUTCMPB1) 100: UART ch2 Reception completion trigger (UART2RXTRG) 101: UART ch2 Transmission completion trigger (UART2TXTRG) 110: TSPI ch2 Receive Completion (TSPI2RXEND) 111: TSPI ch2 Transmit Completion (TSPI2TXEND)
19	—	0	R	Read as "0".
18:17	—	00	R/W	Write as "00".
16	EN6	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	—	0	R	Read as "0".
14:12	INSEL5[2:0]	000	R/W	Input trigger selection (T32A ch2 Timer B internal trigger input) 000: T32A ch2 Timer A underflow trigger (T32A02TRGOUTUFA) 001: T32A ch2 Timer A overflow trigger (T32A02TRGOUTOFA) 010: T32A ch2 Timer register A0 match trigger (T32A02TRGOUTCMPA0) 011: T32A ch2 Timer register A1 match trigger (T32A02TRGOUTCMPA1) 100: A-ENC32 ch0 Divided pulse signal (ENC0TIMPLS) 101: Reserved 110: Reserved 111: Reserved
11	—	0	R	Read as "0".
10:9	—	00	R/W	Write as "00".
8	EN5	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	—	0	R	Read as "0".

Bit	Bit Symbol	After Reset	Type	Description
6:4	INSEL4[2:0]	000	R/W	Input trigger selection (T32A ch2 Timer A internal trigger input) 000: T32A ch2 Timer B underflow trigger (T32A02TRGOUTUFB) 001: T32A ch2 Timer B overflow trigger (T32A02TRGOUTOFB) 010: T32A ch2 Timer register B0 match trigger (T32A02TRGOUTCMPB0) 011: T32A ch2 Timer register B1 match trigger (T32A02TRGOUTCMPB1) 100: UART ch1 Reception completion trigger (UART1RXTRG) 101: UART ch1 Transmission completion trigger (UART1TXTRG) 110: TSPI ch1 Receive Completion (TSPI1RXEND) 111: TSPI ch1 Transmit Completion (TSPI1TXEND)
3	—	0	R	Read as "0".
2:1	—	00	R/W	Write as "00".
0	EN4	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.3. *[TSEL0CR2]* (Control Register 2)

Bit	Bit Symbol	After Reset	Type	Description
31	—	0	R	Read as "0".
30:28	INSEL11[2:0]	000	R/W	Input trigger selection (T32A ch2 Timer C internal trigger input) 000: T32A ch0 Timer C underflow trigger (T32A00TRGOUTUFC) 001: T32A ch0 Timer C overflow trigger (T32A00TRGOUTOFC) 010: T32A ch0 Timer register C0 match trigger (T32A00TRGOUTCMPC0) 011: T32A ch0 Timer register C1 match trigger (T32A00TRGOUTCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	—	0	R	Read as "0".
26:25	—	00	R/W	Write as "00".
24	EN11	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	—	0	R	Read as "0".
22:20	INSEL10[2:0]	000	R/W	Input trigger selection (T32A ch3 Timer C internal trigger input) 000: T32A ch1 Timer C underflow trigger (T32A01TRGOUTUFC) 001: T32A ch1 Timer C overflow trigger (T32A01TRGOUTOFC) 010: T32A ch1 Timer register C0 match trigger (T32A01TRGOUTCMPC0) 011: T32A ch1 Timer register C1 match trigger (T32A01TRGOUTCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	—	0	R	Read as "0".
18:17	—	00	R/W	Write as "00".
16	EN10	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	—	0	R	Read as "0".
14:12	INSEL9[2:0]	000	R/W	Input trigger selection (T32A ch0 Timer C internal trigger input) 000: T32A ch2 Timer C underflow trigger (T32A02TRGOUTUFC) 001: T32A ch2 Timer C overflow trigger (T32A02TRGOUTOFC) 010: T32A ch2 Timer register C0 match trigger (T32A02TRGOUTCMPC0) 011: T32A ch2 Timer register C1 match trigger (T32A02TRGOUTCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	—	0	R	Read as "0".
10:9	—	00	R/W	Write as "00".
8	EN9	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	—	0	R	Read as "0".

Bit	Bit Symbol	After Reset	Type	Description
6:4	INSEL8[2:0]	000	R/W	Input trigger selection (T32A ch1 Timer C internal trigger input) 000: T32A ch3 Timer C underflow trigger (T32A03TRGOUTUFC) 001: T32A ch3 Timer C overflow trigger (T32A03TRGOUTOFC) 010: T32A ch3 Timer register C0 match trigger (T32A03TRGOUTCMPC0) 011: T32A ch3 Timer register C1 match trigger (T32A03TRGOUTCMPC1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	—	0	R	Read as "0".
2:1	—	00	R/W	Write as "00".
0	EN8	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.2.4.4. *[TSEL0CR3]* (Control Register 3)

Bit	Bit Symbol	After Reset	Type	Description
31	—	0	R	Read as "0".
30:28	INSEL15[2:0]	000	R/W	Input trigger selection (TSPI ch2 / UART ch2 Trigger input) 000: T32A ch3 Timer A underflow trigger (T32A03TRGOUTUFA) 001: T32A ch3 Timer A overflow trigger (T32A03TRGOUTOFA) 010: T32A ch3 Timer register A0 match trigger (T32A03TRGOUTCMPA0) 011: T32A ch3 Timer register A1 match trigger (T32A03TRGOUTCMPA1) 100: T32A ch3 Timer B underflow trigger (T32A03TRGOUTUFB) 101: T32A ch3 Timer B overflow trigger (T32A03TRGOUTOFB) 110: T32A ch3 Timer register B0 match trigger (T32A03TRGOUTCMPB0) 111: T32A ch3 Timer register B1 match trigger (T32A03TRGOUTCMPB1)
27	—	0	R	Read as "0".
26:25	—	00	R/W	Write as "00".
24	EN15	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
23	—	0	R	Read as "0".
22:20	INSEL14[2:0]	000	R/W	Input trigger selection (TSPI ch1 / UART ch1 Trigger input) 000: T32A ch2 Timer A underflow trigger (T32A02TRGOUTUFA) 001: T32A ch2 Timer A overflow trigger (T32A02TRGOUTOFA) 010: T32A ch2 Timer register A0 match trigger (T32A02TRGOUTCMPA0) 011: T32A ch2 Timer register A1 match trigger (T32A02TRGOUTCMPA1) 100: T32A ch2 Timer B underflow trigger (T32A02TRGOUTUFB) 101: T32A ch2 Timer B overflow trigger (T32A02TRGOUTOFB) 110: T32A ch2 Timer register B0 match trigger (T32A02TRGOUTCMPB0) 111: T32A ch2 Timer register B1 match trigger (T32A02TRGOUTCMPB1)
19	—	0	R	Read as "0".
18:17	—	00	R/W	Write as "00".
16	EN14	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
15	—	0	R	Read as "0".
14:12	INSEL13[2:0]	000	R/W	Input trigger selection (TSPI ch0 / UART ch0 Trigger input) 000: T32A ch1 Timer A underflow trigger (T32A01TRGOUTUFA) 001: T32A ch1 Timer A overflow trigger (T32A01TRGOUTOFA) 010: T32A ch1 Timer register A0 match trigger (T32A01TRGOUTCMPA0) 011: T32A ch1 Timer register A1 match trigger (T32A01TRGOUTCMPA1) 100: T32A ch1 Timer B underflow trigger (T32A01TRGOUTUFB) 101: T32A ch1 Timer B overflow trigger (T32A01TRGOUTOFB) 110: T32A ch1 Timer register B0 match trigger (T32A01TRGOUTCMPB0) 111: T32A ch1 Timer register B1 match trigger (T32A01TRGOUTCMPB1)
11	—	0	R	Read as "0".
10:9	—	00	R/W	Write as "00".
8	EN13	0	R/W	Trigger output control 0: Disabled. 1: Enabled.
7	—	0	R	Read as "0".

Bit	Bit Symbol	After Reset	Type	Description
6:4	INSEL12[2:0]	000	R/W	Input trigger selection (ADC unit A General purpose trigger) 000: T32A ch0 Timer B underflow trigger (T32A00TRGOUTUFB) 001: T32A ch0 Timer B overflow trigger (T32A00TRGOUTOFB) 010: T32A ch0 Timer register B0 match trigger (T32A00TRGOUTCMPB0) 011: T32A ch0 Timer register B1 match trigger (T32A00TRGOUTCMPB1) 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	—	0	R	Read as "0".
2:1	—	00	R/W	Write as "00".
0	EN12	0	R/W	Trigger output control 0: Disabled. 1: Enabled.

2.3. Clock Selective Watchdog Timer (SIWDT)

2.3.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.4 SIWDT built-in channel

Product	SIWDT channel (✓: Available, —: N/A)
	ch0
M4L2	✓
M4L1	✓

2.3.2. Count clock

The SIWDT can select the clock to count. The clock which can be selected as the following table is shown.

Table 2.5 SIWDT count clock

Clock	Signal name	Selection
System clock	fsys	It selects by the ***[SIWD0MOD]***<WDCLS> register.
Internal High Speed Oscillator 1 Clock	f_{IHOSC1}	
Internal High Speed Oscillator 2 Clock	f_{IHOSC2}	

2.3.3. Oscillation clock protection function

When the Internal High Speed Oscillator 2 (f_{IHOSC2}) is chosen, it is possible to forbid rewriting of the Internal High Speed Oscillator 2.

Table 2.6 SIWDT Oscillation clock protection function

Control Output	Signal name	Remarks
The protection signal of an Internal High Speed Oscillator 2 oscillation control bit (***[CGOSCCR]***<IHOSC2EN>).	OSCPRO	It sets up by the ***[SIWD0OSCCR]***<OSCPRO> register.

2.4. Oscillation Frequency Detection Circuit (OFD)

2.4.1. Built-in List

The following table shows the built-in list for each product.

Table 2.7 Built-in List

Product	Built-in OFD (✓: Available, —: N/A)
M4L2	✓
M4L1	✓

2.4.2. Reference clock

The OFD operates with the clock in the following table as the reference clock.

Table 2.8 OFD reference clock

Reference clock	Signal name	Divide value
Internal High speed oscillator 2	f_{IHOSC2}	256

2.4.3. Detection object clock

The OFD selects clock to monitor from the detection object clock of the following table.

Table 2.9 OFD clock for detection

Detection target clock		Signal name
Input signal	External High speed oscillator clock	f_{EHOSC}
	Selected clock by the ***[CGOSCCR]***<OSCSEL> and ***[CGPLL0SEL]***<PLL0SEL> in CG(Clock control block)	fc

2.5. Debug Interface

2.5.1. Debugging interface terminal list of each product.

Table 2.10 Debugging interface terminal list

Debug function	Debug pin	Port	Product table (✓: Available, —: N/A)	
			M4L2	M4L1
Serial wire	SWDIO	PB0	✓	✓
	SWCLK	PB1	✓	✓
	SWV	PB2	✓	✓
JTAG	TMS	PB0	✓	✓
	TCK	PB1	✓	✓
	TDO	PB2	✓	✓
	TDI	PB3	✓	✓
	TRST_N	(Note 1)	—	—

Note 1: No terminal
Note 2: There is no ETM trace.

2.6. Flash Memory (FLASH)

2.6.1. Clock for the programming/erasing

As for flash memory, the clock of the following tables is used for programming/erasing of the code flash or the data flash.

Table 2.11 Clock for programming/erasing

Clock for programming/erasing
f_{IHOSC1}

Note: The oscillation control register is ***[CGOSCCR]***<IHOSC1EN>.

2.6.2. The code flash block configuration of each product

The code flash memory differs in the block configuration of the memory with the product, as shown in the following table.

Table 2.12 The code flash (Block) of each product

Area	Block name		M4L2FW M4L1FW	Block size (KB)
0	Block0	PG0	✓	4
		PG1	✓	4
		PG2	✓	4
		PG3	✓	4
		PG4	✓	4
		PG5	✓	4
		PG6	✓	4
		PG7	✓	4
	Block1		✓	32
	Block2		✓	32
	Block3		✓	32

2.6.3. Single boot use resource

The peripheral function of the following table is used in single boot.

Table 2.13 Single boot use resource

Peripheral function	Channel	Function	Pin name
BOOT	—	—	PD0 (BOOT_N)
UART	ch0	RXD	PC1 (UT0RXD)
		TXD	PC0 (UT0TXDA)
T32A	ch0	—	—

Table 2.14 The end address in which RAM transmission is possible

Product name	The end address in which RAM transmission is possible
TMPM4L2FWDUG TMPM4L1FWUG	0x20000400 to 0x200017FF

2.7. Programmable Motor Control Circuit Plus (PMD+)

2.7.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.15 PMD+ built-in channel

Product	PMD+ channel (✓: Available, —: N/A)
	ch0
M4L2	✓
M4L1	✓

2.7.2. Function pin and port

The functional terminal is assigned to the following ports.

Table 2.16 PMD+ functional pin

Channel	Function pin		Port	Product table (✓: Available, —: N/A)	
				M4L2	M4L1
ch0	UO0	Output	PE0	✓	✓
	VO0	Output	PE2	✓	✓
	WO0	Output	PE4	✓	✓
	XO0	Output	PE1	✓	✓
	YO0	Output	PE3	✓	✓
	ZO0	Output	PE5	✓	✓
	EMG0_N	Input	PE6	✓	✓
	OVV0_N	Input	PE7	✓	✓

2.7.3. Internal signal connection specification

2.7.3.1. ADC / A-ENC32 / A-VE / T32A connection

PMD+ has a signal internally connected to the peripheral function as shown in the table below.

Table 2.17 PMD+ Internal signal connection specification: Input

Channel	Signal input		Input source	
		Signal name		Signal name
ch0	OVV state signal (AD monitor function 0)	ADACMP0L_N	ADC unit A	ADACP0L_N
	OVV state signal (AD monitor function 1)	ADACMP1L_N		ADACP1L_N
	Commutation trigger (A-ENC position detection synchronization)	INTENC00	A-ENC32 ch0	INTENC00
	Commutation trigger (General-purpose timer synchronization)	PMD0TMR	T32A ch2 Timer B	T32A02TRGOUTCMPB0
	Commutation trigger (A-ENC MCMP completion synchronization)	ENC0CTRGO	A-ENC32 ch0	ENC0CTRGO
	VE U-phase PWM Duty	VE0CMPU	A-VE ch0	VE0CMPU
	VE V-phase PWM Duty	VE0CMPV		VE0CMPV
	VE W-phase PWM Duty	VE0CMPW		VE0CMPW
	VE Trigger compare 0	VE0TRGCMP0		VE0TRGCMP0
	VE Trigger compare 1	VE0TRGCMP1		VE0TRGCMP1
	VE Synchronous trigger output selection	VE0TRGSEL		VE0TRGSEL
	VE Conduction control / output control	VE0OUTCR		VE0OUTCR
	VE EMG return	VE0EMGRS		VE0EMGRS

Table 2.18 PMD+ Internal signal connection specification: Output

Channel	Signal Output		Output destination	
		Signal name		Signal name
ch0	ADC synchronous sampling output 0	PMD0TRG0	ADC unit A	PMDTRG0
	ADC synchronous sampling output 1	PMD0TRG1		PMDTRG1
	ADC synchronous sampling output 2	PMD0TRG2		PMDTRG2
	ADC synchronous sampling output 3	PMD0TRG3		PMDTRG3
	ADC synchronous sampling output 4	PMD0TRG4		PMDTRG4
	ADC synchronous sampling output 5	PMD0TRG5		PMDTRG5
	PWM signal for the encoder input	PMD0PWMON	A-ENC32 ch0	ENC0PWMON
	PWM interrupt	INTPWM0	A-VE ch0	INTPWM0

2.8. Advanced Encoder Input Circuit(32-bit) (A-ENC32)

2.8.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.19 A-ENC32 built-in channel

Product	A-ENC32 channel (✓: Available, —: N/A)
	ch0
M4L2	✓
M4L1	✓

2.8.2. Function pin and port

The functional terminal is assigned to the following ports.

Table 2.20 A-ENC32 Function pin and port

Channel	Function pin		Port	Product table (✓: Available, —: N/A)	
				M4L2	M4L1
ch0	ENC0A	Input	PD1	✓	✓
	ENC0B	Input	PD2	✓	✓
	ENC0Z	Input	PD3	✓	✓

2.8.3. Internal signal connection specification

2.8.3.1. PMD+ / T32A connection

A-ENC32 has a signal internally connected to the peripheral function as shown in the table below.

"—" in the table does not have the corresponding function.

Table 2.21 A-ENC32 Internal signal connection specification: Input

Channel	Signal input		Input source	
		Signal name		Signal name
ch0	General purpose timer output signal	ENC0PSGI	T32A ch2 Timer B	T32A02OUTB
	PWM signal for sampling	ENC0PWMON	PMD+ ch0	PMD0PWMON

Table 2.22 A-ENC32 signal connection specification: Output

Channel	Signal Output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	Division pulse signal	ENC0TIMPLS	***[TSEL0CR1]*** <INSEL5>	T32A ch2 Timer B	T32A02TRGINBPCK
	Commutation trigger for PMD	ENC0CTRGO	—	PMD+ ch0	ENC0CTRGO
	Encoder input interrupt 0	INTENC00	—		INTENC00

2.9. Advanced Vector Engine (A-VE)

2.9.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.23 A-VE built-in channel

Product	A-VE channel (✓: Available, —: N/A)
	ch0
M4L2	✓
M4L1	✓

2.9.2. Internal signal connection specification

2.9.2.1. PMD+ / ADC connection

A-VE has a signal internally connected to the peripheral function as shown in the table below.

Table 2.24 A-VE Internal signal connection specification: Input

Channel	Signal input		Input source	
		Signal name		Signal name
ch0	ADC conversion end interrupt A	INTAD0PDA	ADC unit A	INTADAPDA
	ADC conversion end interrupt B	INTAD0PDB	—	—
	AD conversion result 0	AD0REG0	ADC unit A	ADAREG0
	AD conversion result 1	AD0REG1		ADAREG1
	AD conversion result 2	AD0REG2		ADAREG2
	AD conversion result 3	AD0REG3		ADAREG3
	PWM interrupt	INTPWM0	PMD+ ch0	INTPWM0

Table 2.25 A-VE signal connection specification: Output

Channel	Signal Output		Output destination	
		Signal name		Signal name
ch0	U-phase PWM duty	VE0CMPU	PMD+ ch0	VE0CMPU
	V-phase PWM duty	VE0CMPV		VE0CMPV
	W-phase PWM duty	VE0CMPW		VE0CMPW
	Trigger compare 0	VE0TRGCMP0		VE0TRGCMP0
	Trigger compare 1	VE0TRGCMP1		VE0TRGCMP1
	Synchronous trigger output selection	VE0TRGSEL		VE0TRGSEL
	Conduction control / output control	VE0OUTCR		VE0OUTCR
	EMG return	VE0EMGRS		VE0EMGRS

2.9.3. Start-up trigger mode setting

[VExTRGMODE]<VTRG[1: 0]> = 10 can not be set.

2.10. 12-bit Analog to Digital Converter (ADC)

2.10.1. Built-in unit

Built-in unit per product are shown in the following table.

Table 2.26 ADC built-in unit

Product	ADC unit (✓: Available, —: N/A)
	Unit A
M4L2	✓
M4L1	✓

2.10.2. Conversion result storage register

The table below shows the number of conversion result storage registers for each unit.

Table 2.27 ADC Number of conversion result storage registers

Unit	Number of registers
A	16

2.10.3. Function pin and port

The functional pin is assigned to the port of the following table.

There is also a channel which does not have a functional pin by a product.

Table 2.28 ADC function pin and port

Unit	Signal input	Function pin	Port	Product table(✓: Available, —: N/A)	
				M4L2	M4L1
A	AINA00	AINA00	PF0	✓	✓
	AINA01	AINA01	PG0	✓	✓
	AINA02	AINA02	PG3	✓	—
	AINA03	AINA03	PG1	✓	✓
	AINA04	AINA04	PG2	✓	✓
	AINA05	AINA05	PH0	✓	✓
	AINA06	AINA06	PH1	✓	✓
	AINA07	VREFH	—	✓	✓
	AINA08	VREFL	—	✓	✓
	AINA09	Reference power supply	—	✓	✓
	AINA10 to 23	—	—	—	—

Note1: AINA07 / AINA08 / AINA09 are internally connected for self-diagnosis function support.
Note2: VREFH is connected to AVDD5 and VREFL is connected to AVSS.

2.10.4. Conversion clock for ADC

The clock which shows the 12-bit Analog to Digital Converter in the following table at the conversion clock is used.

Table 2.29 Conversion clock for ADC

Conversion clock
ADCLK

2.10.5. Usage conditions and register settings

Table 2.30 shows the corresponding usage conditions for TMPM4L Group(1).

For Conversion Clock Setting Register (***[ADxCLK]***), Mode Setting Register 1 (***[ADxMOD1]***), and Mode Setting Register 2 (***[ADxMOD2]***), set the values in the table below.

Table 2.30 ADC Usage conditions and register settings

Conversion time [μs]	AVDD5 [V]	ADCLK [MHz]	SCLK [MHz]	Setting value of register		
				[ADxCLK]	*[ADxMOD1]*	*[ADxMOD2]*
1.5	4.5≦AVDD5≦5.5	80MHz	40MHz	0x00000001	0x00004000	0x00000000
		40MHz	40MHz	0x00000000	0x00004000	0x00000000
2.95	2.7≦AVDD5＜4.5	80MHz	40MHz	0x00000009	0x0000B001	0x00000000
		40MHz	40MHz	0x00000008	0x0000B001	0x00000000

2.10.6. Internal signal connection specification

2.10.6.1. Start-up trigger connection

The 12-bit Analog to Digital Converter has a conversion function by the trigger signal.

The input trigger signal which has a register name in the trigger selector column of the following table should select the input trigger used by a trigger selector. "—" in the table does not have the corresponding function.

Table 2.31 ADC start-up trigger connection specification: Input

Unit	Signal input		Trigger Selector	Input source	
		Signal name			Signal name
A	PMD trigger 0	PMDTRG0	—	PMD+ ch0	PMD0TRG0
	PMD trigger 1	PMDTRG1	—		PMD0TRG1
	PMD trigger 2	PMDTRG2	—		PMD0TRG2
	PMD trigger 3	PMDTRG3	—		PMD0TRG3
	PMD trigger 4	PMDTRG4	—		PMD0TRG4
	PMD trigger 5	PMDTRG5	—		PMD0TRG5
	PMD trigger 6	PMDTRG6	—	—	—
	PMD trigger 7	PMDTRG7	—	—	—
	PMD trigger 8	PMDTRG8	—	—	—
	PMD trigger 9	PMDTRG9	—	—	—
	PMD trigger 10	PMDTRG10	—	—	—
	PMD trigger 11	PMDTRG11	—	—	—
	General purpose trigger	ADATRGIN	***[TSEL0CR3]*** <INSEL12>	T32A ch0 Timer B	T32A00TRGOUTUFB
				T32A ch0 Timer B	T32A00TRGOUTOFB
				T32A ch0 Timer B	T32A00TRGOUTCMPB0
				T32A ch0 Timer B	T32A00TRGOUTCMPB1

Note: ***[TSEL0CR3]***<INSEL12> selects the trigger source of the start trigger with the trigger selector.
For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

2.10.6.2. Other connection

In addition, the ADC has signals internally connected to peripheral functions as shown in the table below. "—" in the table does not have the corresponding function.

Table 2.32 ADC Internal signal connection specification: Output

Unit	Signal output		Trigger Selector	Output destination	
		Signal name			Signal name
A	General purpose trigger interrupt	INTADATRG	***[TSEL0CR0]*** <INSEL1>	T32A ch0 Timer B	T32A00TRGINBPCK
	Single conversion interrupt	INTADASGL			
	Continuous conversion interrupt	INTADACNT			
	Monitor function 0 interrupt	INTADACP0			
	Monitor function 1 interrupt	INTADACP1			
	Monitor function 0 output for PMD protect function	ADACP0L_N	—	PMD+ ch0	ADACMP0L_N
	Monitor function 1 output for PMD protect function	ADACP1L_N	—		ADACMP1L_N
	PMD trigger interrupt A	INTADAPDA	—	A-VE ch0	INTADAPDA
	PMD trigger interrupt B	INTADAPDB	—	—	—
	Conversion result storage register	ADAREG0	—	A-VE ch0	ADAREG0
		ADAREG1	—		ADAREG1
		ADAREG2	—		ADAREG2
		ADAREG3	—		ADAREG3

2.11. 32-bit Timer Event Counter (T32A)

2.11.1. Built-in channel

The built-in channel for each product is shown in the following table.

Table 2.33 T32A built-in channel

Product	T32A channel (✓: Available, —: N/A)			
	ch0	ch1	ch2	ch3
M4L2	✓	✓	✓	✓
M4L1	✓	✓	✓	✓

2.11.2. Function pin and port

The functional pin is assigned to the port of the following tables.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.34 T32A functional pin and port

Channel	Function pin		Port	Product table (✓: Available, —: N/A)	
				M4L2	M4L1
ch0	T32A00INA0	Input	PD0	✓	✓
	T32A00OUTA	Output	PD0	✓	✓
	T32A00INB0	Input	PD4	✓	—
	T32A00OUTB	Output	PD4	✓	—
	T32A00INC0	Input	PD0	✓	✓
	T32A00OUTC	Output	PD0	✓	✓
ch1	T32A01INA0	Input	PC3	✓	✓
	T32A01OUTA	Output	PC3	✓	✓
	T32A01INB0	Input	PA3	✓	—
	T32A01OUTB	Output	PA3	✓	—
	T32A01INC0	Input	PC3	✓	✓
	T32A01OUTC	Output	PC3	✓	✓
ch2	T32A02INA0	Input	PC4	✓	✓
	T32A02OUTA	Output	PC5	✓	✓
	T32A02INB0	Input	PC5	✓	✓
	T32A02OUTB	Output	PC4	✓	✓
	T32A02INC0	Input	PC4	✓	✓
	T32A02OUTC	Output	PC5	✓	✓
ch3	T32A03INA0	Input	PA2	✓	✓
	T32A03OUTA	Output	PA1	✓	✓
	T32A03INB0	Input	PA1	✓	✓
	T32A03OUTB	Output	PA2	✓	✓
	T32A03INC0	Input	PA1	✓	✓
	T32A03OUTC	Output	PA2	✓	✓

Note: TMPM4L group(1) don’t have T32AxxINA1, T32AxxINB1, and T32AxxINC1 pin.

2.11.3. Clock for prescaler

The clock shown in the table below is used as the prescaler clock for T32A.

Table 2.35 T32A clock for prescaler

Clock for prescaler
ΦT0

2.11.4. Internal signal connection specification

2.11.4.1. Capture trigger input connection

The following table shows the capture trigger signals connected to the T32A.

The input trigger signal which has a register name in the trigger selector column of the following table should select the input trigger used by a trigger selector.

Table 2.36 T32A Capture trigger input connection specification (1/2)

Channel	Timer	Signal input	Signal name	Trigger Selector	Input source	Signal name
ch0	Timer A	Other timer output	T32A00TRGINAPHCK	—	T32A ch0 Timer B	T32A00OUTB
		Internal trigger input	T32A00TRGINAPCK	***[TSEL0CR0]*** <INSEL0>	T32A ch0 Timer B	T32A00TRGOUTUFB
					T32A ch0 Timer B	T32A00TRGOUTOFB
					T32A ch0 Timer B	T32A00TRGOUTCMPB0
					T32A ch0 Timer B	T32A00TRGOUTCMPB1
	Timer B	Other timer output	T32A00TRGINBPHCK	—	T32A ch0 Timer A	T32A00OUTA
		Internal trigger input	T32A00TRGINBPCK	***[TSEL0CR0]*** <INSEL1>	T32A ch0 Timer A	T32A00TRGOUTUFA
					T32A ch0 Timer A	T32A00TRGOUTOFA
					T32A ch0 Timer A	T32A00TRGOUTCMPA0
					T32A ch0 Timer A	T32A00TRGOUTCMPA1
					ADC unit A	INTADATRG/ INTADASGL/ INTADACNT/ INTADACP0/ INTADACP1
	Timer C	Other timer output	T32A00TRGINCPHCK	—	T32A ch2 Timer C	T32A02OUTC
		Internal trigger input	T32A00TRGINCPCK	***[TSEL0CR2]*** <INSEL9>	T32A ch2 Timer C	T32A02TRGOUTUFC
					T32A ch2 Timer C	T32A02TRGOUTOFC
					T32A ch2 Timer C	T32A02TRGOUTCMPC0
					T32A ch2 Timer C	T32A02TRGOUTCMPC1
ch1	Timer A	Other timer output	T32A01TRGINAPHCK	—	T32A ch1 Timer B	T32A01OUTB
		Internal trigger input	T32A01TRGINAPCK	***[TSEL0CR0]*** <INSEL2>	T32A ch1 Timer B	T32A01TRGOUTUFB
					T32A ch1 Timer B	T32A01TRGOUTOFB
					T32A ch1 Timer B	T32A01TRGOUTCMPB0
					T32A ch1 Timer B	T32A01TRGOUTCMPB1
					UART ch0	UART0RXTRG
					UART ch0	UART0TXTRG
					TSPI ch0	TSPI0RXEND
					TSPI ch0	TSPI0TXEND
	Timer B	Other timer output	T32A01TRGINBPHCK	—	T32A ch1 Timer A	T32A01OUTA
		Internal trigger input	T32A01TRGINBPCK	***[TSEL0CR0]*** <INSEL3>	T32A ch1 Timer A	T32A01TRGOUTUFA
					T32A ch1 Timer A	T32A01TRGOUTOFA
					T32A ch1 Timer A	T32A01TRGOUTCMPA0
					T32A ch1 Timer A	T32A01TRGOUTCMPA1
	Timer C	Other timer output	T32A01TRGINCPHCK	—	T32A ch3 Timer C	T32A03OUTC
		Internal trigger input	T32A01TRGINCPCK	***[TSEL0CR2]*** <INSEL8>	T32A ch3 Timer C	T32A03TRGOUTUFC
					T32A ch3 Timer C	T32A03TRGOUTOFC
					T32A ch3 Timer C	T32A03TRGOUTCMPC0
					T32A ch3 Timer C	T32A03TRGOUTCMPC1

Note: ***[TSEL0CRn]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

Table 2.37 T32A Capture trigger input connection specification (2/2)

Channel		Signal input		Trigger	Input source	
	Timer		Signal name	Selector		Signal name
ch2	Timer A	Other timer output	T32A02TRGINAPHCK	—	T32A ch2 Timer B	T32A02OUTB
		Internal trigger input	T32A02TRGINAPCK	***[TSEL0CR1]*** <INSEL4>	T32A ch2 Timer B	T32A02TRGOUTUFB
					T32A ch2 Timer B	T32A02TRGOUTOFB
					T32A ch2 Timer B	T32A02TRGOUTCMPB0
					T32A ch2 Timer B	T32A02TRGOUTCMPB1
					UART ch1	UART1RXTRG
					UART ch1	UART1TXTRG
					TSPI ch1	TSPI1RXEND
					TSPI ch1	TSPI1TXEND
	Timer B	Other timer output	T32A02TRGINBPHCK	—	T32A ch2 Timer A	T32A02OUTA
		Internal trigger input	T32A02TRGINBPCK	***[TSEL0CR1]*** <INSEL5>	T32A ch2 Timer A	T32A02TRGOUTUFA
					T32A ch2 Timer A	T32A02TRGOUTOFA
					T32A ch2 Timer A	T32A02TRGOUTCMPA0
					T32A ch2 Timer A	T32A02TRGOUTCMPA1
					A-ENC32 ch0	ENC0TIMPLS
	Timer C	Other timer output	T32A02TRGINCPHCK	—	T32A ch0 Timer C	T32A00OUTC
		Internal trigger input	T32A02TRGINCPCK	***[TSEL0CR2]*** <INSEL11>	T32A ch0 Timer C	T32A00TRGOUTUFC
					T32A ch0 Timer C	T32A00TRGOUTOFC
					T32A ch0 Timer C	T32A00TRGOUTCMPC0
					T32A ch0 Timer C	T32A00TRGOUTCMPC1
ch3	Timer A	Other timer output	T32A03TRGINAPHCK	—	T32A ch3 Timer B	T32A03OUTB
		Internal trigger input	T32A03TRGINAPCK	***[TSEL0CR1]*** <INSEL6>	T32A ch3 Timer B	T32A03TRGOUTUFB
					T32A ch3 Timer B	T32A03TRGOUTOFB
					T32A ch3 Timer B	T32A03TRGOUTCMPB0
					T32A ch3 Timer B	T32A03TRGOUTCMPB1
					UART ch2	UART2RXTRG
					UART ch2	UART2TXTRG
					TSPI ch2	TSPI2RXEND
					TSPI ch2	TSPI2TXEND
	Timer B	Other timer output	T32A03TRGINBPHCK	—	T32A ch3 Timer A	T32A03OUTA
		Internal trigger input	T32A03TRGINBPCK	***[TSEL0CR1]*** <INSEL7>	T32A ch3 Timer A	T32A03TRGOUTUFA
					T32A ch3 Timer A	T32A03TRGOUTOFA
					T32A ch3 Timer A	T32A03TRGOUTCMPA0
					T32A ch3 Timer A	T32A03TRGOUTCMPA1
	Timer C	Other timer output	T32A03TRGINCPHCK	—	T32A ch1 Timer C	T32A01OUTC
		Internal trigger input	T32A03TRGINCPCK	***[TSEL0CR2]*** <INSEL10>	T32A ch1 Timer C	T32A01TRGOUTUFC
					T32A ch1 Timer C	T32A01TRGOUTOFC
					T32A ch1 Timer C	T32A01TRGOUTCMPC0
					T32A ch1 Timer C	T32A01TRGOUTCMPC1

Note: ***[TSEL0CRn]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

2.11.4.2. Other connection

Table 2.38 T32A trigger output connection specification (1/4)

Channel		Signal output		Trigger	Output destination	
	Timer		Signal name	Selector		Signal name
ch0	Timer A	Timer output	T32A00OUTA	—	T32A ch0 Timer B	T32A00TRGINBPHCK
					UART ch2	UART2CKINA
		Underflow trigger	T32A00TRGOUTUFA	***[TSEL0CR0]*** <INSEL1>	T32A ch0 Timer B	T32A00TRGINBPCK
		Overflow trigger	T32A00TRGOUTOFA			
		Register A0 match trigger	T32A00TRGOUTCMPA0			
		Register A1 match trigger	T32A00TRGOUTCMPA1			
	Timer B	Timer output	T32A00OUTB	—	T32A ch0 Timer A	T32A00TRGINAPHCK
		Underflow trigger	T32A00TRGOUTUFB	***[TSEL0CR0]*** <INSEL0>	T32A ch0 Timer A	T32A00TRGINAPCK
				[TSEL0CR3] <INSEL12>	ADC unit A	ADATRGIN
		Overflow trigger	T32A00TRGOUTOFB	***[TSEL0CR0]*** <INSEL0>	T32A ch0 Timer A	T32A00TRGINAPCK
				[TSEL0CR3] <INSEL12>	ADC unit A	ADATRGIN
		Register B0 match trigger	T32A00TRGOUTCMPB0	***[TSEL0CR0]*** <INSEL0>	T32A ch0 Timer A	T32A00TRGINAPCK
				[TSEL0CR3] <INSEL12>	ADC unit A	ADATRGIN
		Register B1 match trigger	T32A00TRGOUTCMPB1	***[TSEL0CR0]*** <INSEL0>	T32A ch0 Timer A	T32A00TRGINAPCK
				[TSEL0CR3] <INSEL12>	ADC unit A	ADATRGIN
	Timer C	Timer output	T32A00OUTC	—	T32A ch2 Timer C	T32A02TRGINCPHCK
		Underflow trigger	T32A00TRGOUTUFC	***[TSEL0CR2]*** <INSEL11>	T32A ch2 Timer C	T32A02TRGINCPCK
		Overflow trigger	T32A00TRGOUTOFC			
		Register C0 match trigger	T32A00TRGOUTCMPC0			
		Register C1 match trigger	T32A00TRGOUTCMPC1			

Note: ***[TSEL0CRn]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

Table 2.39 T32A trigger output connection specification (2/4)

Channel		Signal output		Trigger Selector	Output destination	
	Timer		Signal name			Signal name
ch1	Timer A	Timer output	T32A01OUTA	—	T32A ch1 Timer B	T32A01TRGINBPHCK
		Underflow trigger	T32A01TRGOUTUFA	***[TSEL0CR0]*** <INSEL3>	T32A ch1 Timer B	T32A01TRGINBPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
		Overflow trigger	T32A01TRGOUTOFA	***[TSEL0CR0]*** <INSEL3>	T32A ch1 Timer B	T32A01TRGINBPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
		Register A0 match trigger	T32A01TRGOUTCMPA0	***[TSEL0CR0]*** <INSEL3>	T32A ch1 Timer B	T32A01TRGINBPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
		Register A1 match trigger	T32A01TRGOUTCMPA1	***[TSEL0CR0]*** <INSEL3>	T32A ch1 Timer B	T32A01TRGINBPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
	Timer B	Timer output	T32A01OUTB	—	T32A ch1 Timer A	T32A01TRGINAPHCK
					UART ch0	UART0CKINA
					UART ch1	UART1CKINA
		Underflow trigger	T32A01TRGOUTUFB	***[TSEL0CR0]*** <INSEL2>	T32A ch1 Timer A	T32A01TRGINAPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
		Overflow trigger	T32A01TRGOUTOFB	***[TSEL0CR0]*** <INSEL2>	T32A ch1 Timer A	T32A01TRGINAPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
		Register B0 match trigger	T32A01TRGOUTCMPB0	***[TSEL0CR0]*** <INSEL3>	T32A ch1 Timer A	T32A01TRGINAPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
		Register B1 match trigger	T32A01TRGOUTCMPB1	***[TSEL0CR0]*** <INSEL2>	T32A ch1 Timer A	T32A01TRGINAPCK
				[TSEL0CR3] <INSEL13>	UART ch0	UART0TRGIN
					TSPI ch0	TSPI0TRG
	Timer C	Timer output	T32A01OUTC	—	T32A ch3 Timer C	T32A03TRGINCPHCK
		Underflow trigger	T32A01TRGOUTUFC	***[TSEL0CR2]*** <INSEL10>	T32A ch3 Timer C	T32A03TRGINCPCK
		Overflow trigger	T32A01TRGOUTOFC			
		Register C0 match trigger	T32A01TRGOUTCMPC0			
		Register C1 match trigger	T32A01TRGOUTCMPC1			

Note: ***[TSEL0CRn]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

Table 2.40 T32A trigger output connection specification (3/4)

Channel	Timer	Signal output	Signal name	Trigger Selector	Output destination	Signal name
ch2	Timer A	Timer output	T32A02OUTA	—	T32A ch2 Timer B	T32A02TRGINBPHCK
		Underflow trigger	T32A02TRGOUTUFA	***[TSEL0CR1]*** <INSEL5>	T32A ch2 Timer B	T32A02TRGINBPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
		Overflow trigger	T32A02TRGOUTOFA	***[TSEL0CR1]*** <INSEL5>	T32A ch2 Timer B	T32A02TRGINBPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
		Register A0 match trigger	T32A02TRGOUTCMPA0	***[TSEL0CR1]*** <INSEL5>	T32A ch2 Timer B	T32A02TRGINBPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
		Register A1 match trigger	T32A02TRGOUTCMPA1	***[TSEL0CR1]*** <INSEL5>	T32A ch2 Timer B	T32A02TRGINBPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
	Timer B	Timer output	T32A02OUTB	—	T32A ch2 Timer A	T32A02TRGINAPHCK
				—	A-ENC32 ch0	ENC0PSGI
		Underflow trigger	T32A02TRGOUTUFB	***[TSEL0CR1]*** <INSEL4>	T32A ch2 Timer A	T32A02TRGINAPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
		Overflow trigger	T32A02TRGOUTOFB	***[TSEL0CR1]*** <INSEL4>	T32A ch2 Timer A	T32A02TRGINAPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
		Register B0 match trigger	T32A02TRGOUTCMPB0	***[TSEL0CR1]*** <INSEL4>	T32A ch2 Timer A	T32A02TRGINAPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
				—	PMD+ ch0	PMD0TMR
		Register B1 match trigger	T32A02TRGOUTCMPB1	***[TSEL0CR1]*** <INSEL4>	T32A ch2 Timer A	T32A02TRGINAPCK
				[TSEL0CR3] <INSEL14>	UART ch1	UART1TRGIN
					TSPI ch1	TSPI1TRG
	Timer C	Timer output	T32A02OUTC	—	T32A ch0 Timer C	T32A00TRGINCPHCK
		Underflow trigger	T32A02TRGOUTUFC	***[TSEL0CR2]*** <INSEL9>	T32A ch0 Timer C	T32A00TRGINCPCK
		Overflow trigger	T32A02TRGOUTOFC			
		Register C0 match trigger	T32A02TRGOUTCMPC0			
		Register C1 match trigger	T32A02TRGOUTCMPC1			

Note: ***[TSEL0CRn]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

Table 2.41 T32A trigger output connection specification (4/4)

Channel		Signal output		Trigger Selector	Output destination	
	Timer		Signal name			Signal name
ch3	Timer A	Timer output	T32A03OUTA	—	T32A ch3 Timer B	T32A03TRGINBPHCK
		Underflow trigger	T32A03TRGOUTUFA	***[TSEL0CR1]*** <INSEL7>	T32A ch3 Timer B	T32A03TRGINBPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
		Overflow trigger	T32A03TRGOUTOFA	***[TSEL0CR1]*** <INSEL7>	T32A ch3 Timer B	T32A03TRGINBPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
		Register A0 match trigger	T32A03TRGOUTCMPA0	***[TSEL0CR1]*** <INSEL7>	T32A ch3 Timer B	T32A03TRGINBPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
		Register A1 match trigger	T32A03TRGOUTCMPA1	***[TSEL0CR1]*** <INSEL7>	T32A ch3 Timer B	T32A03TRGINBPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
	Timer B	Timer output	T32A03OUTB	—	T32A ch3 Timer A	T32A03TRGINAPHCK
		Underflow trigger	T32A03TRGOUTUFB	***[TSEL0CR1]*** <INSEL6>	T32A ch3 Timer A	T32A03TRGINAPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
		Overflow trigger	T32A03TRGOUTOFB	***[TSEL0CR1]*** <INSEL6>	T32A ch3 Timer A	T32A03TRGINAPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
		Register B0 match trigger	T32A03TRGOUTCMPB0	***[TSEL0CR1]*** <INSEL6>	T32A ch3 Timer A	T32A03TRGINAPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
		Register B1 match trigger	T32A03TRGOUTCMPB1	***[TSEL0CR1]*** <INSEL6>	T32A ch3 Timer A	T32A03TRGINAPCK
				[TSEL0CR3] <INSEL15>	UART ch2	UART2TRGIN
					TSPI ch2	TSPI2TRG
	Timer C	Timer output	T32A03OUTC	—	T32A ch1 Timer C	T32A01TRGINCPHCK
		Underflow trigger	T32A03TRGOUTUFC	***[TSEL0CR2]*** <INSEL9>	T32A ch1 Timer C	T32A01TRGINCPCK
		Overflow trigger	T32A03TRGOUTOFC			
		Register C0 match trigger	T32A03TRGOUTCMPC0			
		Register C1 match trigger	T32A03TRGOUTCMPC1			

Note: ***[TSEL0CRn]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

2.11.4.3. Synchronous control connection

The configuration of T32A synchronous control can be selected from 2 timer synchronization and 4 timer synchronization in the general purpose register ***[GPREG0]***. For details of ***[GPREG0]***, refer to "2.11.4.4. General purpose register details".

Table 2.42 T32A Timer A / Timer B Synchronous control connection specification (ch0, ch2)

Setting *[GPREG0]* <TSNC0SEL>	Master			Slave		
	Channel / timer	Function (Output)	Signal name	Channel / timer	Function (Input)	Signal name
0	ch0 / Timer A	Synchronous start	T32A00SYNCSTARTOUTA	ch0 / Timer B	Synchronous start	T32A00SYNCSTARTB
		Synchronous stop	T32A00SYNCSTOPOUTA		Synchronous stop	T32A00SYNCSTOPB
		Synchronous reload	T32A00SYNCRELOADOUTA		Synchronous reload	T32A00SYNCRELOADB
	ch2 / Timer A	Synchronous start	T32A02SYNCSTARTOUTA	ch2 / Timer B	Synchronous start	T32A02SYNCSTARTB
		Synchronous stop	T32A02SYNCSTOPOUTA		Synchronous stop	T32A02SYNCSTOPB
		Synchronous reload	T32A02SYNCRELOADOUTA		Synchronous reload	T32A02SYNCRELOADB
1	ch2 / Timer A	Synchronous start	T32A02SYNCSTARTOUTA	ch0 / Timer A	Synchronous start	T32A00SYNCSTARTA
				ch0 / Timer B	Synchronous start	T32A00SYNCSTARTB
				ch2 / Timer B	Synchronous start	T32A02SYNCSTARTB
		Synchronous stop	T32A02SYNCSTOPOUTA	ch0 / Timer A	Synchronous stop	T32A00SYNCSTOPA
				ch0 / Timer B	Synchronous stop	T32A00SYNCSTOPB
				ch2 / Timer B	Synchronous stop	T32A02SYNCSTOPB
		Synchronous reload	T32A02SYNCRELOADOUTA	ch0 / Timer A	Synchronous reload	T32A00SYNCRELOADA
				ch0 / Timer B	Synchronous reload	T32A00SYNCRELOADB
				ch2 / Timer B	Synchronous reload	T32A02SYNCRELOADB

Table 2.43 T32A Timer A / Timer B Synchronous control connection specification (ch1, ch3)

Setting *[GPREG0]* <TSNC1SEL>	Master			Slave		
	Channel / timer	**Function (Output)**	Signal name	**Channel / timer**	**Function (Input)**	Signal name
0	ch1 / Timer A	Synchronous start	T32A01SYNCSTARTOUTA	ch1 / Timer B	Synchronous start	T32A01SYNCSTARTB
		Synchronous stop	T32A01SYNCSTOPOUTA		Synchronous stop	T32A01SYNCSTOPB
		Synchronous reload	T32A01SYNCRELOADOUTA		Synchronous reload	T32A01SYNCRELOADB
	ch3 / Timer A	Synchronous start	T32A03SYNCSTARTOUTA	ch3 / Timer B	Synchronous start	T32A03SYNCSTARTB
		Synchronous stop	T32A03SYNCSTOPOUTA		Synchronous stop	T32A03SYNCSTOPB
		Synchronous reload	T32A03SYNCRELOADOUTA		Synchronous reload	T32A03SYNCRELOADB
1	ch3 / Timer A	Synchronous start	T32A03SYNCSTARTOUTA	ch1 / Timer A	Synchronous start	T32A01SYNCSTARTA
				ch1 / Timer B	Synchronous start	T32A01SYNCSTARTB
				ch3 / Timer B	Synchronous start	T32A03SYNCSTARTB
		Synchronous stop	T32A03SYNCSTOPOUTA	ch1 / Timer A	Synchronous stop	T32A01SYNCSTOPA
				ch1 / Timer B	Synchronous stop	T32A01SYNCSTOPB
				ch3 / Timer B	Synchronous stop	T32A03SYNCSTOPB
		Synchronous reload	T32A03SYNCRELOADOUTA	ch1 / Timer A	Synchronous reload	T32A01SYNCRELOADA
				ch1 / Timer B	Synchronous reload	T32A01SYNCRELOADB
				ch3 / Timer B	Synchronous reload	T32A03SYNCRELOADB

Table 2.44 T32A Timer C Synchronous control connection specification

Master			Slave		
Channel	**Function (Output)**	**Signal name**	**Channel**	**Function (Input)**	**Signal name**
ch2	Synchronous start	T32A02SYNCSTARTOUTC	ch0	Synchronous start	T32A00SYNCSTARTC
	Synchronous stop	T32A02SYNCSTOPOUTC		Synchronous stop	T32A00SYNCSTOPC
	Synchronous reload	T32A02SYNCRELOADOUTC		Synchronous reload	T32A00SYNCRELOADC
ch3	Synchronous start	T32A03SYNCSTARTOUTC	ch1	Synchronous start	T32A01SYNCSTARTC
	Synchronous stop	T32A03SYNCSTOPOUTC		Synchronous stop	T32A01SYNCSTOPC
	Synchronous reload	T32A03SYNCRELOADOUTC		Synchronous reload	T32A01SYNCRELOADC

2.11.4.4. General purpose register details

Peripheral function		Channel/Unit	Base address
General purpose register	GP	—	0x4003FF00

Register name		Address(Base+)
General purpose register 0	***[GPREG0]***	0x0000

- ***[GPREG0]*** (General purpose register 0)

Bit	Bit Symbol	After reset	Type	Function
7:2	—	0	R	Read as "0"
1	TSNC1SEL	0	R/W	T32A ch1,ch3 synchronous mode selection 0: In-channel synchronization (2 timer synchronous connection) 1: Inter-channel synchronization (4 timer synchronous connection)
0	TSNC0SEL	0	R/W	T32A ch0,ch2 synchronous mode selection 0: In-channel synchronization (2 timer synchronous connection) 1: Inter-channel synchronization (4 timer synchronous connection)

2.11.5. Pulse count correspondence classified by product

T32A with TMPM4L group(1) supports only 1-phase pulse count.

2.11.6. Non corresponding interrupt

This product does not correspond to Every Count Interrupt (INTT32AxEVRYC).

2.12. Universal Asynchronous Receiver Transmitter (UART)

2.12.1. Built-in channel

The built-in channel for every product is shown in the following table.

In TMPM4L Group (1), Maximum Communication speed of UART is 5 Mbps.

Table 2.45 UART built-in channel

Product	UART channel (✓: Available, —: N/A)		
	ch0	ch1	ch2
M4L2	✓	✓	✓
M4L1	✓	✓	✓

2.12.2. Function pin and port

The functional pin is assigned to the port of the following table.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.46 UART functional pin signal and port

Channel	Function pin		Port	Product table (✓: Available, — N/A)	
				M4L2	M4L1
ch0	UT0TXDA	Output	PC0	✓	✓
			PC1	✓	✓
	UT0RXD	Input	PC0	✓	✓
			PC1	✓	✓
	UT0CTS_N	Output	PC2	✓	✓
ch1	UT1TXDA	Output	PD2	✓	✓
			PD3	✓	✓
	UT1RXD	Input	PD2	✓	✓
			PD3	✓	✓
	UT1CTS_N	Output	PD1	✓	✓
ch2	UT2TXDA	Output	PA1	✓	✓
			PA2	✓	✓
	UT2RXD	Input	PA1	✓	✓
			PA2	✓	✓
	UT2CTS_N	Output	PA0	✓	✓

Note: TMPM4L Group(1) does not have UTxTXDB and UTxRTS_N pins.

2.12.3. Half clock mode list for the each products

The half clock mode of UART mounted in TMPM4L Group(1) is compatible with single terminal mode only.

2.12.4. Clock selection

2.12.4.1. Clock for prescaler

The clock shown in the table below is used as the prescaler clock for UART.

Table 2.47 UART clock for prescaler

Clock
ΦT0

2.12.4.2. Baud rate generator timer output

The UART can select timer output as baud rate generator clock in ***[UARTxCLK]***<CKSEL> setting.

The corresponding timer output is shown in the table below.

Table 2.48 Baud rate generator timer output

Channel	Timer output	
Signal name		Signal name
ch0	UART0CKINA	T32A ch1 Timer B	T32A01OUTB
ch1	UART1CKINA	T32A ch1 Timer B	T32A01OUTB
ch2	UART2CKINA	T32A ch0 Timer A	T32A00OUTA

2.12.5. Internal signal connection specification

2.12.5.1. Trigger transmission signal connection

The UART has the transmission function started by a trigger signal.

The trigger signal is selected from among the trigger sources in the following table by the trigger selector.

Table 2.49 UART trigger transmission signal connection specification: Input

Channel	Signal input		Trigger selector	Input source	
		Signal name			Signal name
ch0	Trigger input for trigger transmission	UART0TRGIN	***[TSEL0CR3]*** <INSEL13>	T32A ch1 Timer A	T32A01TRGOUTUFA
					T32A01TRGOUTOFA
					T32A01TRGOUTCMPA0
					T32A01TRGOUTCMPA1
				T32A ch1 Timer B	T32A01TRGOUTUFB
					T32A01TRGOUTOFB
					T32A01TRGOUTCMPB0
					T32A01TRGOUTCMPB1
ch1	Trigger input for trigger transmission	UART1TRGIN	***[TSEL0CR3]*** <INSEL14>	T32A ch2 Timer A	T32A02TRGOUTUFA
					T32A02TRGOUTOFA
					T32A02TRGOUTCMPA0
					T32A02TRGOUTCMPA1
				T32A ch2 Timer B	T32A02TRGOUTUFB
					T32A02TRGOUTOFB
					T32A02TRGOUTCMPB0
					T32A02TRGOUTCMPB1
ch2	Trigger input for trigger transmission	UART2TRGIN	***[TSEL0CR3]*** <INSEL15>	T32A ch3 Timer A	T32A03TRGOUTUFA
					T32A03TRGOUTOFA
					T32A03TRGOUTCMPA0
					T32A03TRGOUTCMPA1
				T32A ch3 Timer B	T32A03TRGOUTUFB
					T32A03TRGOUTOFB
					T32A03TRGOUTCMPB0
					T32A03TRGOUTCMPB1

Note: ***[TSEL0CR3]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

2.12.5.2. T32A capture trigger connection

In addition, the UART has signals internally connected to peripheral functions as shown in the table below.

Table 2.50 UART Internal connection specification: Output

Channel	Signal output		Trigger selector	Output destination	
		Signal name			Signal name
ch0	Reception completion trigger	UART0RXTRG	***[TSEL0CR0]*** <INSEL2>	T32A ch1 Timer A	T32A01TRGINAPCK
	Transmission completion trigger	UART0TXTRG			
ch1	Reception completion trigger	UART1RXTRG	***[TSEL0CR1]*** <INSEL4>	T32A ch2 Timer A	T32A02TRGINAPCK
	Transmission completion trigger	UART1TXTRG			
ch2	Reception completion trigger	UART2RXTRG	***[TSEL0CR1]*** <INSEL6>	T32A ch3 Timer A	T32A03TRGINAPCK
	Transmission completion trigger	UART2TXTRG			

2.13. Serial Peripheral Interface (TSPI)

2.13.1. Built-in channel

The built-in channel for every product is shown in the following table.

The maximum communication speed of TSPI of TMPM4L Group(1) is 20 Mbps.

Table 2.51 TSPI built-in channel

Product	TSPI channel (✓: Available, —: N/A)		
	ch0	ch1	ch2
M4L2	✓	✓	✓
M4L1	✓	✓	✓

2.13.2. Function pin and port

The functional pin is assigned to the port of the following table.

Please use exclusively the same functional pin currently assigned to plurality.

There is also a channel which does not have a functional pin by a product.

Table 2.52 TSPI function pin and port

Channel	Function pin		Port	Product table (✓: Available, —: N/A)	
				M4L2	M4L1
ch0	TSPI0SCK	I/O	PC2	✓	✓
	TSPI0TXD	Output	PC0	✓	✓
	TSPI0RXD	Input	PC1	✓	✓
ch1	TSPI1SCK	I/O	PD1	✓	✓
	TSPI1TXD	Output	PD2	✓	✓
	TSPI1RXD	Input	PD3	✓	✓
ch2	TSPI2SCK	I/O	PA0	✓	✓
	TSPI2TXD	Output	PA1	✓	✓
	TSPI2RXD	Input	PA2	✓	✓

Note: TMPM4L Group(1) does not have TSPIxCSIN, TSPIxCS0, TSPIxCS1, TSPIxCS2, TSPIxCS3 pins.

2.13.3. Transfer mode list for the each products

TSPI in TMPM4L Group(1) only supports SIO mode.

2.13.4. *[TSPIxCR2]*<RXDLY> set value

For the setting value of TSPI control register 2 (***[TSPIxCR2]*** <RXDLY>), set the values in the following table.

Table 2.53 TSPI *[TSPIxCR2]*<RXDLY> set value

Register name	Value
[TSPIxCR2]<RXDLY>	1

2.13.5. Clock for Prescaler

The clock shown in the table below is used as the prescaler clock for TSPI.

Table 2.54 TSPI clock for prescaler

Clock for prescaler
ΦT0

2.13.6. Internal signal connection specification

2.13.6.1. Trigger transmission signal connection

The TSPI has the transmission function started by a trigger signal.

The trigger signal is selected from among the trigger sources in the following table by the trigger selector.

Table 2.55 TSPI trigger transmission Specification: Input

Channel	Signal input		Trigger selector	Input source	
		Signal name			Signal name
ch0	Trigger input for start communication	TSPI0TRG	***[TSEL0CR3]*** <INSEL13>	T32A ch1 Timer A	T32A01TRGOUTUFA
					T32A01TRGOUTOFA
					T32A01TRGOUTCMPA0
					T32A01TRGOUTCMPA1
				T32A ch1 Timer B	T32A01TRGOUTUFB
					T32A01TRGOUTOFB
					T32A01TRGOUTCMPB0
					T32A01TRGOUTCMPB1
ch1	Trigger input for start communication	TSPI1TRG	***[TSEL0CR3]*** <INSEL14>	T32A ch2 Timer A	T32A02TRGOUTUFA
					T32A02TRGOUTOFA
					T32A02TRGOUTCMPA0
					T32A02TRGOUTCMPA1
				T32A ch2 Timer B	T32A02TRGOUTUFB
					T32A02TRGOUTOFB
					T32A02TRGOUTCMPB0
					T32A02TRGOUTCMPB1
ch2	Trigger input for start communication	TSPI2TRG	***[TSEL0CR3]*** <INSEL15>	T32A ch3 Timer A	T32A03TRGOUTUFA
					T32A03TRGOUTOFA
					T32A03TRGOUTCMPA0
					T32A03TRGOUTCMPA1
				T32A ch3 Timer B	T32A03TRGOUTUFB
					T32A03TRGOUTOFB
					T32A03TRGOUTCMPB0
					T32A03TRGOUTCMPB1

Note: ***[TSEL0CR3]***<INSELm> selects the trigger source of the start trigger with the trigger selector. For details on the connection destination, refer to " 2.2. Trigger Selector (TRGSEL) ".

2.13.6.2. T32A connection

In addition, the TSPI has signals internally connected with peripheral functions as shown in the table below.

Table 2.56 TSPI trigger transmission Specification: Output

Channel	Signal output	Signal name	Trigger selector	Output destination	Signal name
ch0	Receive Completion	TSPI0RXEND	***[TSEL0CR0]*** <INSEL2>	T32A ch1 Timer A	T32A01TRGINAPCK
	Transmit Completion	TSPI0TXEND			
ch1	Receive Completion	TSPI1RXEND	***[TSEL0CR1]*** <INSEL4>	T32A ch2 Timer A	T32A02TRGINAPCK
	Transmit Completion	TSPI1TXEND			
ch2	Receive Completion	TSPI2RXEND	***[TSEL0CR1]*** <INSEL6>	T32A ch3 Timer A	T32A03TRGINAPCK
	Transmit Completion	TSPI2TXEND			

2.14. Digital Noise Filter Circuit (DNF)

2.14.1. Built-in unit

The built-in units for every product is shown in the following table.

Table 2.57 DNF built-in unit

Product	DNF unit (✓: Available, —: N/A)
	unit A
M4L2	✓
M4L1	✓

2.14.2. External interrupt pin and DNF

The digital noise filter circuit corresponds the external interrupt pins as shown in the following table.

Table 2.58 External interrupt pin and DNF

External interrupt pin (signal name)	Port	Setting register name	Product table (✓: Available, —: N/A)	
			M4L2	M4L1
INT00	PC3	***[DNFAENCR]***<NFEN0>	✓	✓
INT01	PG1	***[DNFAENCR]***<NFEN1>	✓	✓
INT02	PG2	***[DNFAENCR]***<NFEN2>	✓	✓
INT03	PH0	***[DNFAENCR***]<NFEN3>	✓	✓
INT04	PH1	***[DNFAENCR]***<NFEN4>	✓	✓
INT05	PC5	***[DNFAENCR]***<NFEN5>	✓	✓
INT06	PC4	***[DNFAENCR]***<NFEN6>	✓	✓
INT07	PA3	***[DNFAENCR]***<NFEN7>	✓	—
—	—	***[DNFAENCR]***<NFEN8> to <NFEN15>	—	—

2.14.3. Sampling Source Clock

The digital noise filter circuit uses the clocks in the table below as the source clock for sampling.

Table 2.59 DNF sampling source clock

Sampling source clock
fc

2.15. Voltage Detection Circuit (LVD)

2.15.1. Built-in List

The following table shows the built-in list for each product.

Table 2.60 Built-in List

Product	Built-in LVD (✓: Available, —: N/A)
M4L2	✓
M4L1	✓

2.15.2. LVD detection power supply

A voltage detecting circuit monitors the power supply of the following table.

Table 2.61 LVD detection power supply

LVD detection power supply	Power supply name
Digital power source terminal	DVDD5A/DVDD5B/DVDD5C

2.16. CRC calculation circuit(CRC)

2.16.1. Built-in Table

The CRC each product is shown in the following table.

Table 2.62 Built-in CRC

Product	Built-in CRC (✓: Available, —: N/A)
M4L2	✓
M4L1	✓

2.17. RAMP Parity(RAMP)

2.17.1. Built-in channel

The following table shows the RAMP built-in channel of each product.

Table 2.63 RAMP built-in channel

Product	RAMP built-in (✓: Available, —: N/A)
	ch0
M4L2	✓
M4L1	✓

2.17.2. Error detection block area

The following table shows the detection RAM block area of each product.

Table 2.64 RAM area and address of RAMP

Channel	Register name	RAM area address	Products (✓: Available, —: N/A)	
			M4L2	M4L1
ch0	***[RPAR0ST]***<RPARFG0>	0x20000000-0x200017FF	✓	✓

2.18. Trimming Circuit (TRM)

2.18.1. Built-in List

The following table shows the built-in list for each product.

Table 2.65 Built-in TRM

Product	Built-in TRM (✓: Available, —: N/A)
M4L2	✓
M4L1	✓

2.18.2. Target Oscillator

The object oscillator of a trimming circuit is an oscillator shown in the following table.

Table 2.66 TRM trimming oscillator

Object oscillator	Oscillator name
Internal high speed oscillator 1	IHOSC1

3. Revision History

Table 3.1 Revision history

Revision	Date	Description
1.0	2018-10-16	First release
1.1	2019-07-29	-2.10.5 Usage conditions and register settings Chenged capter title, Added setting condition

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**