Power Efficiency Optimization and Application Circuits Using Dual-power-supply LDO Regulators

for the Power Supplies of MCUs, CMOS Image Sensors, and RF

Outline:

This application note describes application circuits for low-dropout (LDO) regulators to maximize the efficiency of the power supplies for MCUs, CMOS image sensors, and RF (Wi-Fi®) circuits at low voltage and high current. Toshiba's TCR5BM and TCR8BM dual-power-supply LDO regulator series are used in application circuit examples.

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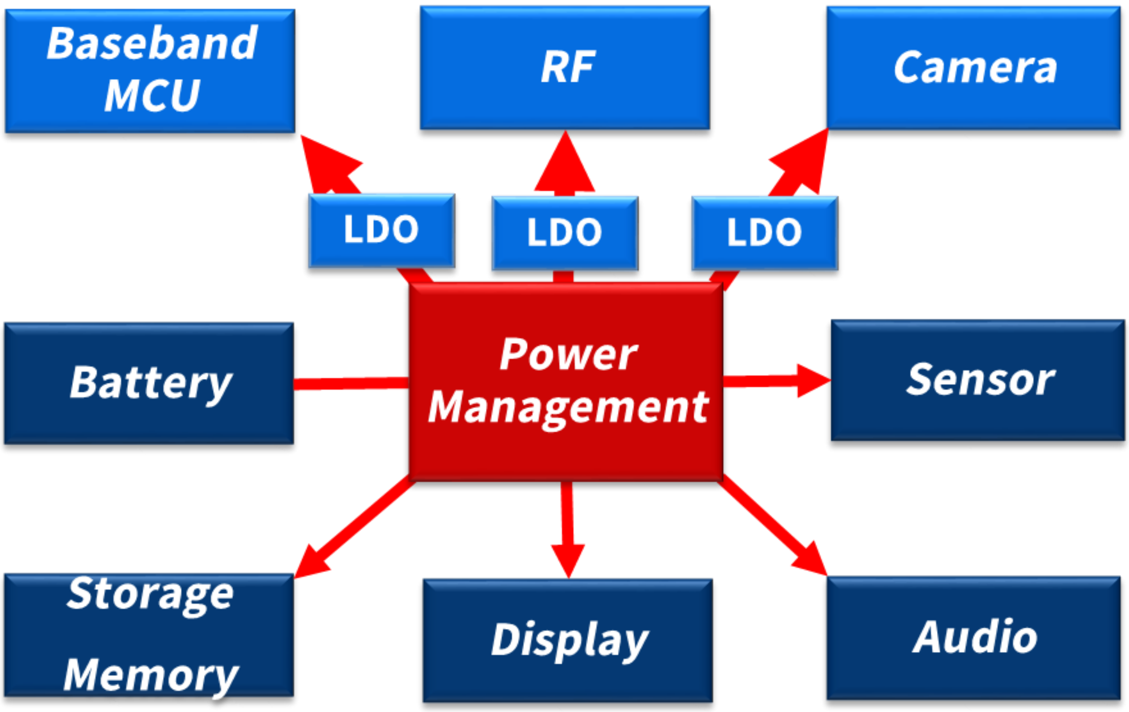
1. Introduction

The average power consumption of mobile devices and other consumer electronics is generally reduced by controlling power supplies according to their power use. Since consumer electronics incorporate various electronic circuits including wireless communication, camera, display, audio, and storage circuits, it is necessary to effectively control their power supplies in order to obtain the optimum performance from each circuit. For this purpose, efficient use of power supply ICs is important.

Figure 1.1 Typical block diagram of consumer electronics
Because power supply circuits are closely related to all the blocks,
reducing their power consumption is crucial.



To prolong battery operating time and reduce heat dissipation, it is necessary to maximize the power efficiency of all the blocks.

Precise voltage conversion to roughly 1.0 V and high-current capability are required for the power supplies of CMOS image sensors, MCUs, and RF circuits. It is therefore extremely important to improve the power efficiency of LDO regulators. The following sections describe how to maximize power efficiency of LDO regulators.

2. Low-dropout characteristics required to maximize the power efficiency of an LDO regulator

2.1 What is dropout voltage?

For typical voltage regulation, the input voltage for an LDO regulator must be higher than the required output voltage. Dropout voltage is defined as the minimum input-output voltage differential required to maintain output voltage regulation at a desired output current. Therefore, dropout voltage is also referred to as the minimum input-output voltage differential. Table 2.1 is an example of a dropout voltage table.

Table 2.1 Dropout voltage of the TCR5BM series (excerpt from the datasheet)

Output voltages	VBIAS input voltage	IOUT = 500 mA			Unit
		Min	Typ.	Max (Note 10)	
0.8 V, 0.85 V	3.3 V	—	90	125	mV
0.9 V, 0.95 V	3.3 V	—	95	130	mV
1.0 V	3.3 V	—	95	135	mV
1.05 V, 1.1 V	3.3 V	—	100	140	mV
1.15 V	3.3 V	—	100	145	mV
1.2 V	3.3 V	—	105	150	mV

Reading a dropout voltage table

Suppose that you want to use an LDO regulator at V_{OUT} = 1.2 V and I_{OUT} = 500 mA. In this case, the maximum dropout voltage is 150 mV. Hence,

Minimum input voltage = 1.2 V + 0.15 V
= 1.35 V

Therefore, input voltage must be 1.35 V or higher, and V_{BIAS} must be over 3.3 V.

2.1.1 Formula for calculating the power loss of an LDO regulator

The equation for calculating the power loss of an LDO regulator is shown below. When the supply current of an LDO regulator is considerably lower than its output current, it exhibits a power loss equal to dropout voltage (V_{IN} – V_{OUT}) multiplied by output current. In this case, a power loss can be reduced by selecting an LDO regulator with low dropout voltage and minimizing its input voltage.

Power loss of an LDO regulator = (input power) – (output power)

$= (V_{IN} \times I_{IN}) - (V_{OUT} \times I_{OUT})$

* When supply current << I_{OUT}, $I_{IN} \approx I_{OUT}$

$\approx (V_{IN} - V_{OUT}) \times I_{OUT}$

This is the minimum dropout voltage.

2.1.2 Formula for calculating the power efficiency of an LDO regulator

The equation for calculating the power efficiency of an LDO regulator is shown below. Power efficiency is defined as output power/input power. Therefore, when the supply current of an LDO regulator is considerably smaller than its output current, power efficiency can be approximated to V_{OUT}/V_{IN}. It is therefore important to minimize V_{IN} as is the case for reducing a power loss. This means that selecting an LDO regulator with low dropout voltage is important.

Power efficiency of an LDO regulator = $\frac{\text{Output power}}{\text{Input power}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$

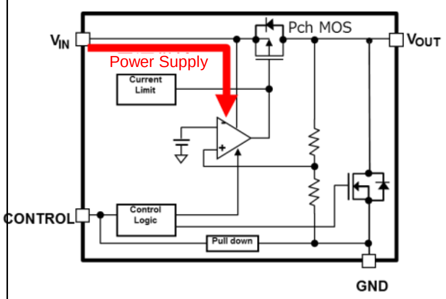
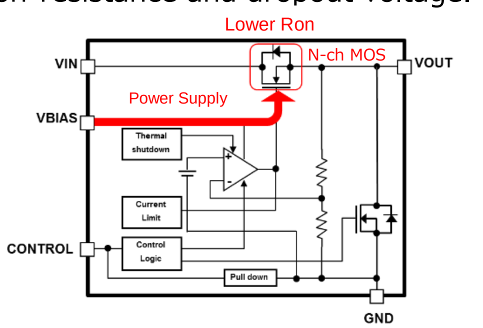
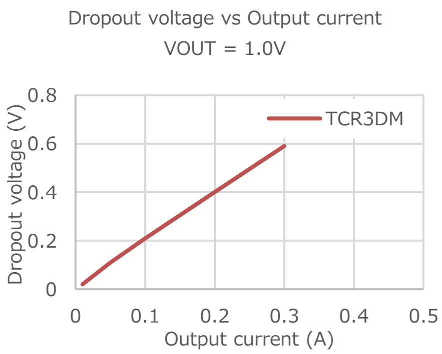
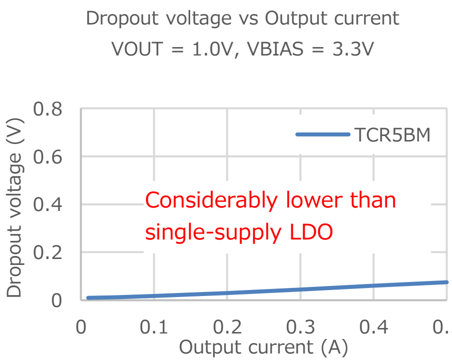
* When supply current << I_{OUT}, $I_{IN} \approx I_{OUT}$

$\approx \frac{V_{OUT}}{V_{IN}}$ **(i.e., the ratio of input voltage to output voltage)**

2.2 Low-dropout characteristics of dual-power-supply LDO regulators

A conventional LDO regulator has a single power supply (VIN), which is used to drive the gate of an internal P-channel MOSFET as shown below. Consequently, when the VIN voltage is low, the MOSFET gate voltage decreases to a level that makes it impossible for the LDO regulator to maintain a regulated output voltage. In contrast, dual-power-supply LDO regulators such as the TCR5BM series incorporate an N-channel MOSFET to reduce on-resistance. In addition to VIN, dual-power-supply LDO regulators have a pin called VBIAS that drives the gate of the internal MOSFET. Being independent of the VIN input, the VBIAS pin helps reduce dropout voltage. This makes it possible to reduce the input voltage, considerably reducing power loss. Dual-power-supply LDO regulators provide precise voltage regulation with minimum power loss. The next subsection discusses the changes in characteristics over a range of voltage applied to the VBIAS pin.

Table 2.2 Comparison between single- and dual-power-supply LDO regulators

Type of LDO regulator	Single-power-supply LDO regulators	Dual-power-supply LDO regulators
Internal MOSFET polarity	P-channel	N-channel
Power supplies	Only VIN	VIN, VBIAS
Dropout characteristics	The gate voltage for the internal P-channel MOSFET is supplied from VIN.  	The gate voltage for the internal N-channel MOSFET is supplied from the VBIAS pin. This circuit configuration reduces the MOSFET on-resistance and dropout voltage. 
Dropout voltage characteristics (V_{OUT} = 1.0 V)	 	

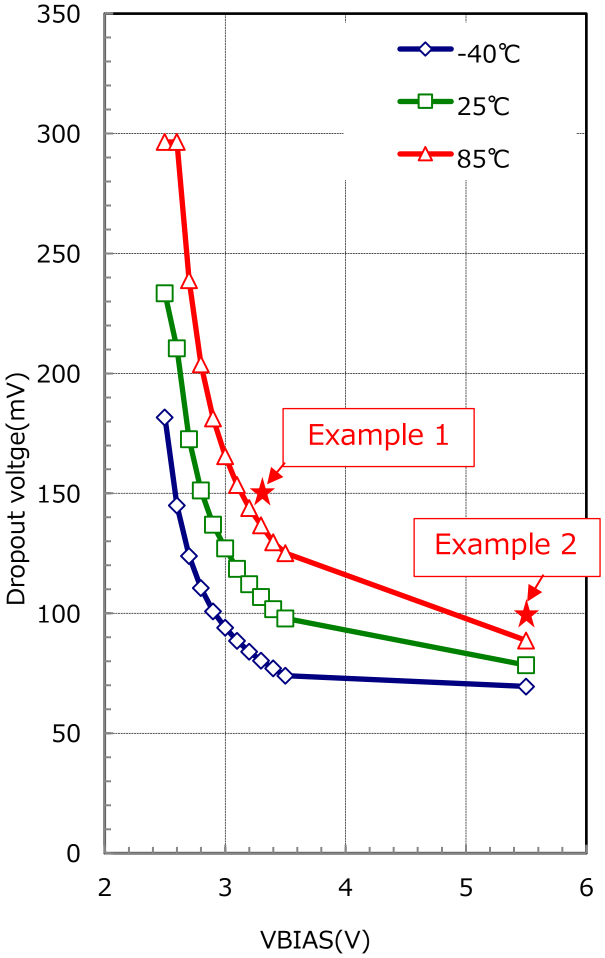
2.3. VBIAS voltage vs. Dropout voltage characteristics

Figure 2.3 shows the V_{BIAS}-vs-dropout voltage curves of the TCR5BM12 (with V_{OUT}=1.2 V) at different temperatures. As shown in Figure 2.3, as V_{BIAS} increases, dropout voltage decreases. Figure 2.3.1 and Figure 2.3.2 show examples of a circuit with V_{BIAS} = 3.3 V and V_{BIAS} = 5.5 V, respectively. Increasing V_{BIAS} from 3.3 V to 5.5 V makes it possible to reduce V_{IN} and thereby improve power efficiency. Be sure to check the "Dropout voltage" table provided in a datasheet when using VIN at low voltage.

If the power supply to the VBIAS pin is connected to other loads in parallel, a sudden change in any of their load currents could cause an instantaneous drop in the VBIAS voltage. In order to maintain the VBIAS pin at a proper voltage even in this situation, a 1-μF or greater capacitor should be added to the VBIAS pin.

Figure 2.3 Dropout voltage

TCR5BM12 (V_{OUT} = 1.2 V,500 mA)



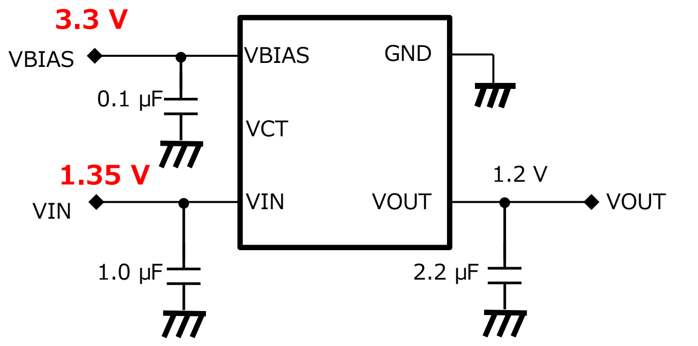


Figure 2.3.1 TCR5BM12 circuit example 1

V_{IN} = 1.35 V and V_{OUT} = 1.2 V when V_{BIAS} ≥ 3.3 V

89% power efficiency at I_{OUT} = 500 mA

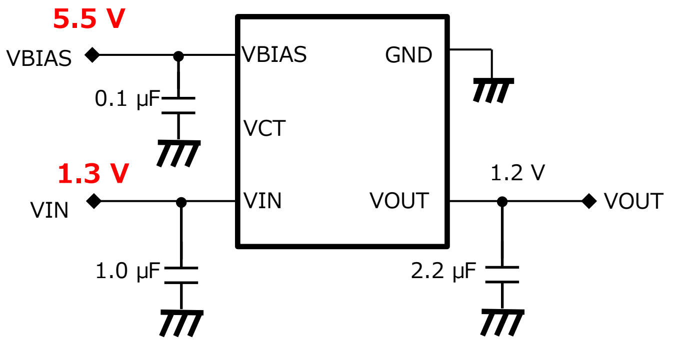


Figure 2.3.2 TCR5BM12 circuit example 2

V_{IN} = 1.3 V and V_{OUT} = 1.2 V when V_{BIAS} = 5.5 V

92% power efficiency at I_{OUT} = 500 mA

3. Examples of application circuits using a dual-power-supply LDO regulator for the power supplies of CMOS image sensors, MCUs, and RF circuits

The following subsections show typical application circuits to obtain the best performance from the TCR5BM and TCR8BM LDO regulators with low dropout characteristics. These application circuits are for the power supplies of CMOS image sensors, MCUs, and RF circuits.

3.1 Example of an application circuit for the power supply of CMOS image sensors

Application circuit with a power efficiency of 89%

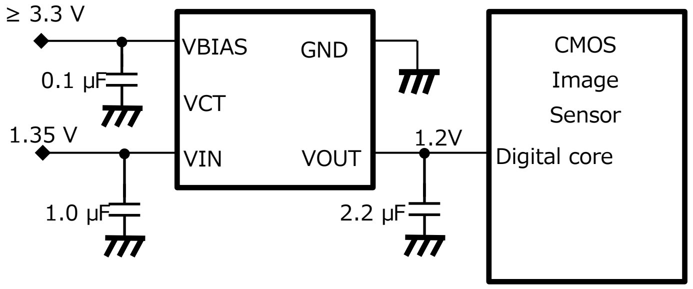


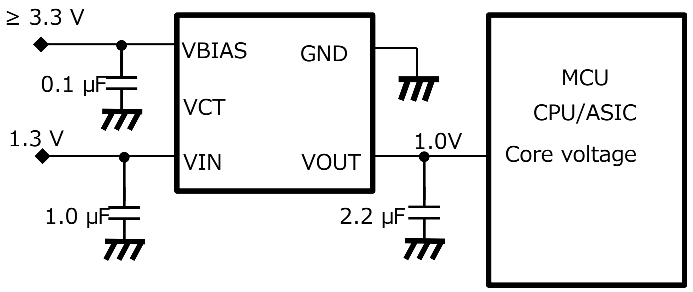
Figure 3.1 TCR5BM12A for CMOS image sensor

Part number	TCR5BM12A
Power loss	75 mW
Power efficiency	89% (V_{OUT}/V_{IN})
VIN	1.35 V
VBIAS	3.3 V
VOUT	1.2 V
IOUT	500 mA
CIN	1 µF
CBIAS	0.1 µF
COUT	2.2 µF

The above application circuit example is intended only as a guide. For load transient response, ripple rejection ratio, and other characteristics, see the application note LDO Regulator Application Circuits for the Power Supplies of CMOS Image Sensors, which will shortly be released.

3.2 Example of an application circuit for the power supply of MCUs

Application circuit with a power efficiency of 77%

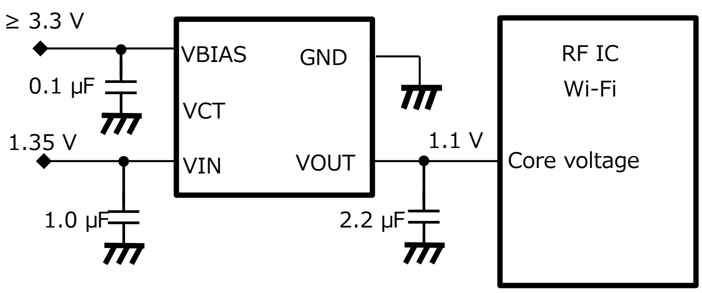


Part number	TCR8BM10A
Power losses	240 mW
Power efficiency	77% (V_{OUT}/V_{IN})
VIN	1.3 V
VBIAS	3.3 V
VOUT	1.0 V
IOUT	800 mA
CIN	1 µF
CBIAS	0.1 µF
COUT	2.2 µF

The above application circuit example is intended only as a guide. For load transient response, ripple rejection ratio, and other characteristics, see the application note LDO Regulator Application Circuits for the Power Supplies of MCUs, which will shortly be released.

3.3 Example of an application circuit for the power supply of RF circuits

Application circuit with a power efficiency of 81%



Part number	TCR5BM11A
Power losses	125 mW
Power efficiency	81% (V_{OUT}/V_{IN})
VIN	1.35 V
VBIAS	3.3 V
VOUT	1.1 V
IOUT	500 mA
CIN	1 µF
CBIAS	0.1 µF
COUT	2.2 µF

The above application circuit example is intended only as a guide. For load transient response, ripple rejection ratio, and other characteristics, see the application note LDO Regulator Application Circuits for the Power Supplies of RF Circuits, which will shortly be released.

4. Summary

Toshiba's dual-power-supply LDO regulators provide a high-current and low-voltage output with high power efficiency and low power loss. These LDO regulators are ideal for the power supplies of the digital cores in CMOS image sensors, MCU cores, and RF circuits. See datasheets for detailed electrical characteristics.

Dual-power-supply low-dropout LDO regulators that provide high power efficiency:

To download the datasheet for the TCR5BM 500-mA LDO regulator→ Click Here

To download the datasheet for the TCR8BM 800-mA LDO regulator → Click Here

To download the datasheet for the TCR13AGADJ 1.3-A LDO regulator→ Click Here

To download the datasheet for the TCR15AG 1.5-A LDO regulator→ Click Here

See the application note Low-Dropout (LDO) Regulator ICs for how to use LDO regulators.
To download the application note Low-Dropout (LDO) Regulator ICs→ Click Here

To view the lineup of other LDO regulators→ Click Here

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