Thermal Design to Maximize the Performance of LDO Regulators

Outline:

Low-dropout (LDO) regulators are semiconductor devices that easily generate heat. This application note describes how to maximize the performance of LDO regulators without compromising system safety and reliability. It also provides thermal design examples using Toshiba's 300-mA TCR3DM LDO regulator as well as the 500-mA TCR5BM and 800-mA TCR8BM dual-power-supply LDO regulators.

Table of Contents

1. Introduction

Mobile devices and other electronic systems are becoming increasingly sophisticated. Various electronic components are used to enhance their performance and functionality, including high-performance semiconductor devices. However, processors and power supply ICs, for example, dissipate lots of power when they operate at high speed or supply large current to a load. The dissipated power is released as heat, which further increases not only the temperature of heat-generating semiconductor chips but also the temperature in a confined space within the chassis of an electronic system. This increases the possibility that the heat-generating chips might malfunction because of a rise in chip temperature. Neighboring electronic devices might also malfunction, being exposed to high temperature.

Although LDO regulators are essential components for mobile devices and other electronic systems, they generate heat due to power dissipation, depending on how they are used. This application note describes the heat generation mechanism of LDO regulators and then discusses thermal design techniques, or more specifically, how to set the supply voltage to obtain the required output voltage and current so that LDO regulators exhibit the maximum performance without generating unnecessary heat.

CMOS LDO regulators are broadly divided into P-channel and N-channel regulators with a MOS output. The following sections use Toshiba's TCR3DM, a 300-mA P-channel CMOS LDO regulator, as well as the TCR5BM and TCR8BM, 500-mA and 800-mA N-channel dual-power-supply CMOS LDO regulators, to show how to calculate chip temperature. The TCR5BM and TCR8BM, N-channel dual-power-supply CMOS LDO regulators, have an advantage over typical P-channel CMOS LDO regulators such as the TCR3DM in terms of both low heat generation and high performance.

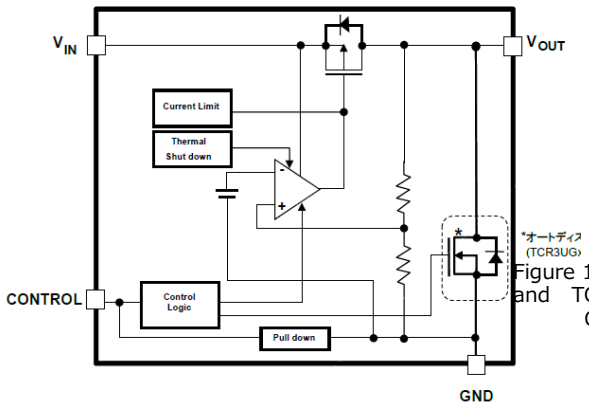

Figure 1.1 Block diagram of the TCR3DM P-channel CMOS LDO regulator

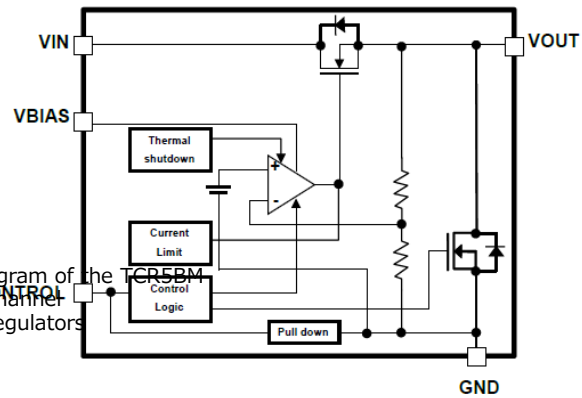

Figure 1.2 Block diagram of the TCR5BM and TCR8BM N-channel dual-power-supply CMOS LDO regulators

2. Heat generation mechanism of LDO regulators and adverse impact of heat generation

2.1 Heat generation mechanism of LDO regulators: Thermal resistance

Figure 2.1 shows a simplified schematic of a typical P-channel CMOS LDO regulator.

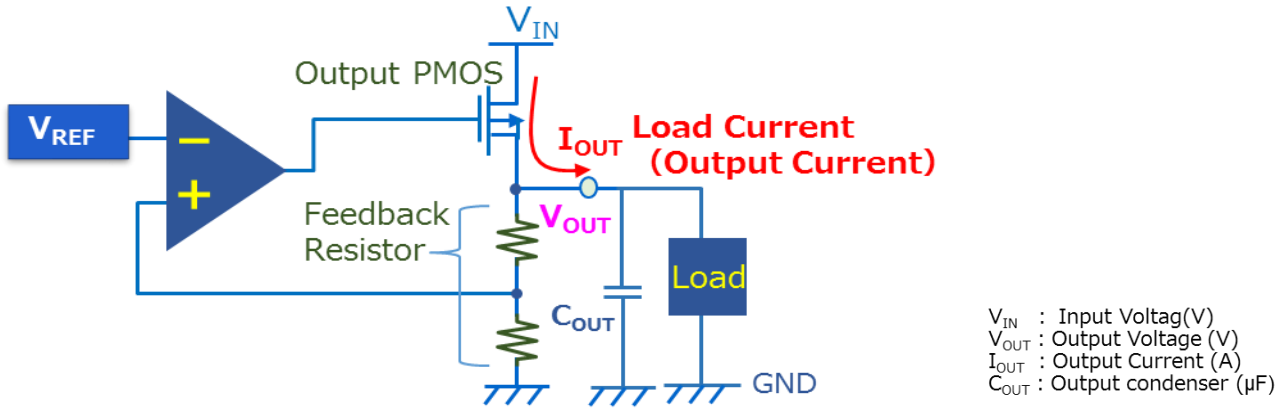

Figure 2.1 Simplified schematic of a typical P-channel CMOS LDO regulator

When an LDO regulator supplies current to a load, it incurs power dissipation (P_D), which is expressed as follows:
This equation indicates that most of the power dissipation of an LDO regulator occurs in the output MOS transistor.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \qquad \text{(W) ..... Equation 1}$$

Therefore, power dissipation increases as the input-output voltage differential and the output current increase. Power dissipation is converted into heat. If the LDO regulator chip is placed in an environment that facilitates heat dissipation, the heat generated by power dissipation is quickly removed and does not cause the chip temperature to rise considerably. However, LDO regulators are generally encapsulated in a molded package with low heat conductivity. Since LDO regulators are commonly used in the narrow chassis of mobile devices, their chip temperature tends to increase because of low thermal dissipation.

The resistance to heat flow is called thermal resistance, which includes the resistance of the molded package and the environment in which an LDO regulator is placed. Figure 2.2 shows a thermal resistance model of an integrated circuit (IC), showing thermal resistances in an IC.

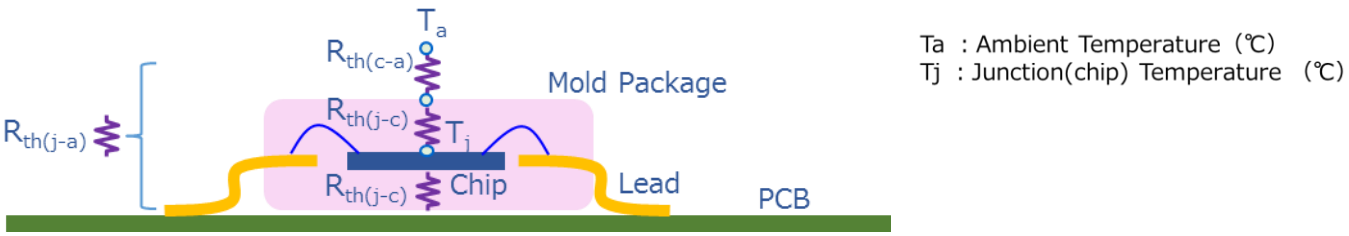

Figure 2.2. Thermal resistance model of an LDO regulator

The model shown in Figure 2.2 consists of two thermal resistances:

- $R_{th(j-c)}$: Junction-to-case (chip-to-molded package) thermal resistance
- $R_{th(c-a)}$: Case-to-ambient thermal resistance

Generally, $R_{th(j-a)}$, which is the sum of $R_{th(j-c)}$ and $R_{th(c-a)}$, is used to calculate a rise in chip temperature with respect to the ambient temperature (T_a):

- $R_{th(j-a)}$: Junction-to-ambient thermal resistance

The $R_{th(j-a)}$ value (in °C/W) shown in a datasheet is the thermal resistance calculated from power dissipation.
In practice, the $R_{th(j-a)}$ value is affected by heat dissipation from the printed circuit board (PCB) on which an LDO regulator is mounted. Therefore, $R_{th(j-a)}$ varies with the PCB size and metal traces on the PCB.

2.2 Adverse effects of heat generation from an LDO regulator

Thermal resistance, $R_{th(j-a)}$, is a measure of an object's ability to resist a heat flow. Because of the presence of $R_{th(j-a)}$, the power dissipation expressed as Equation 1 causes a rise in chip temperature with respect to the ambient temperature.
An LDO regulator might exhibit the following failures in the event of an excessive rise in chip temperature:

1) If chip temperature exceeds the absolute maximum junction temperature (150°C), electrons in the valence band of semiconductor atoms are excited into the conduction band by thermal energy. Consequently, these electrons contribute to electrical conduction in addition to the carriers released by P-type and N-type dopants, making a MOS transistor uncontrollable.
2) The integrated thermal shutdown (TSD) circuit is tripped to shut down the LDO regulator. The LDO regulator returns to normal operation when the chip temperature drops below the TSD recovery threshold. However, if the heating conditions persist, the chip temperature rises again, tripping the TSD circuit. As a result, the LDO regulator cycles in and out of the TSD mode.
3) Heat increases the probabilities of reliability failures such as time-dependent dielectric breakdown (TDDB), negative bias temperature instability (NBTI), and electromigration, adversely affecting the operating stability of an LDO regulator over the long term.

Since a rise in chip temperature causes failures of an LDO regulator and degrades its reliability, appropriate thermal design is crucial.
The next section discusses thermal design for a P-channel CMOS LDO regulator.

3. Thermal design for a P-channel CMOS LDO regulator

3.1 Example of calculating the chip temperature of the TCR3DM P-channel CMOS LDO regulator

This subsection uses the TCR3DM as an example to describe how to calculate chip temperature.

Chip temperature (T_j) is calculated as follows:

$$T_j = T_a + P_D \times R_{th(j-a)} = T_a + (V_{IN} - V_{OUT}) \times I_{OUT} \times R_{th(j-a)} \quad (°C) \text{ ..... Equation 2}$$

Here, assume the following conditions:

Input voltage, V_{in}: 3 V

Output voltage, V_{OUT}: 1 V

Load current, I_{OUT}: 200 mA

Thermal resistance, $R_{th(j-a)}$: 298°C/W (calculated from the 420-mW power dissipation shown in the datasheet)

Conditions for the measurement of power dissipation:

Glass-epoxy board (FR4)

Board size: 40 mm x 40 mm (double-sided board), t = 1.6 mm

Trace percentage: 50% on both the top and bottom layers

Through-holes: 0.5 mm in diameter x 24

When the ambient temperature (T_a) is 25°C and 85°C, chip temperature is calculated as:

T_a=25°C: $T_j = 25℃ + (3\,\mathrm{V} - 1\,\mathrm{V}) \times 200\,\mathrm{mA} \times 298℃/\mathrm{W} = 144°C$

T_a=85°C: $T_j = 85℃ + (3\,\mathrm{V} - 1\,\mathrm{V}) \times 200\,\mathrm{mA} \times 298℃/\mathrm{W} = 204°C$

The chip temperature exceeds the absolute maximum junction temperature (150°C) when the ambient temperature (T_a) is 85°C. To decrease chip temperature, it is necessary to reduce the input voltage.

If the input voltage is 2 V, chip temperature is calculated as:

T_a=25°C: $T_j = 25℃ + (2\,\mathrm{V} - 1\,\mathrm{V}) \times 200\,\mathrm{mA} \times 298℃/\mathrm{W} = 84.6°C$

T_a=85°C: $T_j = 85℃ + (2\,\mathrm{V} - 1\,\mathrm{V}) \times 200\,\mathrm{mA} \times 298℃/\mathrm{W} = 145°C$

At an input voltage of 2 V, chip temperature remains below the absolute maximum junction temperature (150°C) even when the ambient temperature is 85°C. Reducing the input voltage of an LDO regulator is a commonly used technique to reduce its power dissipation and thereby chip temperature.

In the above example, reducing the input voltage to 2 V reduces the chip temperature (T_j) to 145°C when the ambient temperature (T_a) is 85°C. Since this is still close to the absolute maximum junction temperature (150°C), it is necessary to further derate the LDO regulator for

lower input voltage. (Derating at less than 80% of the absolute maximum ratings is recommended.) However, Figure 2.1 indicates that reducing input voltage reduces the gate-source voltage (V_{GS}) of the P-channel output MOS transistor. Therefore, too low input voltage does not provide an LDO regulator with sufficient current drive capability and degrades its electrical characteristics. In such cases, it is necessary to consider dropout voltage, an important characteristic of the LDO regulator, for thermal design, which is discussed in the next subsection.

3.2 Dropout characteristics of an LDO regulator: Minimum input voltage

Dropout voltage, an important characteristic of an LDO regulator, is defined as the minimum input-output voltage differential ($V_{IN}-V_{OUT}$) required to maintain output voltage regulation at the specified output current. In other words, dropout voltage indicates the minimum input voltage required for proper operation of an LDO regulator.

Figure 3.1 shows the dropout characteristics of the TCR3DM P-channel CMOS LDO regulator and the TCR5BM N-channel CMOS LDO regulator at an output voltage (V_{OUT}) of 1.0 V.

* T_a=25°C and V_{BIAS}=3.3 V. Dropout voltage is calculated from the input voltage that provides an output voltage equal to 98% of V_{BIAS} (=3.3 V). (V_{BIAS} is discussed later.)

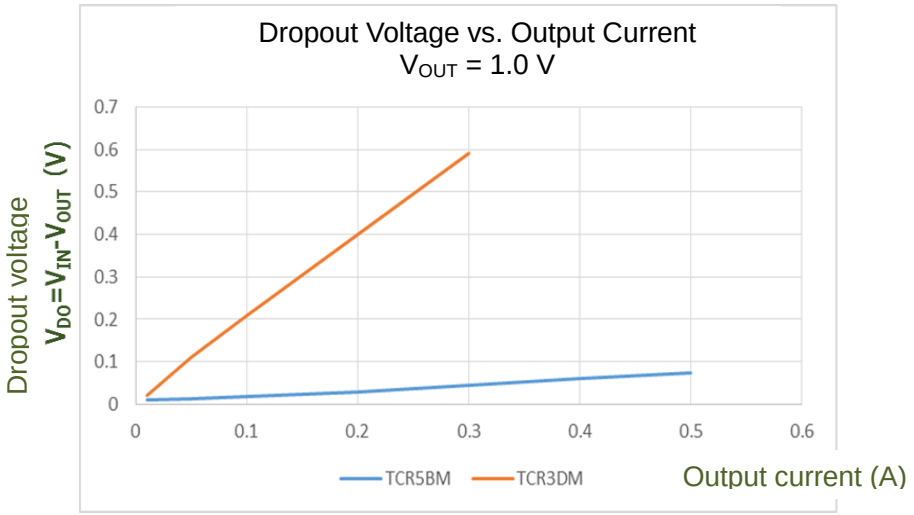

Figure 3.1 TCR3DM/TCR5BM dropout characteristics (V_{OUT} =1 V, T_a = 25°C)

Figure 3.1 shows that the TCR3DM exhibits a dropout voltage of 0.6 V when the load current is 300 mA. Therefore, it requires an input voltage of 1.6 V or higher to regulate output voltage to 1.0 V (T_j=25°C, typical case). Reducing the input voltage below 1.6 V (for example, 1.5 V) to reduce heat dissipation causes the output voltage to decrease and degrades other AC characteristics.

The TCR5BM N-channel dual-power-supply CMOS LDO regulator exhibits a much lower dropout voltage than the TCR3DM. Even at a load current of 500 mA, the TCR5BM has a dropout voltage of only roughly 80 mV. Therefore, the TCR5BM can regulate the output voltage to 1.0 V with V_{IN}=1.08 V.

P-channel CMOS LDO regulators generally have large dropout voltage because of their low current drive capability. (Their dropout voltage tends to increase at low output voltage.) It is therefore advisable to use an N-channel CMOS LDO regulator with higher current drive capability when it is necessary to reduce input voltage so as to reduce heat dissipation. Dual-power-supply LDO regulators are very useful since one supply voltage can be used for the gate drive of an external N-channel MOSFET.

The next section describes Toshiba's N-channel dual-power-supply CMOS LDO regulators and a thermal design technique using them.

4. Thermal design using the TCR5BM and TCR8BM Dual-power-supply N-channel CMOS LDO regulators

Dual-power-supply N-channel CMOS LDO regulators greatly help to maintain output voltage regulation while reducing heat dissipation.
Figure 4.1 shows a simplified schematic of the TCR5BM and TCR8BM.

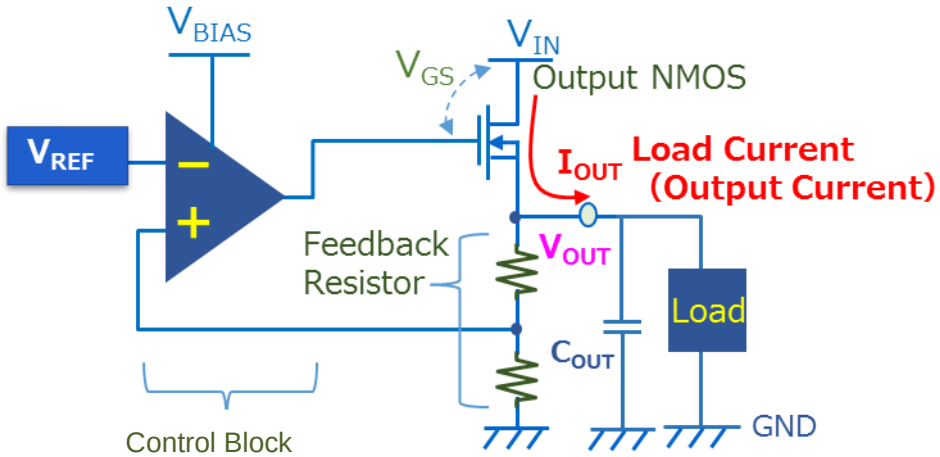

Figure 4.1 Simplified schematic of the TCR5BM and TCR8BM dual-power-supply N-channel CMOS LDO regulators

Because these dual-power-supply LDO regulators incorporate N-channel output MOS transistors, they provide low dropout voltage, making it possible to reduce input voltage.
In addition, the power supply for the control section is separated as bias voltage (V_{BIAS}) from the input voltage (V_{IN}) for the N-channel output MOS transistor. Therefore, it is possible to increase the gate voltage of the output MOS transistor by increasing V_{BIAS}. This helps to further increase the current drive capability of the output MOS transistor. (Since the control section has low supply current, increasing V_{BIAS} hardly contributes to heat dissipation.)

Since this circuit configuration helps to further reduce the dropout voltage, the input voltage (V_{IN}) for the N-channel output MOS transistor of the TCR5BM and TCR8BM can be much lower than that of a P-channel CMOS LDO regulator. Therefore, the TCR5BM and TCR8BM dissipate much less heat. The TCR5BM and TCR8BM simplify thermal design because they combine high performance and low heat dissipation.
The following shows an example of thermal design for the TCR5BM. Here, assume the following conditions:

Input voltage for the N-channel output MOS transistor, V_{IN}: 1.15 V (to make $V_{IN}-V_{OUT}$ greater than the dropout voltage of the TCR5BM)
Bias voltage of the control section, V_{BIAS}: 3.3 V
Output voltage, V_{OUT}: 1 V
Load current, I_{OUT}: 300 mA
Thermal resistance, $R_{th(j-a)}$: 208°C/W (calculated from the 600-mW power

dissipation shown in the datasheet)

Conditions for the measurement of power dissipation:
Glass-epoxy board (FR4)
Board size: 40 mm x 40 mm (double-sided board), t = 1.8 mm
Trace percentage: 70% on all layers

In this case, chip temperature can be calculated as follows:

When T_a=85°C:

$$\mathbf{T_j = 85℃ + (1.15\ V - 1\ V) \times 300\ mA \times 208℃/W} = 94°C$$

Even when the ambient temperature is high, chip temperature is much lower than the absolute maximum junction temperature of 150°C.

Even when the load current is at a maximum of 500 mA,

$$\mathbf{T_j = 85℃ + (1.15\ V - 1\ V) \times 500\ mA \times 208℃/W} = 101°C$$

Still, the chip temperature has a sufficient margin relative to the absolute maximum junction temperature. The dual-power-supply N-channel CMOS LDO regulators provide an outstanding solution for thermal design as they combine low heat dissipation and high performance.

5. Summary

The heat generated by LDO regulators and other semiconductor devices not only degrades their performance and reliability but also adversely affects the entire electronic systems. Reducing input voltage is effective in reducing heat generation. Dual-power-supply N-channel CMOS LDO regulators with low dropout voltage such as the TCR5BM and TCR8BM series simplify thermal design while providing high voltage regulation performance.

Toshiba's TCR5BM and TCR8BM series are available with an output current from 500 mA to 1.5 A, making them suitable for a wide range of applications.

Dual-power-supply low-dropout LDO regulators that provide high power efficiency:

To download the datasheet for the TCR5BM 500-mA LDO regulator→ Click Here

To download the datasheet for the TCR8BM 800-mA LDO regulator → Click Here

To download the datasheet for the TCR13AGADJ 1.3-A LDO regulator→ Click Here

To download the datasheet for the TCR15AG 1.5-A LDO regulator→ Click Here

See the application note Low-Dropout (LDO) Regulator ICs for how to use LDO regulators.
To download the application note Low-Dropout (LDO) Regulator ICs→ Click Here

To view the lineup of other LDO regulators→ Click Here

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