TOSHIBA

Dear Cutomers,

March, 2019

Datasheet Correction: I2C function of TX Family

This informs you that we found the following corrections should be made to the datasheets as shown below. If you have any questions or require any further informaiton, please contact your local Toshiba representatives.

1. Products

M030 Group

TMPM036FW TMPM037FW

M460 Group

TMPM461F10 TMPM461F15 TMPM462F10 TMPM462F15 TMPM46BF10

A900 Group

TMPA900CM TMPA901CM

A910 Group

TMPA910CR TMPA911CR TMPA912CR TMPA913CR

2. Corrections

The function of I^2C use are changed as following.

Note : This information explains the correction using the TMPM037FWUG product.

<Correction 1: Setup time>

Control int the I²C Bus mode

[Old]

13.4.1.1 Clock source

I2CxCR1<SCK[2:0]> is used to set the high and low periods of the serial clock to be output in master mode.

In master mode, the hold time when a start conditions generated and the setup time when a stop condition is generated are defined as t_{HIGH}[S].

When I2CxCR2<PIN> is set to "1" in slave mode, the time to the release of SCLx is defined as tLOW [S].

[New]

13.4.1.1 Clock source

I2CxCR1<SCK[2:0]> is used to set the high and low periods of the serial clock to be output in master mode.

In master mode, the hold time when a start conditions generated and the setup time when a stop condition is generated are defined as the following.

Hold time: t_{HIGH} [S]

Setup time: I2CxPRS<PRSCK>=1: t_{HIGH} [S]

I2CxPRS<PRSCK>≠1: t_{HIGH} - Tprsck [S]

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<Correction 2: I2CxCR register>

Register

[Old]

13.3.5 I2CxCR2(Control register 2)

2	-	R	Read as 0.
1-0	SWRES[1:0]	W	Software reset generation Write "10" followed by "01" to generate a reset. For detail, refer to "13.4.11 Software Reset".

Note 1: Make sure that modes are not changed during a communication session. Ensure that the bus is free before switching the operating mode to the port mode. Ensure that the port is at the "High" level before switching the operating mode from the port mode to the I2C bus mode.

Note 2: The I2CxCR2<I2CM> bit cannot be cleared to 0 to disable I2C operation while transfer operation is being performed. before clearing this bit, mask sure that transfer operation is completely stopped by reading the status register.

[New]

13.3.5 I2CxCR2(Control register 2)

2	-	R	Read as "0".
1-0	SWRES[1:0]	W	Software reset generation Write "10" followed by "01" to generate a reset. For detail, refer to "13.4.11 Software Reset".

Note: Make sure that modes are not changed during a communication session. Ensure that the bus is free before switching the operating mode to the port mode. Ensure that the port is at the "HIGH" level before switching the operating mode from the port mode to the I2C bus mode.

Note: The I2CxCR2<I2CM> bit cannot be cleared to 0 to disable I2C operation while transfer operation is being performed. before clearing this bit, mask sure that transfer operation is completely stopped by reading the status register.

Note: Don't change the contents of the registers, except <SWRST[1:0]>, when the start condition is generated, the stop condition is generated or the data transfer is in progress. Write data to the registers before the start condition is generated or during the period from when an interrupt request is generated for stopping the data transfer until it is released

<Correction 3: Waveform of STOP condition>

Control in the I2C Bus mode

[Old]

No Information

[New]

13.4.8.1 Recognition of STOP condition and SDA tr

This product requires that the recognition period of the STOP condition in master mode is within the range of (a) in the following formula. Please use your product under the following conditions.

(a) = Tprsck x 6 - 1/fsys

Ex: fsys = 80MHz, Tprsck = 150 (ns)

(a) = 150 x 6 - 12.5 = 900 - 12.5 = 877.5 (ns)

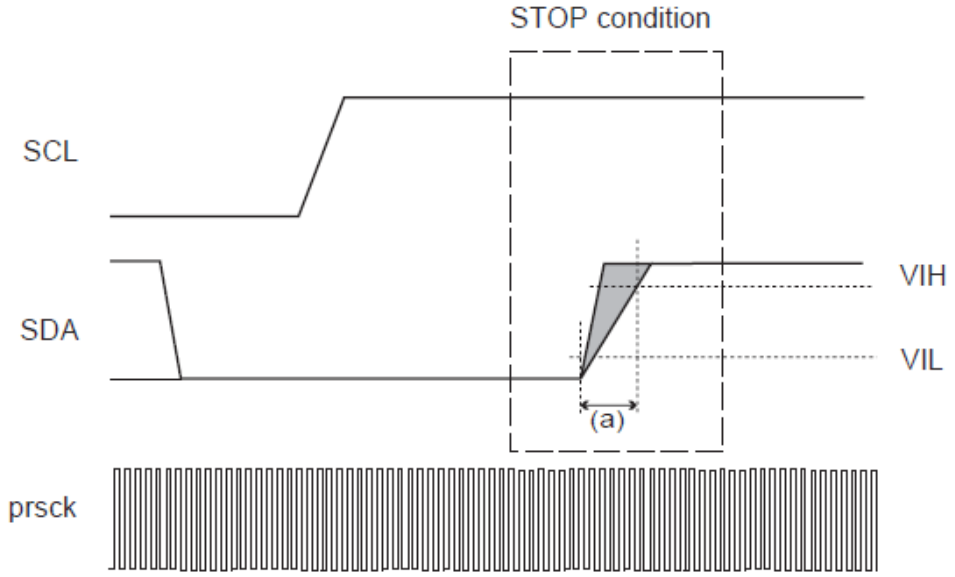

Figure 13-8 Recognition of STOP condition (condition of tr)