Basic Characteristics and Application Circuit Design of IC Couplers for Gate Drive of Power Devices

Outline:

Of Toshiba's photocoupler offerings, this application note focuses on IC-output photocouplers (IC couplers) for the gate drive of power devices (gate-drive photocouplers). It discusses different types of gate-drive photocouplers, key points for the selection of gate-drive photocouplers, and their major electrical characteristics as well as how to calculate their power losses.

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Motor control assumes a key role for many industrial electronic systems. Inverter and servo motors are commonly used for industrial applications. In these applications, motor control signals are transferred from a low-voltage system operating at a few volts to a high-voltage system operating at a few hundred volts driving a motor, also are transferred through the electronic circuit which is composed of power semiconductor devices that directly drives a motor and is exposed to operating electrical potential changes exceeding about 200 to 300 V. Photocouplers are often used to transfer electrical signals between the low-voltage and the high-voltage systems. Typically, photocouplers consist of a light emitting device optically coupled with a light detecting device via a transparent galvanic insulator. They are used to transfer electrical signals between two circuits with different ground potentials by means of light. As industrial applications become progressively smaller, photocouplers are commonly used because they provide high isolation between input and output, suppress induced electromotive force, and simplify noise blocking.

In response to these market requirements, Toshiba provides an extensive portfolio of various high-speed photocouplers consisting of a light emitting diode (LED) and a light detecting IC with short response times. Toshiba's IC-output photocoupler offerings include those specifically designed for the gate drive of power semiconductor devices. This application note discusses different types of IC-output photocouplers for the gate drive of power semiconductor devices (gate-drive photocouplers), key points for the selection of gate-drive photocouplers, and their major electrical characteristics as well as how to calculate their power losses.

1. Lineup and major characteristics of gate-drive photocouplers

1.1 Lineup of gate-drive photocouplers

Table 1.1 lists Toshiba's major gate-drive photocouplers.

They are available with different peak output current, propagation delay time, operating supply voltage, and packaging, allowing you to select the optimum ones according to the gate capacitance, operating frequency, and gate voltage of the driven power devices as well as the safety standards to be complied with and isolation distance.

Table 1.1 Major gate-drive photocouplers

Creepage and clearance distances (Min.)		5 mm	8 mm	8 mm	8 mm
Isolation voltage		3750 Vrms	5000 Vrms	5000 Vrms	5000 Vrms
Peak output current	Propagation delay time	SO6 	SO6L 	SO16L 	DIP8 
6.0 A	500 ns				TLP358H
4.0 A	150 ns		TLP5754 (R-to-R)* TLP5774 (R-to-R)*	TLP5214/ TLP5214A (OCP/AMC/R-to-R)**	
2.5 A	Up to 150 ns		TLP5752 (R-to-R)* TLP5772 (R-to-R)*		
	Up to 200 ns	TLP152	TLP5702		TLP352
	500 ns				TLP250H TLP350H
1.0A	Up to 150 ns		TLP5751 (R-to-R)* TLP5771 (R-to-R)*		
0.6 A	Up to 200 ns	TLP155E			
	500 ns	TLP151A	TLP5701		TLP351A
	700 ns				TLP351H

:Supply voltage: 10 to 30 V

* R-to-R (Rail-to-Rail):

Rail-to-Rail means the output signal swings close to supply voltage levels. Photocouplers with a Rail-to-Rail output can drive the following power device gate at a higher voltage and with lower power loss than those with a non-rail-to-rail output. Photocouplers with a rail-to-rail output also incur lower internal power loss because of low internal resistance.

** OCP (Overcurrent protection):

Gate-drive photocouplers with overcurrent protection monitor the saturation voltage between the collector and emitter (V_{CE}) of the following power device via the DESAT pin to detect overcurrent conditions and shut down their output in the event of overcurrent. Normally, V_{CE} is equal to the collector-emitter saturation voltage, $V_{CE(sat)}$ (lower than roughly 2 V), while an IGBT is on. However, an overcurrent condition brings the IGBT into a non-saturated state, causing V_{CE} to increase. V_{CE} exceeding a rated voltage is a faulty state. In the event of a faulty state, a gate-drive photocoupler slowly shuts down the V_{OUT} output.

** AMC (active Miller clamp):

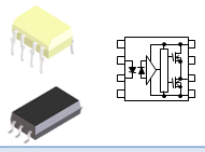
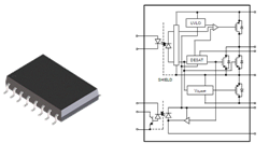
An active Miller clamp connects a gate of a driven power device (e.g., an IGBT) to V_{EE}, bypassing a gate resistor, when it is necessary to prevent an increase in gate-emitter voltage caused by gate-emitter Miller capacitance of the driven power device.

The TLP5214 and TLP5214A are smart gate-drive photocouplers (smart gate driver couplers) incorporating IGBT non-saturation detection, active Miller clamp, FAULT signal feedback, and other functions to protect an IGBT or a power MOSFET from destruction caused by an excessive current from an inverter or other circuit as well as from a malfunction due to noise.

For details of other features and functions of the TLP5214A, see its datasheet and application note.

To download the datasheet for the TLP5214A →
https://toshiba.semicon-storage.com/us/product/opto/photocoupler/detail.TLP5214A.html
To download the application note for the TLP5214A →
https://toshiba.semicon-storage.com/us/design-support/document/application-note.html

Table 1.2 Differences between general-purpose gate-drive photocouplers and TLP5214A/TLP5214

	General-purpose gate driver coupler	**Smart gate driver coupler**
Product name	TLP352, TLP5701, etc.	TLP5214, TLP5214A
Package / internal circuit diagram	DIP8, SO6L, etc. 	SO16L 
Pins	8 pin, 6 pin	16 pin
IGBT gate direct drive	✔	✔
UVLO function	✔	✔
$V_{CE(sat)}$ detection	-	✔
Active Miller clamp	-	✔
FAULT output	-	✔

The peak output current of a gate-drive photocoupler affects the gate charging and discharging times of the following power device and thus its turn-on and turn-off times. The turn-on and turn-off times of the power device should be optimally adjusted because they affect its switching losses and heat dissipation and determine the dead time required to prevent the cross conduction of high-side and low-side power devices in an inverter circuit. Therefore, the peak output current is an important factor in selecting a gate-drive photocoupler.

Figure 1.1 shows guidelines for combinations of Toshiba's gate-drive photocouplers and power IGBTs for typical inverter applications.

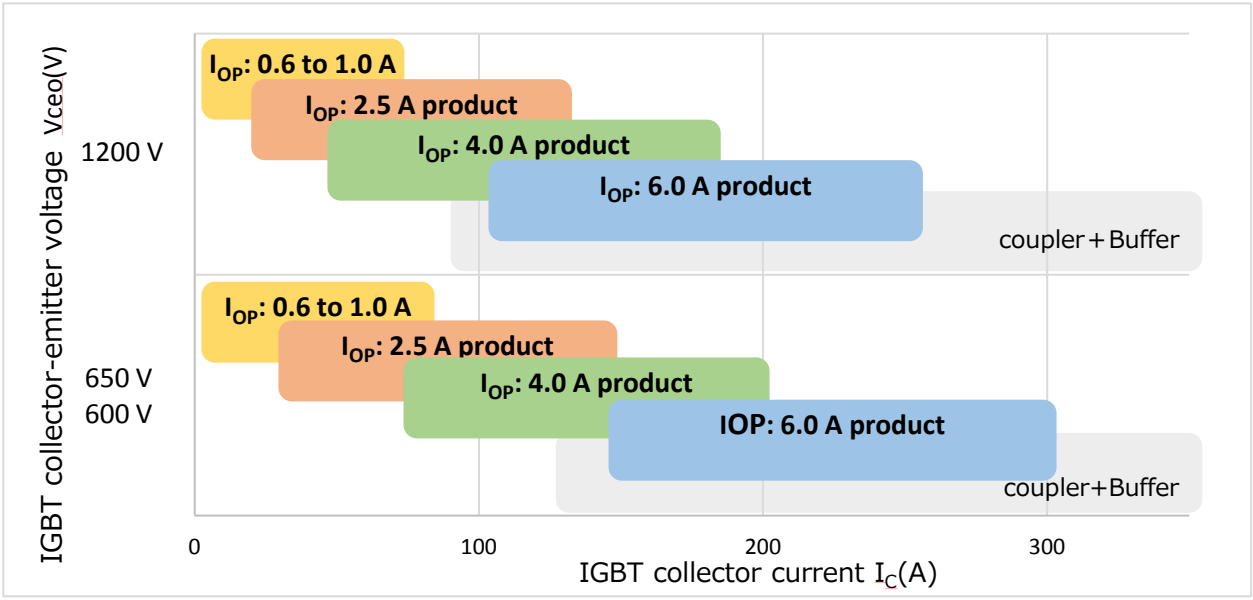


Figure 1.1 Guidelines for combinations of gate-drive photocouplers and power IGBTs

1.2 Major electrical characteristics

This subsection describes peak output current (I_{OP}), parameters related to propagation delays (propagation delay times (t_{pHL} and t_{pLH}), pulse width distortion ($|t_{pHL} - t_{pLH}|$), and propagation delay skew (t_{psk})), supply voltage (V_{CC}), undervoltage lockout (UVLO), and threshold input current (I_{FLH}).

1.2.1 Peak output current (I_{OP})

Peak output current is defined as the maximum permissible output current from a gate-drive photocoupler when it charges and discharges the gate capacitance of a power device.

Figure 1.2 shows the peak high-level output current (I_{OPH}) and peak low-level output current (I_{OPL}) of the TLP5751, which are ±1 A in the ambient temperature (T_a) range from -40 to 110°C.

	Characteristics		Symbol	Note	Rating	Unit
Detector	Peak high-level output current	(T_a = -40 to 110 °C)	I_{OPH}	(Note 2)	-1.0	A
	Peak low-level output current	(T_a = -40 to 110 °C)	I_{OPL}	(Note 2)	+1.0	

Note 2: Exponential waveform. Pulse width ≤ 2 μs, f ≤ 15 kHz

Figure 1.2 Electrical characteristics of the TLP5751 gate-drive photocoupler (excerpt from the datasheet)

The peak output currents (I_{OPH} and I_{OPL}) can be roughly calculated as follows:

$$I_{OPH} = \frac{V_{CC} + |V_{EE}|}{R_{on,H} + R_g + r_g}$$

$$I_{OPL} = \frac{V_{CC} + |V_{EE}|}{R_{on,L} + R_g + r_g}$$

Where:

V_{CC}: Output positive supply voltage V_{EE}: Output negative supply voltage (V_{EE} < 0)
R_g: External gate resistor value r_g: Internal gate resistor value of a power device
$R_{on,H}$: Photocoupler output resistance (high side)
$R_{on,L}$: Photocoupler output resistance (low side)

The on-resistances of the MOSFETs at the output stage of the gate-drive photocoupler ($R_{on,H}$ and $R_{on,L}$) can be estimated as follows:
First, suppose that $R_{on,H}$ and $R_{on,L}$ are 0 Ω to calculate the maximum peak output current ($I_{OP,worst}$):

$$I_{OP,worst} = \frac{V_{CC} + |V_{EE}|}{R_g + r_g}$$

Next, calculate $R_{on,H}$ and $R_{on,L}$ from the (V_{OH} - V_{CC}) - I_{OPH} and V_{OL} - I_{OPL} curves in the datasheet.

$$R_{on,H} = \frac{(V_{OH} - V_{CC})@I_{OP,worst}}{I_{OP,worst}}$$

$$R_{on,L} = \frac{V_{OL}@I_{OP,worst}}{I_{OP,worst}}$$

At this time, read the curve for an ambient temperature (T_a) higher than the temperature at which the gate-drive photocoupler application will be used.
Substitute the $R_{on,H}$ and $R_{on,L}$ values into the I_{OPH} and I_{OPL} equations to calculate peak output currents.

(1) Example of calculating peak output currents (I_{OP})

Figure 1.3 shows a model for calculating the peak output currents of the TLP5751. Let's calculate its peak output currents (I_{OPH} and I_{OPL}) based on the following circuit conditions and parameters:

Calculation conditions: V_{CC} = 15 V, V_{EE} = 0 V, C_g = 10 nF / 20 nF, R_g = 15 Ω,
r_g = 0 Ω, T_a = 85 °C

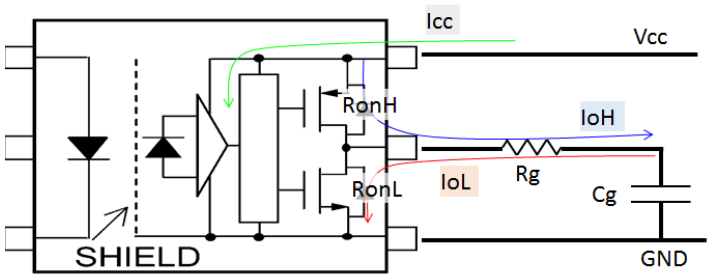


Figure 1.3 Model for calculating the peak output currents of the TLP5751: V_{CC} = 15 V, R_g = 15 Ω

1. Calculate $I_{OP,worst}$.

$$I_{OP,worst} = \frac{V_{CC} + |V_{EE}|}{R_g + r_g}$$

$$= \frac{15(\mathrm{V}) + |0(\mathrm{V})|}{15(\Omega) + 0(\Omega)}$$

$$= 1\ (\mathrm{A})$$

2. Estimate $R_{on,H}$ and $R_{on,L}$ based on $I_{OP,worst}$.

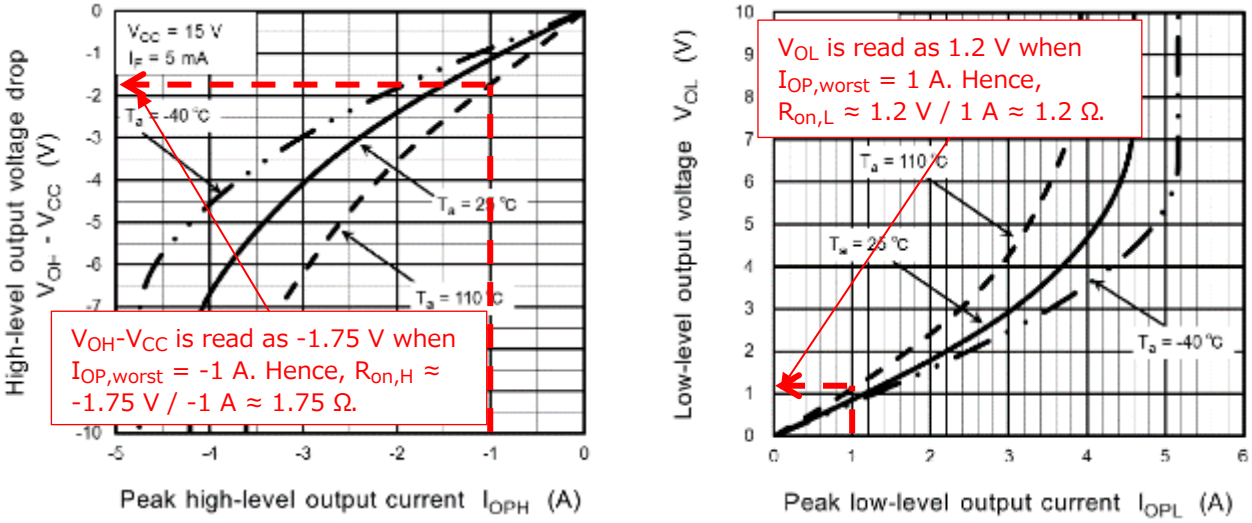


Figure 1.4 Calculating the $R_{on,H}$ and $R_{on,L}$ values of the TLP5751 gate-drive photocoupler (using (V_{OH} - V_{CC}) - I_{OPH} and V_{OL} - I_{OPL} curves)

3. Calculate I_{OPH} and I_{OPL}.

$$I_{OPH} = \frac{V_{CC} + |V_{EE}|}{R_{on,H} + R_g + r_g}$$

$$= \frac{15(\mathrm{V}) + |0(\mathrm{V})|}{1.75(\Omega) + 15(\Omega) + 0(\Omega)}$$

$$\approx 0.9\ (\mathrm{A})$$

$$I_{OPL} = \frac{V_{CC} + |V_{EE}|}{R_{on,L} + R_g + r_g}$$
$$= \frac{15(\mathrm{V}) + |0(\mathrm{V})|}{1.2(\Omega) + 15(\Omega) + 0(\Omega)}$$
$$\approx 0.93\ \mathrm{A}$$

This confirms that our application example works properly because the peak output currents (I_{OPH} and I_{OPL}) of the TLP5751 are ±1 A in the ambient temperature (T_a) range from -40 to 110 °C.

The I_{OPH} and I_{OPL} values of an actual circuit tend to be lower than the results of these calculations because of the circuit inductance, the gate capacitance of a power device, and other factors. Figure 1.5 shows the test circuit for the measurement of peak output currents of the TLP5751, and Figure 1.6 shows the measured output current waveforms. Perform an on-board evaluation to know peak output current characteristics in detail.

The peak output currents of a gate-drive photocoupler affect the gate charging and discharging times of the following power device, which determine its turn-on and turn-off times.

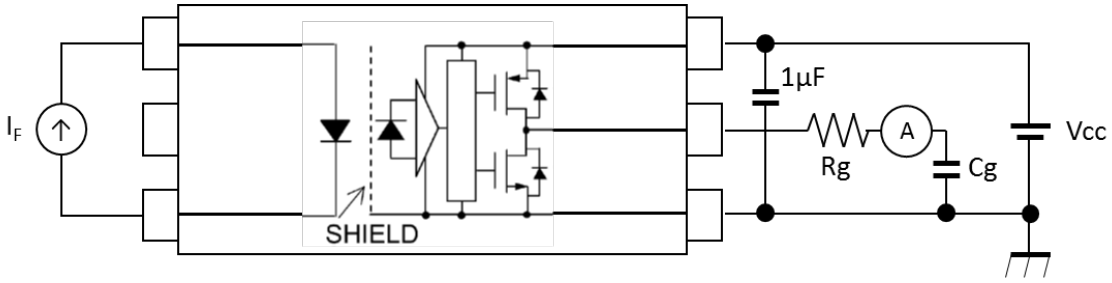
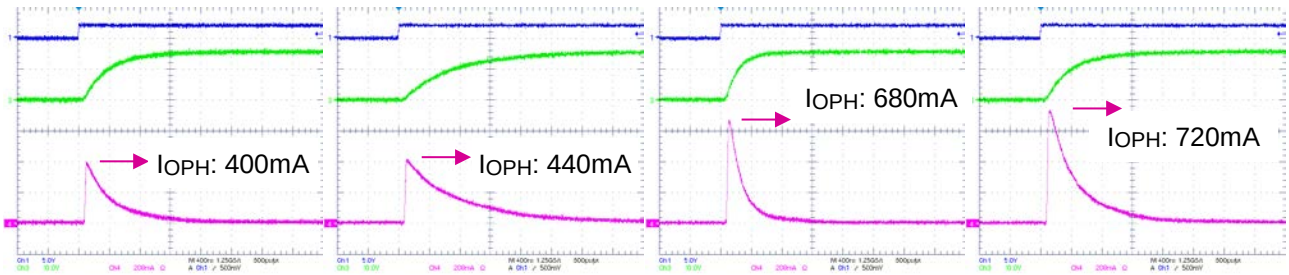


Figure 1.5 Test circuit for the peak output currents of the TLP5751



V_{CC}=15V, I_F=5mA	V_{CC}=15V, I_F=5mA	V_{CC}=15V, I_F=5mA	V_{CC}=15V, I_F=5mA
R_g=30Ω, C_g=10nF	R_g=30Ω, C_g=20nF	Rg=15Ω, Cg=10nF	Rg=15Ω, Cg=20nF

y axis upper I_F:10mA/div, middle V_O:10V/div, lower I_{OP}:200mA/div
x axis time 400ns/div

Figure 1.6 Measured peak output current (I_{OP}) waveforms of the TLP5751

1.2.2 Propagation delay times (t_{pHL} and t_{pLH}), pulse width distortion ($|t_{pHL} - t_{pLH}|$), propagation delay skew (t_{psk})

(1) Propagation delay times (t_{pHL} and t_{pLH})

Propagation delay times are defined as the time required from when the LED in a gate-drive photocoupler turns on or off to when V_O reaches 50% of V_{OH}.

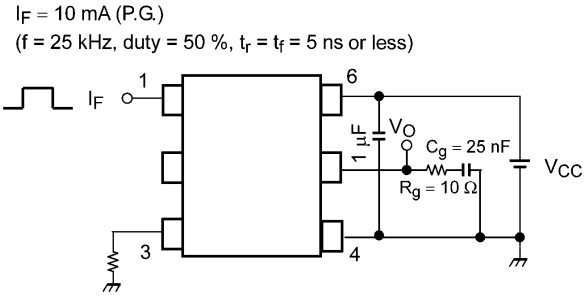


Figure 1.7 Example of a test circuit for propagation delay times

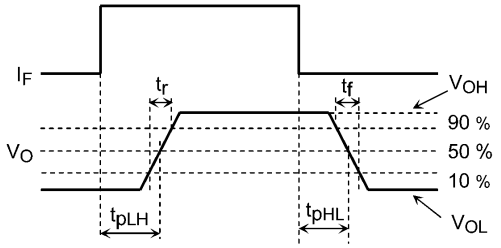


Figure 1.8 Example of the measurement points of propagation delay times

(2) Pulse width distortion ($|t_{pHL} - t_{pLH}|$)

Pulse width distortion is defined as the absolute value of the difference between low-to-high and high-to-low propagation delay times (t_{pHL} and t_{pLH}).

(3) Propagation delay skew (t_{psk})

Propagation delay skew is defined as a difference between the minimum and maximum propagation delay times (t_{pHL} or t_{pLH}) among multiple instances of a gate-drive photocoupler. The propagation delay times of multiple instances of a gate-drive photocoupler are measured under the same conditions (e.g., supply voltage, input current, and temperature) to determine t_{psk}.

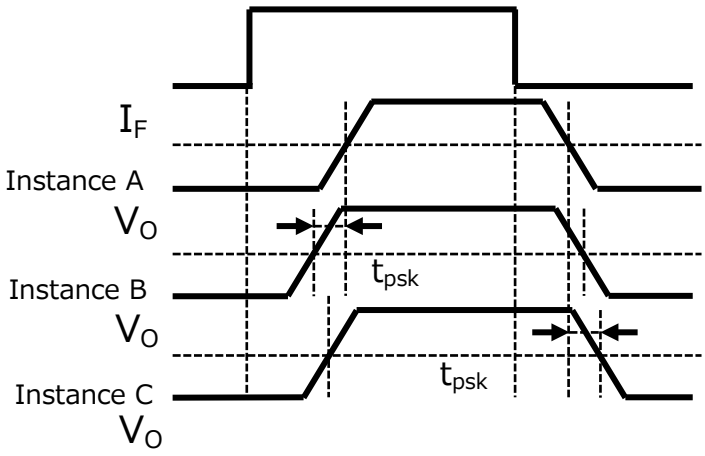


Figure 1.9 Measurement points of propagation delay skew

An inverter circuit is composed of multiple gate drivers in the upper and lower arms. When considering a short-circuit between the upper and lower arms, it is necessary to take

account of not only the propagation delay times and the variations of individual gate drivers but also differences in the propagation delay time among multiple gate drivers. The propagation delay skew parameter is used for this verification.

The propagation delay times shown in the datasheet of a gate-drive photocoupler are the results of measurement under prescribed conditions. Therefore, the propagation delay times of a gate-drive photocoupler driving a power device differ from the datasheet values. Be sure to measure propagation delay times in an actual application to determine dead-time and other requirements.

Figure 1.10 shows the t_{pHL}, t_{pLH}, $|t_{pHL} - t_{pLH}|$, and t_{psk} characteristics of the TLP5751.

(T_a = -40 to 110 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 13.1.7	I_F = 0 → 10 mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	50	—	150	ns
Propagation delay time (H/L)	t_{pHL}			I_F = 10 → 0 mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	50	—	150	
Pulse width distortion	$\|t_{pHL}-t_{pLH}\|$	(Note 1)		I_F = 0 ←→ 10 mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	—	—	50	
Propagation delay skew (device to device)	t_{psk}	(Note 1), (Note 2)			-80	—	80	

Note 1: Input signal (f = 25 kHz, duty = 50 %, t_r = t_f = 5 ns or less).
C_L is approximately 15 pF which includes probe and stray wiring capacitance.

Figure 1.10 Electrical characteristics of the TLP5751 gate-drive photocoupler (excerpt from the datasheet)

1.2.3 Supply voltage (V_{CC})

Supply voltage (V_{CC}) is defined as a voltage that can be applied across V_{CC} and GND.
Figure 1.11 shows the V_{CC} characteristics of the TLP5751.

(T_a = −40 to 110 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Supply voltage	V_{CC}			—	15	—	30	V

Figure 1.11 Electrical characteristics of the TLP5751 gate-drive photocoupler (excerpt from the datasheet)

If the supply voltage is lower than the lower V_{CC} limit shown in the Recommended Operating Conditions table, undervoltage lockout (UVLO) is tripped to shut down the output of a gate-drive photocoupler. If the supply voltage exceeds the upper V_{CC} limit, the device might be permanently damaged. Be sure to maintain the supply voltage in the specified range.

A voltage close or equal to V_{CC} appears at the V_O output of a gate-drive photocoupler, which becomes the gate voltage of a power device.

When the V_O output is off, the supply voltage can be set to a negative value in order to prevent a false turn-on of a power device. In that case, the sum of the positive and negative supply voltages must not exceed the rated supply voltage (V_{CC}).

To drive a power device with a low gate-source voltage (V_{GSS}), the supply voltage of the gate-drive photocoupler must be set to a low value accordingly. In such cases, select a low-V_{CC} (10 to 30 V) gate-drive photocoupler with a low UVLO threshold voltage (described in the next subsection).

1.2.4 Undervoltage lockout (UVLO)

At power-on, UVLO disables the V_O output of a gate-drive photocoupler via the internal circuit on the output side until its supply voltage reaches the ULVO recovery voltage (V_{UVLO+}). ULVO prevents a malfunction while the input voltage is rising.

When the supply voltage drops below the ULVO threshold voltage (V_{UVLO-}) during operation, ULVO is also tripped to prevent under-driven conditions of a power device. UVLO is disabled when the supply voltage rises back above the ULVO recovery voltage (V_{UVLO+}).

Note that the gate-drive photocoupler does not function if its supply voltage is set lower than V_{UVLO-}.

Figure 1.12 shows the UVLO characteristics of the TLP5751.

(T_a = −40 to 110 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
UVLO threshold voltage	V_{UVLO+}			I_F = 5 mA, V_O > 2.5 V	12.1	12.7	13.5	V
	V_{UVLO-}			I_F = 5 mA, V_O < 2.5 V	11.1	11.7	12.4	

Figure 1.12 Electrical characteristics of the TLP5751 gate-drive photocoupler (excerpt from the datasheet)

Please note that if a gate-drive photocoupler is driven by positive and negative power supply, it is necessary to consider that the UVLO threshold is offset by the negateive voltage.

1.2.5 Threshold input current (I_{FLH})

Gate-drive photocouplers with an amplifier circuit logically toggle its output when the input current (I_F) exceeds a certain value. This value is called the threshold input current and denoted by the symbol I_{FLH}. The characters “LH” in I_{FLH} indicate the direction of a change in voltage that occurs in response to an LED input current. Because the output of the gate-drive photocoupler makes a low-to-high transition in response to an LED input current, its threshold input current is denoted by I_{FLH}. For most gate-drive photocouplers, the threshold input current is guaranteed over the operating ambient temperature range (T_a) from -40 to 110˚C, as is the case with the TLP5751.

Figure 1.13 shows the threshold input current characteristics of the TLP5751.

(T_a = −40 to 110 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Threshold input current (L/H)	I_{FLH}			V_{CC} = 15 V, V_O > 1 V	—	1.4	4	mA

Figure 1.13 Electrical characteristics of the TLP5751 gate-drive photocoupler (excerpt from the datasheet)

In the case of the TLP5751, the maximum I_{FLH} value is specified as 4 mA. Although I_{FLH} varies from one device to another and with temperature, this means I_{FLH} never exceeds 4 mA at the maximum. So, setting I_F must be at least 4 mA for applications.

2. Examples of an application circuit for a gate-drive photocoupler and power loss calculation

Gate-drive photocouplers are commonly used to drive power devices in an inverter circuit for motor drive applications while providing electrical insulation. Because gate-drive photocouplers precede power devices, they are often located in a high-temperature environment. In addition, gate-drive photocouplers require lots of power to drive the gates of power devices. It is therefore essential to calculate the power losses of gate-drive photocouplers to determine whether they are suitable for a given application. This section describes how to calculate the power losses of gate-drive photocouplers using an example.

2.1 Example of an application circuit for IGBT/MOSFET gate-drive photocouplers

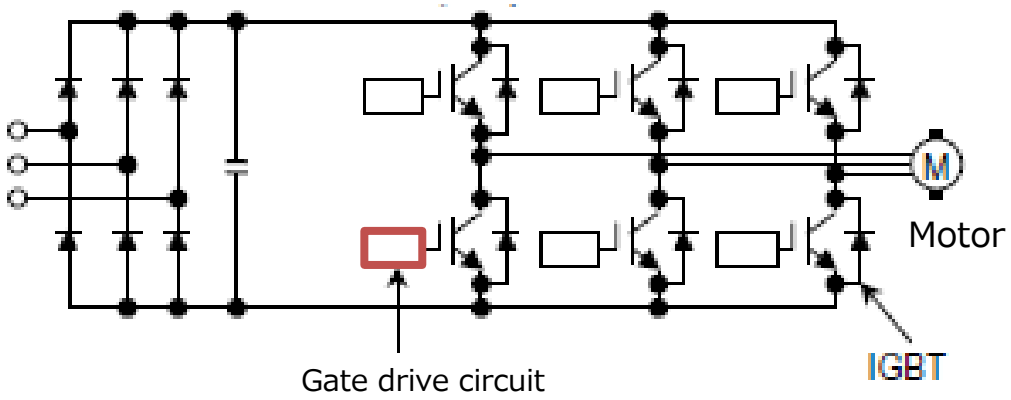


Figure 2.1(a) Example of an inverter circuit using gate-drive photocouplers

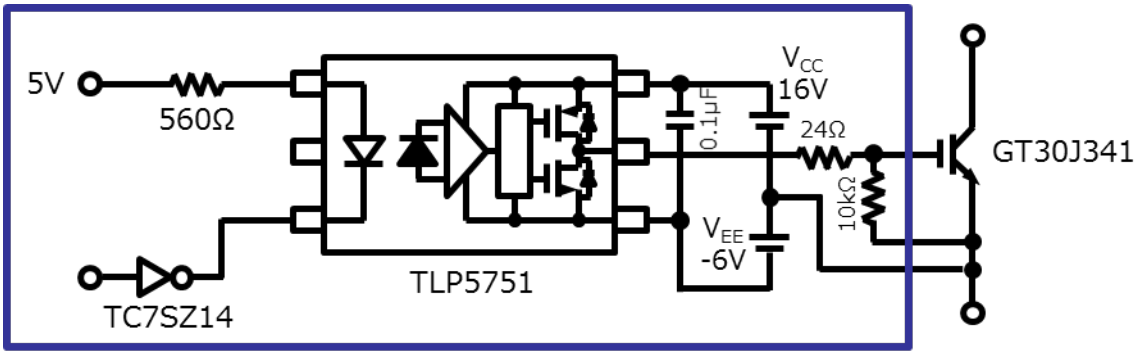


Figure 2.1(b) Example of component values in the gate drive circuit using the TLP5751

The following paragraphs describe the reasons why the component values shown in Figure 2.1(b) were selected.

Input forward current (I_F): ≈ 6 mA. The maximum threshold input current of the TLP5751 is 4 mA. The input forward current of 6 mA includes a margin to allow for LED degradation due to aging.

V_{cc}: 16 V. Based on the collector-emitter saturation voltage specification of the GT30J341

V_{EE}: -6 V. Selected so that the sum of V_{CC} and V_{EE} does not exceed the rated gate-emitter voltage of the IGBT

Gate resistor (R_g): 24 Ω. The resistor value given as a test condition for the switching time of the GT30J341 was selected so that (V_{CC} + $|V_{EE}|$) / R_g will not exceed the I_{OP} of the TLP5751.

2.2 Calculating the power losses of a gate-drive photocoupler

This subsection describes how to calculate the power losses of a gate-drive photocoupler.

To charge and discharge the gate capacitance of an IGBT or other power device in a short period of time, the output of a gate-drive photocoupler needs to sink and source a large current rapidly. It is therefore necessary to take the switching losses and heat dissipation of the photocoupler into consideration. The switching losses are determined by the operating frequency and drive voltage of the photocoupler as well as the gate capacitance and resistance of the power device. When designing neighboring circuits, care should be exercised to ensure that the permissible power dissipation values of the LED and photodetector chips in the gate-drive photocoupler will not be exceeded.

The following table defines the symbols used in this subsection.

Symbol	Characteristics	Symbol	Characteristics
P_{in}	Power dissipated in the input LED	P_o	Power dissipated in the output
Duty	Duty ratio of the photocoupler operation		
I_F	LED forward current	V_F	LED forward voltage
$P_{O(bias)}$	DC power dissipated when the output is in DC operation		
$P_{O(bias:on)}$	DC power dissipated in the output when the LED is active	$P_{O(bias:off)}$	DC power dissipated in the output when the LED is off
$P_{O(swg)}$	Power dissipated in the output when a following power device is switching		
$P_{O(swg:H)}$	Power dissipated in the output when a following power device switches to on	$P_{O(swg:L)}$	Power dissipated in the output when a following power device switches to off
I_{CCH}	High-level supply current	I_{CCL}	Low-level supply current
E_{sw}	Electrostatic energy in the gate of a following power device charged and discharged per switching transition		
f_{sw}	Switching frequency		
R_g	External gate resistor value	r_g	Internal gate resistance of a power device

$R_{on,H}$	Output resistance of a photocoupler (high side)	$R_{on,L}$	Output resistance of a photocoupler (low side)
Q_g	Amount of gate charge of a power device		
$I_{OP,worst}$	Maximum peak output current		
$T_{j,LED}$	Junction temperature of the LED chip	$T_{j,Photo}$	Junction temperature of the photodetector chip
$R_{th(j-a),LED}$	Thermal resistance of the LED chip	$R_{th(j-a),Photo}$	Thermal resistance of the photodetector chip

2.2.1 Calculating power losses

(1) Input power dissipation: P_{in}

$$P_{in} = Duty \times I_F \times V_F$$

(2) Output power dissipation: Po

$$P_O = P_{O(bias)} + P_{O(swg)}$$

The following shows how to calculate $P_{O(bias)}$ and $P_{O(swg)}$.

1. Power supply dissipation: $P_{O(bias)}$

$$P_{O(bias)} = P_{O(bias:on)} + P_{O(bias:off)}$$
$$= Duty \times I_{CCH} \times (V_{CC} + |V_{EE}|) + (1 - Duty) \times I_{CCL} \times (V_{CC} + |V_{EE}|)$$

2. Switching loss: $P_{O(swg)}$

   E_{sw}, i.e., the amount of energy charged into or discharged from the gate capacitance of a power device per switching transition is calculated as follows:

$$E_{sw} = \frac{1}{2} \times C_g \times V^2 = \frac{1}{2} \times Q_g \times (V_{CC} + |V_{EE}|)$$

   E_{sw} is dissipated f_{sw} times per second by $R_{on,H}$ and $R_{on,L}$ connected in series as well as R_g, and r_g. Of the sum of the power dissipated by these devices, the switching loss, $P_{O(swg)}$, of the gate-drive photocoupler can be calculated as follows:

$$P_{O(swg)} = E_{SW} \times \left(\frac{R_{on,H}}{R_g + R_{on,H}} + \frac{R_{on,L}}{R_g + R_{on,L}} \right) \times f_{sw}$$
$$= \frac{1}{2} \times Q_g \times (V_{CC} + |V_{EE}|) \times \left(\frac{R_{on,H}}{R_g + R_{on,H}} + \frac{R_{on,L}}{R_g + R_{on,L}} \right) \times f_{sw}$$

Here, the gate charge (Q_g) of the power device is determined as follows:
Read the Q_g values of the power device at V_{CC} and V_{EE} and calculate their sum.

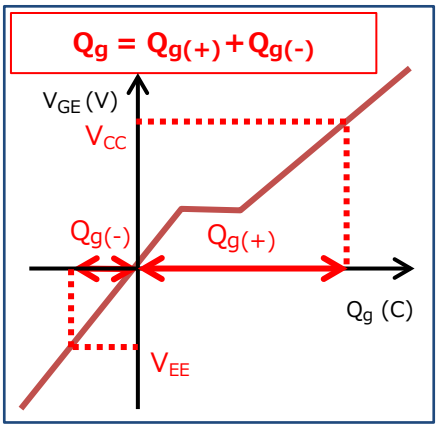


Figure 2.2 Example of the V_{GE} - Q_g curve of a power device following the gate-drive photocoupler

2.2.2 Calculation example

Let's calculate the power loss of the gate-drive photocoupler based on the circuit conditions and parameters shown in the gate drive circuit of Figure 2.1(b).

Calculation conditions:

V_{CC} = 16 V, V_{EE} = -6 V,
I_{CCH} = 3 mA, I_{CCL} = 3 mA (maximum rated value of the TLP5751),
Q_g = 150 nC, R_g = 24 Ω, r_g = 0 Ω, Duty ratio = 0.5, f_{sw} = 15 kHz, T_a = 85 °C
I_F = 6 mA, V_F = 1.4 V (voltage read from the TLP5751 I_F - V_F curve at T_a = 110 °C and I_F = 6 mA)

(1) Input power dissipation: P_{in}

$$P_{in} = Duty \times I_F \times V_F$$
$$= 0.5 \times 6(mA) \times 1.4(V) = 4.2\ (mW)$$

This confirms that the gate drive circuit shown in Figure 2.1(b) is satisfactory because the input power dissipation (P_D) of the TLP5751 is rated at 400 mW at a Ta of 85 °C.

(2) Output power dissipation: P_o

$$P_O = P_{O(bias)} + P_{O(swg)}$$

1. Power supply dissipation: $P_{O(bias)}$

$$P_{O(bias)} = P_{O(bias:on)} + P_{O(bias:off)}$$
$$= Duty \times I_{CCH} \times (V_{CC} + |V_{EE}|)$$
$$+ (1 - Duty) \times I_{CCL} \times (V_{CC} + |V_{EE}|)$$
$$= 0.5 \times 3(mA) \times 22(V) + (1 - 0.5) \times 3(mA) \times 22(V)$$
$$= 66\ (mW)$$

2. Switching loss: $P_{O(swg)}$

Estimate the on-resistance of the gate-drive photocoupler output stage based on the maximum peak output current.

First, calculate the maximum peak output current, $I_{OP,worst}$:

$$I_{OP,worst} = \frac{V_{CC} + |V_{EE}|}{R_g + r_g}$$

$$= \frac{16(\mathrm{V}) + |-6(\mathrm{V})|}{24(\Omega) + 0(\Omega)}$$

$$\approx 0.92\ (A)$$

To obtain $(V_{OH} - V_{CC})@I_{OP,worst}$ and $V_{OL}@I_{OP,worst}$, read the $(V_{OH} - V_{CC}) - I_{OPH}$ and $V_{OL} - I_{OPL}$ curves shown in Figure 2.3 at 0.92 A. They are read as -1.6 V and 1.0 V, respectively.

Hence, on-resistance of the gate driver photocoupler output stage ($R_{on,H}$ and $R_{on,L}$) are calculated as follows:

$$R_{on,H} = \frac{(V_{OH} - V_{CC})@I_{OP,worst}}{I_{OP,worst}}$$

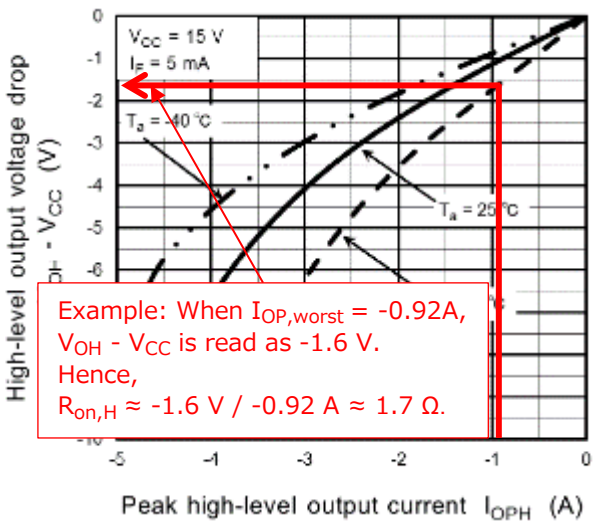
$$= \frac{-1.6(\mathrm{V})}{-0.92(\mathrm{A})}$$

$$\approx 1.7\ (\Omega)$$

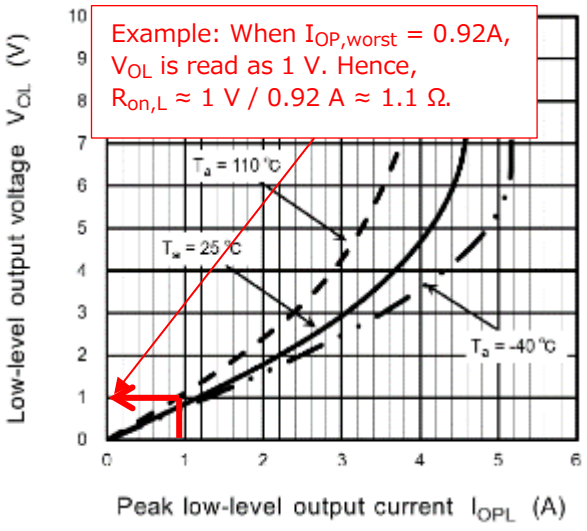
$$R_{on,L} = \frac{V_{OL}@I_{OP,worst}}{I_{OP,worst}}$$

$$= \frac{1.0(\mathrm{V})}{0.92(\mathrm{A})}$$

$$\approx 1.1\ (\Omega)$$



(a) TLP5751 $(V_{OH} - V_{CC}) - I_{OPH}$



(b) TLP5751 $V_{OL} - I_{OPL}$

Figure 2.3 Estimating the $R_{on,H}$ and $R_{on,L}$ values of the gate-drive photocoupler

Next, substitute the $R_{on,H}$ and $R_{on,L}$ values into the following equation:

$$P_{O(swg)} = E_{sw} \times \left(\frac{R_{on,H}}{R_g + R_{on,H}} + \frac{R_{on,L}}{R_g + R_{on,L}} \right) \times f_{sw}$$

$$= \frac{1}{2} \times Q_g \times (V_{CC} + |V_{EE}|) \times \left(\frac{R_{on,H}}{R_g + R_{on,H}} + \frac{R_{on,L}}{R_g + R_{on,L}} \right) \times f_{sw}$$

$$= \frac{1}{2} \times 150(\mathrm{nC}) \times 22(\mathrm{V}) \times \left(\frac{1.7(\Omega)}{24(\Omega) + 1.7(\Omega)} + \frac{1.1(\Omega)}{24(\Omega) + 1.1(\Omega)} \right) \times 15(\mathrm{kHz})$$

$$= 2.7\ (mW)$$

Hence, the output power dissipation is:

$$P_O = P_{O(bias)} + P_{O(swg)}$$

$$= 66\ (mW)\ +\ 2.7\ (mW)\ =\ 68.7\ (mW)$$

This confirms that the gate drive circuit shown in Figure 2.1(b) is satisfactory because the output power dissipation (P_O) of the TLP5751 is rated at 450 mW at a T_a of up to 85 °C.

3. Terms

(General terms)

Term	Symbol	Description
Absolute Maximum Ratings		Maximum value that must not be exceeded even for an instant during operation
Isolation Voltage	BV_S	Isolating voltage between input and output under the specified conditions
Capacitance (Input to Output), Total Capacitance (Input to Output)	C_S	Electrostatic capacitance between the input and output pins
Capacitance (Input), Input Capacitance	C_T C_t	Electrostatic capacitance between the anode and cathode pins of the LED
Forward Current, Input Forward Current	I_F	Rated current that can flow continuously in the forward direction of the LED
Pulse Forward Current, Input Forward Current (Pulsed)	I_{FP}	Rated current that can flow momentarily in the forward direction of the LED
Transient Forward Current, Peak Transient Forward Current	I_{FPT}	Rated current that can flow momentarily in the forward direction of the LED
Reverse Voltage, Input Reverse Voltage	V_R	Rated reverse voltage that can be applied across the LED's cathode and anode
Reverse Current, Input Reverse Current	I_R	Leakage current flowing in the reverse direction of the LED (from cathode to anode)
Forward Voltage, Input Forward Voltage	V_F	Voltage drop across the anode and cathode pins of the LED under the specified forward-current condition
LED Power Dissipation, Input Power Dissipation	P_D	Rated power that can be dissipated in the LED
Total Power Dissipation	P_T	Total rated power that can be dissipated in both the input and output devices
Isolation Resistance	R_S	Resistance between the input and output pins at the specified voltage
Junction Temperature	T_j	Permissible temperature of the junction of the photodetector or LED
Operating Temperature	T_{opr}	Ambient temperature range in which the device can operate without loss of functionality
Lead Soldering Temperature	T_{sol}	Rated temperature at which the device pins can be soldered without loss of functionality
Storage Temperature	T_{stg}	Ambient temperature range in which the device can be stored without operation
Creepage Distance		Shortest distance along the surface of insulation between the path of two conductive parts (input and output)
Clearance (Clearance Distance)		Shortest distance through air between the path of two conductive parts (input and output)
Internal Isolation Thickness, Insulation Thickness		Distance through insulation. Shortest thickness through internal insulation between the path of two conductive parts (input and output)

(Transistor output)

Term	Symbol	Description
Collector Current	I_C	Rated current allowed to flow to collector
Current Transfer Ratio	I_C/I_F (CTR)	Ratio of output current, I_C, to input current, I_F: $I_C/I_F \times 100$ (unit: %)
Collector Dark Current, Dark Current	I_{CEO} I_{DARK}	Leakage current flowing between collector and emitter
Off-State Collector Current	$I_{C(off)}$	Leakage current flowing between collector and emitter when Low voltage is applied to input
Current Gain Factor	h_{FE}	h_{FE} for phototransistor
Base Photo-Current	I_{PB}	Photo-current generated by the specified input current, I_F, in the phototransistor base block
Collector Power Dissipation	P_C	Rated power that can be dissipated in collector
Turn-On Time	t_{ON} t_{on}	Time required for the output waveform to change from 100% (0%) to 10% (90%) when the input is turned off and back on under the specified conditions
Turn-Off time	t_{OFF} t_{off}	Time required for the output waveform to change from 0% (100%) to 90% (10%) when the input is turned on and back off under the specified conditions
Storage Time	t_S	Time required for the output waveform to change from 0% (100%) to 10% (90%) when input is turned on and back off under the specified conditions
Fall Time	t_f	Time required for the output waveform to change from 90% to 10%
Rise Time	t_r	Time required for the output waveform to change from 10% to 90%
Collector-Emitter Saturation Voltage	$V_{CE\ (sat)}$	Voltage between collector and emitter under the specified saturation conditions
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	Breakdown voltage between collector and base when emitter is open
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	Breakdown voltage between collector and emitter (when base is open)
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	Breakdown voltage between emitter and base when collector is open
Emitter-Collector Breakdown Voltage	$V_{(BR)ECO}$	Breakdown voltage between emitter and collector (when base is open)
Collector-Base Voltage	V_{CBO}	Rated voltage that can be applied across collector and base
Collector-Emitter Voltage	V_{CEO}	Rated voltage that can be applied across collector and emitter
Emitter-Base Voltage	V_{EBO}	Rated voltage that can be applied across emitter and base
Emitter-Collector Voltage	V_{ECO}	Rated voltage which can be applied across emitter and collector
Capacitance (Collector to Emitter), Collector-Emitter Capacitance	C_{CE}	Electrostatic capacitance between the collector and emitter pins

(IC output)

Term	Symbol	Description
Common-Mode Transient Immunity at Output High	CM_H	Maximum tolerable rate of rise (fall) of input/output common-mode voltage at which the specified High level can be maintained
Common-Mode Transient Immunity at Output Low	CM_L	Maximum tolerable rate of rise (fall) of input/output common-mode voltage at which the specified Low level can be maintained
High-Level Supply Current	I_{CCH} I_{DDH}	Current supply to the circuit that flows to power supply pins when the output is at the High level
Low-Level Supply Current	I_{CCL} I_{DDL}	Current supply to the circuit that flows to power supply pins when the output is at the Low level
Threshold Input Current	I_{FHL} (I_{FLH})	Minimum input current, I_F, necessary to change the output from High (Low) to Low (High) (*1)
Input Current Hysteresis	I_{HYS}	Difference between I_{FLH} and I_{FHL} for a given device
Threshold Input Voltage	V_{FLH} (V_{FHL})	Maximum input voltage, V_F, necessary to hold the initial output High (Low), or to return the output from Low (High) to High (Low) after the initial output changes from High (Low) to Low (High)
Current Transfer Ratio	I_O/I_F	Ratio of output current, I_O, to input current, I_F: $I_O/I_F \times 100$ (unit: %)
High-Level Output Current	I_{OH}	Output current under the specified High-level output voltage
Peak High-Level Output Current	I_{OPH}	Peak output current under the specified High-level output voltage
Low-Level Output Current	I_{OL}	Output current under the specified Low-level output voltage
Peak Low-Level Output Current	I_{OPL}	Peak output current under the specified Low-level output voltage
High-Level Short-Circuit Output Current	I_{OSH}	Output current under the specified High-level output and short-circuit conditions
Low-Level Short-Circuit Output Current	I_{OSL}	Output current under the specified Low-level output and short-circuit conditions
High-Level Output Voltage	V_{OH}	Output voltage under the specified High-level output current condition
Low-Level Output Voltage	V_{OL}	Output voltage under the specified Low-level output current condition
Output Power Dissipation	P_O	Rated power that can be dissipated in the output stage
Propagation Delay Time (H → L)	t_{pHL}	Time required from when the input changes from the OFF (ON) state to the ON (OFF) state to when the output waveform changes from the High level to specified Low level
Propagation Delay Time (L → H)	t_{pLH}	Time required from when the input changes from the ON (OFF) state to the OFF (ON) state to when the output waveform changes from the Low level to the specified High level
Output Current	I_O	Rated current that can flow to output pins
Peak Output Current	I_{OP}	Rated peak current that can be applied between output pins
Supply Voltage	V_{CC} V_{DD}	Rated voltage that can be applied to power supply pins
Output Voltage	V_O	Rated voltage that can be applied to output pins
UVLO Threshold Voltage	V_{UVLO}	Threshold voltage at which the undervoltage lockout (UVLO) function is tripped
Three-State Enable Voltage	V_E	Rated voltage that can be applied to the enable pin
High-Level Enable Voltage	V_{EH}	Voltage at which the enable pin functions as the High level
Low-Level Enable Voltage	V_{EL}	Voltage at which the enable pin functions as the Low level

(*1) I_F greater than the maximum I_{FHL} (I_{FLH}) is required to ensure that the IC output photocouplers from High (Low) to Low (High)

Revision History

Revision	Date	Page	Description
Rev. 1.0	2019-06-01	-	First edition

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