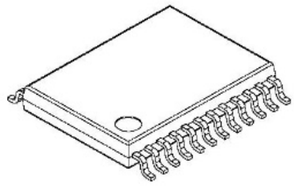
Toshiba Bi-CMOS integrated circuit silicon monolithic

TB9062FNG

1. Outline

TB9062FNG is an automotive 3 phase brushless sensorless motor control IC. 3 phase BLDC motor control logic circuit for 120 degrees square wave operation is built-in. External FETs are supposed Pch/Nch.



SSOP24-P-300-0.65A

2. Usage

Automotive 3 phase brushless sensorless motor control IC witch built-in 3 phase BLDC motor control logic circuit.

3. Feature

- 120 degrees square wave drive sensorless operation
- Motor speed is controlled by external PWM input signal
- Pre-driver for external Pch/Nch MOSFET (3 phase drive by 6 pre-driver output signal)
- Selectable lead angle setting
- Built-in 8bit ADC to detect over/under operating voltage
- Built-in 1ch comparator to detect EMF zero cross point for motor position detection
- Automated start duty control to maintain start up torque
- Abnormal detections (motor over-current, over voltage, under voltage, IC over temperature)
- Built-in internal 4 MHz OSC (at external R=39kΩ)
- Built-in 5V regulator with power on reset function
- Operating temperature : -40 to 125℃
- Small flat package SSOP-24pin (0.65 mm pitch)

Start of commercial production
2019-12

4. IC block diagram

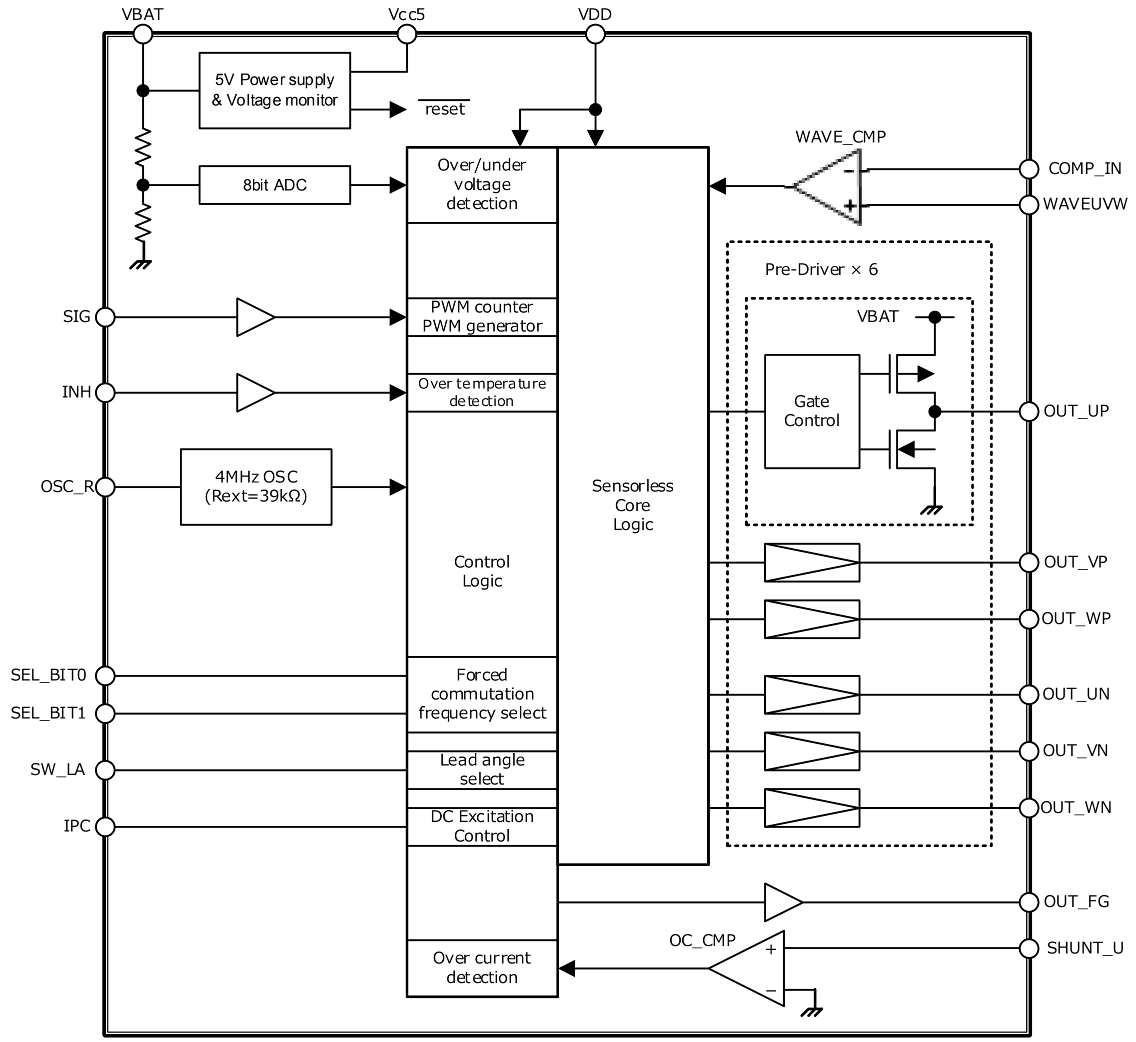


Fig. 4.1 Block diagram

【Caution】
Some of the functional circuit block, or constants in the block diagram may be omitted or simplified for brevity.

5. Pin layout

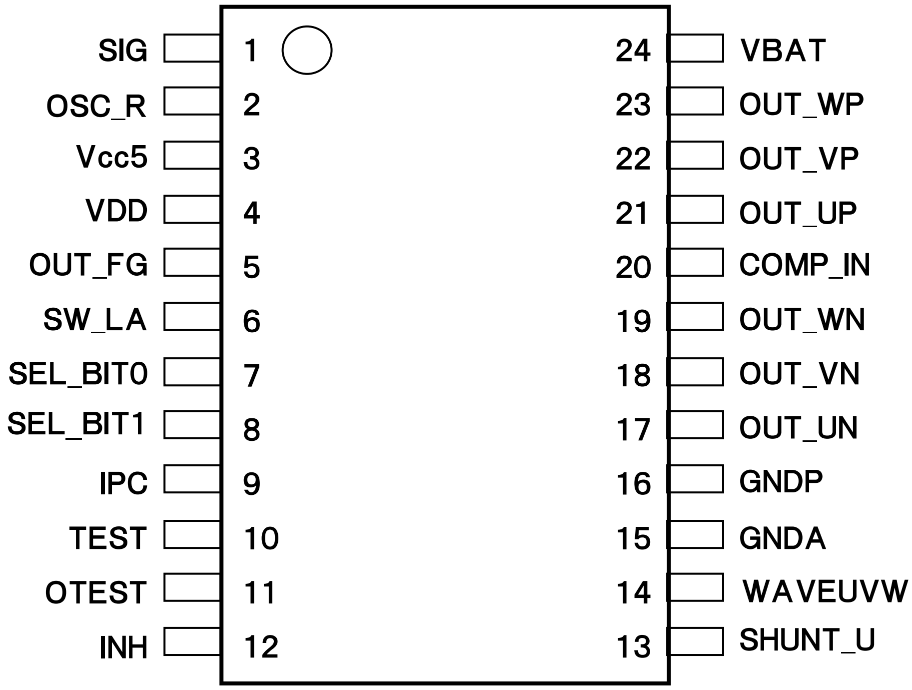


Fig. 5.1 Pin layout

6. Pin description

Table 6.1 Pin description

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th><th>IN/
OUT</th><th>I/O
voltage</th><th>Notes</th></tr>
<tr><td>1</td><td>SIG</td><td>External PWM input pin
”H” active</td><td>IN</td><td>VBAT</td><td>100kΩ
Pull down</td></tr>
<tr><td>2</td><td>OSC_R</td><td>Internal OSC frequency setting by Rext.
fosc=4MHz at Rext=39.0kΩ</td><td>OUT</td><td>5V</td><td>-</td></tr>
<tr><td>3</td><td>Vcc5</td><td>Internal 5Vreg. output
(current capacity 10mA(max))</td><td>OUT</td><td>5V</td><td>-</td></tr>
<tr><td>4</td><td>VDD</td><td>Input of internal logic power supply (5V typ.)</td><td>IN</td><td>5V</td><td>-</td></tr>
<tr><td>5</td><td>OUT_FG</td><td>Sensorless operation monitoring output</td><td>OUT</td><td>5V</td><td>-</td></tr>
<tr><td>6</td><td>SW_LA</td><td>Lead angle setting input
・SW_LA=L：Lead angle 7.5°
・SW_LA=H：Lead angle 15°</td><td>IN</td><td>5V</td><td>100kΩ
Pull down</td></tr>
<tr><td>7</td><td>SEL_BIT0</td><td rowspan="2">Forced commutation frequency setting input<table><tr><th>SEL_BIT0</th><th>SEL_BIT1</th><th>FC (rpm)</th></tr><tr><td>L(open)</td><td>L(open)</td><td>600</td></tr><tr><td>L(open)</td><td>H</td><td>2400</td></tr><tr><td>H</td><td>L(open)</td><td>1200</td></tr><tr><td>H</td><td>H</td><td>300</td></tr></table></td><td>IN</td><td>5V</td><td>100kΩ
Pull down</td></tr>
<tr><td>8</td><td>SEL_BIT1</td><td>IN</td><td>5V</td><td>100kΩ
Pull down</td></tr>
<tr><td>9</td><td>IPC</td><td>DC excitation time length setting input.
External cap. set on “IPC”
TIP [ms] = 400×CIP [μF]</td><td>IN</td><td>5V</td><td>10μA
Pull up</td></tr>
</table>

Pin	Name	Description	IN/ OUT	I/O voltage	Notes
10	TEST	Test pin (short to GND on PCB)	IN	5V	10kΩ Pull down
11	OTEST	Test pin (short to GND on PCB)	OUT	5V	-
12	INH	Pre-driver output enable ・INH=H：pre-driver OFF(Hi-Z) ・INH=L：normal operation	IN	5V	100kΩ Pull down
13	SHUNT_U	External shunt R connection pin for motor over current detection	IN	5V	-
14	WAVEUVW	Motor EMF zero cross detection pin for motor position detection	IN	VBAT	-
15	GNDA	Ground pin for small signal line	-	-	-
16	GNDP	Ground pin for power line	-	-	-
17	OUT_UN	Output for U phase Nch MOSFET	OUT	VBAT	-
18	OUT_VN	Output for V phase Nch MOSFET	OUT	VBAT	-
19	OUT_WN	Output for W phase Nch MOSFET	OUT	VBAT	-
20	COMP_IN	Ref. voltage input for detecting motor EMF zero cross detection	IN	VBAT	-
21	OUT_UP	Output for U phase Pch MOSFET	OUT	VBAT	-
22	OUT_VP	Output for V phase Pch MOSFET	OUT	VBAT	-
23	OUT_WP	Output for W phase Pch MOSFET	OUT	VBAT	-
24	VBAT	Battery power supply	IN	VBAT	-

【Caution】

*1：Improper pin connection may cause faults in motor protection, unstable operation or to stop altogether.

*2：Adjacent pin short may cause damage to the IC or entire system.

*3：Improper mounting may cause damage to the IC or entire system.

7. Function

7.1. Summery

TB9062FNG controls 3 phase BLDC motor by PWM duty based on input PWM signal.
The input PWM signal requirement is as below.

【Input PWM signal】
・Frequency : 5Hz to 1.2kHz
・PWM duty : 0% to 100%
・Voltage: 0V to VBAT

The TB9062FNG generates 17kHz PWM output signal (@ 4MHz OSC frequency) based on input PWM signal by its on-chip logic.

【Output PWM signal】
・Frequency : 17kHz (at 4MHz Internal OSC)
・PWM duty : Compensated duty of input PWM (ref. 7.4.1)
・Voltage: 0V to VBAT

TB9062FNG may not operate properly if the input PWM signal is out of this range.

7.2. Sensorless operation

When TB9062FNG detect 2nd rising edge of input PWM signal, internal counter is started to count the input PWM frequency and duty. Input PWM duty is compensated based on (7.3.3 input compensation circuit). When those frequency and PWM duty with the compensation is within spec., sensorless start up sequence is initiated. Sensorless start up sequence is firstly performed by DC excitation to set fixed position of the motor during the setting time period and after that setting time up, forced commutation is started by setting frequency. During forced commutation, if the motor position is detected by zero crossing, TB9062FNG sensorless operation shall commence.

7.2.1. Start up sequence setting and sensorless operation

The sensorless operation mode of TB9062FNG and start up sequence setting is as follows.

Fig. 7.2.1 Operation mode and start up setting

<table>
<tr><td>Operation mode</td><td colspan="3">120 degrees Square Operation</td></tr>
<tr><td>CW/CCW</td><td colspan="3">One direction (CW)</td></tr>
<tr><td>PWM</td><td colspan="3">Upper PWM operation</td></tr>
<tr><td rowspan="6">Start up sequence setting</td><td rowspan="2">Lead angle</td><td>7.5 °</td><td>Pin” SW_LA”= “L”</td></tr>
<tr><td>15 °</td><td>Pin “SW_LA”= “H”</td></tr>
<tr><td rowspan="4">Forced commutation frequency (electrical angle)</td><td>600 rpm</td><td>Pin “SEL_BIT0” = “L”, pin “SEL_BIT1”= “L”</td></tr>
<tr><td>2400 rpm</td><td>Pin “SEL_BIT0” = “L”, pin “SEL_BIT1”= “H”</td></tr>
<tr><td>1200 rpm</td><td>Pin “SEL_BIT0” = “H”, pin “SEL_BIT1”= “L”</td></tr>
<tr><td>300 rpm</td><td>Pin “SEL_BIT0” = “H”. pin “SEL_BIT1”= “H”</td></tr>
</table>

(Note) Each pin “SW_LA”, “SEL_BIT0”, “SEL_BIT1” has built-in pull down resistor. Thus, in the case of each pin open, the setting is the same as the above setting “L”. Regardless, connection to “L” is recommended.

- Setting lead angle is performed after starting sensorless operation. During DC excitation and force commutation of start up sequence, lead angle is fixed at 0 °.
- We recommend sufficient input PWM signal duty level to prevent motor phase-out. The minimum duty shall be determined by specific motor and its load on the system.
- TB9062FNG cannot keep proper sensorless commutation with lower motor rotation speed than setting forced commutation frequency. In that case, TB9062FNG perform next commutation without zero cross detection and motor rotation speed shall become unstable.
- Sensorless start up sequence initiate by DC excitation to set fixed position of the motor during the setting time period and after that setting time is up, forced commutation is started by setting frequency. During forced commutation, zero cross point is determined by motor position detected by motor EMF (electromotive force), then TB9062FNG sensorless operation shall commence. Refer to fig. 7.2.1 for the timing chart of operation.

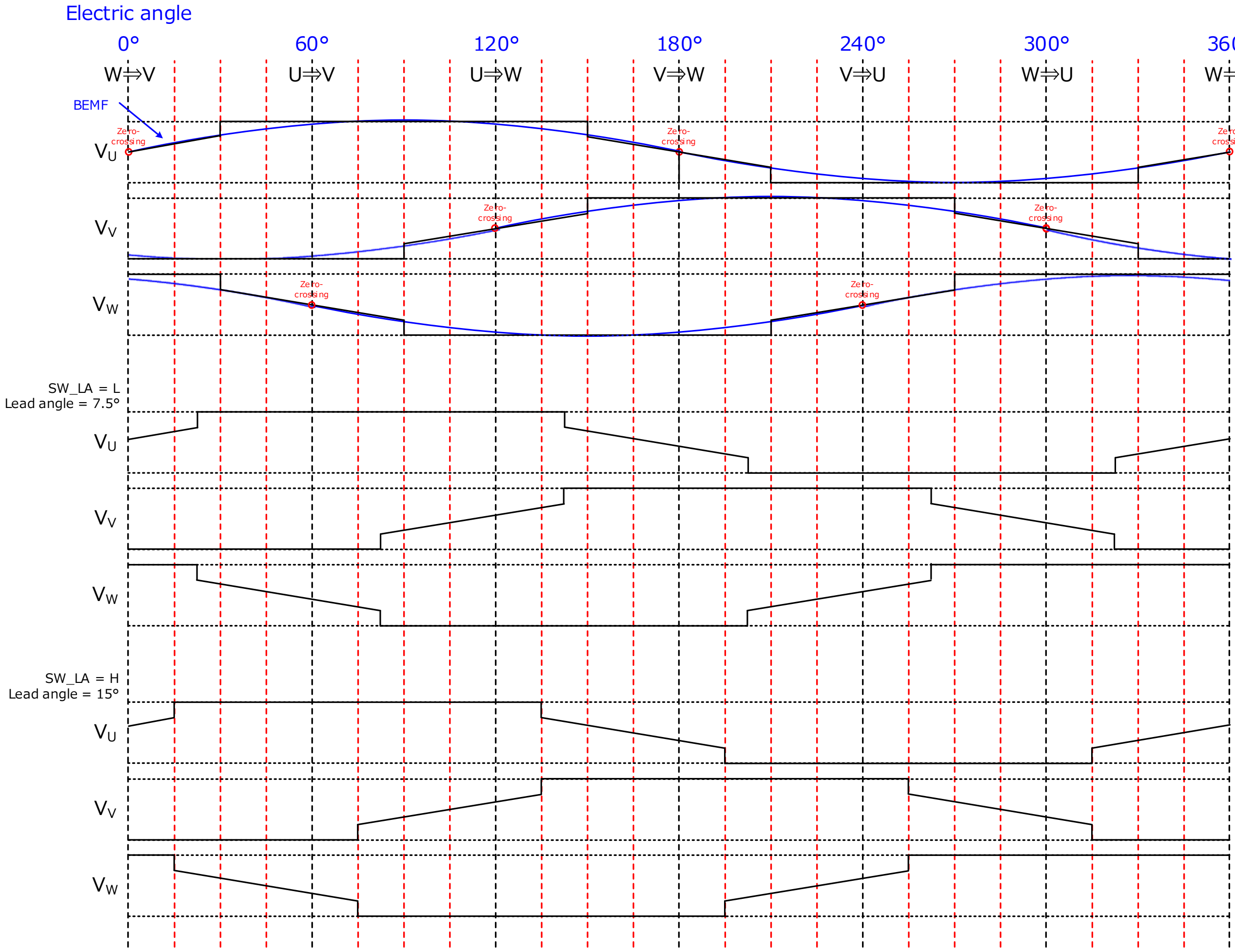


Fig.7.2.1 The timing of 120 degrees sensorless operation

7.2.2. DC excitation of start up sequence

To perform sensorless start up sequence, TB9062FNG initially will set up pre-set voltage level on each 3 phases (dc excitation) to set motor rotor on pre-set positon. The excitation time length is set by external capacitor on pin "IPC" by the following formula.

DC excitation time : TIP [ms] = 400×CIP [μF]

In the case that DC excitation is not required, external capacitor on pin "IPC" does not need to set and "IPC" pin can be kept open on PCB.

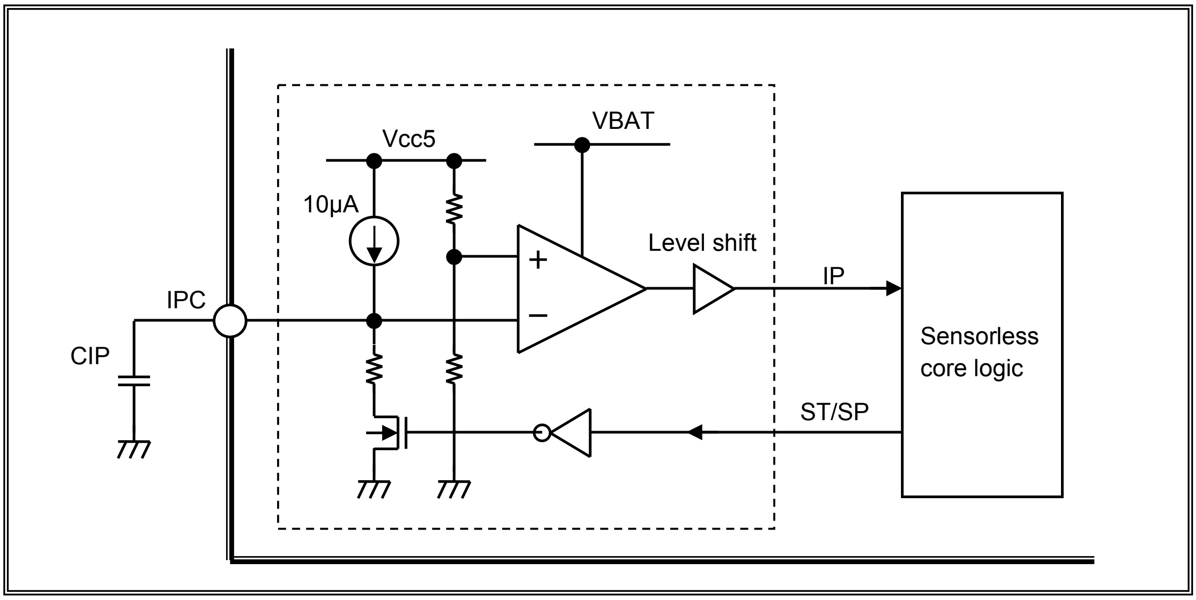


Fig.7.2.2.1 : Block circuit of DC excitation

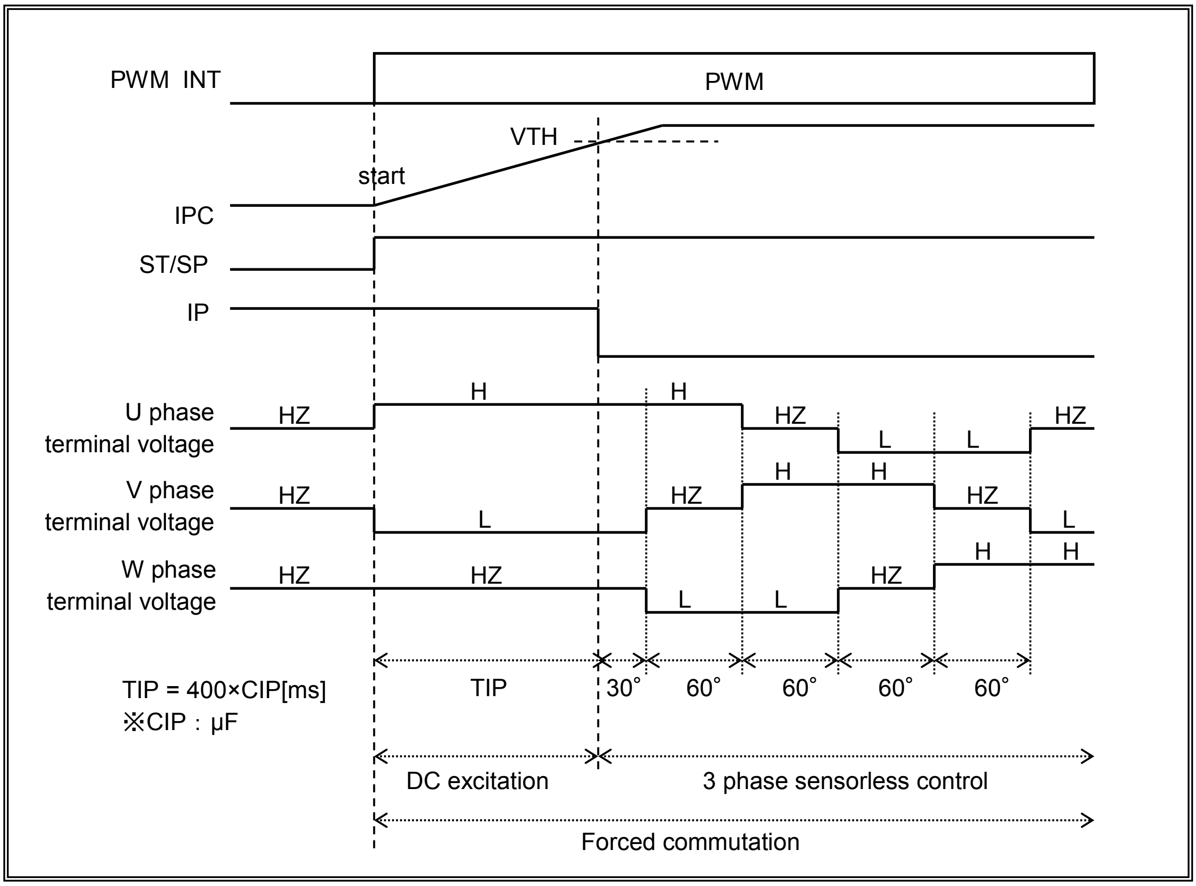


Fig. 7.2.2.2 : DC excitation timing

(Note)

- In the case that the DC excitation time period is too short, there is the possibility that forced commutation is started before setting motor rotor on the pre-setting position and cannot start proper sensorless operation. In the case that the setting time of DC excitation is too long during DC excitation, DC current is released between 2 phases and there is possibility to damage the external MOSFET. Please consider appropriate time period based on the system.

- Regardless of lead angle, electrical angle of first forced commutation is 30°.

7.2.3. Auto start up PWM duty control

During sensorless start up sequence, i.e. DC excitation and force commutation, the input PWM duty is ignored and the output PWM duty is automatically set according to VBAT as following table for stable torque generation.

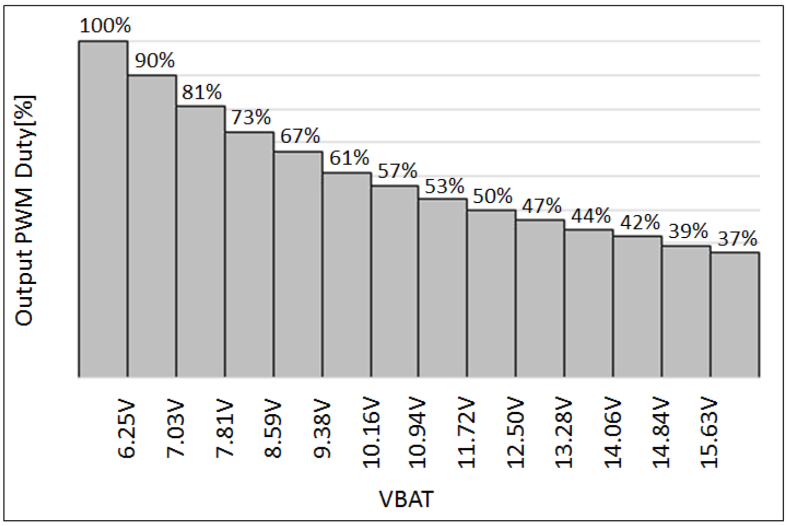


Fig. 7.2.3 Automatic start up duty control

Table 7.2.3 Start up output PWM duty

VBAT	PWM Duty
< 6.25V	100%
6.25V to 7.03V	90%
7.03V to 7.81V	81%
7.81V to 8.59V	73%
8.59V to 9.38V	67%
9.38V to 10.16V	61%
10.16V to 10.94V	57%
10.94V to 11.72V	53%
11.72V to 12.50V	50%
12.50V to 13.28V	47%
13.28V to 14.06V	44%
14.06V to 14.84V	42%
14.84V to 15.63V	39%
15.63V <	37%

7.3. Input

7.3.1. Input digital filter

TB9062FNG has digital filter for the input PWM signal, rejecting input if below 6μs(2μs×3) and passing if above 8μs(2μs×4).

7.3.2. Input PWM signal frequency conversion circuit

The input PWM signal from pin “SIG” is checked for frequency and duty by TB9062FNG. In the case that frequency is over the spec (5Hz to 1.2kHz) or the duty is out of the spec, it is considered as fault and TB9062FNG shall stop pre-driver output (Hi-Z).

7.3.3. Input compensation circuit

TB9062FNG build-in input PWM duty compensation circuit by the following formula and the figure.

$$y = (255/179) \times (x-39)$$

In the case input PWM duty range is lower than 15%, output PWM duty become 0%.
In the case input PWM duty range is upper than 85%, output PWM duty become 100%.

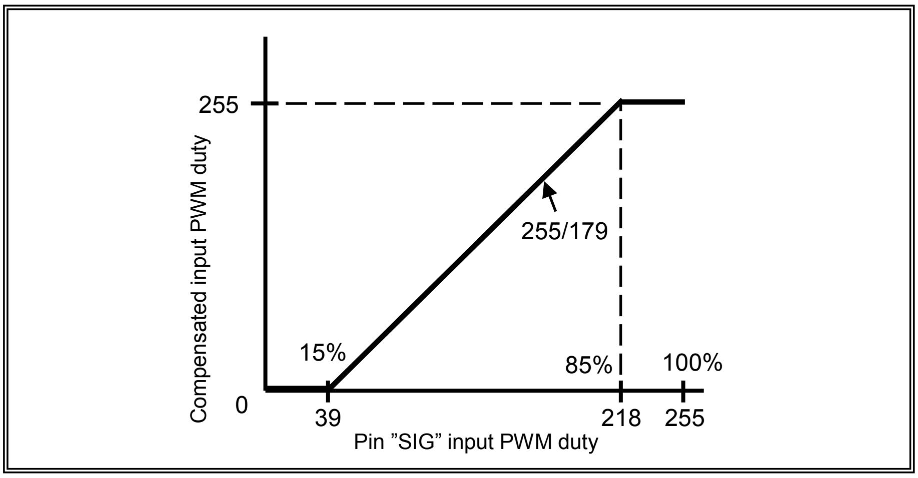


Fig. 7.3.3 ”SIG” pin input PWM duty compensation

7.4. Output

7.4.1. Output PWM signal generator circuit

The input PWM signal frequency (5Hz to 1.2kHz) is converted to 17kHz (typ.). The output PWM signal duty is converted from compensated input PWM duty as following fig.7.4.1. The resolution of output PWM signal duty is 0.25μs. (dividing by 236)

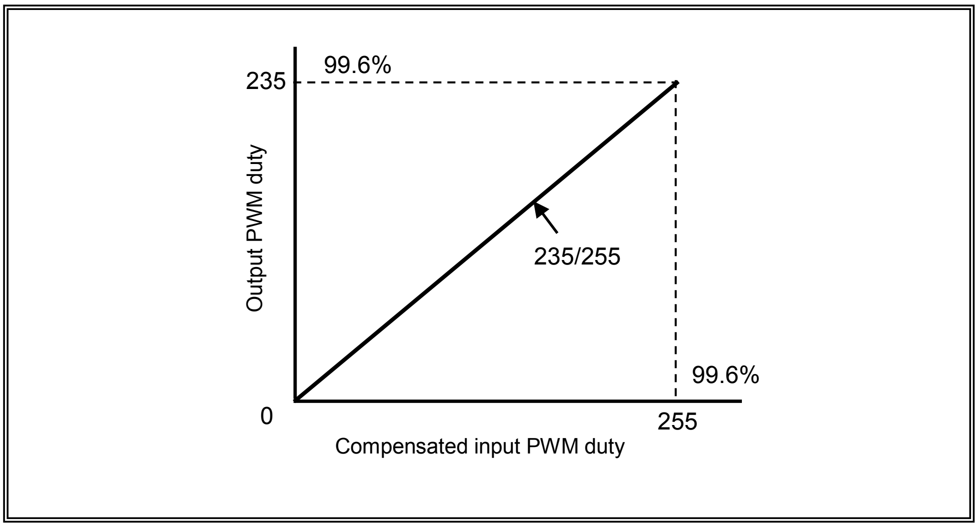


Fig. 7.4.1 Compensated input PWM duty vs output PWM duty

7.4.2. Automatic soft speed changing control

TB9062FNG has a filter circuit for prevention of stepping out by input PWM duty changed suddenly. Next PWM duty is average of present input PWM duty and previous output PWM duty (Fig. 7.4.2).

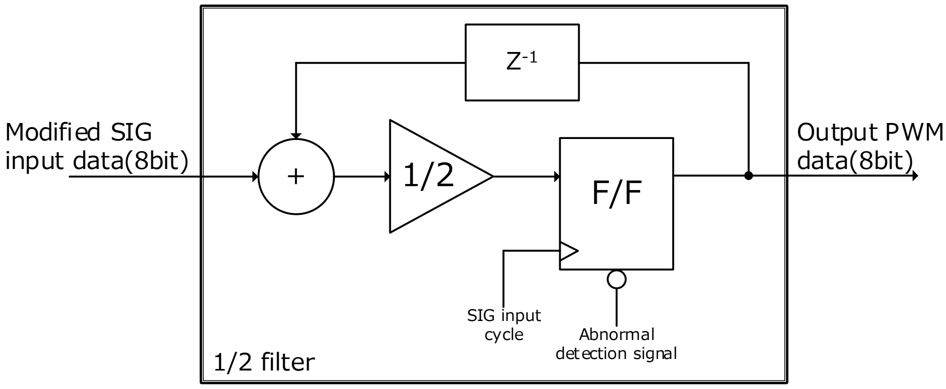


Fig. 7.4.2 Automatic soft speed changing control circuit

(Example) In the case that input PWM duty is changed from 0% to 50%, output PWM duty is changed as follows. The Calculation is done every input PWM period.

0%→25% → 37.25% → 43.75% → 46.875% → 48.4375%
→ 49.21875% → 49.609% → 49.805% →(continuous calculation)

In the case of input PWM duty is 100%(“high”), the cycle is changed to every 262ms.

7.4.3. Pre-driver for external MOSFET drive

TB9062FNG build-in pre-driver for external Pch/Nch MOSFET.

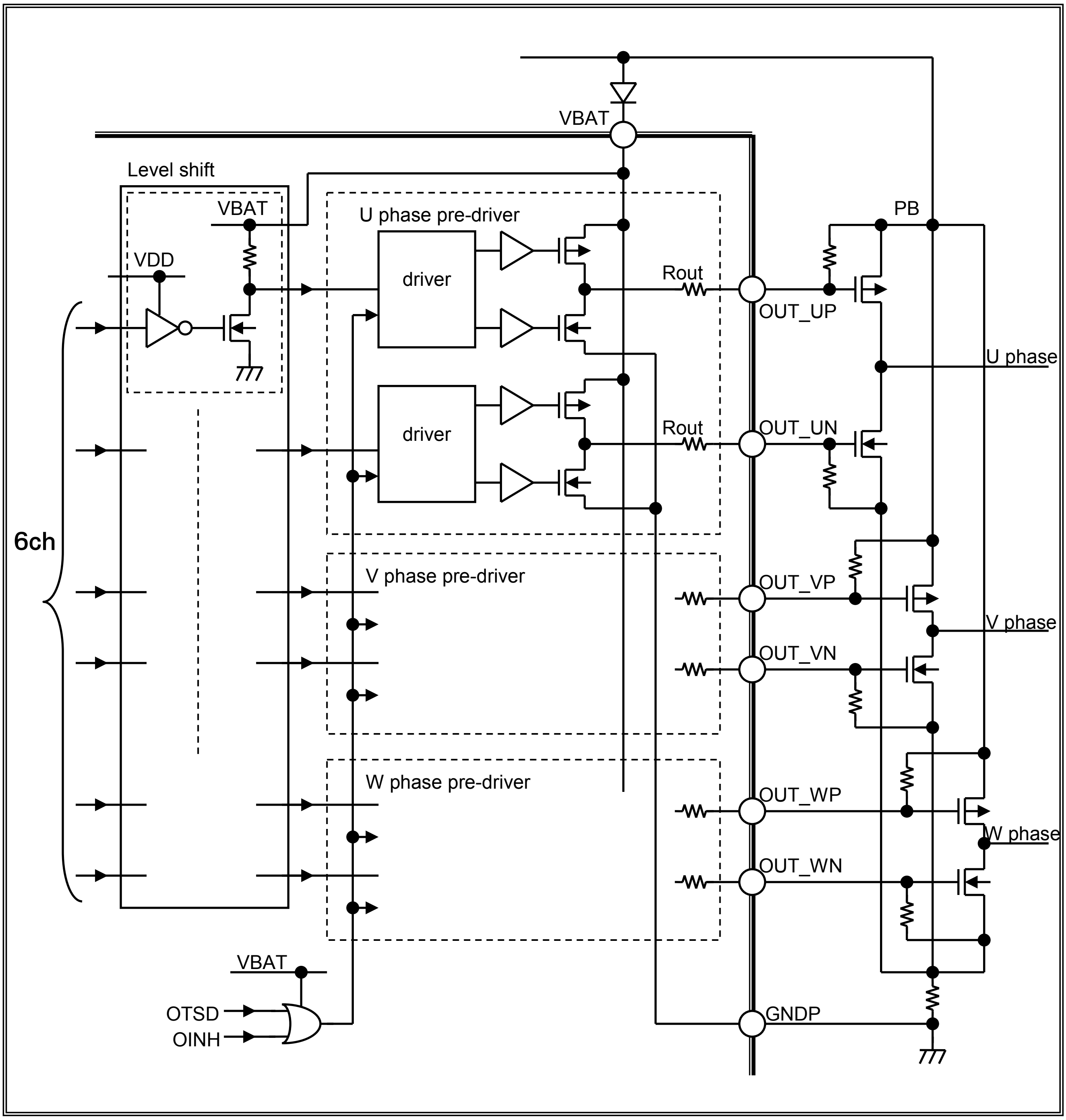


Fig. 7.4.3 Pre-driver circuit block diagram

7.4.4. Motor rotation speed output signal "OUT_FG"

TB9062FNG outputs motor rotation speed from "OUT_FG".

When TB9062FNG detects zero cross from motor EMF and sensorless operation is under way, from "H" level is output at OUT_FG every 360° (electrical angle) as in (fig.7.4.4.2). In the case that motor fault is detected "H" is not observed.

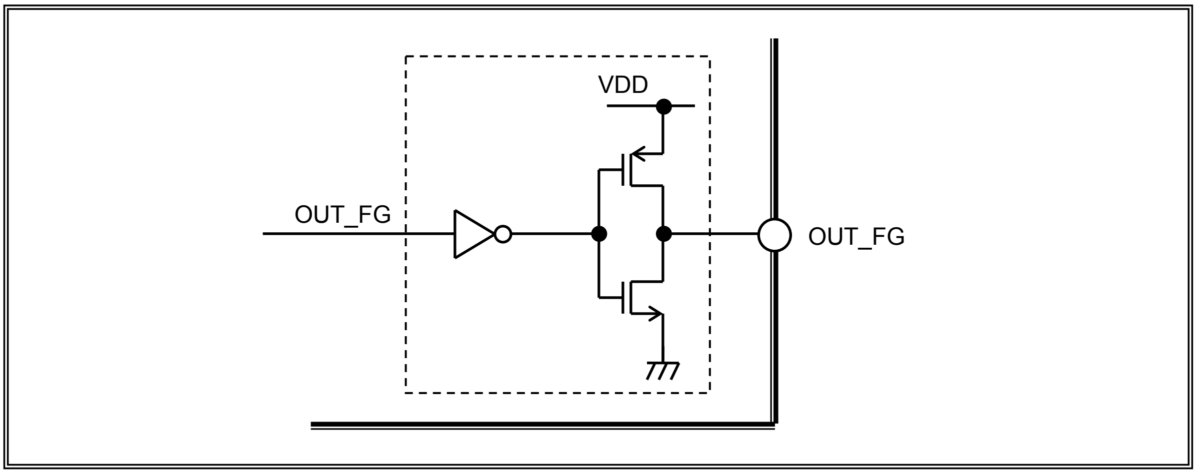


Fig. 7.4.4.1：OUT_FG circuit block diagram

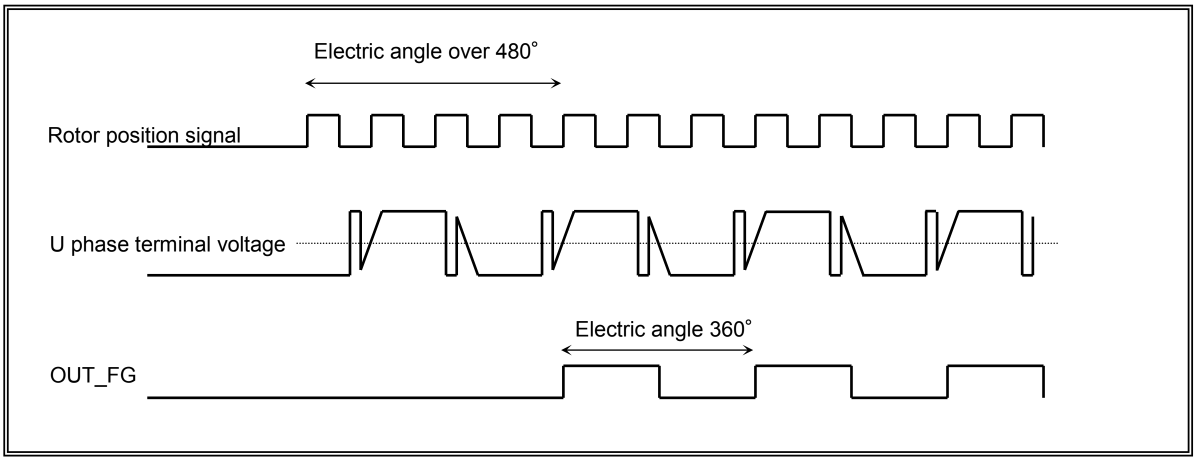


Fig. 7.4.4.2：Output timing of signal from "OUT_FG"

7.5. Internal power supply

7.5.1. 5V regulator

TB9062FNG build-in 5V regulator with phase compensation capacitor and output Pch transistor. The current capacity is 10mA and can be used for external circuit like external over temp circuit within 5mA current load. (ref. 7.8.1)

7.5.2. Vcc5 voltage monitoring circuit

The Output of internal 5V regulator is monitored. Power on reset (POR) release and low voltage detection is triggered when rising Vcc5=4.6V (typ.) and falling Vcc5=4.2V (typ.) respectively. In case of the latter, internal logic is reset. Internal filters will ignore ripples that are shorter than 10μs.

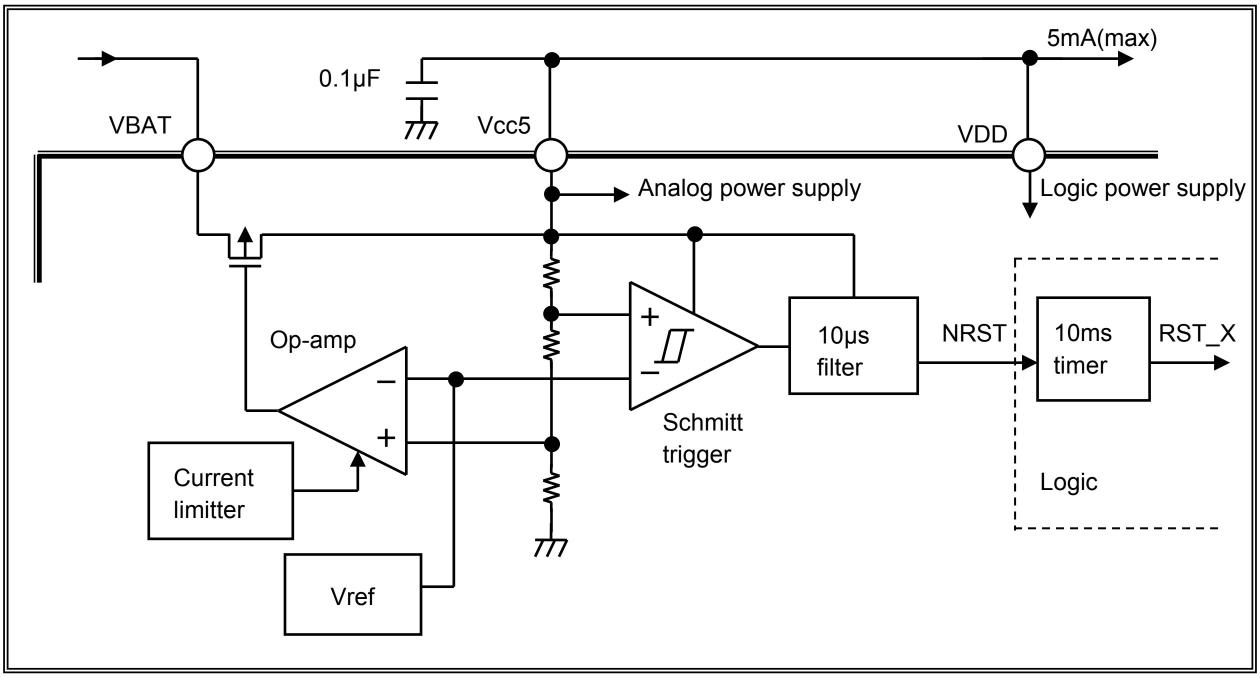


Fig. 7.5.2.1 : Vcc5 regulator and monitoring block diagram

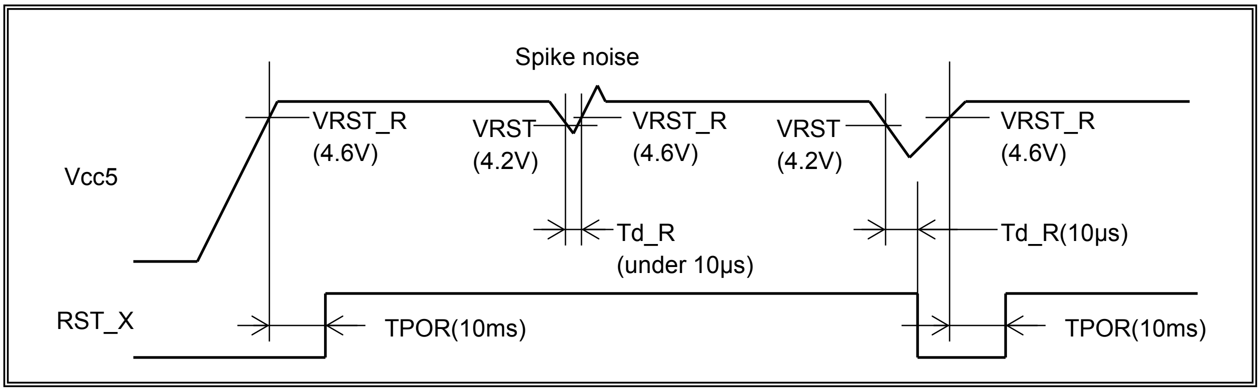


Fig. 7.5.2.2 : Vcc5 output POR timing

7.6. Oscillator Circuit

TB9062FNG has oscillator circuit for logic circuit, timers, sensorless commutation operation. Oscillator frequency is 4MHz (typ.) (Rext=39.0kΩ). The frequency can be set by the range of Rext=39.0kΩ±20%, the power is supplied by internal 5V regulator. Even in the case of abnormal detection of Vcc5, VBAT, this circuit maintains its function.

7.7. Motor Position Detection Circuit

TB9062FNG has comparator for motor position detection as described in reference circuit below. This comparator doesn’t have hysteresis characteristics. The capacitor on pin ”WAVEUVW” performs filtering.

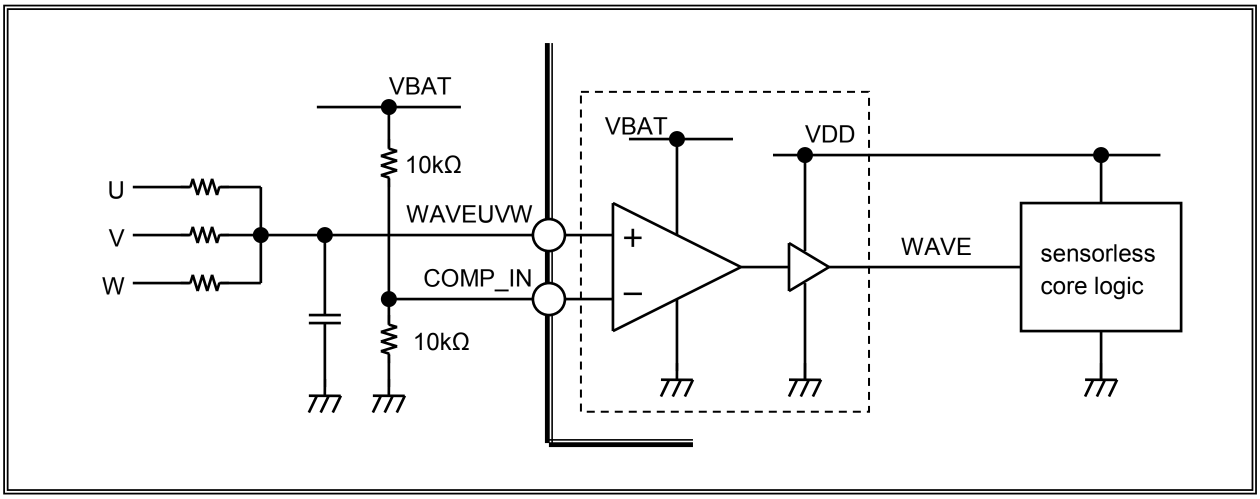


Fig. 7.7 : Motor positon detection reference circuit

7.8. Miscellaneous Abnormal Detection

TB9062FNG built-in miscellaneous abnormal detection as below table.

Table 7.8 Fault detection

item	abnormal mode	detection / release	response	notes
External over temp. detection	over temp.	detect VINH ≥Vcc5×0.52 release ≤Vcc5×0.48	Pre-driver OFF (Hi-Z)	Return to normal operation by 10ms after release level detected
Chip internal over temp.	over temp.	detect Tj ≥159℃ release ≤157℃	Pre-driver="L" (PWM OFF)	
VBAT abnormal	over voltage	detect VBAT ≥17.8V release ≤17.2V		
	low voltage	detect VBAT ≤6V release ≥7V		
Over motor current	over current	detect VSHUNT ≥50mV release ≤50mV	Pre-driver output "L" from over current detection to the next falling edge of generated internal PWM signal	
Vcc5 low voltage	low voltage	detect Vcc5 ≤4.2V release ≥4.6V	Rising：internal logic reset release at Vcc5 = 4.6V(typ.) Falling：internal logic reset at Vcc5 ≦ 4.2V(typ.)	

7.8.1. External Over Temperature Detection (Pre-driver Output Enable/Disable Control)

Pin "INH" disables output of TB9062FNG each pre-driver(INH = "H"). Below is an example using external thermistor.

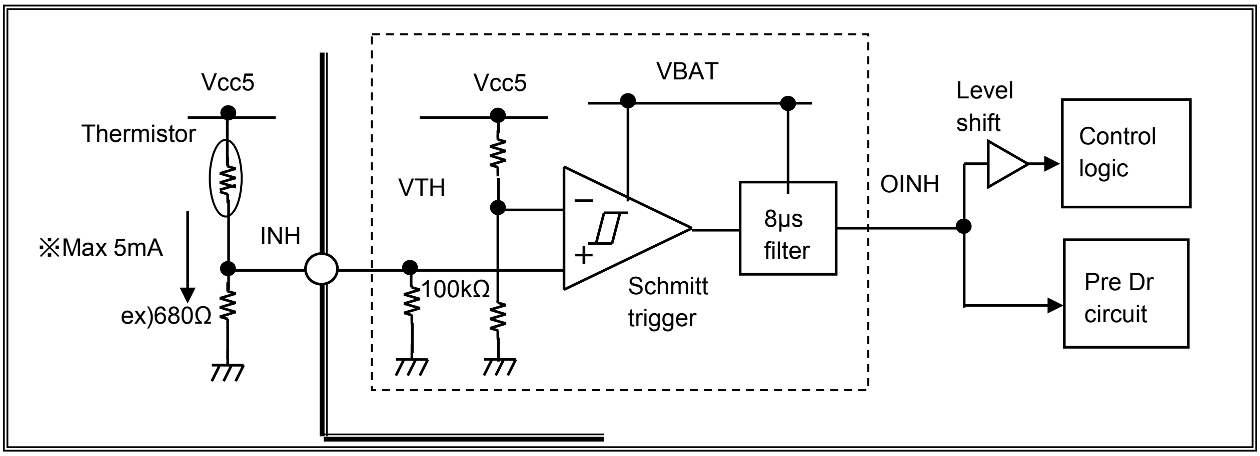


Fig. 7.8.1.1：Pre-driver Inhibit Circuit

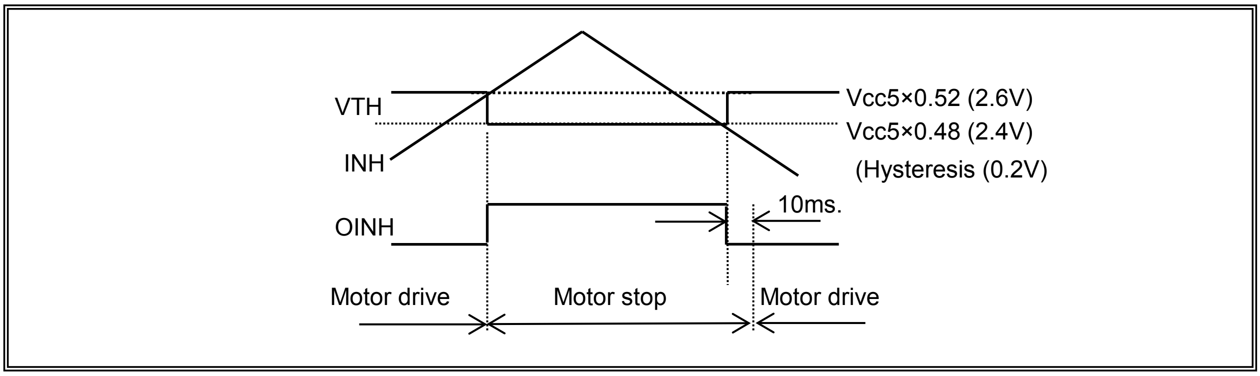


Fig. 7.8.1.2：Inhibit Pre-driver timing

7.8.2. IC internal circuit over temperature detection

TB9062FNG built-in temperature detection circuit will shut off output PWM when temperature above 159°C (typ.) is detected and will resume 10ms after 157°C (typ.) is reached.

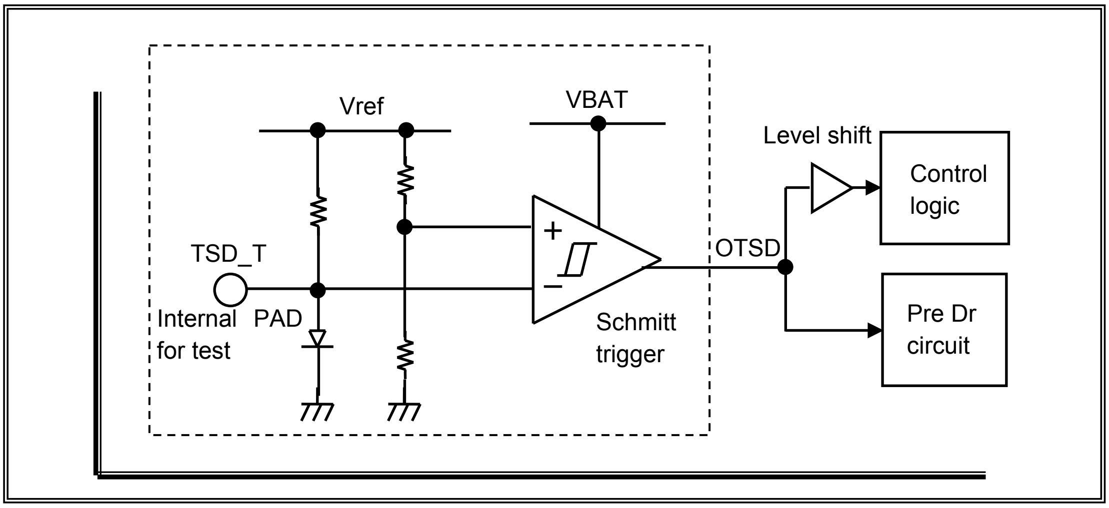


Fig. 7.8.2.1 : IC Internal Over Temperature Detection Circuit Block Diagram

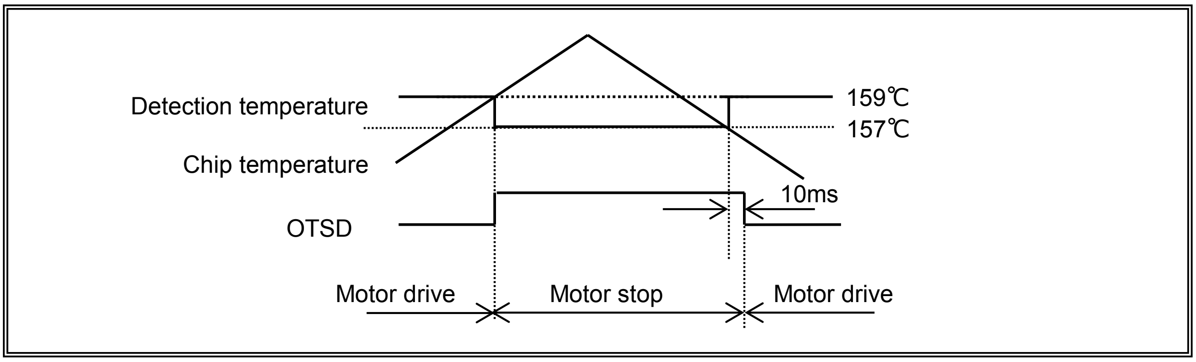


Fig. 7.8.2.2 : IC internal over temperature detection timing

7.8.3. VBAT over voltage/under voltage detection

TB9062FNG built-in VBAT voltage detection circuit. Output PWM will be shut off when VBAT reaches 17.8V(typ.) or below 6.0V(typ.) and resumes with 10ms delay when 17.2V(typ.) or 7.0V(typ.) is reached, respectively.

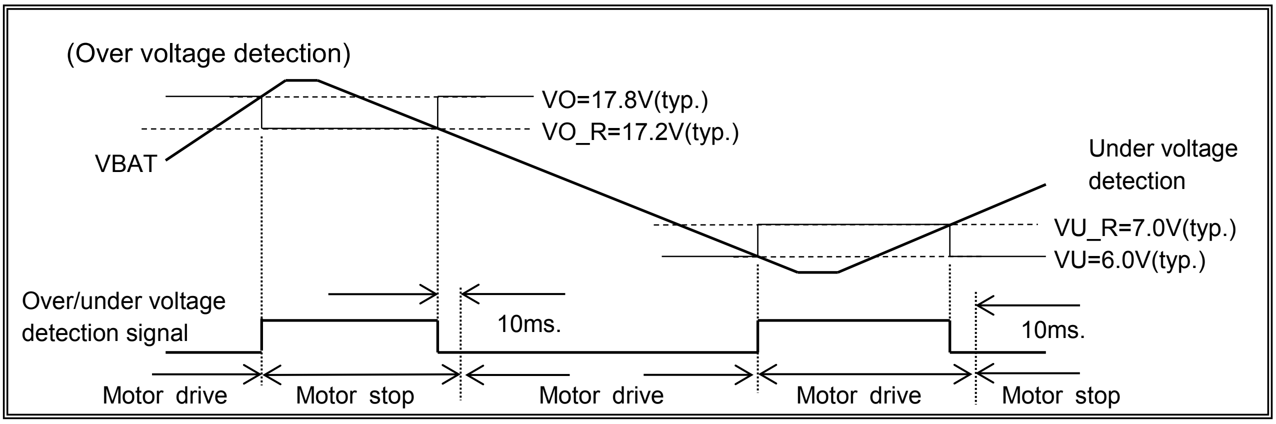


Fig. 7.8.3 : Over / under voltage detection of VBAT

7.8.4. Motor over current detection

TB9062FNG has an over current detection circuit. Please set up the motor over current detection value as below.

(Example) In case of over current detection value is set 5[A].
Because of over current detection threshold = 50[mV], please connect 10[mΩ] (= 50[mV] / 5[A]) external Rs.

When motor over current is detected, pre-driver output PWM will be shut down to reduce PWM duty. When SHUNT_U voltage (VSHUNT) falls below 50mV, pre-driver output resumes on the next falling edge of internal PWM.

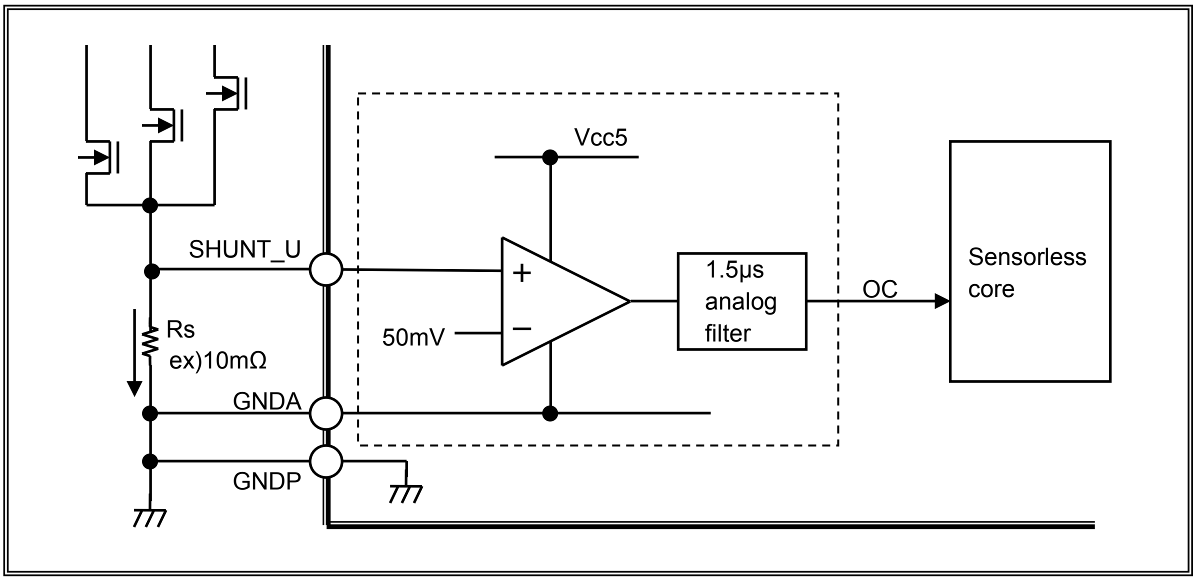


Fig. 7.8.4.1 : Motor over current detection circuit

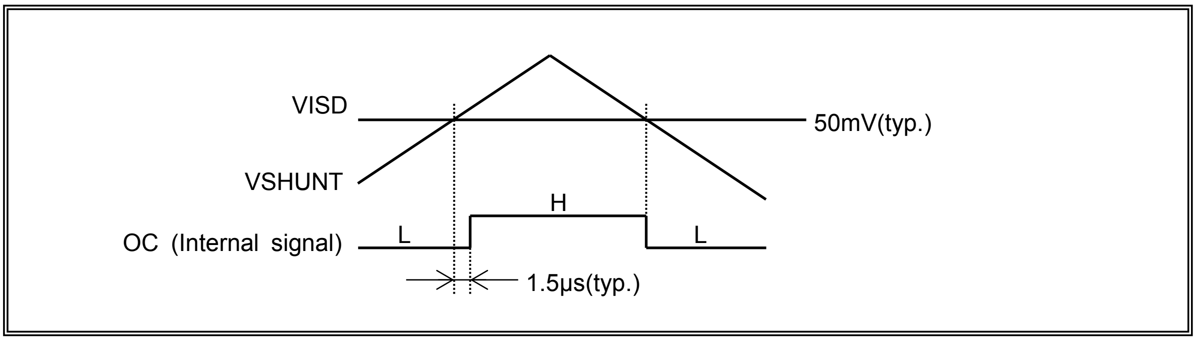


Fig. 7.8.4.2 : Motor over current detection function

The below figure shows the motor over current detection timing.

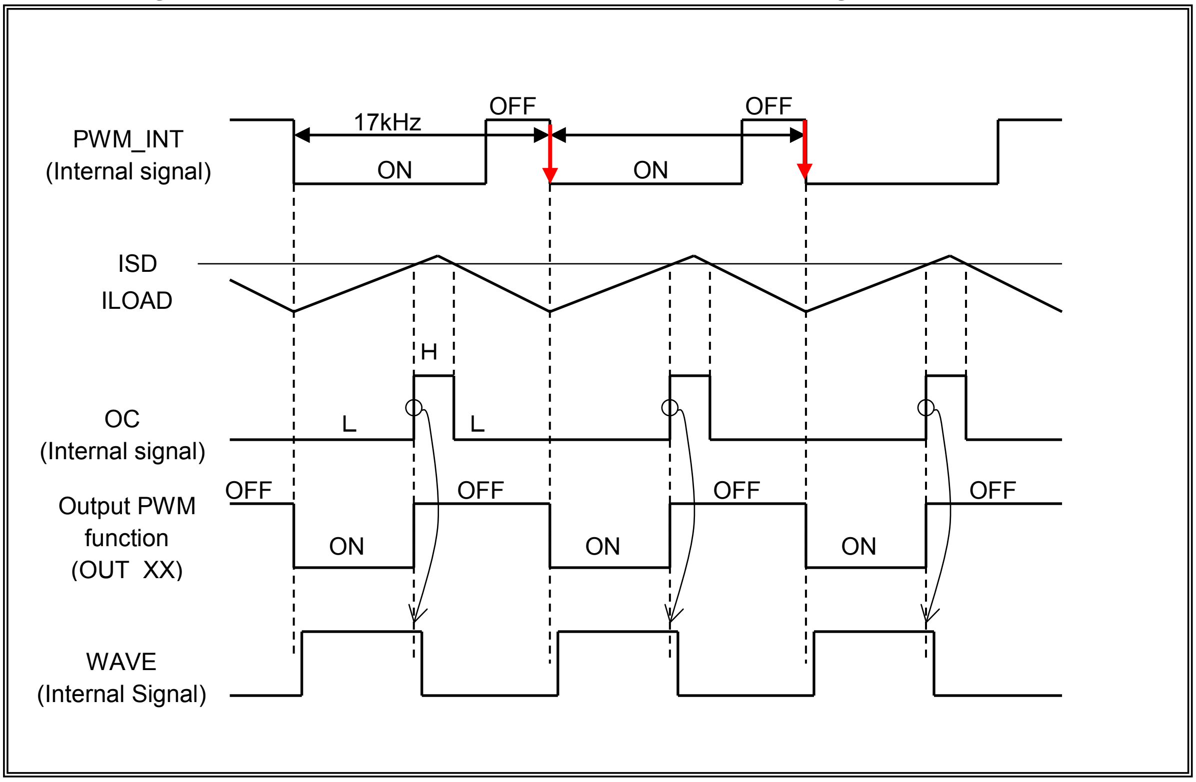


Fig. 7.8.4.3 Motor over current detection timing

(Stepping Out Detection Time)

If the over current condition is longer than the below "Toc_off", TB9062FNG determines as motor stall and commences forced commutation. If motor over current condition remains, motor shall not commutate as well position detection is not performed.

Toc_off (max) = Tfst / 6 — Tfst : Forced commutation speed [s]
Toc_off (min) = (Tfst-Tfuvw) / 6 — Tfuvw : Motor rotation speed [s]

(ex.) FC 600rpm(EA)→100ms、Motor speed 16,000rpm(EA)→3.75ms
Toc_off (max)＝100ms / 6 = 16.67ms
Toc_off (min) = (100ms－3.75ms) / 6＝16.04ms.
(ref. fig7.8.4.4 for Toc_off)

■Over current detection sequence (Fig. 7.8.4.4)
The following is the sequence of motor over current detection. Input PWM signal is continuously Input in the below cases.

① When TB9062FNG detect motor over current, all output PWM are off and stop to detect motor position signal from pin ”WAVEUVW”

② When motor current is falls below limit, Pre-drier output is resumed at falling edge of PWM_INT.

③ If the over current condition is over the following time, it is considered motor stall and forced commutation mode is initiated. But during this period, output PWM are kept off and motor is not rotated.

④ When motor current falls below limit, pre-driver output resumes and begin forced commutation, and sensorless operation is achieved at zero cross point detect.

⑤ After 480° electrical angle, “OUT_FG” is output in sync with U phase position detection.

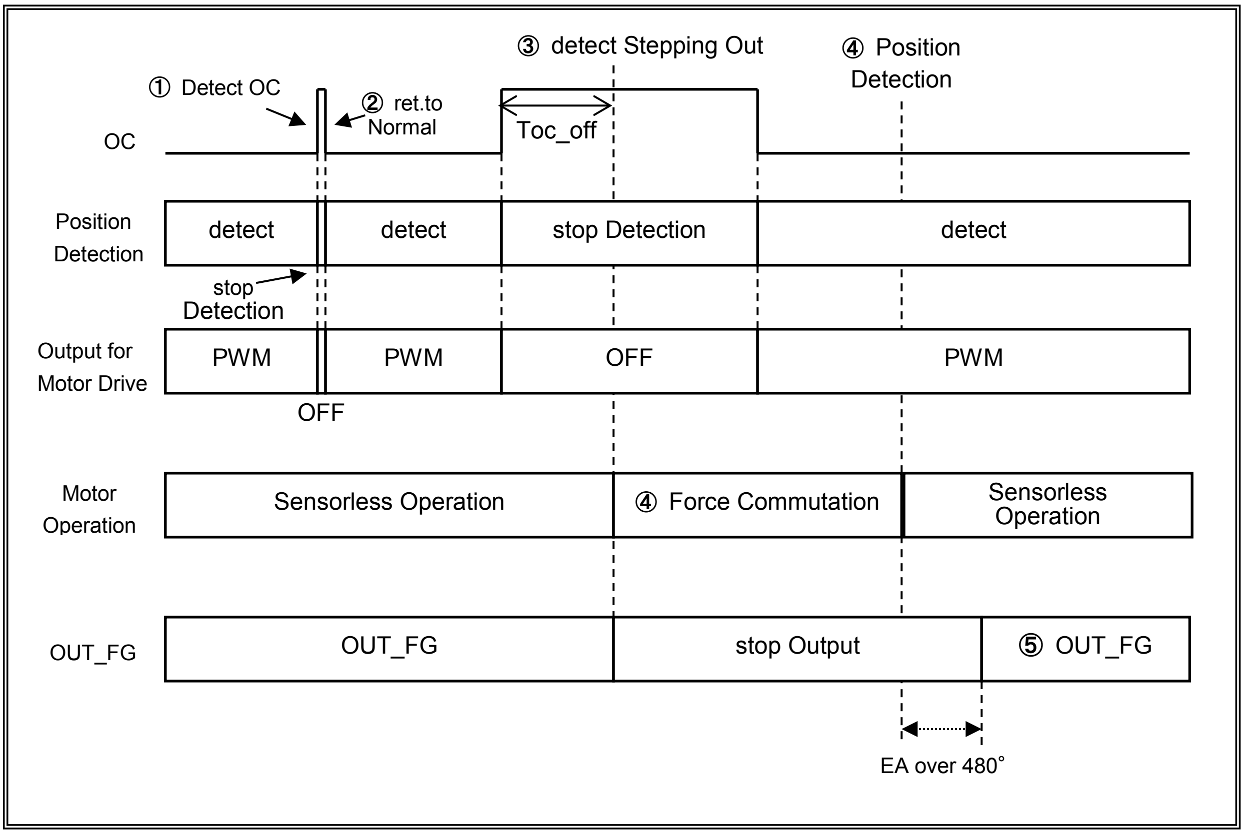


Fig. 7.8.4.4 Over current detection operation sequence

8. Absolute maximum ratings (Ta = 25°C) (Note.1)

Table 8.1 Absolute maximum ratings

Characteristics	Symbol	Adaptable pins	Rating	Unit
Power supply voltage	VBAT	VBAT	-0.3 to +35	V
			40(300ms)	
	Vcc5	Vcc5	-0.3 to +6	
	VDD	VDD	-0.3 to +6	
Input current	IIN1	SIG	5(Note.3)	mA
Input voltage	VIN1	SIG	-0.3 to VBAT	V
	VIN2	COMP_IN、WAVEUVW	-0.3 to 30	
	VIN3	SW_LA、SEL_BIT0、SEL_BIT1 TEST	-0.3 to VDD	
	VIN4	OSC_R、INH、IPC SHUNT_U	-0.3 to Vcc5	
Output current	IOUT1	OUT_UP、OUT_VP、OUT_WP、OUT_UN、OUT_VN、OUT_WN	±20(DC)	mA
	IOUT2		±320(5μs)	
	IOUT3	OUT_FG、OTEST	±1	
	ILOAD	Vcc5	-10	
Output voltage	VOUT1	OUT_UP、OUT_VP OUT_WP、OUT_UN OUT_VN、OUT_WN	-0.3 to VBAT	V
	VOUT2	OUT_FG、OTEST	-0.3 to VDD	
Storage temperature	Tstg	-	-55 to +150	℃.
Power dissipation	P_D	-	0.89(Note.2)	W

Note.1 : The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded during operation, even for an instant. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may damage any other equipment. Applications using the device should be designed such that the absolute maximum ratings will never be exceeded in any operating conditions. The device must be used within the specified operating range.

Note2 : Mounted on a board (50 × 50 × 1.6 mm, Cu: 40%) when Ta = 25℃

Note3 : Clamp voltage of SIG terminal is 30V (Ta=25℃).

9. Operating Range

Table 9.1 Operating range

Characteristics	Symbol	Rating	Unit	Remarks
Power supply voltage	VBAT	8 to 16	V	Recommended operating voltage range with all spec parameters warranted
		6.5 to 8	V	Outside of electrical characteristics assurance (Note)
	VDD	3 to 5.5	V	-
Operating temperature	Topr	-40 to 125	℃	Ta (Ambient temperature)
		-40 to 150	℃	Tj (Junction temperature)
Input PWM frequency	PWM	5 to 1.2k	Hz	Rext=39.0kΩ

(Note) Not tested.

10. Electrical Characteristics

Table 10.1 IC general characteristics

VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
Current Consumption	IBAT	VBAT	-	1	-	4	mA
Input voltage	VIH	SW_LA SEL_BIT0 SEL_BIT1 TEST	-	0.8 ×VDD	-	VDD	V
	VIL		-	−0.3	-	0.2 ×VDD	V
Input current	IIH	SW_LA SEL_BIT0、SEL_BIT1	VDD=5V、VIN=5V	25	50	100	μA
	IIL		VDD=5V、VIN=0V	-10	-	10	
	IIH	TEST	VDD=5V、VIN=5V	0.25	0.5	1	mA
	IIL		VDD=5V、VIN=0V	-10	-	10	μA
Output voltage	VOH	OUT_FG OTEST	IOH=-1mA	0.8 ×VDD	-	VDD	V
			IOH=-500μA	0.9 ×VDD	-	VDD	
	VOL		IOL=1mA	0	-	0.2 ×VDD	V

Table 10.2 SIG input

VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
Threshold voltage	VIH	SIG	-	Vcc5 ×0.57	Vcc5 ×0.62	Vcc5 ×0.67	V
	VIL		-	Vcc5 ×0.53	Vcc5 ×0.58	Vcc5 ×0.63	
Input hysteresis voltage	dVTH	SIG	-	0.15	0.2	0.25	V
Input current	IIH	SIG	VIN=16V	80	160	320	μA
	IIL		VIN=0V	-10	-	10	
Input clamp voltage	Vclmp	SIG	IIN=5mA	25	30	35	V
Input noise filter	TFIL	SIG	-	5.26	8	9.30	μs

Table 10.3 5V regulator & reset

VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
5V Regulator Output voltage	Vcc5	Vcc5	-	4.85	5.0	5.15	V
Current limiter	Ilimit	Vcc5	-	10	-	50	mA
line regulation	VLINE	Vcc5	VBAT=8 to 16V	-26	-	26	mV
Load regulation	VLOAD	Vcc5	ILOAD=1 to 10mA	-52	-	52	mV
Wake up speed	T_VccLH	Vcc5	CVcc5=0.1μF	10	50	100	μs
Power On Reset Voltage	VRST	Vcc5	-	Vcc5 ×0.81	Vcc5 ×0.84	Vcc5 ×0.87	V
				4.0	4.2	4.4	
Reset release voltage	VRST_R	Vcc5	-	4.4	4.6	4.8	V
Hysteresis of detect voltage	dVRST	Vcc5	VRST_R－VRST	0.3	0.4	0.5	V
Power-on reset timer	TPOR	-	-	8	10	12	ms
Reset detection filter	Td_R	-	-	5	-	25	μs

Table 10.4 Motor pre-driver

VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
Output voltage	VOH1	OUT_UP OUT_VP OUT_WP OUT_UN OUT_VN OUT_WN	IOH=-1mA	VBAT -0.5	-	VBAT	V
			IOH=-20mA	VBAT -3	VBAT -2	VBAT	
	VOL1		IOL=1mA	0	-	0.5	V
			IOL=20mA	0	2	3	
Output OFF leakage current	ILEAK		-	-10	-	10	μA
Propagation delay time	TPLH TPHL		PWM_INT → OUT_XX	0	-	10	μs
Output resistance	Rout		-	60	100	150	Ω

Table 10.5 Abnormal Detection

VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics		Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
Over Current Detection		VISD	SHUNT_ U－GNDA	-	45	50	55	mV
		ISD	-	Shunt resistance Rs=10mΩ	4.5	5.0	5.5	A
Over Current Noise Filter		td_ISD	SHUNT_U	-	0.7	1.5	3.0	μs
Over Voltage Detection		VO	VBAT	-	16.6	17.8	19.0	V
Over Voltage Detection Release		VO_R		-	16.0	17.2	18.4	
Over Voltage Hysteresis		dVO		-	0.2	0.6	1.0	
Low Voltage Detection		VU	VBAT	-	5.5	6.0	6.5	V
Low Voltage Release		VU_R		-	6.5	7.0	7.4	
Low Voltage Hysteresis		dVU		-	0.6	1.0	1.4	
Input PWM	Abnormal “H” length	TOH	SIG	High-level period	229	262	305	ms
	Abnormal “L” length (long)	TOC		Low-level period (long)	229	262	305	
	Abnormal “L” length (short)	TUC		Low-level period (short)	0.58	0.67	0.78	
Overtemperature detection		TSD	-	Detect	150	159	-	℃
		TSD_R	-	Release	-	157	-	

Table 10.6 Clock, PWM

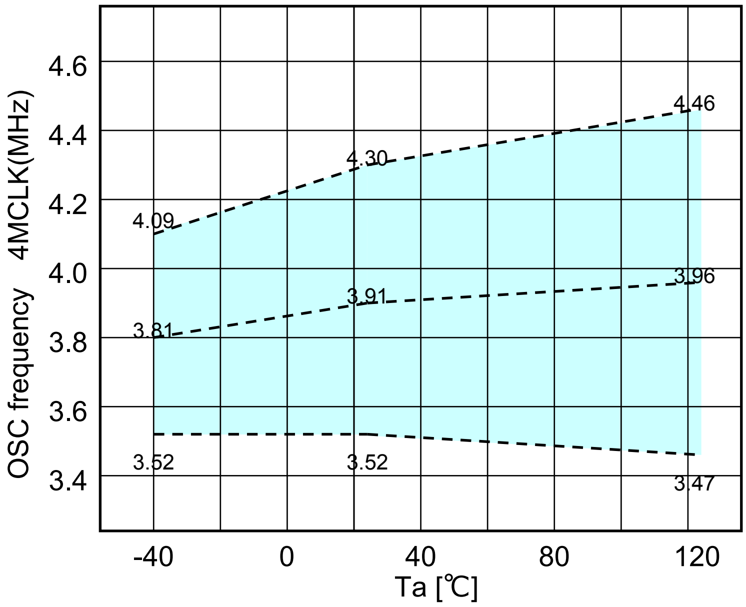
VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
Internal OSC Frequency	4MCLK	-	Rext=39.0kΩ	3.44	4.00	4.56	MHz
Output PWM frequency	PWM_INT	-	Rext=39.0kΩ	14.6	17.0	19.4	kHz
Terminal Voltage	Vref	OSC_R	Rext=39.0kΩ	1.12	1.22	1.32	V

※Rext accuracy and temperature characteristics are not included.

◆Oscillator frequency changing in each temperature

Bellow graph shows only oscillator frequency of IC at Rext = 39.0kΩ. Rext accuracy and temperature characteristics are not included.



※The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Table 10.7 VBAT Accuracy of Start Up Duty Control (Ref. Fig.7.2.3)

VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
VBAT Accuracy of each step	ADbd	VBAT	VBAT Accuracy of the step Vbd1 to 13	-6.7	—	6.7	%
Each Gap Voltage of the step	SVbd		VBAT Voltage Gap of each step	0.586	0.781	0.976	V

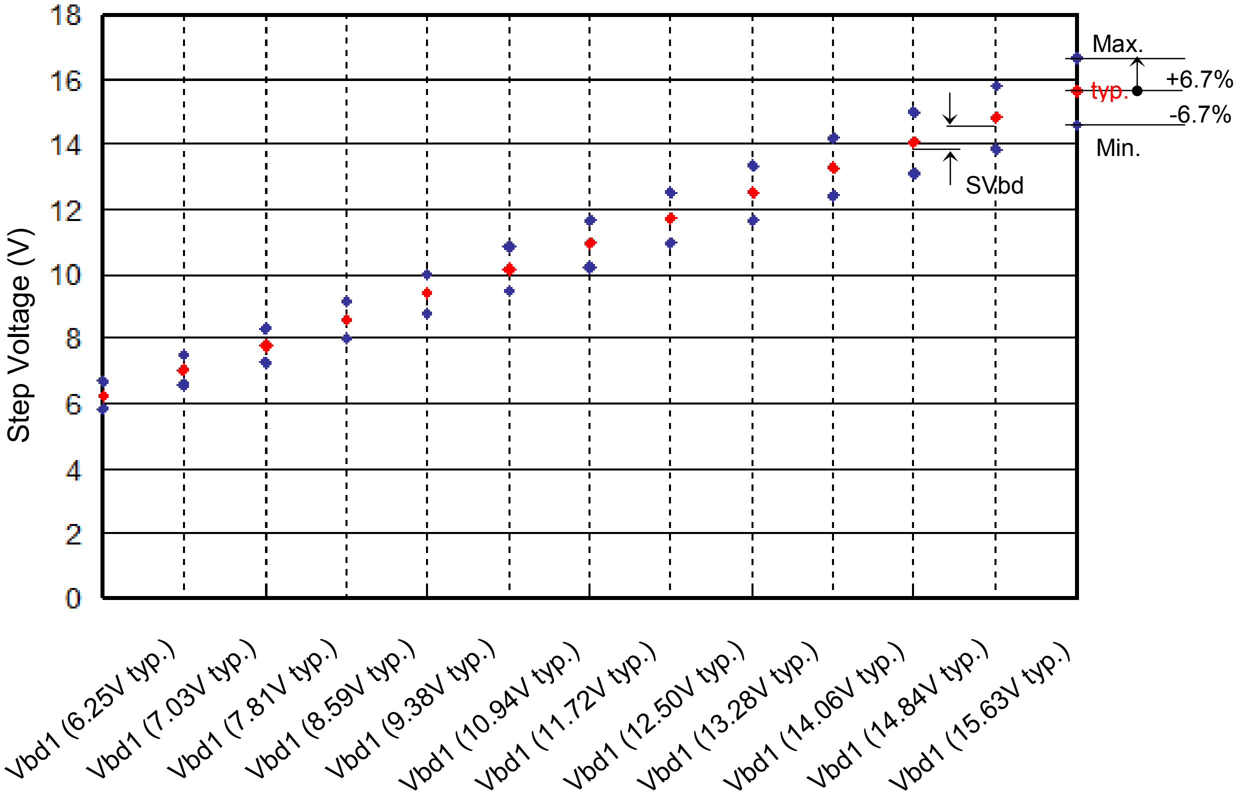


Fig. 10.1 The Voltage of Start up Duty control (Vbd1toVbd13)

Table 10.8 Comparators

VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
Input offset voltage	VIO	WAVEUVW、COMP_IN	-	-10	-	+10	mV
Common input voltage range	CMVIN		-	2	VBAT ／2	VBAT -2	V
Input current	IIN		VIN=0V to VBAT	-1	-	1	μA
Input voltage range	VIN	SHUNT_U	-	0	-	1	V
Input current	IIN		VIN=0 to 1V	-1	-	1	μA
Input voltage	VIH	INH	-	Vcc5 ×0.49	Vcc5 ×0.52	Vcc5 ×0.55	V
	VIL		-	Vcc5 ×0.45	Vcc5 ×0.48	Vcc5 ×0.51	
Hysteresis of input voltage	dVTH		-	0.15	0.2	0.25	V
Input current	IIH		VIN=Vcc5	25	50	100	μA
	IIL		VIN=0V	-1	-	1	

Table 10.9 IPC control

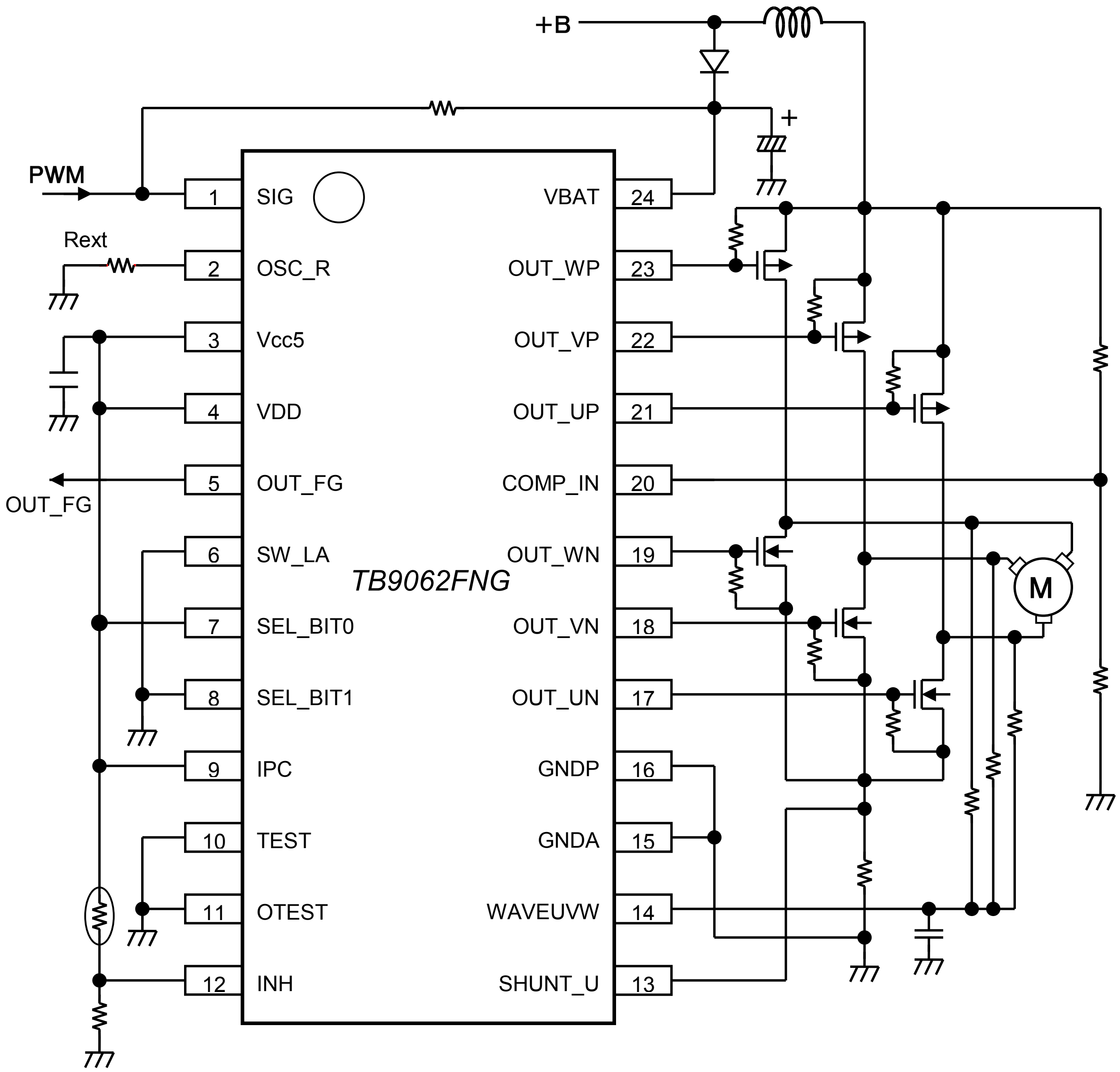
VBAT=8 to 16V, VDD=Vcc5, Ta=-40 to 125℃, Rext=39.0kΩ, unless otherwise specified.

Characteristics	Symbol	Adaptable Pins	Test Condition	Min.	Typ.	Max	Unit
Threshold voltage	VTH	IPC	-	Vcc5× 0.74	Vcc5× 0.8	Vcc5× 0.86	V
Input current	IIN		VIN=0V to VTH	-15	-10	-7	μA
DC excitation time	TIP	-	-	240× CIP	400× CIP	560× CIP	ms

※CIP (uF) : External Cap on PIN"IPC"

11. Reference Circuit Diagram

- Input : PWM
- Force Commutation Frequency : 1200rpm (Electrical Ange)
- Lead Angle : 7.5℃



(Caution)

Note 1: Some of the functional blocks, circuits in the block diagram may be omitted or simplified for explanatory purposes.

Note 2: Do not insert devices in the wrong orientation or incorrectly. Otherwise, it may cause device breakdown, damage and/or deterioration.

Note 3: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Note 4: Careful attention should be paid to the layout of the output line, VBAT, VCC and GND line since IC may be destroyed due to short-circuit between outputs, to the power supply, or to the ground.

Note 5: For the board design, it is necessary to consider the solid pattern of AGND and PGND.

12. Package

SSOP24-P-300-0.65A

Weight: 0.14 g(typ.)

(Unit mm)

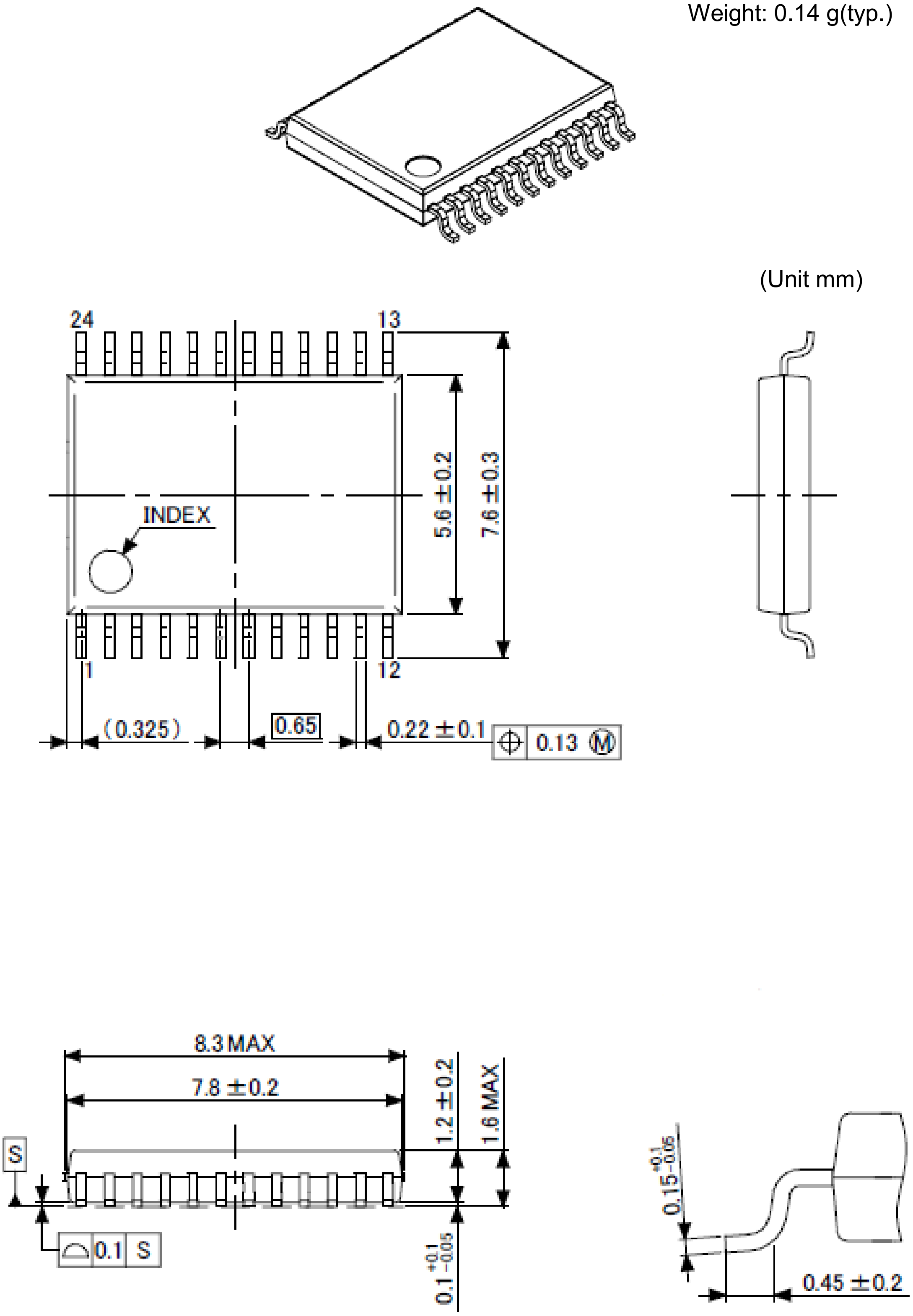


Fig. 12.1 Package size

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