Simple Guide to Improving Ripple Rejection Ratio of LDO Regulators

Outline:

This document explains the principles of suppressing ripple of the output voltage, which is caused by the ripple of the input , i.e. the ripple compressibility (PSRR).

It also explains the frequency characteristics of PSRR and the effects of the output capacitor.

Table of Contents

1. Introduction

Various semiconductor (electronic) components are used to enhance the performance and functionality of increasingly sophisticated mobile and other electronic devices. Nowadays, these semiconductor components supplied from LDOs operate at low supply voltage, and some types of devices such as image sensors are sensitive to the accuracy and stability of supply voltage.

Without accurate voltage regulation of the LDO, electronic devices might not work properly or even be degraded in terms of their electrical characteristics. LDOs must supply a precisely regulated voltage so that the semiconductor devices that actualize high-performance electronic devices operate properly. One of the factors that affect the output voltage of an LDO is the change in its input voltage. Suppose, for example, that the input voltage of an LDO comes from a DC-DC converter. Then, the switching and other noise at the output of the DC-DC converter propagates to the input of the LDO. Because an LDO derives the output voltage from the input voltage, it is stringently required to suppress any input voltage ripple to the output so as not to adversely affect its load; i.e., it is a sensitive high-performance device. The capability of an LDO to reject (suppress) input voltage ripple is called the power supply rejection ratio (PSRR), which is the most important parameter for the LDO.

This application note describes the basics of PSRR. It also discusses how PSRR changes with frequency and the effect of an output capacitor on PSRR. Its purpose is to help you select LDOs suitable for your applications and use them properly.

2. Importance and definition of the PSRR of LDOs

An LDO is a linear voltage regulator that steps down a DC voltage (that comes from a battery, a DC-DC converter, etc.) from its input to its output. The input voltage of an LDO might not be the ideal DC voltage. For example, when its input voltage comes from a DC-DC converter, it might contain ripple that has undesirable effects on the electronic devices supplied from the LDO. The LDO is capable of suppressing voltage ripple. Nowadays, the PSRR of the LDO, i.e., its capability to suppress power supply ripple, is considered crucial. A high PSRR was previously required in the low-frequency region, but now a very high PSRR is often required both in the low- and high-frequency regions. The following sections provide the basics of the PSRR, including its frequency dependence.

The PSRR of an LDO, i.e., its capability to suppress ripple on the input voltage (V_{IN}), is specified by the following equation. Figure 2.1.1 shows a typical LDO with a PMOS pass device and the waveform of the output voltage supplied to its load.

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} \quad (dB)$$

V_{INRPL}: Ripple on the input voltage (V_{IN}) of the LDO
V_{OUTRPL}: Ripple on the output voltage (V_{OUT}) of the LDO

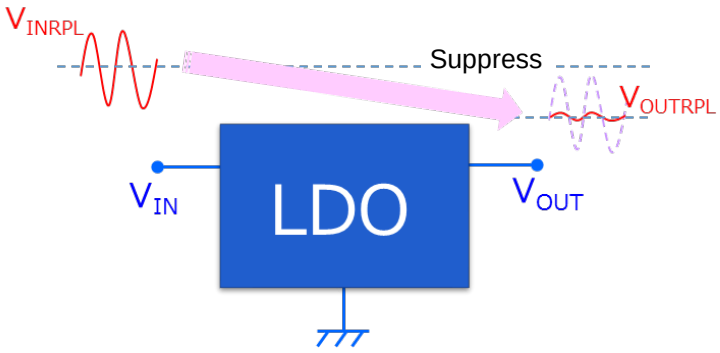


Figure 2.1.1 Rejection of input voltage ripple by an LDO

Section 3.1 and Section 3.2 describe the basics of PSRR. Section 3.3 discusses the PSRR of the LDO, which can be broken down into the following three frequency regions:

- Low-frequency region from DC to a few kilohertz
- High-frequency region from a few kilohertz to roughly 100 kHz
- Ultra-high-frequency region above 100 kHz

3. Basics of the frequency dependence of the LDO's PSRR

3.1. Factors that determine the PSRR

What factors determine the PSRR of an LDO? First, look at the circuit diagram of a typical LDO shown in Figure 3.1.1. If the ripple on the gate voltage of the PMOS pass device is equal to the ripple on V_{IN} (V_{INRPL}), the gate voltage varies simultaneously with V_{IN} while maintaining a constant difference in voltage. In this case, the PMOS pass device does not pass any current due to the V_{IN} ripple to the output. This is true because, theoretically, the gate voltage of the PMOS pass device and the input voltage (V_{IN}) have equal ripple. In this case, the V_{IN} ripple voltage is divided according to the ratio of the output impedance (Z_{OUT}) of an LDO (i.e., low impedance with negative feedback) and the output resistance (r_{DS}) of the PMOS pass device. Therefore, PSRR is determined by this voltage division ratio.

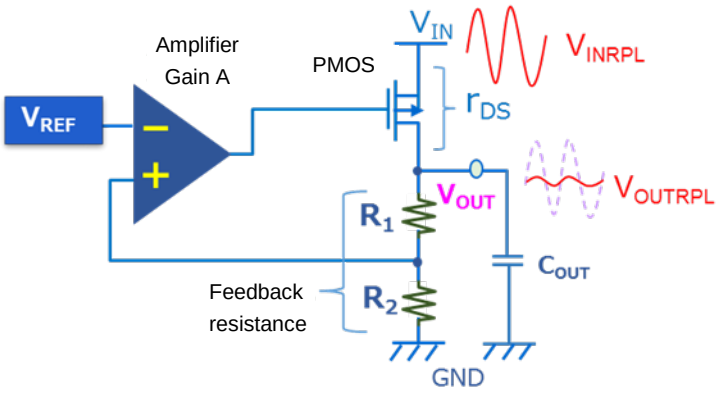


Figure 3.1.1 Circuit diagram of a typical LDO and its PSRR

PSRR definition: $PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{OUT}+r_{DS}}{Z_{OUT}} \quad (dB)$

The LDO has low output impedance (Z_{OUT}) because of negative feedback (Z_{OFB} described later). The gain of the internal amplifier is an important factor to achieve low output impedance. Because the amplifier gain is dependent on frequency, PSRR is also dependent on frequency. The next subsection describes how the PSRR of an LDO is determined.

3.2. Effect of negative feedback on the reduction in an LDO's output impedance

The LDO uses voltage-voltage feedback (series-parallel feedback) to apply the output voltage (V_{OUT}) to the input so as to maintain the regulated output voltage. The added benefit of using negative feedback is reduced output impedance (Z_{OUT}).

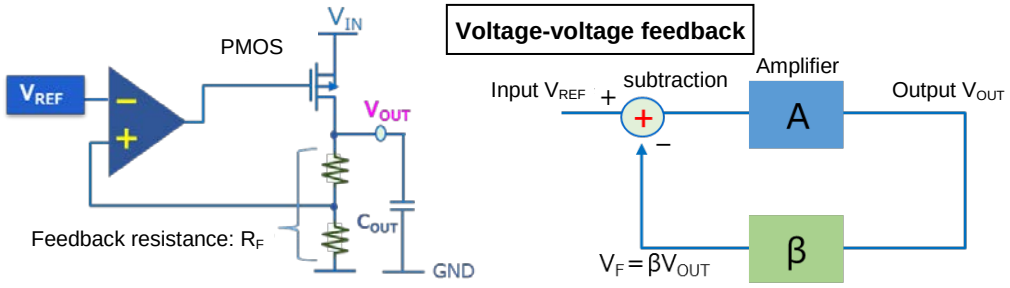


Figure 3.2.1 Circuit diagram of a typical LDO and the negative feedback of the LDO

The output resistance can be calculated by applying a test signal (V_T) to the output, as shown in Figure 3.2.2. The negative feedback reduces the output resistance (R_{OUT}) to roughly 1/Aβ (where A is the gain of the internal amplifier and β is the feedback factor).

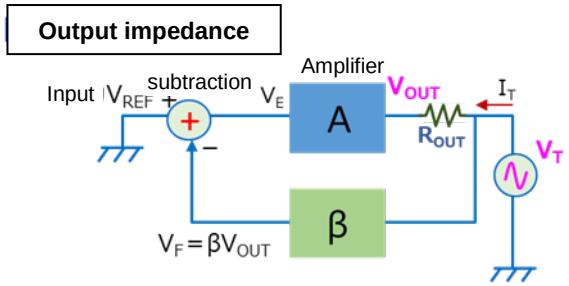


Figure 3.2.2 Calculating the output impedance of an LDO with negative feedback

Output resistance when there is no feedback: R_{OUT}

Error voltage, V_E: $V_E = -\beta V_{OUT} = -\beta V_T$

Output voltage, V_{OUT}: $V_{OUT} = AV_E = -A\beta V_T$

Test current, I_T: $I_T = \frac{(V_T - V_{OUT})}{R_{OUT}} = \frac{(V_T + A\beta V_T)}{R_{OUT}} = \frac{V_T(1+A\beta)}{R_{OUT}}$

Therefore, the output impedance (Z_{OFB}) of an LDO with negative feedback can be calculated as follows:

$$Z_{OFB} = \frac{V_T}{I_T} = \frac{R_{OUT}}{(1+A\beta)}$$

Since the amplifier in typical negative feedback systems has a large gain (A) on the order of 100 dB, the output impedance (Z_{OFB}) is negligibly small—less than a hundred-thousandth of the inherent output impedance (R_{OUT}) of the amplifier. Taking this into account, the PSRR can be calculated as follows:

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{OFB}+r_{DS}}{Z_{OFB}} = 20\log\left(1+\frac{r_{DS}}{Z_{OFB}}\right) \quad (dB)$$

From this equation, it can be seen that an LDO provides high PSRR when the output impedance (Z_{OFB}) is much smaller than the output resistance (r_{DS}) of the PMOS pass device. It should be noted here that the output impedance (Z_{OFB}) in the above equation is a function of the gain of the internal amplifier in an LDO, which is dependent on frequency. The gain decreases in the high-frequency region. Therefore, negative feedback has less effect on the reduction in output impedance in the high-frequency region, causing PSRR to decrease accordingly.
The next subsection discusses the frequency dependence of PSRR.

3.3. Details of the frequency dependence of LDOs

As described above, the PSRR of the LDO is dependent on frequency. Typically, the LDO provides high PSRR in the low-frequency region, which decreases in the high-frequency region as shown in Figure 3.3.1.
The PSRR for an LDO can be broken down into three frequency regions:

- Low-frequency region from DC to a few kHz (hereinafter, low-frequency region)
- High-frequency region from a few kHz to 100 kHz (hereinafter, high-frequency region)
- Ultra-high-frequency region above 100 kHz (hereinafter, ultra-high-frequency region)

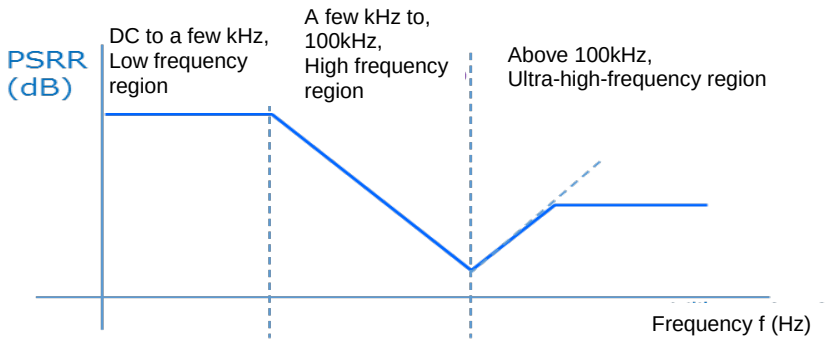


Figure 3.3.1 Typical PSRR curve of an LDO

The following subsections explain why the PSRR is dependent on frequency as shown above.

3.3.1. PSRR in the low-frequency region from DC to Low frequency range

Figure 3.3.2 shows a simplified diagram of an LDO, including an external output capacitor (C_{OUT}).

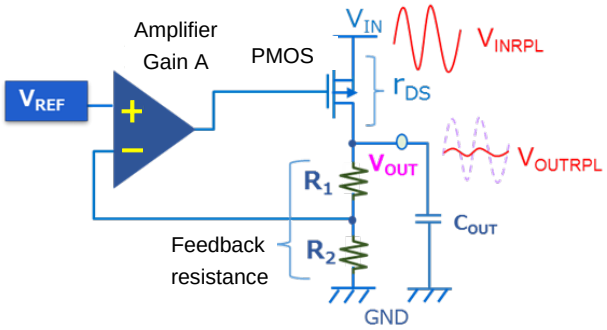


Figure 3.3.2 Simplified diagram of an LDO with an external output capacitor (C_{OUT})

As discussed in Section 3.1, the PSRR in the low-frequency region is the V_{IN} ripple divided by the ratio of the output impedance (Z_{OFB}) of an LDO with negative feedback and the output resistance (r_{DS}) of the PMOS pass device (because the gain of the internal amplifier is constant at low frequency):

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{OFB}+r_{DS}}{Z_{OFB}} \quad (dB)$$

The above equation consists of the following parameters for which low frequency is taken into consideration:

Output impedance of an LDO with negative feedback: $Z_{OFB} = \frac{Z_{OUT}}{(1+A\beta)}$

Output impedance of an LDO without negative feedback: $Z_{OUT} = r_{DS}//Z_{CO}//(R_1+R_2) = r_{DS}//\frac{Z_{CO}(R_1+R_2)}{Z_{CO}+(R_1+R_2)}$

$$\cong r_{DS}//R_1+R_2$$

Impedance of the output capacitor (C_{OUT}), including equivalent series resistance (ESR: R_{ESR}): Z_{CO}

DC gain of the internal amplifier of an LDO: A

Feedback factor of negative feedback: $\frac{R_1}{R_1+R_2}$

The above PSRR equation can be restated as shown below. The feedback resistance value (R_1+R_2) in this equation can be ignored because it is considerably higher than the value of the output resistor for the PMOS pass device (r_{DS}).

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{OFB}+r_{DS}}{Z_{OFB}} = 20\log\frac{\frac{Z_{OUT}}{(1+A\beta)}+r_{DS}}{\frac{Z_{OUT}}{(1+A\beta)}} = 20\log\frac{\frac{r_{DS}//R_1+R_2}{(1+A\beta)}+r_{DS}}{\frac{r_{DS}//R_1+R_2}{(1+A\beta)}} \quad (dB)$$

$$\cong 20\log\frac{\frac{r_{DS}}{(1+A\beta)}+r_{DS}}{\frac{r_{DS}}{(1+A\beta)}} \cong 20\log A\beta$$

This equation indicates that the LDO exhibits very high PSRR in the low-frequency region. Suppose, for example, that the internal amplifier in an LDO has a DC gain of 100 dB and a feedback factor (β) of 0.5. Then, its PSRR is calculated to be roughly 94 dB.

3.3.2. PSRR in the high-frequency region from Low frequency range to roughly 100 kHz

As is the case with the low-frequency region, the PSRR in the high-frequency region is the V_{IN} ripple divided by the ratio of the output impedance (Z_{OFB}) of an LDO with negative feedback and the output resistance (r_{DS}) of the PMOS pass device. In the high-frequency region, the gain of the internal amplifier, which determines the output impedance (Z_{OFB}) of the LDO, is dependent on frequency. Therefore, Z_{OFB} decreases with frequency. In this case, PSRR decreases as the gain decreases, as shown in Figure 3.3.1.
The PSRR in the high-frequency region is described below.

Basically, the PSRR equation for the low-frequency region can be used at frequencies near the boundary between the low- and high-frequency regions. At such frequencies, the output capacitor (C_{OUT}) can be considered to have no effect on PSRR. However, unlike in the low-frequency region, the gain (A) of the internal amplifier is dependent on frequency. When this is taken into consideration, the PSRR in the high-frequency region can be calculated as follows:

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{OFB}+r_{DS}}{Z_{OFB}} \cong 20\log\frac{\frac{r_{DS}}{(1+A\beta)}+r_{DS}}{\frac{r_{DS}}{(1+A\beta)}} \cong 20\log\frac{\frac{1}{(A\beta)}+1}{\frac{1}{(A\beta)}} \Rightarrow 20log\left(1+\frac{A}{1+\frac{s}{p}}\beta\right)$$

where, *p* is the cut-off frequency of the internal amplifier and *s* (=jω) is the Laplacian operator. As can be seen from this equation, PSRR decreases as frequency increases. Next, let's consider the PSRR at a frequency close to the boundary with the ultra-high-frequency region shown in Figure 3.3.1.

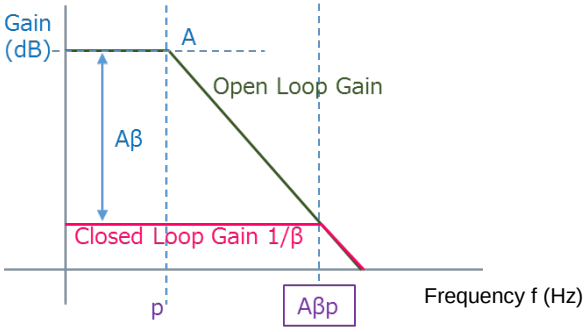


Figure 3.3.3 Relationship between the open-loop and closed-loop gains of an LDO

Figure 3.3.3 shows the relationship between the open-loop and closed-loop gains of an LDO. According to the negative feedback theory, the cut-off frequency of the closed-loop transfer function is Aβ times that of the open-loop transfer function, that is, Aβp. Aβp is considered to be near the boundary with the ultra-high-frequency region. When the frequency of the input voltage ripple is Aβp Hz, the PSRR of an LDO can be calculated as follows:

$$PSRR|_{s=A\beta p} = 20log(1+\frac{A\beta}{1+\frac{A\beta p}{p}}) = 20log(1+\frac{A\beta}{1+A\beta}) \cong 20\log(\frac{A\beta}{A\beta}+1) = 20log(1+1) = 6dB$$

3.3.3. PSRR in the ultra-high-frequency region above roughly 100 kHz

In the ultra-high-frequency region shown in Figure 3.3.1, the impedance (Z_{CO}) of the output capacitor (C_{OUT}) including the equivalent series resistance (ESR: R_{ESR}) is dominant. Therefore, PSRR can be calculated as follows:

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{CO}+r_{DS}}{Z_{CO}} = 20\log\frac{\frac{1}{sC_{OUT}}+R_{ESR}+r_{DS}}{\frac{1}{sC_{OUT}}+R_{ESR}} \quad (dB)$$

In the frequency region in which the capacitive impedance of the output capacitor (C_{OUT}) is larger than its equivalent series resistance (R_{ESR}), PSRR can be calculated as follows:

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{CO}+r_{DS}}{Z_{CO}} = 20\log\frac{\frac{1}{sC_{OUT}}+r_{DS}}{\frac{1}{sC_{OUT}}} = 20\log\left(1+sC_{OUT}r_{DS}\right) \quad (dB)$$

When the frequency exceeds the point at which the capacitive impedance of the output capacitor (C_{OUT}) becomes zero, PSRR is dominated by its equivalent series resistance (R_{ESR}). Therefore, PSRR does not exhibit any dependency on frequency.

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{CO}+r_{DS}}{Z_{CO}} = 20\log\frac{R_{ESR}+r_{DS}}{R_{ESR}} \quad (dB)$$

Figure 3.3.4 shows the PSRR-vs-frequency curve over the frequency regions described above.

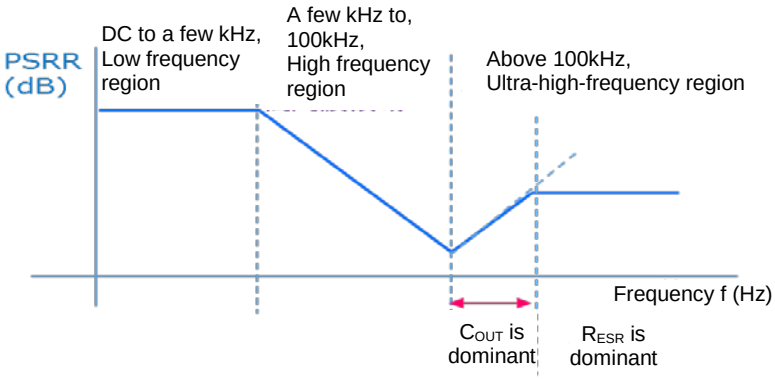


Figure 3.3.4 Frequency ranges in which the output capacitor (C_{OUT}) and equivalent series resistance (R_{ESR}) are dominant in the ultra-high-frequency region

As described above, PSRR is dependent on frequency.

3.3.4. Effect of the output capacitor (C_{OUT}) on PSRR in the high- and ultra-high-frequency regions

At low frequencies, the output capacitor (C_{OUT}) works as a pure capacitor since its impedance is a function of capacitance alone and changes with frequency. However, when frequency reaches a certain point, the impedance of C_{OUT} diminishes to almost zero and the equivalent series resistance (R_{ESR}) becomes dominant. At frequencies close to the boundary between high- and ultra-high-frequency regions, the impedance of C_{OUT} is dominant. First, let's consider how the capacitance of C_{OUT} affects PSRR at such frequencies.

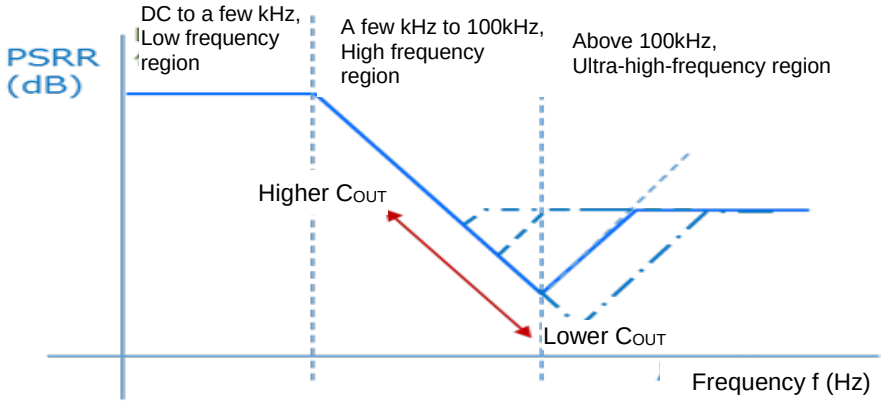


Figure 3.3.5 Effect of capacitive impedance on PSRR at frequencies near the boundary between high- and ultra-high-frequency regions

The following is the equation for PSRR in the frequency region in which the capacitive impedance is dominant.

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{\frac{1}{sC_{OUT}}+r_{DS}}{\frac{1}{sC_{OUT}}} = 20\log\left(1+sC_{OUT}r_{DS}\right) \quad (dB)$$

This equation indicates that a larger output capacitor (C_{OUT}) provides higher PSRR. As shown in Figure 3.3.5, PSRR decreases in the high-frequency region. A larger capacitor (C_{OUT}) causes PSRR to increase again at relatively lower frequency because it provides lower capacitive impedance (i.e., larger C_{OUT}). Therefore, a large output capacitor helps maintain high PSRR at high frequency. In contrast, when the output capacitor (C_{OUT}) is small, PSRR continues to decline up to a relatively high frequency. (The assumption is that the equivalent series resistance (R_{ESR}) is constant.)

Next, let's consider the effect of the equivalent series resistance (R_{ESR}).

Figure 3.3.6 shows the effect of the equivalent series resistance (R_{ESR}) in the ultra-high-frequency region.

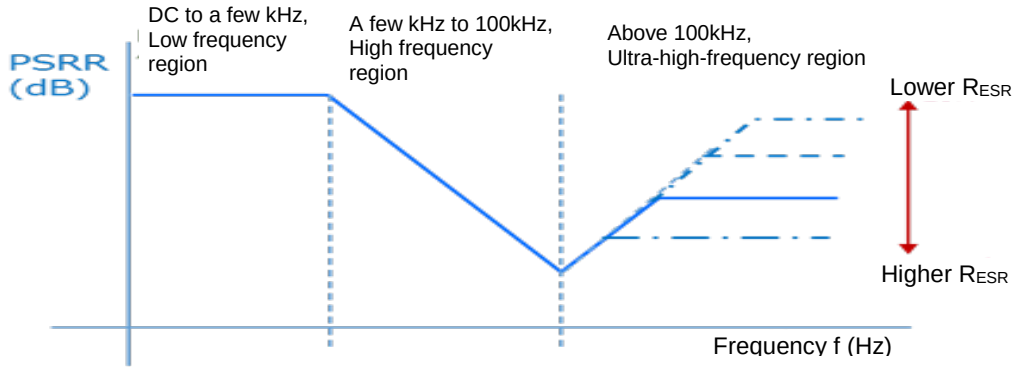


Figure 3.3.6 Effect of the equivalent series resistance (R_{ESR}) in the ultra-high-frequency region

Let's look at the PSRR equation again when the capacitive impedance of the output capacitor (C_{OUT}) becomes zero at high frequency:

$$PSRR = 20\log\frac{V_{INRPL}}{V_{OUTRPL}} = 20\log\frac{Z_{CO}+r_{DS}}{Z_{CO}} = 20\log\frac{R_{ESR}+r_{DS}}{R_{ESR}} = 20\log\left(1+\frac{r_{DS}}{R_{ESR}}\right) \quad (dB)$$

As indicated by this equation, in the ultra-high-frequency region, an output capacitor (C_{OUT}) with lower equivalent series resistance (R_{ESR}) provides higher PSRR. This is illustrated in Figure 3.3.6. (The assumption is that the output capacitance (C_{OUT}) is constant.)

Therefore, to increase the PSRR, it is beneficial to use an output capacitor (C_{OUT}) with maximal capacitance and small equivalent series resistance (R_{ESR}). However, a large output capacitor (C_{OUT}) causes an increase in inrush current during the rise of an LDO's output voltage (V_{OUT}) or even oscillation in the worst case. Also, an output capacitor with small equivalent series resistance (R_{ESR}) does not provide sufficient immunity to oscillation.

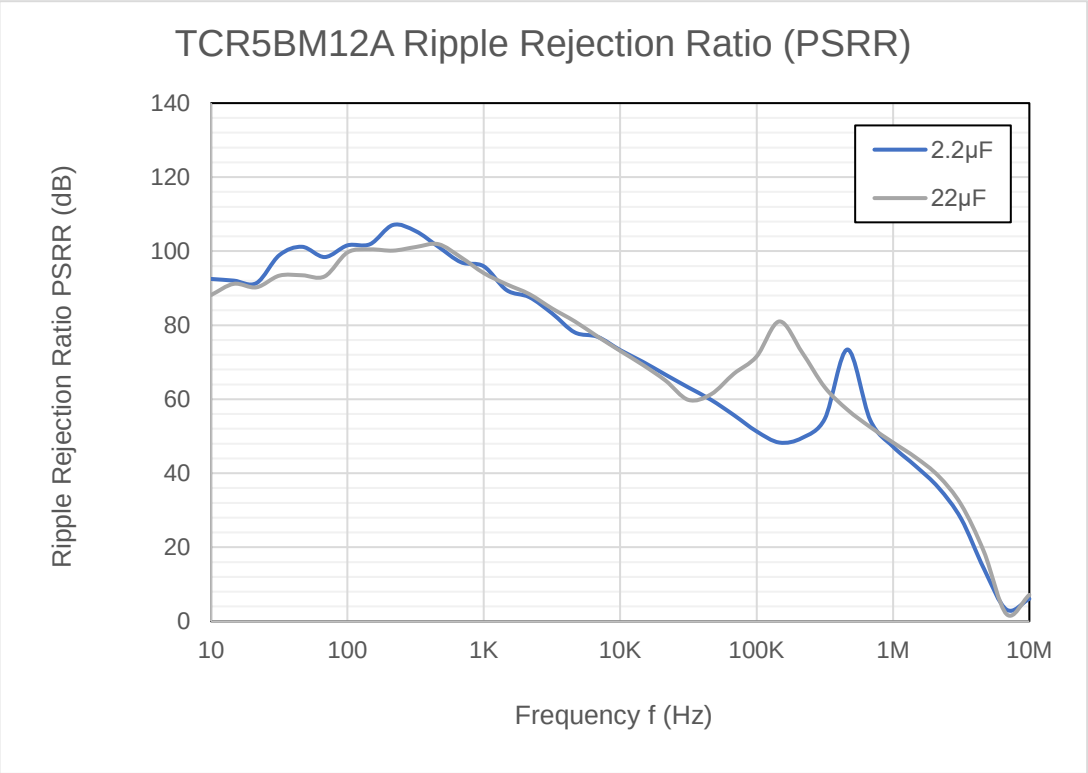
Figure 3.3.5 and Figure 3.3.6 are simplified to explain the theory of operation. In reality, the frequency dependency of PSRR exhibits a complicated waveform in the ultra-high-frequency region above roughly 100 kHz because of the effects of parasitic inductance and reactance present in and outside an LDO.

4. Outstanding PSRR characteristics of dual-power-supply LDOs

The following shows the PSRR curves of the TCR5BM12A, Toshiba's typical 500-mA LDO of the TCR5BM series.

The TCR5BM12A features high PSRR (specified as a ripple rejection ratio (R.R.) in the datasheet). A 22-µF output capacitor (C_{OUT}) provides higher PSRR than a 2.2-µF capacitor. With a 22-µF output capacitor, PSRR begins to turn upward at a low frequency of around 100 kHz as shown below.

TCR5BM12A test conditions: V_{IN} = 1.35 V, V_{BIAS} = 3.3 V, C_{IN} = open, C_{OUT} = 2.2/22 µF, I_{OUT} = 10 mA
Capacitor used: Murata



5. Conclusion

Nowadays, a high PSRR is required even at high frequency. PSRR is one of the important factors in selecting LDOs. To increase the PSRR, it is effective to use an output capacitor (C_{OUT}) with maximal capacitance and low equivalent series resistance (R_{ESR}). However, inrush current and oscillation should also be taken into consideration when selecting LDOs. LDOs with high PSRR are preferred, but such LDOs are more susceptible to oscillation and draw higher supply current because the internal amplifier has a high DC gain and good frequency response.
Toshiba's LDOs are very easy to use because they are optimized in terms of a trade-off between the PSRR and other characteristics.

Toshiba's LDOs with high PSRR:

To download the data sheet: TCR5BM 500-mA fixed-output LDO regulator → Click Here

To download the data sheet: TCR8BM 800-mA fixed-output LDO regulator → Click Here

To download the data sheet: TCR13AGADJ 1.3-A adjustable-output LDO regulator → Click Here

To download the data sheet: TCR15AG series 1.5-A fixed- and adjustable-output LDO regulators → Click Here

To download the reference design: TCR15AG series adjustable-output LDOs→ Click Here

For more information on the usage of LDO regulators, see the Application Note for Low Drop Out (LDO) regulator IC.
To download the Application Note for Low Drop-Out (LDO) Regulator IC → Click Here

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