

Oscillation Principles and Improvement of Oscillation Resistance of LDO

Outline:

This application note discusses how circuits with negative feedback such as low-dropout (LDO) regulators and operational amplifiers go into oscillation and how oscillation can be suppressed by means of phase compensation. This application note describes not only the effect of phase compensation on fixed-output LDOs whose output voltage is internally determined but also the effect of an external phase compensation capacitor (C_{FB}) on reducing the oscillation susceptibility of adjustable-output LDOs whose output voltage is programmable via external resistors. It provides information about how to obtain the best performance from LDOs while maintaining the regulated output voltage in system applications.

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1. Introduction

Various semiconductor (electronic) devices are used to enhance the performance and functionality of increasingly sophisticated mobile devices and other electronic devices.

Recent semiconductor devices operate at very high frequencies to achieve high performance. To realize such high performance, ICs generally incorporate an amplifier with a high gain so as to maintain its frequency response over a wide range of frequencies. However, if these high-performance semiconductor devices have negative feedback, periodic AC voltage variations might be superimposed on the output signal, causing electronic devices to fail. This phenomenon called oscillation produces AC voltage that cannot be controlled by an LDO.

Basically, LDOs and op-amps are designed not to produce an oscillation. However, phase compensation might be required for system applications if you need to further reduce the susceptibility of some adjustable-output LDOs to oscillation or to use op-amps that do not incorporate a phase compensation circuit.

It should be noted that even phase-compensated LDOs and op-amps might oscillate owing to the common impedance of power supply and GND lines as well as the capacitance of PCB traces. This application note describes the mechanism of oscillation and several circuit techniques for preventing oscillation. This information will help you obtain the maximum performance from LDOs while maintaining their regulated output voltage in system applications.

2. LDO oscillation and its impact

Figure 2.1.1 shows the concept of oscillation of an LDO.

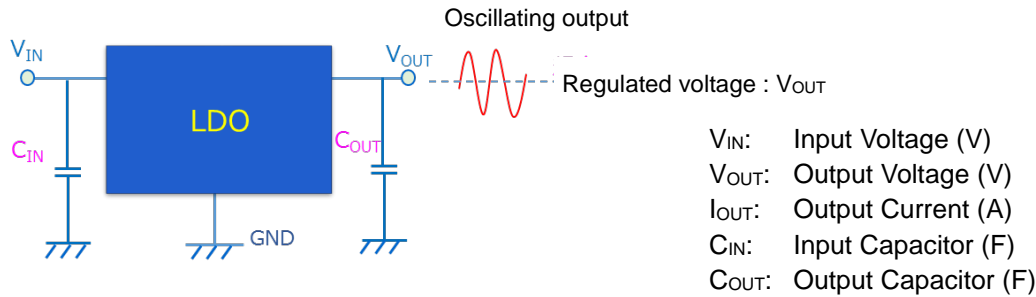


Figure 2.1.1 Image of LDO oscillation

In Figure 2.1.1, the output (V_{OUT}) is oscillating.

An LDO is designed to provide a regulated DC output voltage. However, in the event of oscillation, unwanted AC voltage is superimposed on the DC output voltage as shown in Figure 2.1.1. Although Toshiba's LDOs are designed not to oscillate under the specified operating conditions, they might go into oscillation, for example, when you use an output capacitor (C_{OUT}) smaller than the recommended value. If oscillation occurs, semiconductor devices supplied by an LDO might malfunction. If the oscillating output contains a high-frequency AC component, the resulting electromagnetic interference (EMI) might induce noise in neighboring devices or even across a board, causing them to malfunction. It is therefore crucial to prevent LDO oscillation.

Section 3 first describes negative feedback used in LDOs and op-amps, and Section 4 discusses why LDOs oscillate.

3. Negative feedback theory

3.1. What is negative feedback?—Advantages of negative feedback

Figure 3.1.1 shows the concept of negative feedback and a simplified diagram of an LDO that uses negative feedback.

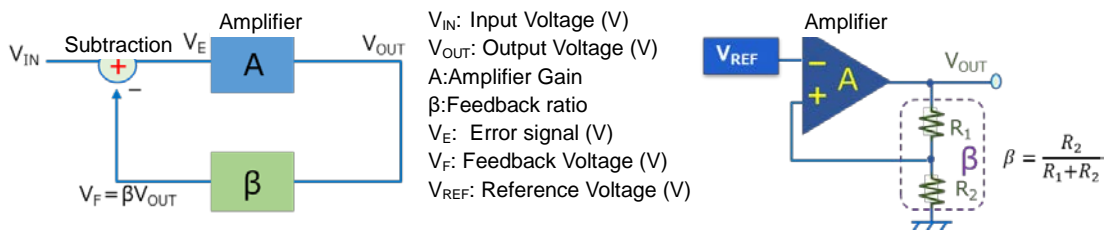


Figure 3.1.1 Concept of negative feedback and a simplified diagram of an LDO

As shown in Figure 3.1.1, negative feedback is a circuit system that returns the output (V_{OUT}) to the input with a feedback ratio β and subtracts it from the input V_{IN} . Therefore, the voltage of the error signal applied to an amplifier is lower than V_{IN} .

$$V_E = V_{IN} - V_F = V_{IN} - \beta V_{OUT}$$

Without negative feedback, the output voltage (V_{OUT}) is equal to AV_{IN} . However, negative feedback causes V_{OUT} to become lower than AV_{IN} , as expressed by the following equation:

$$V_{OUT} = AV_E = A(V_{IN} - \beta V_{OUT}) \quad \dots (1)$$

Why do we need to reduce the output voltage? In fact, negative feedback provides more advantages than the disadvantage of reduced output voltage such as:

- Gain stability
- Reduction in distortion
- Increase in frequency response
- Suppression of external disturbance
- Ability to modulate input and output impedances

There are four types of negative feedback, which have different characteristics as summarized in the table below:

- Voltage-voltage feedback (series-parallel feedback)
- Current-voltage feedback (series-series feedback)
- Voltage-current feedback (parallel-parallel feedback)
- Current-current feedback (parallel-series feedback)

Table 3.1.1 Four types of negative feedback

Type	Feedback type	Input and output impedance modulation	Characteristic to be stabilized
Voltage-voltage feedback (series-parallel feedback)	Return the output voltage as a voltage to the input.	Input impedance $A\beta$ times at No feedback	Output Voltage (V_{OUT}/V_{IN})
		Output impedance $1/A\beta$ times at No feedback	
Current-voltage feedback (series-series feedback)	Return the output current as a voltage to the input	Input impedance $A\beta$ times at No feedback	Output Current (I_{OUT}/V_{IN})
		Output impedance $A\beta$ times at No feedback	
Voltage-current feedback (parallel-parallel feedback)	Return the output voltage as current to the input	Input impedance $1/A\beta$ times at No feedback	Output Voltage (V_{OUT}/I_{IN})
		Output impedance $1/A\beta$ times at No feedback	
Current-current feedback (parallel-series feedback)	Return the output current as current to the input	Input impedance $1/A\beta$ times at No feedback	Output Current (I_{OUT}/I_{IN})
		Output impedance $A\beta$ times at No feedback	

LDOs use voltage-voltage feedback.

When the internal regulator circuit is regarded as a negative-feedback amplifier, an LDO can be considered to be an amplification system that generates a regulated output voltage from a reference input voltage (V_{REF}). Therefore, voltage-voltage feedback is the best type of feedback for LDOs. One of the advantages of voltage-voltage feedback is that it helps stabilize system output voltage even in the presence of load variations because voltage-voltage feedback reduces the output impedance of the LDO regulator circuit to one- $A\beta$ th, compared to the no-feedback condition. In addition, voltage-voltage feedback increases its input impedance by $A\beta$ times, compared to the no-feedback condition. Therefore, the internal reference voltage (V_{REF}) generator circuit does not need a high current drive capability to drive a differential amplifier at the input of the regulator circuit and can therefore be designed with a low supply current. Thus, voltage-voltage feedback is the optimal type of negative feedback for LDOs.

The next section discusses the mechanism of oscillation of a voltage-voltage feedback system.

3.2 Closed- and loop gains of a negative feedback system

This subsection describes the basic concept of negative feedback.

Equation 1 shown in Section 3.1 can be rewritten as:

$$\begin{aligned} V_{OUT} &= A(V_{IN} - \beta V_{OUT}) \\ &= AV_{IN} - A\beta V_{OUT} \\ V_{OUT} + A\beta V_{OUT} &= AV_{IN} \\ (1 + A\beta)V_{OUT} &= AV_{IN} \end{aligned}$$

Hence, the gain of a negative feedback system (closed-loop gain), $A_{CL} = V_{OUT} / V_{IN}$, can be expressed as shown below.

$A\beta$ in this equation is called a loop gain, which is extremely important for the analysis of oscillation.

$$A_{CL} = \frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} = \frac{1}{\frac{1}{A} + \beta}$$

Suppose that the amplifier shown in Figure 3.1.1 has a large gain (A). Then, the closed-loop gain (A_{CL}) of a negative feedback system can be approximated as follows:

$$A_{CL} = \frac{1}{\frac{1}{A} + \beta} \cong \frac{1}{\beta}$$

This equation indicates that if the amplifier has a large gain (A), the closed-loop gain (A_{CL}) is determined only by feedback ratio β independently of the internal amplifier. In the case of the negative feedback system shown in Figure 3.1.1, the feedback ratio (β) is determined only by the ratio of the values of R_1 and R_2 , i.e., passive resistors. In this case, changes in the gain (A) of the amplifier have no effect on the feedback factor, making it possible to stabilize the gain. However, the gain (A) of the amplifier in a negative feedback system is normally dependent on frequency. For example, if it has a first-order characteristic, its frequency response looks like Figure 3.1.2. ($1/\beta$ shown in this figure represents the closed-loop gain (A_{CL}) of the negative feedback system.) In this case, because the gain (A) of the amplifier decreases with frequency as shown in Figure 3.1.2, the closed-loop gain (A_{CL}) becomes less stable as frequency increases. At a frequency of f_c , the closed-loop gain (A_{CL}) is equal to the gain of the amplifier.

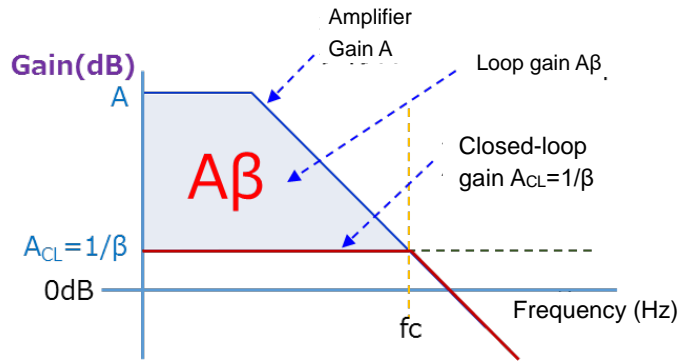


Figure 3.1.2 Relationship of the gain (A) of the amplifier in a negative feedback system and its closed-loop gain (A_{CL})

From Figure 3.1.2, it can be seen that the loop gain ($A\beta$) is equal to the difference between the amplifier's gain (A) and the closed-loop gain ($A_{CL} = 1/\beta$), i.e., the area surrounded by the amplifier's gain (A) and the closed-loop gain ($1/\beta$).

4. Mechanism of oscillation of an LDO (negative feedback system)

4.1. Mechanism of LDO oscillation

Why do negative feedback systems such as LDOs oscillate?
Take another look at the typical equation for a closed-loop gain.

$$A_{CL} = \frac{A}{1+A\beta} \cong \frac{1}{\beta}$$

When the loop gain ($A\beta$) is -1, the denominator of this equation becomes zero. This makes the closed-loop gain (A_{CL}) infinite, which means that the negative feedback system provides an output even when there is no input. This is the oscillating state. Then, can the loop gain ($A\beta$) take a value of -1?

In the discussion of Figure 3.1.2, we assumed that the loop gain ($A\beta$) of the amplifier in the negative feedback system has a first-order characteristic in the frequency range in which $A\beta > 0$ dB (i.e., $A\beta$ is greater than 1). Figure 4.1.1 shows the frequency response of such a negative feedback system, including a phase plot.

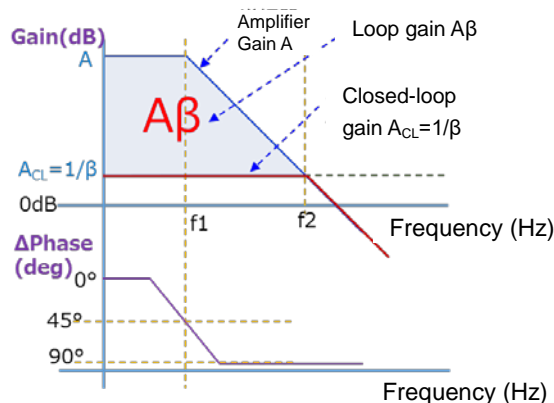


Figure 4.1.1 Frequency response of a negative feedback system with an amplifier having a first-

order characteristic

In the case of this negative feedback system, the loop gain phase is 45° at frequency f1 (called a pole) at which the gain drops by 3 dB and then eventually shifts by 90°. Also, the loop gain (Aβ) decreases at a rate of -20 dB/dec at frequencies above the pole (f1) and reaches the 0-dB line (i.e., 1) at a frequency of f2. In the case of an amplifier having a first-order characteristic, its loop gain phase shifts by only 90° even when the loop gain (Aβ) is at the 0-dB point (i.e., 1), which means that it never goes into oscillation (i.e., the loop gain does not become negative). In contrast, Figure 4.1.2 shows the Bode plot of a negative feedback system when its internal amplifier has a second-order characteristic in the frequency range in which the loop gain (Aβ) > 0 dB (i.e., 1).

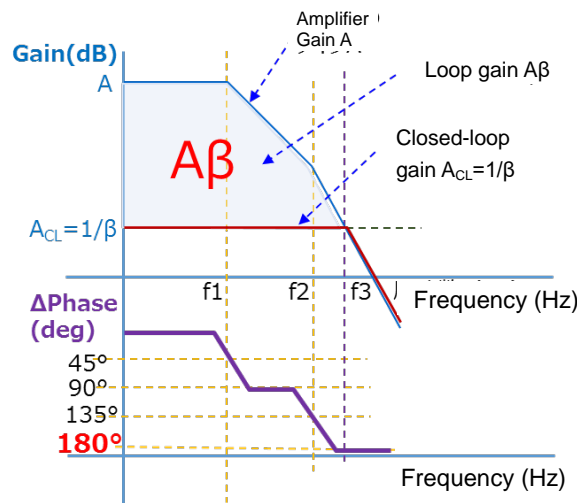


Figure 4.1.2 Frequency response of a negative feedback system with an amplifier having a second-order characteristic

As can be seen from Figure 4.1.2, when the amplifier has a second-order characteristic in the frequency range in which the loop gain (Aβ) > 0 dB (i.e., 1), the loop gain (Aβ) phase might eventually shift by 180° in that frequency range, or in other words, become inverted. This is equivalent to multiplying Aβ by -1, and at a frequency of f3, the loop gain (Aβ) reaches the 0-dB point (i.e., 1). Therefore, when the amplifier has a second- or higher-order characteristic in the frequency range in which the loop gain (Aβ) > 0 dB (i.e., 1), Aβ might take a value of -1. In that case, the closed-loop gain (A_{CL}) becomes infinite as shown below, causing a negative feedback system to go into oscillation.

$$A_{CL} = \frac{A}{1+A\beta} = \frac{A}{1-1} = \infty$$

At frequencies above the second pole (f2), the amplifier gain decreases at a rate of -40 dB/dec.

As described above, each pole introduces a 45° shift in the loop gain (Aβ) phase, resulting in a

90° shift eventually. Poles always occur at circuit nodes with resistive and capacitive components. When the amplifier in a negative feedback system has a first-order characteristic in the frequency range in which its loop gain ($A\beta$) > 0 dB (i.e., 1), the amplifier can be considered to have a single-stage configuration as shown in Figure 4.1.3. From the viewpoint of oscillation, the amplifier should desirably have a first-order characteristic (single-stage configuration) with a single pole. However, in order for an LDO to obtain good DC and AC characteristics, it is required to increase the gain of an internal amplifier and extend its frequency response as described above. For this purpose, it is necessary to configure a two-stage (or multiple-stage) amplifier as shown in Figure 4.1.4 and implement a countermeasure for reducing supply current. An amplifier with a two-stage configuration exhibits at least two poles in the frequency range in which the loop gain ($A\beta$) > 0 dB (i.e., 1), which means that the negative feedback system has a frequency response like the one shown in Figure 4.1.2, making it susceptible to oscillation. In this case, some circuit technique must be used to avoid oscillation. Section 5 and Section 6 describe a technique called phase compensation.

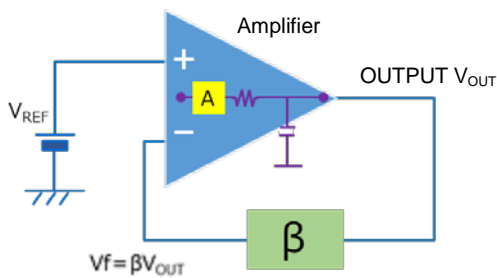


Figure 4.1.3 LDO with a first-order characteristic

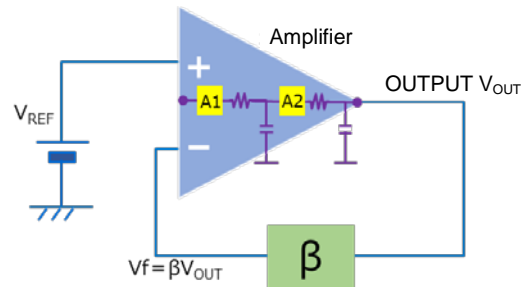


Figure 4.1.4 LDO with a second-order characteristic

4.2. Phase margin and gain margin

As described in the previous subsection, if the amplifier in a negative feedback system has a second- or higher-order characteristic in the frequency range in which $A\beta > 0$ dB (i.e., 1), it goes into oscillation when its loop gain ($A\beta$) becomes -1. In contrast, if the amplifier has a first-order characteristic, the negative feedback system does not oscillate even when its loop gain ($A\beta$) becomes -1 because the loop gain phase shifts only by 90°. Phase margin and gain margin are the measures of the stability of a closed-loop system in relation to oscillation. Phase margin and gain margin are defined as follows:

- Phase margin: Difference between the phase and 180° at a frequency that provides a loop gain ($A\beta$) of 0 dB
- Gain margin: Difference between the gain and 0 dB at a frequency at which the phase of the loop gain ($A\beta$) has shifted by 180°

Generally, the following phase and gain margins are desired so as to ensure system stability against oscillation.

- Phase margin: 60° or higher
- Gain margin: 6 dB or higher

Figure 4.2 shows the concepts of phase and gain margins.

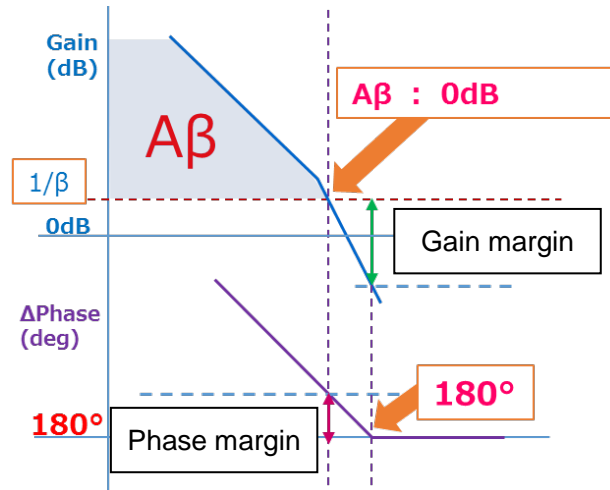


Figure 4.2 Concepts of phase and gain margins

5. LDO phase compensation: Oscillation suppression

5.1. Circuit techniques for phase compensation used inside an LDO

5.1.1. Miller compensation

For example, In the event that an LDO fails because a negative feedback system goes into oscillation as discussed in Section 4, electronic devices supplied from the LDO also fail, causing the entire system to fail. Therefore, it must be ensured that the LDO does not oscillate under any conditions. Although it is necessary to increase the number of amplifier stages in an LDO to obtain good electrical characteristics, this makes the LDO more susceptible to oscillation. Section 5 describes a technique for preventing LDO oscillation called phase compensation. Phase compensation prevents a 180° shift (i.e., inversion) of the loop gain ($A\beta$) phase at the 0-dB point as shown in Figure 4.1.2. The mostly commonly used phase compensation technique is called Miller compensation. In the case of a two-stage LDO, Miller compensation deliberately degrades an amplifier's frequency response by adding a phase compensation capacitor (C_C) between the input and output of the LDO's output stage (i.e., an inverting amplifier) as shown in Figure 5.1.2 so that the output of the input differential amplifier has a large capacitance of $A_2 \cdot C_C$ (phase compensation capacitance multiplied by the output-stage gain). Without phase compensation, the two-stage LDO has two poles at f_1 and f_2 in the frequency range in which the loop gain ($A\beta$) is equal to or greater than 0 dB (i.e., 1). Phase compensation causes the LDO to exhibit only one pole at f_1' . This is equivalent to an amplifier with a first-order characteristic whose $A\beta$ phase shifts only by 90° at frequency f_3 at which the loop gain ($A\beta$) is 0 dB (i.e., 1), and therefore prevents oscillation. As can be seen from Figure 5.1.3, phase compensation causes the poles f_1 and f_2 to shift away from each other to f_1' and f_2' . This effect is called pole splitting, which helps improve LDO stability by increasing the frequency at which the phase shift reaches 180°.

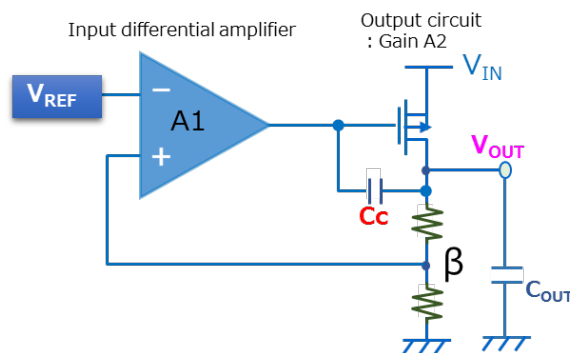


Figure 5.1.2 Commonly used Miller compensation technique

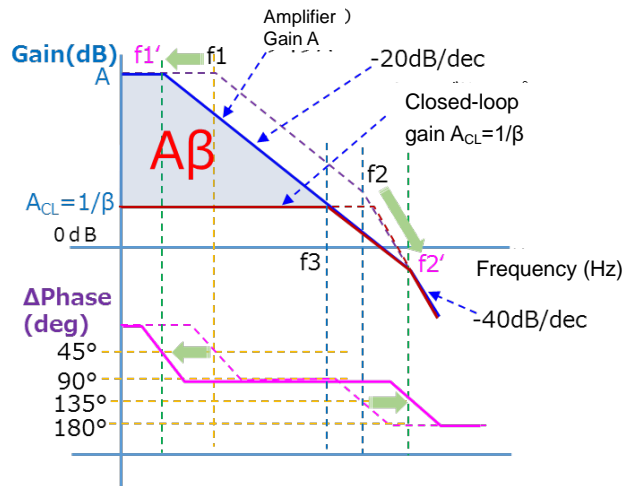


Figure 5.1.3 Effect of Miller compensation (pole splitting)

Figure 5.1.3 indicates that an LDO is likely to oscillate if there is a frequency range in which the gain decreases at a rate of -40 dB/dec before the loop gain ($A\beta$) reaches the 0-dB point whereas it does not oscillate if the gain decreases only at a rate of -20 dB/dec. It is necessary to consider oscillation in this way for phase compensation using C_{FB} for an adjustable-output LDO. It should be noted here that Miller compensation prevents oscillation by means of pole splitting but introduces a different type of instability called right-half-plane (RHP) zero (i.e., a zero on the right-half plane of the s-plane) in some designs. The LDO might oscillate if a zero lies in the low-frequency region. The next subsection describes how to avoid an RHP zero.

5.1.2. Lag-lead phase compensation for preventing oscillation due to an RHP zero

Although Miller compensation is effective in stabilizing a negative feedback system, it produces an RHP zero in the low-frequency region in some designs, which might cause the negative feedback system to oscillate. Suppose, for example, that an RHP zero occurs at frequency f_z as shown in Figure 5.1.4. Then, the loop gain ($A\beta$) does not decrease at frequencies above f_z whereas the phase shift continues until it reaches 180°. Despite pole splitting using Miller compensation, the LDO goes into oscillation at frequency f_4 because the loop gain ($A\beta$) phase becomes inverted before $A\beta$ reaches the 0-dB point.

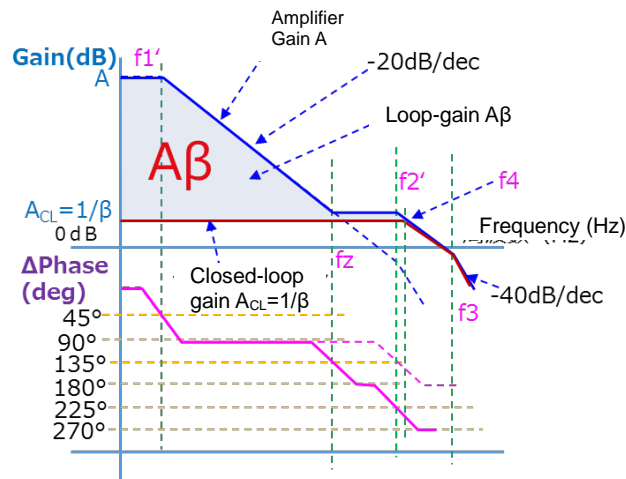


Figure 5.1.4 Frequency response in the event of an RHP zero being introduced by Miller compensation

A solution for this problem is to add a resistor (R_C) in series with the Miller compensation capacitor (C_C) as shown in Figure 5.1.5. This phase compensation technique called Lag-Lead phase compensation effectively nullifies the RHP zero.

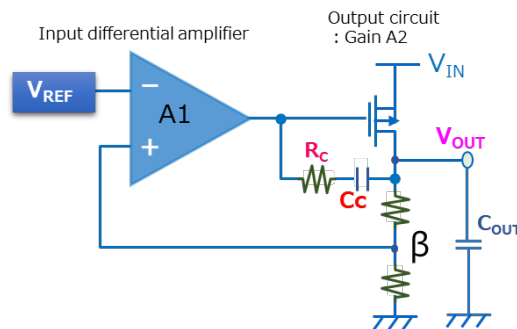


Figure 5.1.5 LDO with Lag-Lead phase compensation

Theoretically, an RHP zero is calculated as follows when a series resistor (R_C) is added. (g_{m2} is the transconductance of the PMOS pass device.)

$$f_z = \frac{1}{2\pi C_C \times \left(\frac{1}{g_{m2}} - R_C \right)}$$

Setting the value of the series resistor (R_C) as follows causes the RHP zero frequency due to Miller compensation to become infinite, effectively nullifying the RHP zero. This is equivalent to an LDO with a first-order characteristic, stabilizing a negative feedback system.

$$\frac{1}{g_{m2}} = R_C$$

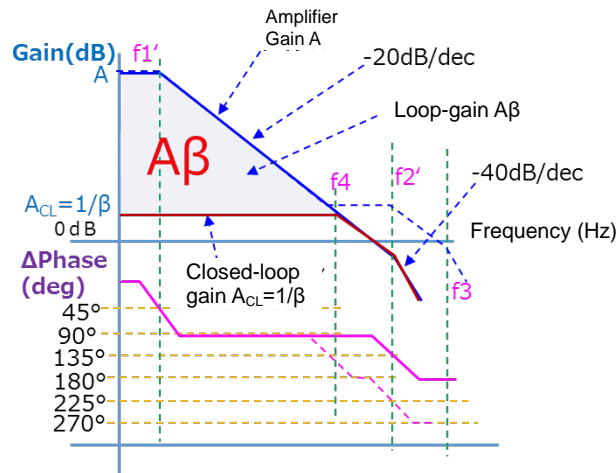


Figure 5.1.6 Frequency response of an LDO when an RHP zero is nullified by means of Lag-Lead compensation

5.1.3 Phase compensation for an LDO with a large external output capacitor: Adding a zero

As described in the previous subsections, both the Miller and Lag-Lead compensation techniques considerably reduce an LDO's susceptibility to oscillation. However, an LDO requires a large output capacitor (C_{OUT}) to obtain a good load transient response and thereby maintain a regulated output voltage. Even if a Miller-compensated LDO exhibits only one pole in the frequency range before $A\beta$ reaches the 0-dB point, adding a large output capacitor (C_{OUT}) shifts the pole toward a low frequency (f_0) as shown in Figure 5.1.7, creating a second-order characteristic. This condition increases the likelihood of LDO oscillation.

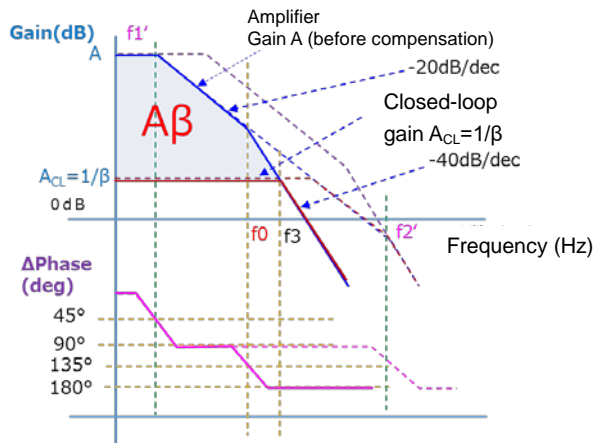


Figure 5.1.7 Change in the phase of the loop gain ($A\beta$) due to a large output capacitor (C_{OUT}) added to the Miller-compensated LDO

In this state, the loop gain ($A\beta$) phase shifts by 180° at frequency f_3 at which $A\beta$ reaches the 0-dB point, causing an LDO to go into oscillation. In order to prevent oscillation, it is necessary to 1) reduce the number of poles to one or 2) reduce the rate of fall of the loop gain ($A\beta$) to -20 dB/dec. The latter technique is commonly employed. Figure 5.1.8 shows the resulting phase-vs-frequency characteristics.

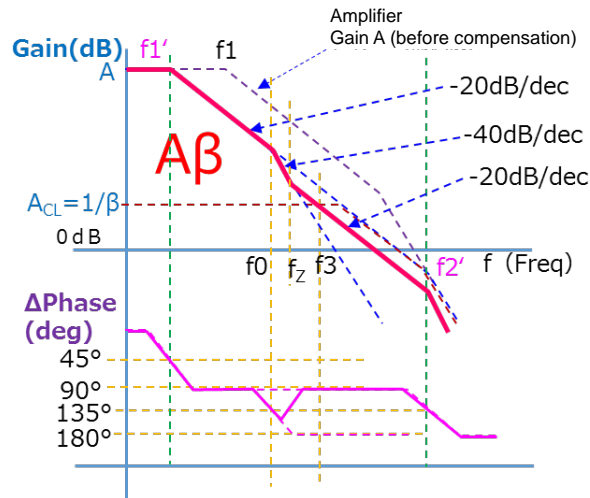


Figure 5.1.8 Phase compensation for the pole at f_0 introduced by a large output capacitor (C_{OUT})

As shown in Figure 5.1.8, a zero is added at f_z , at which the rate of fall of the loop gain ($A\beta$) changes from -40 dB/dec back to -20 dB/dec, bringing the phase shift back to 90°.

Consequently, the phase does not shift by 180° before the loop gain ($A\beta$) reaches the 0-dB point. This prevents LDO oscillation. The Lag-Lead compensation technique shown in Figure 5.1.5 can be used to introduce a zero at f_z .

The following equation represents a zero introduced by Lag-Lead compensation.

$$f_z = \frac{1}{2\pi C_C \times \left(\frac{1}{g_{m2}} - R_C \right)}$$

Suppose that the following relationship is true:

$$\frac{1}{g_{m2}} < R_C$$

Then, it is possible to introduce a zero at f_z while transforming the RHP zero due to Miller compensation discussed in Section 5.1.2 into a left-half-plane (LHP) zero.

This phase compensation transforms the easily oscillatable condition shown in Figure 5.1.7 into a stable condition shown in Figure 5.1.8.

The Miller and Lag-Lead compensation techniques discussed in this subsection are used for the internal circuit of an LDO to stabilize a negative feedback system. The next subsection describes a phase compensation technique used outside an LDO.

5.2. Phase compensation technique used outside an LDO

5.2.1 Introducing a zero at fz using the equivalent series resistance (RESR) of an output capacitor

Figure 5.2.1 shows a simplified diagram of an LDO with an output capacitor (COUT) having equivalent series resistance (ESR).

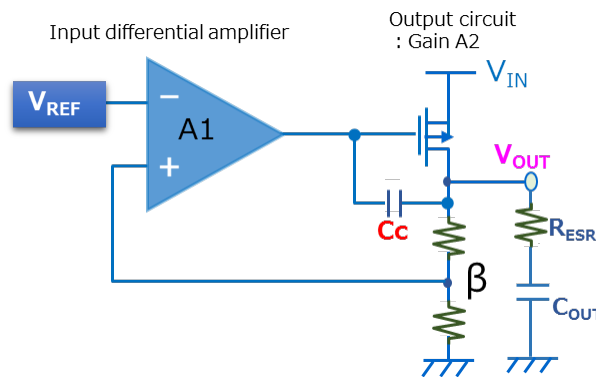


Figure 5.2.1 Simplified diagram of an LDO with an output capacitor (COUT) having equivalent series resistance (RESR)

As described above, when a large output capacitor (COUT) is connected to an LDO, it is necessary to add a zero for phase compensation in some way so as to prevent LDO oscillation. Section 5.1 discussed the Miller and Lag-Lead compensation techniques for use in an LDO. Alternatively, a zero can be added by using the equivalent series resistance (RESR) of an external output capacitor (COUT).

A zero is introduced by the equivalent series resistance (RESR) at the following frequency:

$$f_Z = \frac{1}{2\pi C_{OUT} \times R_{ESR}}$$

Therefore, a zero can be introduced at a desired frequency (fz) within the frequency range in which the loop gain (Aβ) > 0 dB (i.e., 1) by selecting an output capacitor (COUT) with appropriate equivalent series resistance (RESR). Adding a zero transforms the easily oscillatable condition shown in Figure 5.1.7 into a stable condition shown in Figure 5.1.8. Care should be taken, however, because an output capacitor (COUT) with a large equivalent series resistance (RESR) might degrade the load transient response and other AC characteristics of an LDO. To introduce a zero using the equivalent series resistance (RESR) of an output capacitor (COUT), a trade-off with AC characteristics should be considered.

6. External phase compensation capacitor for an adjustable-output LDO: Effect of C_{FB}

Adjustable-output LDOs allow the output voltage to be programmed via external resistors. (Figure 6.1.1)

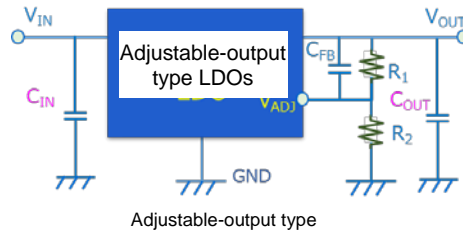


Figure 6.1.1 Adjustable-output LDO

Toshiba’s adjustable-output LDOs are designed to operate stably without connecting a phase compensation capacitor (C_{FB}) in parallel with the external resistor (R_1) as shown in Figure 6.1.1. However, a phase compensation capacitor (C_{FB}) may be added to ensure the prevention of oscillation or improve load transient response. For example, a phase compensation capacitor (C_{FB}) is effective for the prevention of oscillation when the feedback pin of an adjustable-output LDO (A_{ADJ} in Figure 6.1.1) has parasitic capacitance due to PCB traces. This section describes the typical effect of a phase compensation capacitor (C_{FB}) on phase compensation.

For example, an LDO might have a second-order characteristic in the frequency range in which the loop gain ($A\beta$) > 0 dB (i.e., 1) if the feedback pin (V_{ADJ}) of an adjustable-output LDO has parasitic capacitance as shown in Figure 6.1.2.

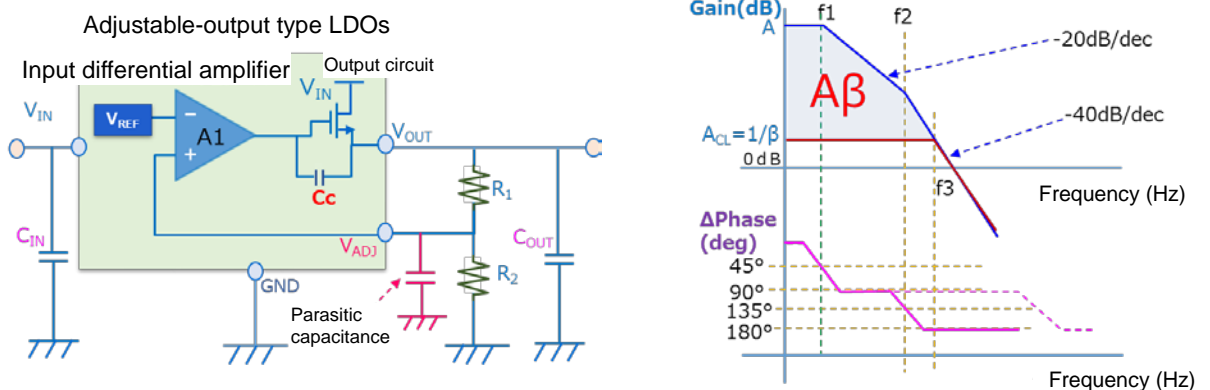


Figure 6.1.2 Frequency response of an adjustable-output LDO when its feedback pin (A_{ADJ}) has parasitic capacitance

In Figure 6.1.2, the phase shift of the loop gain ($A\beta$) reaches 180° at frequency f_3 at which the loop gain is 0 dB (i.e., 1), causing the LDO to oscillate. With only an external resistor (R_1), the feedback factor (β) is constant regardless of frequency. However, when a phase compensation capacitor (C_{FB}) is connected in parallel with R_1 , the feedback factor (β) becomes dependent on frequency as shown in Figure 6.1.3.

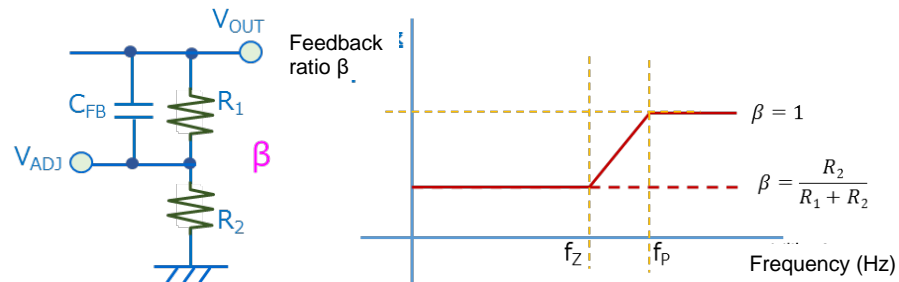


Figure 6.1.3 Feedback factor (β) when a phase compensation capacitor (C_{FB}) is connected in parallel with an external resistor (R_1)

When there is no phase compensation capacitor (C_{FB}), the feedback factor (β) is constant at $R_2/(R_1 + R_2)$ irrespective of frequency. With a phase compensation capacitor (C_{FB}), the slope of the feedback factor (β) changes at frequencies f_Z and f_P as shown in Figure 6.1.3. f_Z and f_P are determined by:

$$f_Z = \frac{1}{2\pi C_{FB} \times R_1}$$

$$f_P = \frac{1}{2\pi C_{FB} \times (R_1 // R_2)}$$

When the feedback ratio β has the frequency characteristics shown in Figure 6.1.3, the closed-loop gain (A_{CL}) (which is equal to the reciprocal of the feedback factor ($1/\beta$)), the loop gain, and the loop gain-vs-phase curve change as shown in Figure 6.1.4.

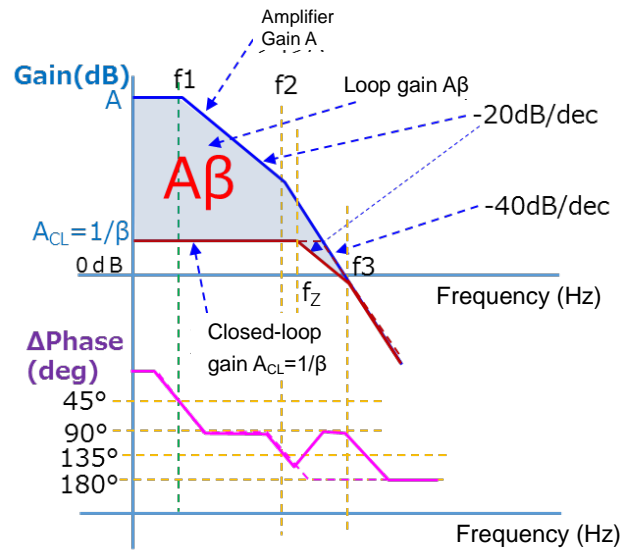


Figure 6.1.4 Closed-loop gain (A_{CL}) vs frequency, loop gain ($A\beta$) vs its phase when there is a phase compensation capacitor (C_{FB})

Figure 6.1.4 indicates that the gain of the LDO's internal amplifier has two poles at f_1 and f_2 . The closed-loop gain ($A_{CL} = 1/\beta$) begins to fall at the rate of -20 dB/dec at a pole frequency of f_z . The loop gain ($A\beta$), which is represented by the difference between the gain (A) and the closed-loop gain ($A_{CL} = 1/\beta$) of the LDO's internal amplifier, has two poles at f_1 and f_2 before the loop gain reaches 0 dB (i.e., 1) at f_3 . However, at the pole f_z of the closed-loop gain ($A_{CL} = 1/\beta$), the rate of fall of the loop gain decreases from -40 dB/dec to -20 dB/dec.

Rate of fall of the loop gain above the pole frequency (f_z) of the closed-loop gain ($A_{CL} = 1/\beta$):

$$\begin{aligned} \text{Rate of fall of loop gain } (A\beta) &= \text{rate of fall of amplifier's gain } (A) - \text{rate of fall of closed-loop gain } (A_{CL}) \\ &= (-40\text{dB/dec}) - (-20\text{dB/dec}) = -20\text{dB/dec} \end{aligned}$$

Remember that the loop gain ($A\beta$) falls at a rate of -40 dB/dec when $A\beta$ phase shifts by 180° . Therefore, the loop gain phase shifts only by 90° in the frequency range in which $A\beta$ falls at a rate of -20 dB/dec. In this case, the loop gain ($A\beta$)-vs-phase curve recovers toward 90° between f_z and f_3 (at which the loop gain ($A\beta$) becomes 0 dB) instead of increasing up to 180° . In other words, the loop gain ($A\beta$) is equivalent to having a first-order characteristic between f_z and f_3 . The phase compensation capacitor (C_{FB}) causes the feedback factor (β) to become dependent on frequency. This reduces the phase shift, causing the loop gain ($A\beta$) phase not to become inverted and thus preventing oscillation.

However, care should be taken as to the value of the external phase compensation capacitor (C_{FB}) because an excessive C_{FB} value degrades the frequency response of the closed-loop gain. When a zero is introduced at a frequency below the second pole (f_2), its effect on phase

recovery disappears at a low frequency as shown in Figure 6.1.5, causing the loop gain ($A\beta$) phase to shift by 180° . In the case of Figure 6.1.5, the effect of the external phase compensation capacitor (C_{FB}) disappears at a frequency below the pole (f_2) of the gain of the LDO's internal amplifier, causing the closed-loop gain ($A\beta$) to drop to 0 dB. In this situation, the rate of fall of the loop gain ($A\beta$) changes to -40 dB/dec at a frequency above f_2 , causing its phase to shift by 180° in the frequency range in which the loop gain ($A\beta$) is greater than 0 dB. Therefore, an external phase compensation capacitor (C_{FB}) with a minimal value should be selected, considering a trade-off between oscillation immunity and an LDO's AC characteristics.

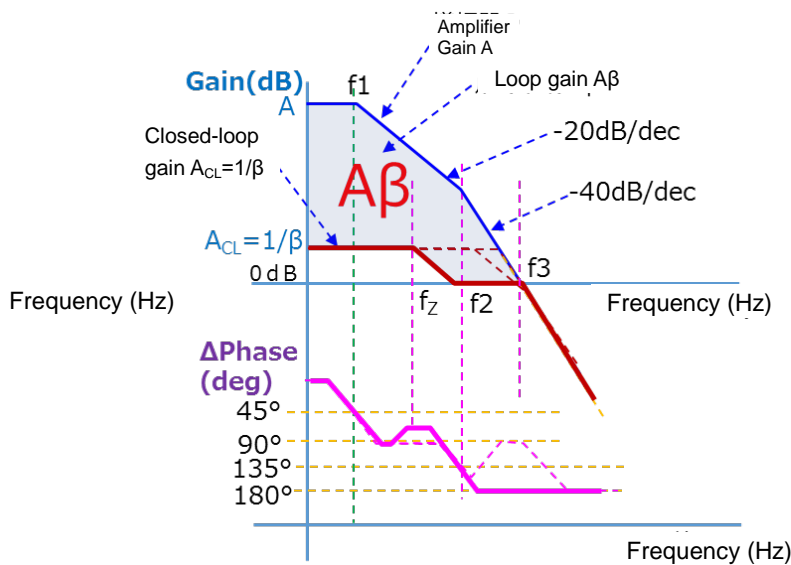


Figure 6.1.5 Frequency response of an adjustable-output LDO with a large external phase compensation capacitor (C_{FB})

Adding an external phase compensation capacitor (C_{FB}) is effective in reducing the susceptibility to oscillation, as described above. Basically, however, it is recommended to minimize parasitic capacitance as shown in Figure 6.1.6, for example, by reducing the distance from the connection point of the feedback resistors (R_1 and R_2) to the feedback pin (A_{ADJ}).

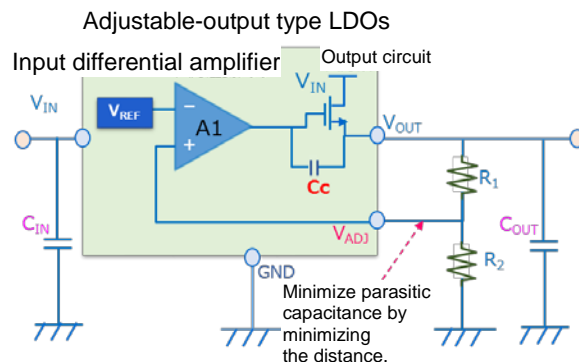


Figure 6.1.6 Distance from the connection point of the feedback resistors (R_1 and R_2) to the feedback pin (A_{ADJ}) of an adjustable-output LDO

7. Conclusion

A negative feedback system goes into oscillation when the loop gain ($A\beta$) phase shifts by 180° at a frequency at which $A\beta$ is equal to or greater than 0 dB. The loop gain ($A\beta$) phase shifts by 180° when it has a second- or higher-order characteristic. In this case, it is essential to prevent oscillation by means of phase compensation. LDOs are phase-compensated through Miller compensation and introduction of a zero so as to prevent oscillation. It is also effective to introduce a new zero using the equivalent series resistance (ESR) of an output capacitor (C_{OUT}). For adjustable-output LDOs whose output voltage is programmed via external resistors, the susceptibility to oscillation can be reduced by adding a phase compensation capacitor (C_{FB}) in parallel with a feedback resistor connected to the output pin (V_{OUT}). It is also possible to reduce the susceptibility to oscillation by minimizing the parasitic capacitance (for example, by reducing the distance from the connection point of two feedback resistors to the feedback pin (V_{ADJ})).

Toshiba's LDOs use these phase compensation techniques and other circuit techniques to prevent oscillation while incorporating a circuit to improve AC characteristics so as to combine both safety and performance.

Toshiba's typical LDO regulators:

To download the data sheet for the TCR3DM 300-mA fixed-output LDO regulator →

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To download the data sheet for the TCR5BM 500-mA fixed-output LDO regulator →

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To download the data sheet for the TCR8BM 800-mA fixed-output LDO regulator →

[Click Here](#)

Adjustable-output LDO regulators to which C_{FB} can be added

To download the data sheet for the TCR13AGADJ 1.3-A adjustable-output LDO regulator →

[Click Here](#)

To download the data sheet for the TCR15AG series of 1.5-A fixed- and adjustable-output LDO regulators →

[Click Here](#)

For more information on the usage of LDO regulators, see the Application Note for Low Drop Out (LDO) regulator IC:

To download the Application Note for Low Drop-Out (LDO) regulator IC →

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8.

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