Isolation amplifier TLP7820/7920/7830/7930 Application note

Outline

This application note explains the product briefs of TLP7820/7920 and TLP7830/7930, and application designs for the isolation amplifiers.

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Introduction

Recent control products for industrial use such as AC servo motor controllers, inverters for factory automation and power conditioners for renewable energy are required higher efficiency / accuracy operation. To realize that, high accuracy current / voltage sensing is a key factor. The designing point of this sensing block is required high accuracy, stability and isolation performances.

Toshiba's

- Isolation amplifier (analog output) : TLP7820 / TLP7920
- ΔΣ modulator (digital output) : TLP7830 / TLP7930

have a delta-sigma A/D converter with optically coupled isolation. It contributes a higher accuracy gain linearity with a higher isolation to sense current / voltage. User can select our products depends on the system design (post signal process IC etc.).

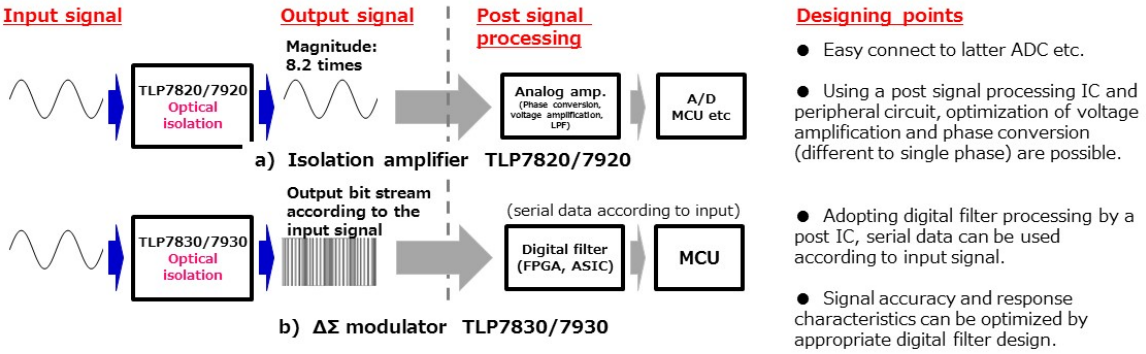


Fig.1 Signal processing using TLP7820/7920/7830/7930

Furthermore, Toshiba has the SO8L and DIP8 packages for each type of isolation amplifier.

Table 1 TLP7820/7920/7830/7930 Product matrix

Creepage Distance	8mm	7 or 8mm
Output Configuration	SO8L	DIP8
Analog output type	TLP7820	TLP7920
Digital output type	TLP7830	TLP7930

Below gain rank bins are available for TLP7820/7920

Rank	Gain Rank Marking	Gain (Min)	Gain (Typ.)	Gain (Max)	Unit
None (±3 %)	Blank, A, B	7.95	8.2	8.44	V/V
Rank A (±1 %)	A, B	8.12	8.2	8.28	
Rank B (±0.5 %)	B	8.16	8.2	8.24	

This application note explains the product briefs of TLP7820/7920 and TLP7830/7930, and describes about application designs for the isolation amplifiers.

1. Optically-coupled isolation amp. TLP7820/7920

The TLP7820/7920 are optically-coupled isolation amplifiers (input: analog, output: analog). This section describes TLP7820/7920 product briefs.

These products have a galvanic isolation and signal transmission function between input and output side by a LED and a photo-diode. High accuracy signal transmission is achieved by digital decoding of the transmitted light.

Fig.2 shows the TLP7820/7920 block diagram. Input analog signal is transmitted to the output side by optical signal, which is converted through ΔΣ ADC at the input side to the LED after encoded to digital code data. At the output side, the photo diode detects the optical signal, then it is decoded by TIA and decoder. Finally analog output signal is generated through DAC and LPF.

Fig.3 shows the input-output characteristics of the TLP7820/7920. 8.2(typ.) magnitude signal is output as differential voltage across V_{OUT+} to V_{OUT-} pins according to the differential voltage across V_{IN+} to V_{IN-} pins.

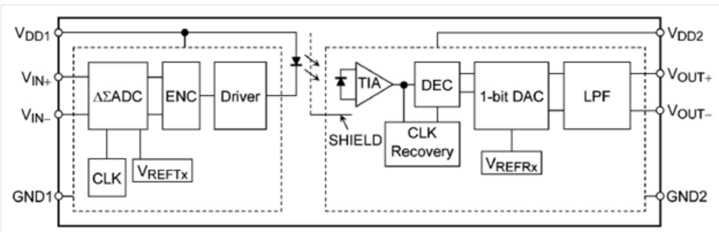


Fig.2 TLP7820/7920 Block diagram

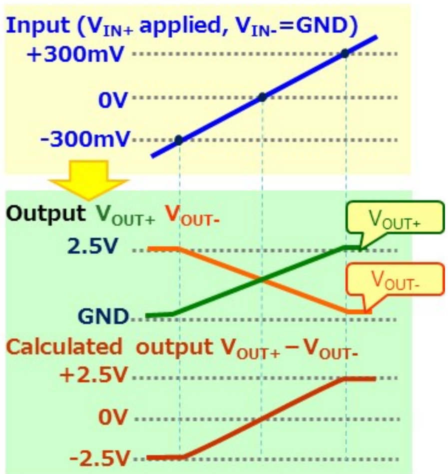


Fig.3 TLP7820/7920 Input-Output characteristic

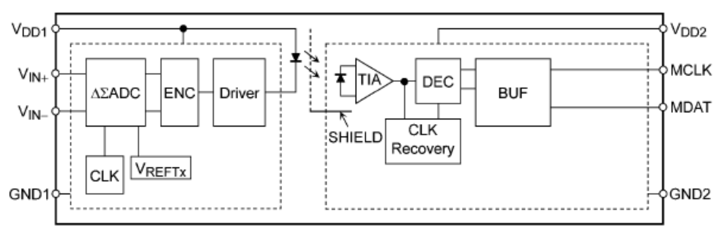
Please refer product’s Web sites (TLP7820 TLP7920) and Glossary of Isolation Amplifier Terms for details.

2. Optically-coupled ΔΣ modulator TLP7830/7930

The TLP7830/7930 is optically-coupled ΔΣ modulator (input: analog, output: digital).
This section describes TLP7830/7930 product brief.

Fig.4 shows the TLP7830/7930 block diagram. Compared to the TLP7820/7920 (analog output type), the TLP7830/7930 is eliminated DAC block and later block, thus those couplers output bit stream and clock signal. Applying this signal to post process IC, serial data is obtained according to the input analog signal.

Fig.5 shows the input-output characteristics of the TLP7830/7930. These items can output clock signal with 10MHz (typ.) and bit stream data from MCLK and MDAT pins, respectively. Bit stream data’s coarse and dense are according to the differential voltage across V_{IN+} to V_{IN-} pins.



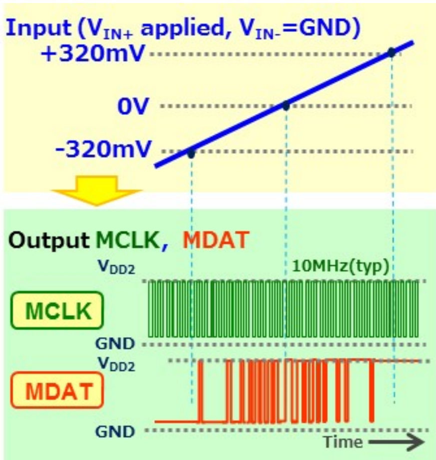


Fig.4 TLP7830/7930 Block diagram

Fig.5 TLP7830/7930 Input-Output characteristic

Please refer product’s Web sites (TLP7830 TLP7930) and Glossary of Isolation Amplifier Terms for details.

3. Application design (for current sensing)

Using application circuit for motor current sensing as example, this section explains a design for current sensing.

3-1. Power line design (both input and output side)

a) 0.1 μF ceramic capacitors should be connected to V_{DD1} - GND1 and V_{DD2}-GND2 to obtain the stabilized operation. The bypass capacitors should be placed as close as possible (within 10mm is recommended) to each pin (C_2 and C_4 shown in Fig.6).

b) When a high voltage power supply such as for a gate drive is utilized as V_{DD1}, applying voltage to the isolation amplifier must be stepped down not to exceeding the maximum rating. (Using voltage regulator, DC-DC converter, Zener diode etc.).

3-2. Input side line design

a) A clock-operated switched capacitor is embedded at the ADC input, 0.01μF bypass capacitor should be connected at input pins to obtain certain accuracy and follow the clock operation (C_3 shown in Fig.6).

b) Preventing influences of aliasing noise to the ADC, an anti-aliasing low-pass filter should be placed. The filter can be formed using the bypass capacitor (C_3) and a resistor (R_1 shown in Fig.6). Since filtering frequency range of the anti-aliasing filter should be between the signal bandwidth and the Nyquist frequency, the frequency from 400 kHz to 1 MHz is recommended.

Design example) Anti-aliasing filter constant R_1

Aliasing filter design frequency: 400 kHz, Bypass capacitor (input side): 0.01 μF

$R_1 = 1 / (2 \times \pi \times 0.01\ \mu F \times 400\ kHz) = 39\ \Omega$

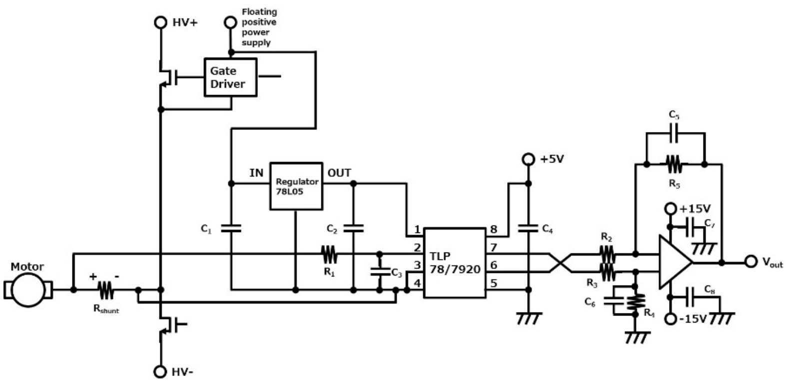


Fig.6 Motor current sensing circuit example using TLP7820/7920

3-3. Current sensing resistor (shunt resistor) value

a) The shunt resistor value should be set with consideration of both power dissipation at the resistor and the sensing accuracy. Smaller shunt resistance is desired in terms of the power dissipation, on the other hand, the input voltage amplitude of ±200 mV is desired in terms of the sensing accuracy (e.g. linearity, SNR). Fig.7 shows the relationship between the shunt resistance and power dissipation. In this graph, a point at intersection of the solid line (relationship between shunt resistance and power dissipation) with dotted line (input voltage amplitude auxiliary line) is a typical setting value. To obtain sufficient current sense accuracy, the input voltage amplitude of ±200 mV is recommended. Please check if the power dissipation is satisfied from this graph and the sensed current.

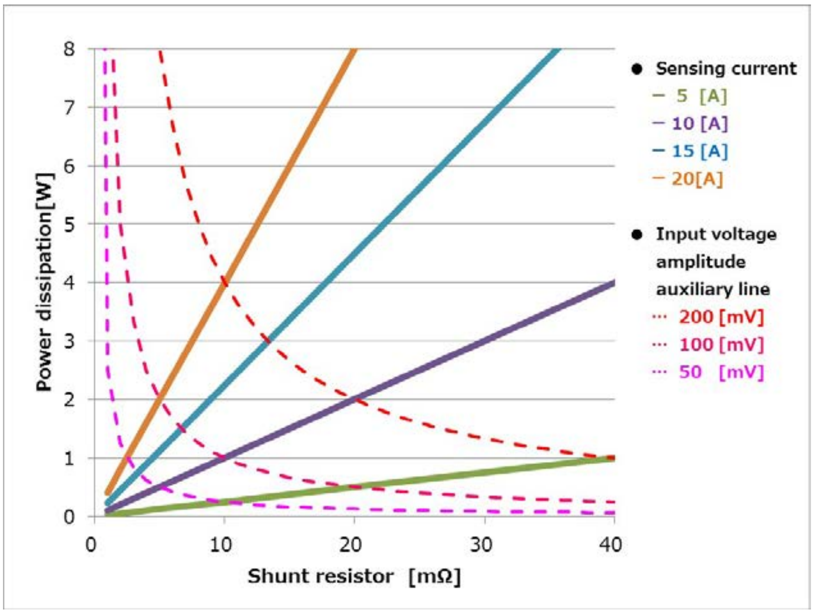


Fig.7 Relationship between shunt resistor and power dissipation

Design example) Design values of input amplitude V_{in}, shunt resistor R_{shunt}, and Power dissipation P_{shunt} in case of sensing current of 20 A

Case 1) In case of priority is the sensing accuracy, input amplitude V_{in} = 200 mV

- **Shunt resistor R_{shunt} = 200 mV / 20 A = 10 mΩ**
- **Power dissipation at the shunt resistor P_{shunt}**

  $= I^2 \times R = (20\ A)^2 \times 10\ m\Omega = 4\ W$

Case 2) In case of priority is the power dissipation, P_{shunt} = 1 W

- **Since the sensing current is 20 A, $R_{shunt} = 1\ W / (20\ A)^2 = 2.5\ m\Omega$**
- **In this case, input voltage amplitude is; $V_{in} = 20\ A \times 2.5\ m\Omega = 50\ mV$**

3-4. Output line design

a) PCB line length connected to a latter IC should be shorten as much as possible to minimize line capacitance.

b) For the analog output type, the output signal conversion to single phase, amplitude adjustment and adding noise filter are possible by adopting an external post amplifier. This post amplifier with certain accuracy (offset gain, response characteristic and each temperature dependence) should be used. In case of that either VOUT+ or VOUT- terminal is used as single phase output, another terminal should be open.

c) For the digital type, output conversion (bit stream → bit code) and high frequency band noise reduction are possible using FPGA or ASIC with SINC filter function.

●Order of the digital filter

The TLP7830/7930 implements 2nd order ΔΣ A/D converter. In terms of the out-band noise suppression, use of 3rd order digital filter is recommended.

●Decimation rate

Table 2 shows the relationship between decimation rate and design parameters of the $SINC^3$ filter. The design should be considered trade-off relationship between responsiveness (response time, bandwidth) and the SN performance.

Table 2 $SINC^3$ filter Relationship between decimation rate and design parameters

Decimation rate	Output data size [bits]	Response time [μs]	Output data rate [kSPS]	Freq. range [kHz]	Nyquist freq. [kHz]	SNR (theoretical) [dB]	ENOB (theoretical)[bits]
4	6	1.2	2500.0	655.0	1250.0	14.0	2.0
8	9	2.4	1250.0	327.5	625.0	30.8	4.8
16	12	4.8	625.0	163.8	312.5	45.7	7.3
32	15	9.6	312.5	81.9	156.3	59.7	9.6
64	18	19.2	156.3	40.9	78.1	68.2	11.0
128	21	38.4	78.1	20.5	39.1	71.9	11.7
256	24	76.8	39.1	10.2	19.5	74.9	12.1

The TLP7830/7930 guarantees characteristics with $SINC^3$ filter under 256 decimation rate and 16 bit resolution. Fig.8 shows representative example of $SINC^3$ filter configuration, and List 1 shows the program code, respectively.

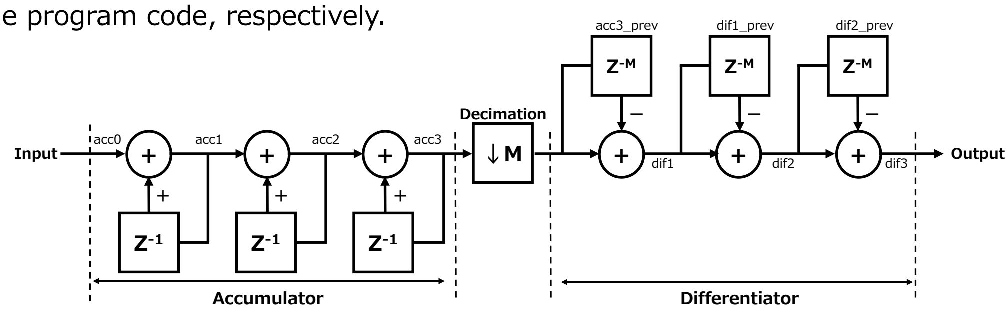


Fig.8 Relationship between shunt resistor and power dissipation

List 1 The program code example of SINC^3 filter with Verilog HDL

```
/* ----- Toshiba Electronic Devices & Storage Corporation -----   */
/* SINC3 Digital filter example with VerilogHDL for TLP7830/7930 */

module SINC3_VerilogHDL
(
input MCLK, MDAT,            /* Output of TLP7830/7930 */
input RST,                   /* Filter reset signal */
input [15:0] DEC,            /* Decimation Rate */
output reg [15:0] SNCOUT,    /* SINC3 filter output with 16bit */
output reg ENBL              /* SNCOUT Enable signal */
);

reg [24:0] acc0,acc1,acc2,acc3,acc3_prev;
reg [24:0] dif1,dif2,dif3,dif1_prev,dif2_prev;
/* Registor for Accumlation and Differentiation */

reg [15:0] mclkcnt; /* MCLK Counter */
reg decclk; /* CLK by decimation rating based

/* ---------- 3 times Accumulation ---------- */
always @ (MDAT)
if(MDAT==0)
    acc0 <= 25'd0;
else
    acc0 <= 25'd1;

always @ (negedge MCLK, posedge RST)
begin
    if (RST)
    begin /* Initialization */
            acc1 <= 25'd0;
            acc2 <= 25'd0;
            acc3 <= 25'd0;
    end
    else
    begin /* Accumulation */
            acc1 <= acc1 + acc0;
            acc2 <= acc2 + acc1;
            acc3 <= acc3 + acc2;
    end
end

/* ---------- Decimation clock gen ---------- */
always @ (posedge MCLK, posedge RST)
begin
    if (RST)
            mclkcnt <= 16'd0;
    else
    begin
            if ( mclkcnt == DEC - 1 )
                    mclkcnt <= 16'd0;
            else
                    mclkcnt <= mclkcnt +16'b1;
    end
end

always @ ( posedge MCLK, posedge RST )
begin
    if ( RST )
            decclk <= 1'b0;
    else
    begin
            if ( mclkcnt == DEC/2 - 1 )
                    decclk <= 1'b1;
            else if ( mclkcnt == DEC - 1 )
                    decclk <= 1'b0;
    end
end
```

```
    /* ---------- 3 times Differntiation ---------- */
    always @ (posedge decclk, posedge RST)
    begin
        if(RST)
        begin /* Initialization */
                acc3_prev <= 25'd0;
                dif1_prev <= 25'd0;
                dif2_prev <= 25'd0;
                dif1 <= 25'd0;
                dif2 <= 25'd0;
                dif3 <= 25'd0;
        end
        else
        begin /* Differentiation */
                dif1 <= acc3 - acc3_prev;
                dif2 <= dif1 - dif1_prev;
                dif3 <= dif2 - dif2_prev;
                acc3_prev <= acc3;
                dif1_prev <= dif1;
                dif2_prev <= dif2;
        end
    end

    /* ---------- Output bit number will be set to 16bits ---------- */
    always @ ( posedge decclk )
    begin
        case ( DEC )
                16'd64:begin
                        SNCOUT <= (dif3[18:2] == 17'h10000) ? 16'hFFFF : dif3[17:2];
                end
                16'd128:begin
                        SNCOUT <= (dif3[21:5] == 17'h10000) ? 16'hFFFF : dif3[20:5];
                end
                16'd256:begin
                        SNCOUT <= (dif3[24:8] == 17'h10000) ? 16'hFFFF : dif3[23:8];
                end
                default:begin
                        SNCOUT <= (dif3[24:8] == 17'h10000) ? 16'hFFFF : dif3[23:8];
                end
        endcase
    end

    /* ---------- Making Enable signal ---------- */
    always@ ( posedge MCLK, posedge RST )
    begin
        if ( RST )
        begin /* Initialization */
                ENBL <= 1'b0;
        end
        else
        begin /* Making Enable signal */
                if ( mclkcnt == DEC/2 - 1)
                begin
                        ENBL <= 1'b1;
                end
                else
                        ENBL <= 1'b0;
        end
    end
endmodule
```

3-5. Other notes

a) When either V_{IN+} or V_{IN-} or both are equal to or greater than V_{DD1}-2 V (e.g., if V_{DD1} = 5 V, when V_{IN+} and/or V_{IN-} are equal to or greater than 5 V − 2 V = 3 V), isolation amplifiers go into one of the test modes※. Do not raise either V_{IN+} or V_{IN-} above this voltage to keep the device in functional mode.

* TLP7820/7920/7830/7930 have the test mode to check the internal clock generator, decoder, encoder and LED performances, and to enhance qualities, the internal operating margins are checked in manufacturing process in addition to product's characteristics.

4. Application design (for voltage sensing)

This section explains designing points for voltage sensing application. (Example: inverter bus voltage sense, Fig.9)

4-1. Resistor value for the voltage sense

a) Although the bus voltage is much higher than allowable input current range of the isolation amplifier, the voltage sense is possible using a voltage-dividing circuit.

b) Depends on low pass filter design which is determined R_1, R_2 and C_1 (input side line capacitor), responsiveness (bandwidth) is changed. The responsiveness can be improved using smaller R_1, R_2 and C_1. However, the current flow at the divider becomes higher and the sensing accuracy becomes lower. Please adjust those setting values considering your application.

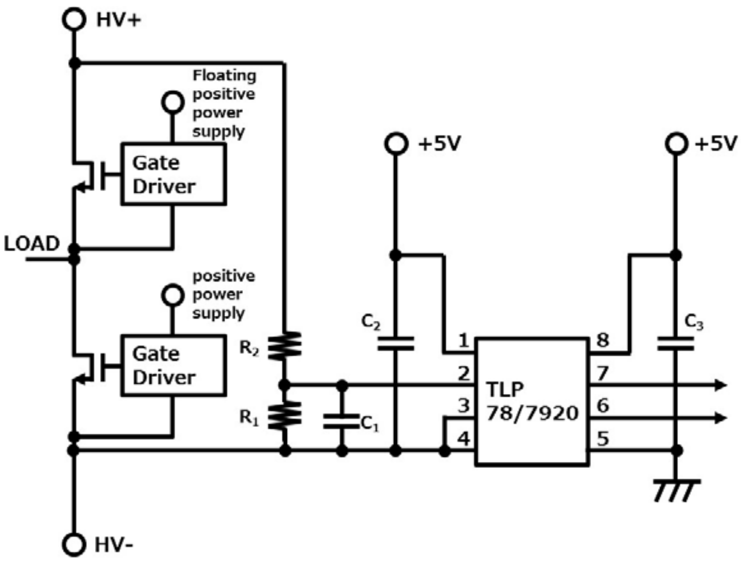


Fig.9 Inverter bus voltage sensing circuit example using TLP7820/7920

Design example) Voltage division resistor design (Sensing error : below 0.5%)

Equivalent input resistor of TLP7820 R_i : 80 kΩ

$R_1 : R_1 // R_i = R_1 : (R_1 \times 80k\Omega) / (R_1 + 80k\Omega) = 1 : 0.995$

$0.995 = 80k\Omega / (R_1 + 80k\Omega)$

$0.995 \times R_1 + 0.995 \times 80k\Omega = 80\ k\Omega$ **$R_1 ≒ 402\ \Omega$**

In case of applied voltage : 400 V, and detecting voltage : 200 mV

$400V : 200mV = (R_2 + 402\Omega) : 402\ \Omega$

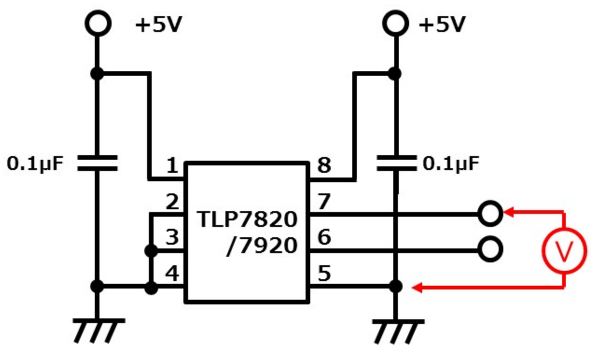
$200mV \times R_2 + 200mV \times 402\Omega = 400V \times 402\Omega$ **$R_2 ≒ 804k\Omega$**

5. Characterization data other than the items listed in the datasheet

This section describes the characteristics of our isolation amplifiers those are considered important for applications other than those listed on the datasheet.

5-1. Output noise characteristics of isolation amplifiers TLP7820/7920

White noise (random fluctuation of the output voltage over time) is observed in the output of the isolation amplifier due to the influence of thermal noise in the semiconductor IC mounted inside the isolation amplifier. This is defined as the output noise characteristics, and Fig. 11 shows the evaluation results of the V_{OUT+} terminal output noise of the TLP7820/7920(V_{DD1}=V_{DD2}=5V, T_a = 25°C) in the measuring circuit diagram shown in Fig. 10. In this evaluation, it was confirmed that the V_{OUT+} single-phase output noise was approximately 4 mV_{rms}.



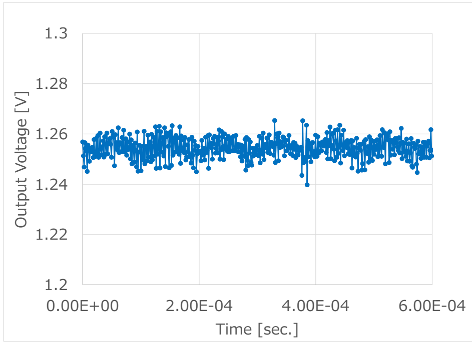
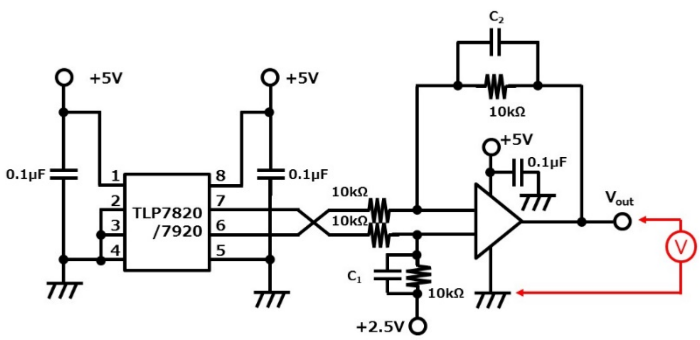


Fig.10 Evaluation circuit of V_{OUT+} terminal output noise Fig.11 Evaluation result of V_{OUT+} terminal output noise

Fig. 13 shows the results (Ta = 25°C) obtained by changing the cut-off frequency of the post-amplifier by the capacitor C1, C2 in the configuration including the post-amplifier shown in Fig. 12, and confirming the effect of suppressing the output noise. Lowering the cut-off frequency of the post-amplifier suppresses the white noise component in the high frequency range and improves the output noise characteristic. On the other hand, if the cut-off frequency is lowered to a level of the signal frequency, the gain will be lowered, therefore it is important to optimize the cut-off frequency according to the operating conditions.



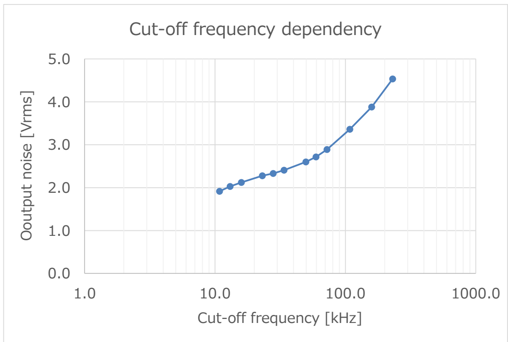


Fig.12 Evaluation circuit of output noise suppression Fig.13 Evaluation result of output noise suppression

5-2. SN characteristics of the isolation amplifier TLP7820/7920

The signal accuracy of operational amplifiers and A/D converters is measured by SN characteristics which indicates the degree of signal-to-noise ratio and signal distortion in the power spectrum. Typical properties are SNR, SNDR, and THD, as defined in Table 3.

Table 3　Definition of SN characteristics items

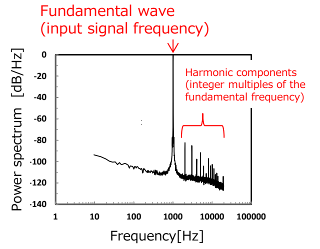
Term	Symbol	Description	Characteristic Curve
Signal-to-noise ratio	SNR	The ratio of signal components to noise components (excluding harmonics).	
Signal to (noise + distortion) ratio	SNDR	The ratio of signal components to noise components (including harmonics).	
Total harmonic distortion	THD	Ratio of fundamental components to harmonics.	

Fig. 15 shows the evaluation results of temperature dependence of SNR, SNDR, and THD at V_{OUT+}-V_{OUT-} differential output terminal of the TLP7820/7920 (input frequency of 1kHz, input amplitude of 400 mV $_{p\text{-}p}$, V_{DD1}=V_{DD2}=5V, and BW=22kHz) in the measuring circuit diagram shown in Fig. 14. The characteristics of SNR=69 [dB], SNDR=67 [dB], and THD=-72 [dB] at T_a=25℃ were confirmed in this evaluation. In order to further improve the SN characteristics, it is effective to suppress noise as much as possible by inserting an appropriate noise filter in the rear stage of isolation amplifier same manner as the output noise mentioned above, in the range of that the gain and distortion of the signal are not impaired.

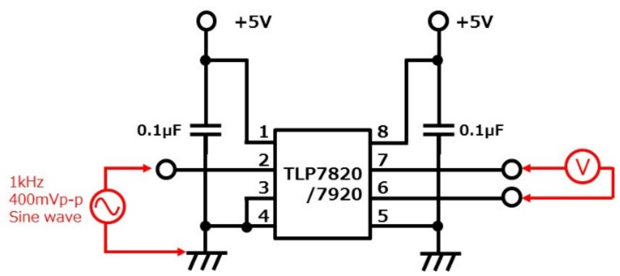


Fig.14 Evaluation circuit of SN characteristics for V_{OUT+}-V_{OUT-} differential output

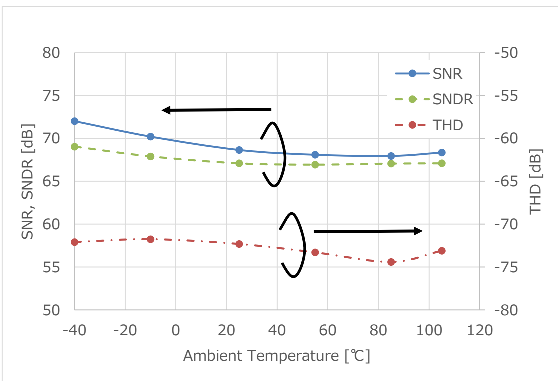


Fig.15 Evaluation results of SN characteristic temperature dependence

5-3. PSRR Characteristics of Isolation Amplifier TLP7820/7920

The PSRR, Power Supply Rejection Ratio, is an index to show how stable the output can be obtained without being affected by the ripple superimposed on the power supply of the Op-Amp-AD converter.PSRR is defined by the equation below, which indicates that the higher the value, the less susceptible to ripple noise, resulting in a stable output. Since TLP7820/7920 has ΔΣADC on the input side, ripple to the input-side power supply may affect the AD-converted value. Fig. 17 shows PSRR of TLP7820/7920 evaluated using the measuring circuit diagram shown in Fig. 16.

$$\mathrm{PSRR} = \mathbf{20log}\frac{V_{DDINRPL}}{V_{OUTRPL}}\ [\mathrm{dB}]$$

$V_{DDINRPL}$: Ripple components of isolation amplifier power supply (V_{DD})

V_{OUTRPL} : Ripple components of isolation amplifier output voltage (V_{OUT})

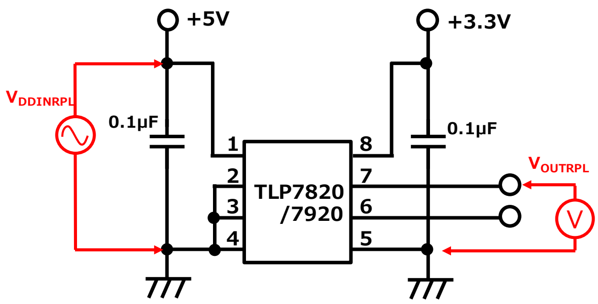


Fig.16 PSRR measurement circuit

In the measurement circuit diagram shown in Figure 17 shows the PSRR evaluation results of monitoring the output voltage V_{OUT+}(7pin) when 1Vp-p ripple noise is superimposed on the input side power supply (pin 1) at a frequency of 100Hz to 1000kHz in the measurement circuit diagram shown in Figure 16.

(The horizontal axis (X-axis) of the graph indicates the frequency band, and the vertical axis (Y-axis) indicates PSRR.)

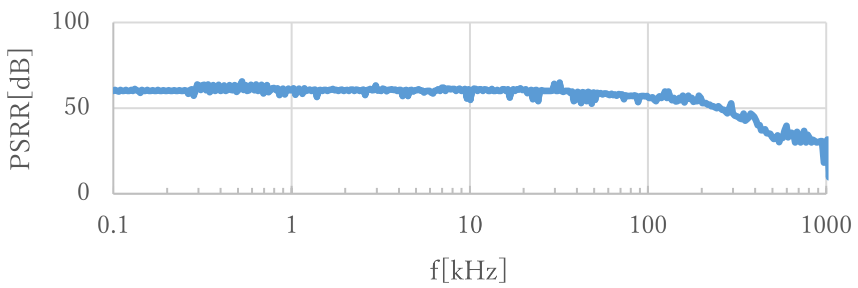


Fig.17 PSRR Evaluation Results

The frequency band of the ripple noise is maintained at 60dB up to 100kHz, worsening from around 200kHz. This result shows that PSRR decreases when ripples in a higher frequency band of 100 kHz or higher are superimposed on the DC voltage supplied to the input-side power supply.

Ripples in the frequency band of 100kHz or higher can affect the power output. Suppose the operation and performance of this equipment are affected. In that case, the filter against ripples in a wide frequency band can be expected to be effective by supplying power through LDOs with excellent PSRR or by adding a bypass capacitor.

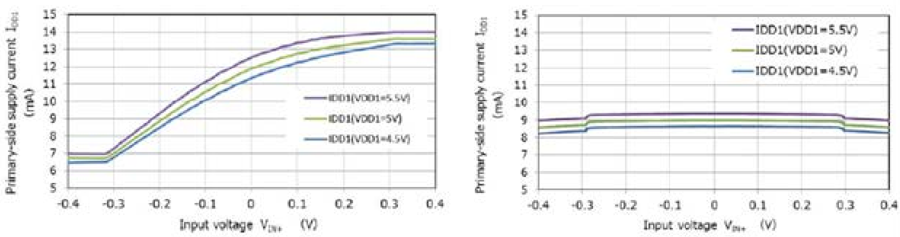
6. Features of TLP7820/7920/7830/7930

TLP7820/7920/7830/7930 basic performances are similar to competitor items, moreover, below features contribute your better circuit design.

6-1. Input side power consumption reduction

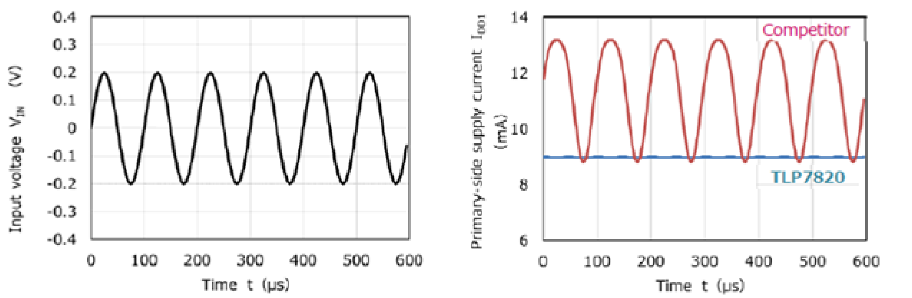
Fig.18 shows the relationships between the input voltage and the primary-side supply current of the TLP7820 and a competitor's. The primary-side supply current of the competitor's isolation amplifier increases with input voltage while the TLP7820 has a unique digital encoder/decoder technology to maintain the primary-side supply current at almost a constant level around 9 mA (typical) over a range of input voltage (recommend operating range: -0.2 to +0.2 V). This contributes reduction of the maximum circuit current, simplifying the design of a primary-side power supply.

Fig.19 shows the changes in the primary-side supply current in response to input voltage changes at a given frequency. The primary-side supply current of the competitor's isolation amplifier changes between 9mA and 13 mA in response to changes in input voltage while the primary-side supply current of the TLP7820 remains around 9 mA regardless of input voltage change. For example, a floating power supply such as a bootstrap is used as a primary-side power supply for an isolation amplifier since the floating power supply allows the use of small-value capacitors to reduce the circuit size. Obviously, the constant supply current of the TLP7820 contributes power supply consumption reduction and the circuit size reduction. In the trend of increasing system speed, this also contributes suppress electromagnetic interference (EMI) caused by large supply voltage fluctuations.



A) Competitor A　　　B) TLP7820

Fig.18 Relationships between the input voltage and the primary-side supply current



A) Input voltage changes　　　B) Primary-side supply current waveforms

Fig.19 Primary-side supply current waveforms in response to input voltage changes

6-2. Low-profile SO8L package

Fig.20 shows package comparison between TLP7820/7830 and competitor item. The TLP7820/7830 adopts a low profile (height: 2.3mm max) package which is thinner than competitor item. This is suitable for compact size applications.

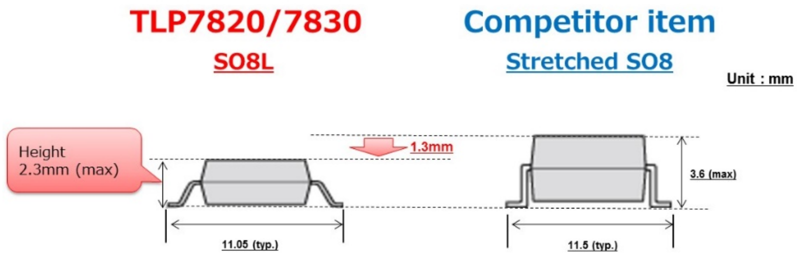
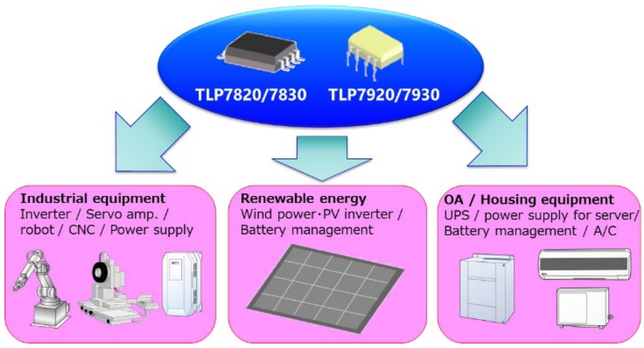


Fig.20 Package side view TLP7820 vs. competitor item

7. Applications

TLP7820/7920/7830/7930 is suitable for applications which need inverter such as industrial inverters, PV inverters, UPSs, BMSs, etc.



Application example) Inverter

Fig.21 shows an example of inverter application. Isolation amplifier is suitable for below application.

① Motor phase current sense

② Bus voltage sense

③ Over current sense

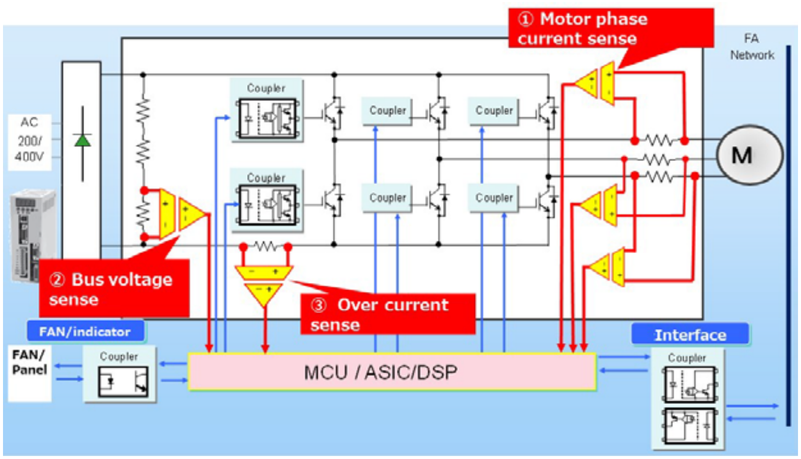


Fig.21 Application example of Isolation amp. for Inverter system

Revision History

Revision	Date	Page	Description
Rev. 1.0	2015/08/18	-	1st edition
Rev. 2.0	2019/9/3	All pages	Revision due to format changes
Rev. 3.0	2019/11/6	P7 P9,10	・The comment for single phase output usage is added in “3-4 Output line design b)” ・The contents of “5. Characterization data other than the items listed in the data sheet” was added.
Rev. 4.0	2020/8/17	P7-9	The examples of digital filter’s program and configuration were added.
Rev. 5.0	2021/12/15	P14-15	The contents of “PSRR Characteristics of Isolation Amplifier TLP7820/7920” was added.

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