

eFuse IC Glossary

Outline:

eFuse ICs can interrupt a power supply with higher current accuracy and in a shorter time than tubular glass fuses and polyswitches (also known as resettable fuses and polyfuses). If a tubular glass fuse burns out, it must be replaced after removing the factors that cause excessive current. In contrast, eFuse ICs are free from the drawbacks of conventional fuses since they are composed of a MOSFET that interrupts a power supply and various protection functions. Without being susceptible to permanent destruction, eFuse ICs eliminate the need for fuse replacement and enhance system reliability.

This document defines the terms used in relation to eFuse ICs.

Table of Contents

Outline:.....	1
Table of Contents	2
1. Absolute Maximum Ratings.....	3
2. Operating range.....	4
3. Electrical characteristics.....	5
3.1. DC characteristics	5
3.2. AC characteristics.....	7
RESTRICTIONS ON PRODUCT USE	8

1. Absolute Maximum Ratings

Term	Symbol	Description
Input voltage	V_{IN}	The maximum rated voltage that can be applied to the VIN pin without causing permanent damage to an IC or degrading its characteristics or reliability
ILIM voltage	V_{ILIM}	The maximum rated voltage that can be applied to the ILIM pin without causing permanent damage to an IC or degrading its characteristics or reliability
dV/dT voltage	$V_{dV/dT}$	The maximum rated voltage that can be applied to the dV/dT pin without causing permanent damage to an IC or degrading its characteristics or reliability
Control voltage	$V_{EN/UVLO}$	The maximum rated voltage that can be applied to the EN/UVLO pin without causing permanent damage to an IC or degrading its characteristics or reliability
Output voltage	V_{OUT}	The maximum rated voltage that can be applied to the VOUT pin without causing permanent damage to an IC or degrading its characteristics or reliability
External MOSFET voltage	V_{EFET}	The maximum rated voltage that can be applied to the EFET pin without causing permanent damage to an IC or degrading its characteristics or reliability
Power dissipation	P_D	The maximum power dissipation that does not cause permanent damage to an IC over the entire operating range
Junction temperature	T_j	The maximum junction temperature tolerated by an IC
Storage temperature	T_{stg}	The ambient temperature range in which an IC can be stored and transported without voltage application

2. Operating range

Term	Symbol	Description
Input voltage	V_{IN}	The input voltage range in which the proper operation and electrical characteristics of an IC are guaranteed
Output current	I_{OUT}	The output current range in which the proper operation and electrical characteristics of an IC are guaranteed
ILIM External resistance	R_{ILIM}	The range of the value of the resistor connected to the ILIM pin whereby the proper operation and electrical characteristics of an IC are guaranteed
Control voltage	$V_{EN/UVLO}$	The control voltage range in which the proper operation and electrical characteristics of an IC are guaranteed
External MOSFET voltage	V_{EFET}	The range of the EFET pin voltage in which the proper operation and electrical characteristics of an IC are guaranteed
Operating temperature	T_{a_opr}	The ambient temperature range in which the proper operation and electrical characteristics of an IC are guaranteed
External capacitor for the dV/dT pin	$C_{dV/dT}$	The range of the value or the maximum value of the capacitor connected to the dV/dT pin with which the proper operation and electrical characteristics of an IC are guaranteed

3. Electrical characteristics

3.1. DC characteristics

Term	Symbol	Description
Basic operation		
VIN undervoltage lockout (UVLO) rising threshold	V_{IN_UVLO}	The input voltage at which undervoltage lockout (UVLO) is disabled during a rising transition of VIN under the specified test conditions
VIN undervoltage lockout (UVLO) hysteresis	V_{IN_UVhyst}	The hysteresis width between the input voltage at which undervoltage lockout (UVLO) is tripped (V_{IN}) and the input voltage at which it is disabled (V_{IN_UVLO})
EN/UVLO threshold voltage, rising	V_{ENR}	The voltage at the EN/UVLO pin at which an IC is guaranteed to turn on under the specified test conditions
EN/UVLO threshold voltage, falling	V_{ENF}	The voltage at the EN/UVLO pin at which an IC is guaranteed to turn off under the specified test conditions
On resistance	R_{ON}	The on-resistance between the VIN and VOUT pins under the specified test conditions
Quiescent current (ON state)	I_Q	The current that flows through an IC under the specified test conditions when it is on
Quiescent current (OFF state)	$I_{Q(OFF)}$	The current that flows through an IC under the specified test conditions when it is off
dV/dT control		
CdV/dT voltage	$V_{dV/dT}$	The voltage at the dV/dT pin under specified test conditions
Charging current	$I_{dV/dT}$	The current sourced from the dV/dT pin under the specified test conditions
Discharge resistance	$R_{dV/dT}$	The resistance between the dV/dT and GND pins under the specified test conditions
dV/dT-to-OUT gain	$GAIN_{dV/dT}$	The ratio of the dV/dT pin voltage to the output voltage. This is guaranteed by virtue of design and is not tested in production.

Term	Symbol	Description
External FET gate driver		
Charging current	I_{EFET}	The current sourced from the EFET pin under the specified test conditions. The gate of an external N-channel MOSFET is charged by this current.
Output voltage	V_{EFET}	The voltage at the EFET pin under specified test conditions
Discharge resistance	R_{EFET}	The value of the resistor between the EFET and GND pins under the specified test conditions. The gate of an external N-channel MOSFET is discharged through this resistor.
Overvoltage lockout		
Overvoltage clamp (OVC)	V_{OVC}	The voltage level at which the output is clamped by the overvoltage protection function under the specified test conditions
Overcurrent protection		
Overcurrent limit	I_{LIM} (I_{OUT_CL})	The current level at which the output is clamped by the overcurrent protection function under the specified test conditions
Short-circuit current limit	I_{SCL}	The output current that flows when the output pin (VOUT) is kept in the short-circuited state under the specified test conditions. This is guaranteed by virtue of design and is not tested in production.
Fast trip comparator level	$I_{FASTTRIP}$ (I_{SHORT_TRIP})	The output current at which short-circuit protection is tripped under the specified test conditions
ILIM short resistor detect threshold	$R_{SHORTLIM}$	The resistor value at which R_{ILIM} connected to the ILIM pin is determined to be short-circuited. This is guaranteed by virtue of design and is not tested in production.
Thermal shutdown (TSD)		
Thermal shutdown threshold temperature	T_{SD}	The junction temperature at which an IC is shut down by the TSD function under the specified test conditions
Thermal shutdown hysteresis	T_{SDH}	The hysteresis width between the junction temperature at which the TSD function is disabled to turn an IC back on and the thermal shutdown threshold temperature (T_{SD})

3.2. AC characteristics

Term	Symbol	Description
V _{OUT} on time	t _{ON}	The time required under the specified test conditions from when a Low-to-High transition is applied to the EN/UVLO input pin to when V _{OUT} (I _{OUT}) rises to the specified condition. This characteristic is specified only as a guide.
V _{OUT} off time	t _{OFF}	The time required under the specified test conditions from when a High-to-Low transition is applied to the EN/UVLO input pin to when V _{OUT} (I _{OUT}) falls to the specified condition. This characteristic is specified only as a guide.
Output ramp time	t _{dV/dT}	The time required under the specified test conditions from when a Low-to-High transition is applied to the EN/UVLO input pin to when V _{OUT} (I _{OUT}) rises to the specified condition. This characteristic is specified only as a guide.
Fast trip comparator delay	t _{FastOffDly}	The time required under the specified test conditions from when the output pin (V _{OUT}) is short-circuited to when the output current (I _{OUT}) turns off. This characteristic is specified only as a guide.
EFET on time	t _{EFET-ON}	The time required under the specified test conditions from when a Low-to-High transition is applied to the EN/UVLO input pin to when the EFET pin voltage (V _{EFET}) rises to the specified voltage. This characteristic is specified only as a guide.
EFET off time	t _{EFET-OFF}	The time required under the specified test conditions from when a High-to-Low transition is applied to the EN/UVLO input pin to when the EFET pin voltage (V _{EFET}) falls to the specified voltage. This characteristic is specified only as a guide.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**