

# TLP5231

## 1. Applications

- IGBT Gate Drivers
- MOSFET Gate Drivers
- Industrial Inverters
- AC Servos
- Photovoltaic (PV) Power Conditioning Systems
- Air Conditioner Inverters

## 2. General

The TLP5231 is a 2.5 A dual-output IGBT gate pre-drive photocoupler including highly integrated multi-functional IC that is housed in SO16L package having a long creepage and clearance. This photocoupler is suitable as a pre-driver to driver power devices via external p- and n- channel MOSFET as buffers.

The smart gate driver photocoupler includes functions of IGBT/power MOSFET desaturation detection, isolated fault status feedback, configurable soft gate turn-off, and under voltage lockout (UVLO).

The TLP5231 consists of two infrared light-emitting diodes (LEDs) and two high-gain and high-speed light-receiving IC chips. Thereby, they realize the control of output current and the feedback function of the fault signal while keeping a insulation between a primary side and secondary side electrically.

## 3. Features

- (1) Output peak current:  $\pm 2.5$  A (max)
- (2) Operating temperature:  $-40$  to  $110$  °C
- (3) Threshold input current: 3.5 mA (max)
- (4) Propagation delay time: 300 ns (max)
- (5) Common-mode transient immunity:  $\pm 25$  kV/ $\mu$ s (min)
- (6) Isolation voltage: 5000 Vrms (min)
- (7) Dual output drive for external complementary type MOS buffer.
- (8) Under Voltage Lock-Out protection for positive and negative gate power supply.
- (9) Safety standards

UL-recognized: UL 1577, File No.E67349

cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

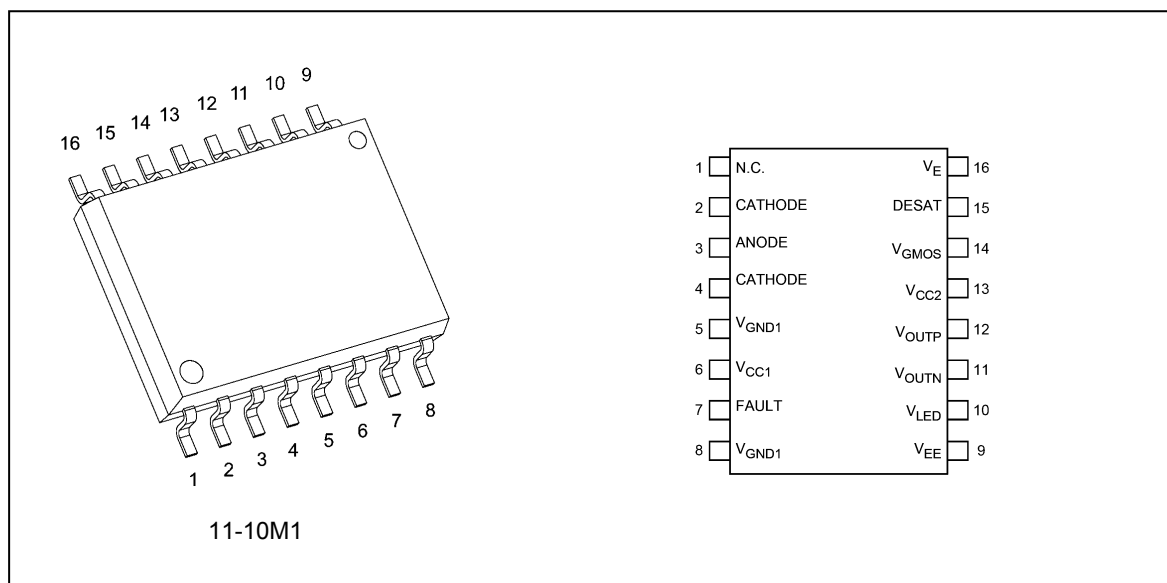
VDE-approved: EN 60747-5-5, EN 62368-1 (**Note 1**)

CQC-approved: GB4943.1, GB8898 Japan Factory

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

Start of commercial production  
2020-01

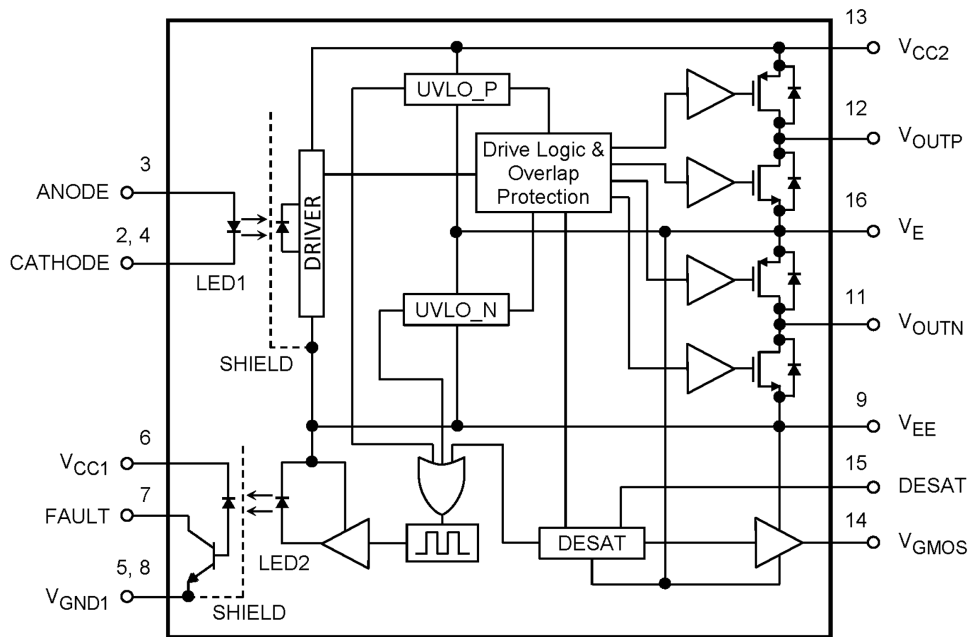
## 4. Packaging and Pin Assignment



### 4.1. Pin Description

| Pin No. | Symbol     | Description  |
|---------|------------|--|
| 1       | N.C.       | No connection  |
| 2       | CATHODE    | Cathode  |
| 3       | ANODE      | Anode  |
| 4       | CATHODE    | Cathode  |
| 5       | $V_{GND1}$ | Input side ground  |
| 6       | $V_{CC1}$  | Positive input supply voltage  |
| 7       | FAULT      | Fault output   |
| 8       | $V_{GND1}$ | Input side ground  |
| 9       | $V_{EE}$   | Negative output supply voltage   |
| 10      | $V_{LED}$  | Not connect, for testing only  |
| 11      | $V_{OUTN}$ | Low side voltage output  |
| 12      | $V_{OUTP}$ | High side voltage output   |
| 13      | $V_{CC2}$  | Positive output supply voltage   |
| 14      | $V_{GMOS}$ | External MOSFET control pin  |
| 15      | DESAT      | Short-circuit detection of The Desat terminal                                    |
| 16      | $V_E$      | Common output power supply terminal (emitter or source terminal of power device) |

## 5. Internal Circuit (Note)



Note: A 10 $\mu$ F bypass capacitor must be connected between pins 9 and 13, and A 1 $\mu$ F bypass capacitor must be connected between pins 13 and 16, and pins 9 and 16.  
A 0.33 $\mu$ F bypass capacitor must be connected between pins 6 and 5, or pins 6 and 8.

## 6. Principle of Operation

### 6.1. Truth Table

| Input current $I_F$ | Under Voltage Lock-Out UVLO_P, UVLO_N | DESAT function               | FAULT pin7 OUTPUT | $V_{OUTP}$      | $V_{OUTN}$     | $V_{GMOS}$     |
|---------------------|---------------------------------------|------------------------------|-------------------|-----------------|----------------|----------------|
| X                   | Active                                | Not active                   | H ( $V_{CC1}$ )   | H ( $V_{CC2}$ ) | H ( $V_E$ )    | H ( $V_E$ )    |
| ON                  | Not active                            | Active (with DESAT fault)    | H ( $V_{CC1}$ )   | H ( $V_{CC2}$ ) | L ( $V_{EE}$ ) | H ( $V_E$ )    |
| ON                  | Not active                            | Active (without DESAT fault) | L ( $V_{GND1}$ )  | L ( $V_E$ )     | L ( $V_{EE}$ ) | L ( $V_{EE}$ ) |
| OFF                 | Not active                            | Not active                   | L ( $V_{GND1}$ )  | H ( $V_{CC2}$ ) | H ( $V_E$ )    | L ( $V_{EE}$ ) |

### 6.2. Mechanical Parameters

| Characteristics              | Dimensions | Unit |
|------------------------------|------------|------|
| Creepage distances           | 8.0 (min)  | mm   |
| Clearance distances          |            |      |
| Internal isolation thickness | 0.4 (min)  |      |

## 7. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

|                                      | Characteristics   | Symbol                      | Note     | Rating                         | Unit                 |
|--------------------------------------|---|-----------------------------|----------|--------------------------------|----------------------|
| LED<br>(controller<br>side)          | Input forward current   | $I_F$                       |          | 25                             | mA                   |
|                                      | Input forward current derating<br>( $T_a \geq 95\text{ }^\circ\text{C}$ )                   | $\Delta I_F/\Delta T_a$     |          | -0.84                          | mA/ $^\circ\text{C}$ |
|                                      | Peak transient input forward<br>current   | $I_{FPT}$                   | (Note 1) | 1                              | A                    |
|                                      | Peak transient input forward<br>current derating<br>( $T_a \geq 95\text{ }^\circ\text{C}$ ) | $\Delta I_{FPT}/\Delta T_a$ | (Note 2) | -34                            | mA/ $^\circ\text{C}$ |
|                                      | Input reverse voltage   | $V_R$                       |          | 5                              | V                    |
|                                      | Positive input supply voltage   | $V_{CC1}$                   |          | -0.5 to 7                      | V                    |
|                                      | FAULT output current  | $I_{FAULT}$                 |          | 8                              | mA                   |
|                                      | FAULT terminal voltage  | $V_{FAULT}$                 |          | -0.5 to $V_{CC1}$              | V                    |
|                                      | Input power dissipation   | $P_D$                       |          | 150                            | mW                   |
|                                      | Input power dissipation<br>derating<br>( $T_a \geq 95\text{ }^\circ\text{C}$ )              | $\Delta P_D/\Delta T_a$     | (Note 2) | -5.0                           | mW/ $^\circ\text{C}$ |
| Detector<br>(gate<br>driver<br>side) | Peak high-level output current<br>( $T_a = -40$ to $110\text{ }^\circ\text{C}$ )            | $I_{OPH}$                   | (Note 3) | -2.5                           | A                    |
|                                      | Peak low-level output current<br>( $T_a = -40$ to $110\text{ }^\circ\text{C}$ )             | $I_{OPL}$                   | (Note 3) | +2.5                           | A                    |
|                                      | Total output supply voltage   | $(V_{CC2}-V_{EE})$          | (Note 4) | -0.5 to 35                     | V                    |
|                                      | Negative output supply voltage  | $(V_E-V_{EE})$              | (Note 4) | -0.5 to 17                     | V                    |
|                                      | Positive output supply voltage  | $(V_{CC2}-V_E)$             | (Note 4) | -0.5 to 30                     | V                    |
|                                      | High side output voltage  | $V_{OUTP(Peak)}$            |          | $V_E - 0.5$ to $V_{CC2} + 0.5$ | V                    |
|                                      | Low side output voltage   | $V_{OUTN(Peak)}$            |          | $V_{EE} - 0.5$ to $V_E + 0.5$  | V                    |
|                                      | DESAT voltage   | $V_{DESAT}$                 |          | $V_E - 0.5$ to $V_{CC2} + 0.5$ | V                    |
|                                      | $V_{GMOS}$ voltage  | $V_{GMOS}$                  |          | $V_{EE} - 0.5$ to $V_E + 0.5$  | V                    |
|                                      | Output power dissipation  | $P_O$                       |          | 410                            | mW                   |
|                                      | Output power dissipation<br>derating<br>( $T_a \geq 95\text{ }^\circ\text{C}$ )             | $\Delta P_O/\Delta T_a$     | (Note 2) | -14.0                          | mW/ $^\circ\text{C}$ |
| Common                               | Operating temperature   | $T_{opr}$                   |          | -40 to 110                     | $^\circ\text{C}$     |
|                                      | Storage temperature   | $T_{stg}$                   |          | -55 to 125                     | $^\circ\text{C}$     |
|                                      | Lead soldering temperature<br>(10 s)  | $T_{sol}$                   | (Note 5) | 260                            | $^\circ\text{C}$     |
|                                      | Isolation voltage<br>(AC, 60 s, R.H. $\leq 60\%$ )  | $BV_S$                      | (Note 6) | 5000                           | Vrms                 |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width (PW)  $\leq 1\mu\text{s}$ , 300pps

Note 2: Mounting on the substrate made in accordance with JEDEC JESD51-7.

Note 3: Exponential waveform. Pulse width  $\leq 0.2\mu\text{s}$ ,  $f \leq 15\text{ kHz}$ ,  $V_{CC2} = 15\text{ V}$

Note 4: Positive and Negative power supply ( $V_{CC2}/V_{EE}$ ) must be used in the gate drive circuit.

Note 5:  $\geq 2\text{ mm}$  below seating plane.

Note 6: This device is considered as a two-terminal device: Pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.

## 8. Recommended Operating Conditions (Note)

| Characteristics                | Symbol             | Note     | Min  | Typ. | Max                   | Unit |
|--------------------------------|--------------------|----------|------|------|-----------------------|------|
| Total output supply voltage    | $(V_{CC2}-V_{EE})$ | (Note 1) | 21.5 | —    | 30                    | V    |
| Negative output supply voltage | $(V_E-V_{EE})$     | (Note 1) | -15  | —    | -6.5                  | V    |
| Positive output supply voltage | $(V_{CC2}-V_E)$    | (Note 1) | 15   | —    | $30 - (V_E - V_{EE})$ | V    |
| Positive input supply voltage  | $V_{CC1}$          |          | 3.3  | —    | 5.5                   | V    |
| Input on-state current         | $I_{F(ON)}$        | (Note 2) | 5.3  | —    | 12                    | mA   |
| Input off-state voltage        | $V_{F(OFF)}$       | (Note 2) | 0    | —    | 0.8                   | V    |

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (10  $\mu$ F) must be connected between pins 9 ( $V_{EE}$ ) and 13 ( $V_{CC2}$ ), and a ceramic capacitor (1  $\mu$ F) must be connected between pins 13 ( $V_{CC2}$ ) and 16 ( $V_E$ ), and pins 9 ( $V_{EE}$ ) and 16 ( $V_E$ ) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: If the rising slopes of  $V_{CC2}$  and  $V_{EE}$  are so steep, the internal circuit operation may not be stable. In that case please design the slopes that  $V_{CC2}$  and  $V_{EE}$  go up to become 0.1 V/ $\mu$ s or less.

Note 2: The rise and fall times of the input on-current should be less than 0.5  $\mu$ s.

## 9. Electrical Characteristics

### 9.1. Electrical Characteristics (Note)

(Unless otherwise specified,  $T_a = -40$  to  $110$  °C,  $V_{CC2} - V_E = 15$  V,  $V_E - V_{EE} = 8$  V)

| Characteristics                         | Symbol       | Note     | Test Circuit | Test Condition  | Min              | Typ.             | Max            | Unit |
|---|--------------|----------|--------------|---|------------------|------------------|----------------|------|
| Input forward voltage                   | $V_F$        |          |              | $I_F = 10$ mA, $T_a = 25$ °C  | 1.45             | —                | 1.7            | V    |
| Input reverse current                   | $I_R$        |          |              | $V_R = 5$ V   | —                | —                | 10             | μA   |
| Input capacitance                       | $C_t$        |          |              | $V = 0$ V, $f = 1$ MHz, $T_a = 25$ °C   | —                | 60               | —              | pF   |
| FAULT low level output voltage          | $V_{FAULTL}$ |          |              | $V_{DESAT} = 0$ V, $R_F = 10$ kΩ, $C_F = 1$ nF, $V_{CC1} = 3.3$ or $5$ V          | —                | 0.1              | 0.25           | V    |
| FAULT high level output voltage         | $V_{FAULTH}$ |          |              | $V_{DESAT} = \text{Open}$ , $R_F = 10$ kΩ, $C_F = 1$ nF, $V_{CC1} = 3.3$ or $5$ V | —                | $V_{CC1}$        | —              | V    |
| FAULT low level output current          | $I_{FAULTL}$ |          |              | $V_{FAULT} = 0.15$ V, $V_{CC1} = 3.3$ or $5$ V                                    | —                | 1.2              | —              | mA   |
| FAULT high level output current         | $I_{FAULTH}$ |          |              | $V_{FAULT} = V_{CC1} = 3.3$ or $5$ V  | —                | 0.01             | 1              | μA   |
| $V_{OUTP}$ high level output current    | $I_{OUTPH}$  | (Note 1) | Fig.13.1.1   | $V_{CC2} - V_{OUTP} = 7$ V  | —                | —                | -1.0           | A    |
| $V_{OUTP}$ low level output current     | $I_{OUTPL}$  | (Note 1) | Fig.13.1.2   | $V_{OUTP} - V_E = 7$ V, $I_F = 8$ mA  | 1.0              | —                | —              | A    |
| $V_{OUTN}$ high level output current    | $I_{OUTNH}$  | (Note 1) | Fig.13.1.3   | $V_E - V_{OUTN} = 7$ V  | —                | —                | -1.0           | A    |
| $V_{OUTN}$ low level output current     | $I_{OUTNL}$  | (Note 1) | Fig.13.1.4   | $V_{OUTN} - V_{EE} = 7$ V, $I_F = 8$ mA   | 1.0              | —                | —              | A    |
| $V_{OUTP}$ high level output resistance | $R_{OUTPH}$  | (Note 1) | Fig.13.1.5   | $I_{OUTP} = -1.0$ A, $V_F = 0$ V  | —                | 1.6              | 4.4            | Ω    |
| $V_{OUTP}$ low level output resistance  | $R_{OUTPL}$  | (Note 1) | Fig.13.1.6   | $I_{OUTP} = 1.0$ A, $I_F = 8$ mA  | —                | 1.2              | 3.3            | Ω    |
| $V_{OUTN}$ high level output resistance | $R_{OUTNH}$  | (Note 1) | Fig.13.1.7   | $I_{OUTN} = -1.0$ A, $V_F = 0$ V  | —                | 1.9              | 5.0            | Ω    |
| $V_{OUTN}$ low level output resistance  | $R_{OUTNL}$  | (Note 1) | Fig.13.1.8   | $I_{OUTN} = 1.0$ A, $I_F = 8$ mA  | —                | 1.0              | 3.3            | Ω    |
| $V_{OUTP}$ high level output voltage    | $V_{OUTPH}$  |          | Fig.13.1.5   | $I_{OUTP} = -100$ mA, $V_F = 0$ V   | $V_{CC2} - 0.43$ | $V_{CC2} - 0.14$ | —              | V    |
| $V_{OUTP}$ low level output voltage     | $V_{OUTPL}$  |          | Fig.13.1.6   | $I_{OUTP} = 100$ mA, $I_F = 8$ mA   | —                | $V_E + 0.1$      | $V_E + 0.32$   | V    |
| $V_{OUTN}$ high level output voltage    | $V_{OUTNH}$  |          | Fig.13.1.7   | $I_{OUTN} = -100$ mA, $V_F = 0$ V   | $V_E - 0.4$      | $V_E - 0.17$     | —              | V    |
| $V_{OUTN}$ low level output voltage     | $V_{OUTNL}$  |          | Fig.13.1.8   | $I_{OUTN} = 100$ mA, $I_F = 8$ mA   | —                | $V_{EE} + 0.1$   | $V_{EE} + 0.3$ | V    |

Note: All typical values are at  $T_a = 25$  °C.

Note:  $C_F$  means smoothing capacitor. It attaches between pin 7 and pin 5, or pin 7 and pin 8 certainly.

Note 1:  $I_O$  application time  $\leq 10$  μs; single pulse.

## 9.2. Electrical Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $110$ °C, $V_{CC2} - V_E = 15$ V, $V_E - V_{EE} = 8$ V)

| Characteristics                         | Symbol           | Note                  | Test Circuit | Test Condition  | Min   | Typ.     | Max   | Unit     |
|---|------------------|-----------------------|--------------|---|-------|----------|-------|----------|
| $V_{GMOS}$ high level output current    | $I_{OUTGH}$      |                       | Fig.13.1.9   | $V_E - V_{GMOS} = 8$ V,<br>$I_F = 8$ mA, DESAT = Open         | —     | —        | -105  | mA       |
| $V_{GMOS}$ low level output current     | $I_{OUTGL}$      |                       | Fig.13.1.10  | $V_{GMOS} - V_{EE} = 8$ V,<br>$V_F = 0$ V, DESAT = Open       | 90    | —        | —     |          |
| $V_{GMOS}$ high level output resistance | $R_{OUTGH}$      |                       | Fig.13.1.11  | $I_{OUTG} = -80$ mA, $I_F = 8$ mA                             | —     | 10       | 30    | $\Omega$ |
| $V_{GMOS}$ low level output resistance  | $R_{OUTGL}$      |                       | Fig.13.1.12  | $I_{OUTG} = 80$ mA, $V_F = 0$ V,<br>DESAT = Open              | —     | 4        | 10    |          |
| $V_{GMOS}$ high level output voltage    | $V_{OUTGH}$      |                       | Fig.13.1.11  | $I_{OUTG} = -1$ mA, $I_F = 8$ mA,<br>DESAT = Open             | —     | $V_E$    | —     | V        |
| $V_{GMOS}$ low level output voltage     | $V_{OUTGL}$      |                       | Fig.13.1.12  | $I_{OUTG} = 1$ mA, $V_F = 0$ V,<br>DESAT = Open               | —     | $V_{EE}$ | —     |          |
| High level supply current ( $V_{CC2}$ ) | $I_{CC2H}$       |                       | Fig.13.1.13  | $V_F = 0$ V, no load  | —     | 5.8      | 10.2  | mA       |
| Low level supply current ( $V_{CC2}$ )  | $I_{CC2L}$       |                       | Fig.13.1.14  | $I_F = 8$ mA, no load   | —     | 6.2      | 10.2  |          |
| High level supply current ( $V_{EE}$ )  | $I_{EEH}$        |                       | Fig.13.1.13  | $V_F = 0$ V, no load  | -9.2  | -5.2     | —     |          |
| Low level supply current ( $V_{EE}$ )   | $I_{EEL}$        |                       | Fig.13.1.14  | $I_F = 8$ mA, no load   | -9.2  | -5.5     | —     |          |
| Threshold input current (H/L)           | $I_{FHL}$        |                       | Fig.13.1.15  | $V_{OUTP} - V_E < 5$ V,<br>$V_{OUTN} - V_{EE} < 1$ V          | —     | 1        | 3.5   |          |
| Threshold input voltage (L/H)           | $V_{FLH}$        |                       |              | $V_{OUTP} - V_E > 5$ V,<br>$V_{OUTN} - V_{EE} > 1$ V          | 0.8   | —        | —     | V        |
| UVLO_P threshold ( $V_{CC2}-V_E$ )      | $V_{UVLOP+}$     | (Note 1),<br>(Note 2) |              | $I_F = 8$ mA,<br>$V_{OUTP} - V_E < 5$ V                       | 12    | 13       | 14    |          |
| UVLO_P threshold ( $V_{CC2}-V_E$ )      | $V_{UVLOP-}$     | (Note 1)              |              | $I_F = 8$ mA,<br>$V_{OUTP} - V_E > 5$ V                       | 11    | 12       | 13    |          |
| UVLO_P hysteresis ( $V_{CC2}-V_E$ )     | $V_{UVLOP\_HYS}$ | (Note 1)              |              | $V_{UVLOP+} - V_{UVLOP-}$                                     | —     | 1        | —     |          |
| UVLO_N threshold ( $V_E-V_{EE}$ )       | $V_{UVLON+}$     | (Note 1),<br>(Note 2) |              | $I_F = 8$ mA,<br>$V_{OUTN} - V_{EE} < 1$ V                    | -6    | -5.3     | -5    |          |
| UVLO_N threshold ( $V_E-V_{EE}$ )       | $V_{UVLON-}$     | (Note 1)              |              | $I_F = 8$ mA,<br>$V_{OUTN} - V_{EE} > 1$ V                    | -5.7  | -5.0     | -4.7  |          |
| UVLO_N hysteresis ( $V_E-V_{EE}$ )      | $V_{UVLON\_HYS}$ | (Note 1)              |              | $V_{UVLON+} - V_{UVLON-}$                                     | —     | 0.3      | —     |          |
| DESAT threshold                         | $V_{DESAT}$      | (Note 2)              |              | $V_{CC2} - V_E > V_{UVLOP+}$ ,<br>$V_E - V_{EE} > V_{UVLON-}$ | 7.5   | 8.0      | 9.0   |          |
| Blanking capacitor charging current     | $I_{CHG}$        |                       | Fig.13.1.16  | $V_{DESAT} = 2$ V   | -0.82 | -0.54    | -0.29 | mA       |
| Blanking capacitor discharging voltage  | $V_{DSCHG}$      |                       |              | $I_{DSCHG} = 10$ mA   | —     | 1.1      | 3.0   | V        |

Note: All typical values are at  $T_a = 25$  °C.

Note 1:  $V_{UVLOP+}$  is the increasing of  $V_{CC2}-V_E$ .  $V_{UVLOP-}$  is the decreasing of  $V_{CC2}-V_E$ .

15V is the recommended minimum  $V_{CC2}$  to ensure adequate margin in excess of the maximum  $V_{UVLOP+}$ .

$V_{UVLON+}$  is the increasing of  $V_E-V_{EE}$ .  $V_{UVLON-}$  is the decreasing of  $V_E-V_{EE}$ .

-6.5V is the recommended maximum  $V_{EE}$  to ensure adequate margin in excess of the minimum  $V_{UVLON+}$ .

Note 2 : Once  $V_{OUTP}$  and  $V_{OUTN}$  are allowed to go low, the DESAT detection feature will be the primary source of power device protection.

In order for to DESAT function, un-activating of UVLO is required. ( $V_{CC2}-V_E > V_{UVLOP}$ ,  $V_E-V_{EE} > V_{UVLON}$ )

## 10. Isolation Characteristics (Unless otherwise specified, $T_a = 25\text{ °C}$ )

| Characteristics                     | Symbol | Note     | Test Condition                          | Min       | Typ.      | Max | Unit     |
|-------------------------------------|--------|----------|---|-----------|-----------|-----|----------|
| Total capacitance (input to output) | $C_S$  | (Note 1) | $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$ | —         | 1.0       | —   | pF       |
| Isolation resistance                | $R_S$  | (Note 1) | $V_S = 500\text{ V}$ , R.H. $\leq 60\%$ | $10^{12}$ | $10^{14}$ | —   | $\Omega$ |
| Isolation voltage                   | $BV_S$ | (Note 1) | AC, 60 s                                | 5000      | —         | —   | Vrms     |

Note 1: This device is considered as a two-terminal device: Pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.

## 11. Switching Characteristics

### 11.1. Switching Characteristics (Note)

(Unless otherwise specified,  $T_a = -40$  to  $110$  °C,  $V_{CC2} - V_E = 15$  V,  $V_E - V_{EE} = 8$  V)

| Characteristics                           | Symbol                          | Note               | Test Circuit  | Test Condition  | Min | Typ. | Max | Unit |
|---|---------------------------------|--------------------|---|---|-----|------|-----|------|
| Propagation delay time (L/H)              | $t_{pLH}$                       | (Note 1)           | Fig.13.1.17   | $I_F = 8 \rightarrow 0$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | 100 | 200  | 300 | ns   |
| Propagation delay time (H/L)              | $t_{pHL}$                       |                    |   | $I_F = 0 \rightarrow 8$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | 100 | 200  | 300 |      |
| Pulse width distortion                    | $ \frac{t_{pHL}}{t_{pLH}} - 1 $ |                    |   | $I_F = 0 \leftrightarrow 8$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 % | —   | —    | 150 |      |
| Propagation delay skew (device to device) | $t_{psk}$                       | (Note 1), (Note 2) |   | -200  | —   | 200  |     |      |
| $V_{OUTP}$ rise time at LED-OFF (90 %)    | $t_{DP}$                        | (Note 1)           |   | $I_F = 8 \rightarrow 0$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | 50  | 150  | 250 |      |
| $V_{OUTN}$ fall time at LED-ON (10%)      | $t_{DN}$                        |                    |   | $I_F = 0 \rightarrow 8$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | 50  | 150  | 250 |      |
| Outputs non-overlap time (L/H)            | $t_{NLH}$                       |                    |   | $I_F = 8 \rightarrow 0$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | —   | 60   | —   |      |
| Outputs non-overlap time (H/L)            | $t_{NHL}$                       |                    |   | $I_F = 0 \rightarrow 8$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | —   | 50   | —   |      |
| Rise time of $V_{OUTP}$                   | $t_{PR}$                        |                    |   | $I_F = 8 \rightarrow 0$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | —   | 50   | —   |      |
| Fall time of $V_{OUTP}$                   | $t_{PF}$                        |                    |   | $I_F = 0 \rightarrow 8$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 %     | —   | 50   | —   |      |
| Rise time of $V_{OUTN}$                   | $t_{NR}$                        |                    | $I_F = 8 \rightarrow 0$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 % | —   | 50  | —    |     |      |
| Fall time of $V_{OUTN}$                   | $t_{NF}$                        |                    | $I_F = 0 \rightarrow 8$ mA, $C_P = C_N = 4$ nF, $f = 20$ kHz, duty = 50 % | —   | 40  | —    |     |      |

Note: All typical values are at  $T_a = 25$  °C.

$C_P$  and  $C_N$  mean the gate capacitance of an external MOSFET buffer.

Note 1: Input signal duty = 50 %,  $t_r = t_f = 5$  ns or less

Note 2: The propagation delay skew,  $t_{psk}$ , is equal to the magnitude of the worst-case difference in  $t_{pHL}$  and/or  $t_{pLH}$  that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

## 11.2. Switching Characteristics (Note)

(Unless otherwise specified,  $T_a = -40$  to  $110$  °C,  $V_{CC2} - V_E = 15$  V,  $V_E - V_{EE} = 8$  V)

| Characteristics  | Symbol                  | Note     | Test Circuit             | Test Condition  | Min      | Typ. | Max | Unit        |
|--|-------------------------|----------|--------------------------|---|----------|------|-----|-------------|
| Propagation delay time from DESAT threshold to 50% of high $V_{GMOS}$  | $t_1$                   | (Note 1) | Fig.13.1.18              | $C_P = C_N = 4$ nF, $C_G = 1$ nF, $f = 100$ Hz, duty = 50 %, $I_F = 8$ mA, $C_{BLANK} = 200$ pF, $V_{DESAT} = 8.0$ V                | —        | 450  | 750 | ns          |
| Propagation delay time from DESAT threshold to 50% of high $V_{OUTP}$  | $t_2$                   |          |                          |   | —        | 380  | 700 |             |
| Propagation delay time from DESAT threshold to 50% of high $V_{FAULT}$ | $t_3$                   |          |                          | $R_F = 10$ k $\Omega$ , $C_F = 1$ nF, $V_{CC1} = 3.3$ or $5$ V, $f = 100$ Hz, duty = 50 %, $I_F = 8$ mA                             | —        | 8    | 20  | $\mu$ s     |
| Propagation delay time from 50% $V_{GMOS}$ to 50% of $V_{OUTN}$        | $t_4$                   |          |                          | $C_P = C_N = 4$ nF, $C_G = 1$ nF, $f = 100$ Hz, duty = 50 %, $I_F = 8$ mA   | —        | 45   | —   | ns          |
| DESAT Mute time  | $t_{MUTE}$              | (Note 2) |                          | $I_F = 8$ mA  | 0.68     | 1.1  | 1.7 | ms          |
| DESAT leading edge blanking time                                       | $t_{DESAT(L\text{EB})}$ | (Note 3) |                          | —   | —        | 580  | —   | ns          |
| DESAT filter time  | $t_{DESAT(FILTER)}$     | (Note 4) |                          | $R_{DESAT} = 100$ $\Omega$ , $V_{in} = 10$ V, $PW = 1$ $\mu$ s, monitor: $V_{OUTP}$ , $V_{GMOS}$                                    | —        | 290  | —   |             |
| High-level common-mode transient immunity                              | $CM_H$                  | (Note 5) | Fig.13.1.19, Fig.13.1.21 | $T_a = 25$ °C, $ V_{CM}  = 1500$ V <sub>p-p</sub> , $V_{CC1} = 5$ V ( $I_F = 0$ mA), $R_{in} = 220$ $\Omega$ (with split resistors) | $\pm 25$ | —    | —   | kV/ $\mu$ s |
| Low-level common-mode transient immunity                               | $CM_L$                  | (Note 6) | Fig.13.1.20, Fig.13.1.22 | $T_a = 25$ °C, $ V_{CM}  = 1500$ V <sub>p-p</sub> , $V_{CC1} = 5$ V ( $I_F = 8$ mA), $R_{in} = 220$ $\Omega$ (with split resistors) | $\pm 25$ | —    | —   |             |

Note: All typical values are at  $T_a = 25$  °C.

$C_G$  means the external MOSFET gate capacitance for soft gate turn-off.

Note 1: Input signal duty = 50 %,  $t_r = t_f = 5$  ns or less

Note 2: Automatic reset time from protected operation. If the input voltage of a DESAT pin exceeds  $V_{DESAT}$ ,  $V_{OUTP}$  moves to high level,  $V_{OUTN}$  set to low level,  $V_{GMOS}$  moves to high level and FAULT moves to high level, then protected operation will start. If a gate input signal returns to a low level, automatic reset of the protected operation will be carried out after  $t_{MUTE}$ . Refer to Fig. 13.2.2 and Fig. 13.2.3.

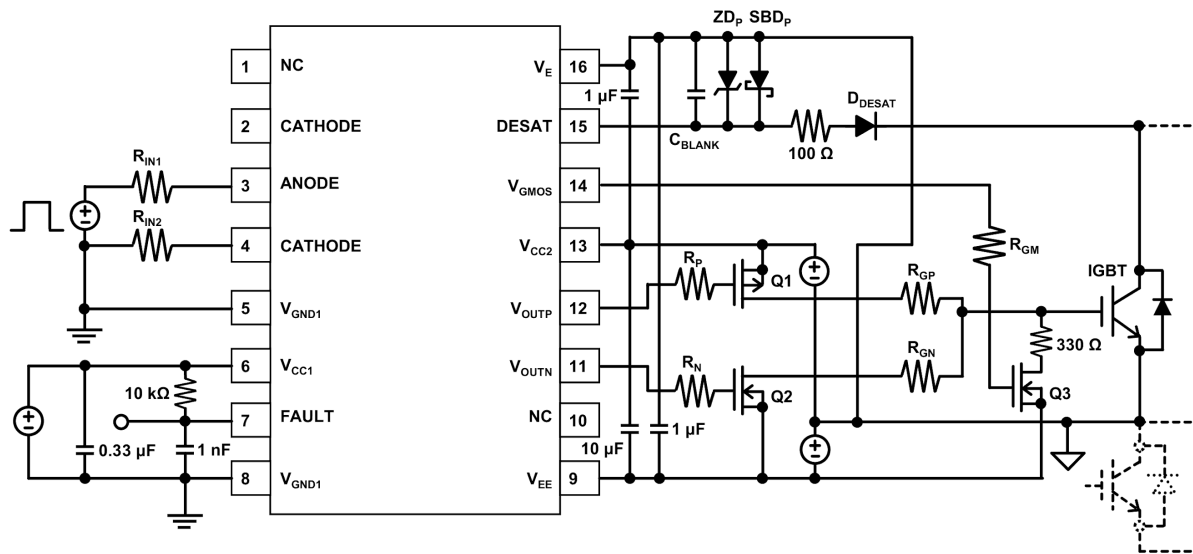
Note 3: Disabling time for incorrect detection prevention in case a gate control signal inputs. Refer to Fig. 13.2.2.

Note 4: Disabling time for incorrect detection prevention when the input voltage to a DESAT pin exceeds  $V_{DESAT}$ . ( $t_{DESAT(FILTER)} < t_1, t_2$ )

Note 5:  $CM_H$  is the maximum rate of fall of the common mode voltage that can sustained with the output voltage in the logic high state ( $V_{OUTP} - V_E > 12$  V,  $V_{OUTN} - V_{EE} > 5$  V or  $V_{FAULT} > 2$  V).

Note 6:  $CM_L$  is the maximum rate of rise of the common mode voltage that can sustained with the output voltage in the logic low state ( $V_{OUTP} - V_E < 1$  V,  $V_{OUTN} - V_{EE} < 1$  V or  $V_{FAULT} < 0.8$  V).

## 12. Application Information



**Fig. 12.1 Recommended Application Circuit**

- Note: The gate circuit of a power device requires both a positive power supply ( $V_{CC2}$ ) and a negative power supply ( $V_{EE}$ ).
- Attach external P channel MOSFET and N channel MOSFET to a  $V_{OUTP}$  pin and a  $V_{OUTN}$  pin.
- Refer to the connection of pin 14, pin 15, and pin 16 for a DESAT detection function and an over-current protection soft gate turn-off function.
- A smoothing capacitor is absolutely attached between pin 7 and pin 5, or pin 7 and pin 8.

## 13. Reference Drawings

### 13.1. Test Circuits

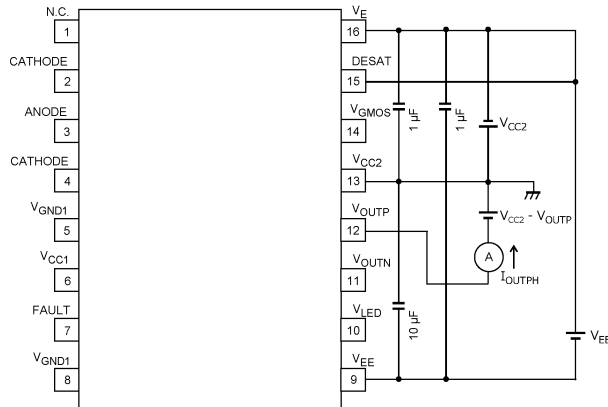


Fig. 13.1.1 I<sub>OUTPH</sub> Test Circuit

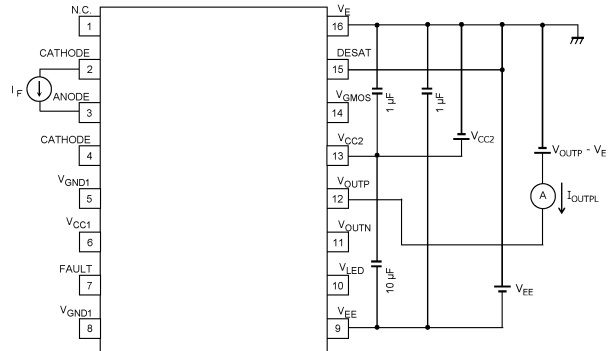


Fig. 13.1.2 I<sub>OUTPL</sub> Test Circuit

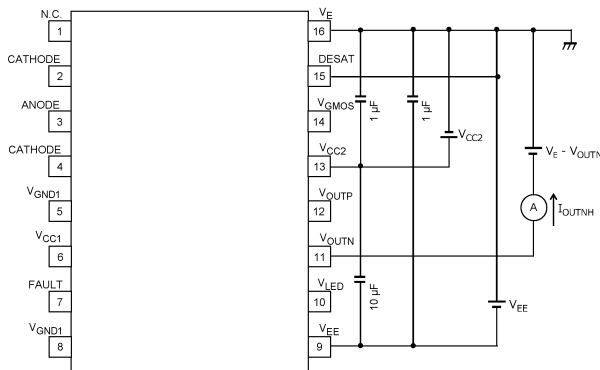


Fig. 13.1.3 I<sub>OUTNH</sub> Test Circuit

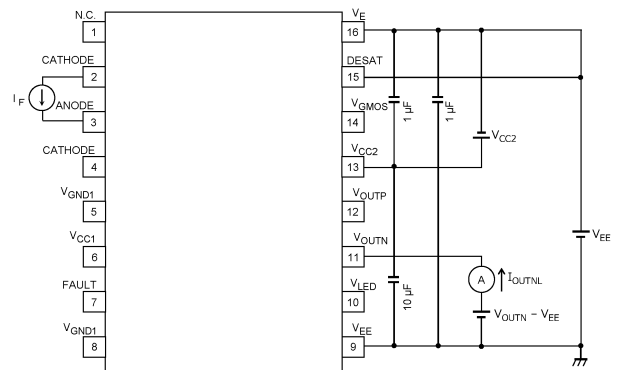


Fig. 13.1.4 I<sub>OUTNL</sub> Test Circuit

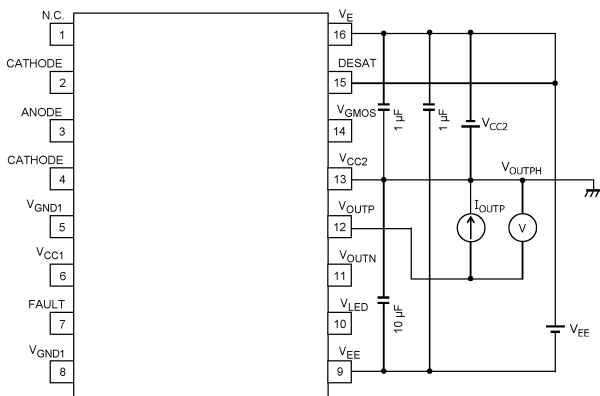


Fig. 13.1.5 V<sub>OUTPH</sub>, R<sub>OUTPH</sub> Test Circuit

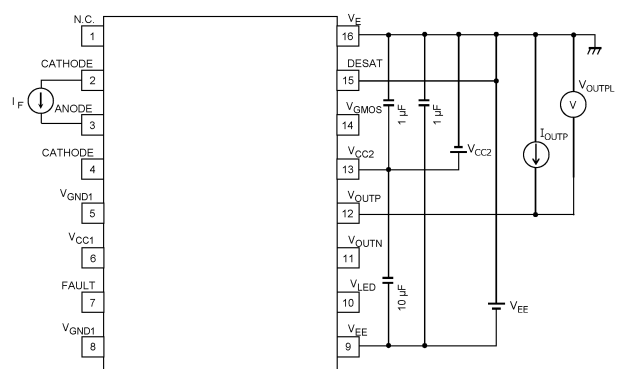


Fig. 13.1.6 V<sub>OUTPL</sub>, R<sub>OUTPL</sub> Test Circuit

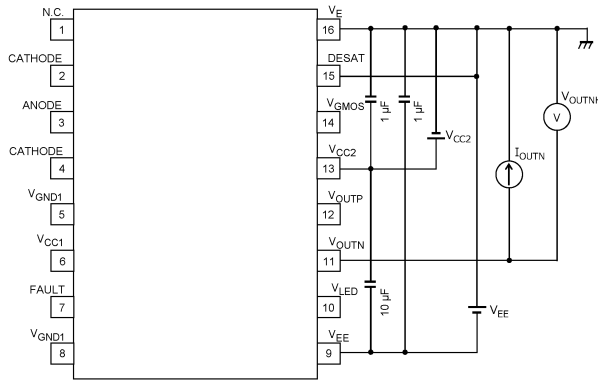


Fig. 13.1.7 V<sub>OUTNH</sub>, R<sub>OUTNH</sub> Test Circuit

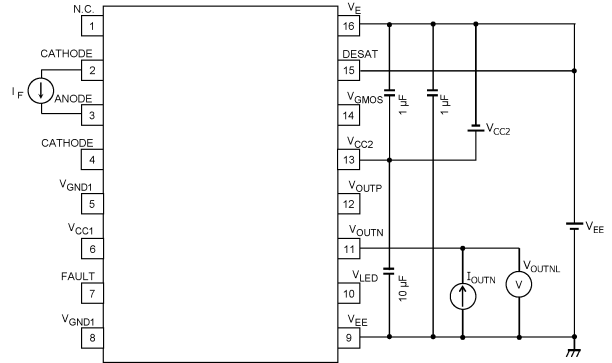


Fig. 13.1.8 V<sub>OUTNL</sub>, R<sub>OUTNL</sub> Test Circuit

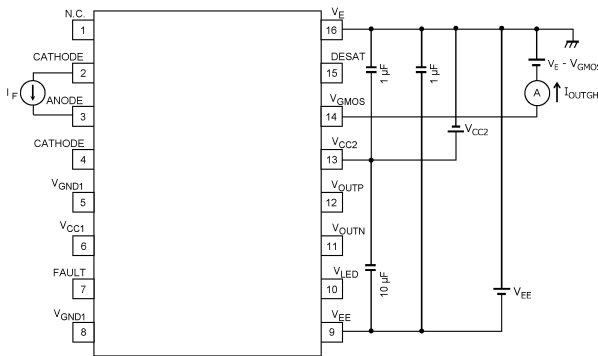


Fig. 13.1.9 I<sub>OUTGH</sub> Test Circuit

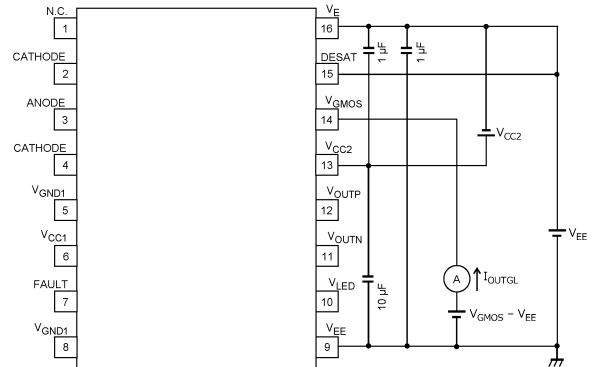


Fig. 13.1.10 I<sub>OUTGL</sub> Test Circuit

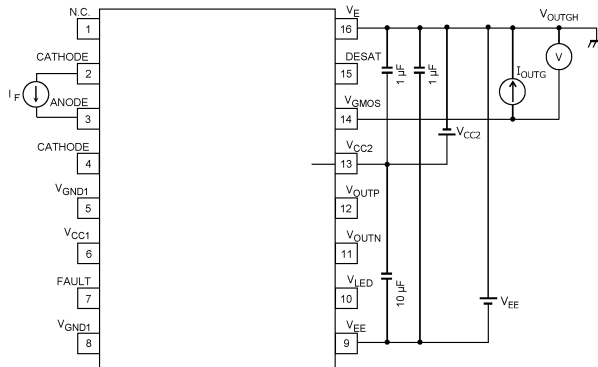


Fig. 13.1.11 V<sub>OUTGH</sub>, R<sub>OUTGH</sub> Test Circuit

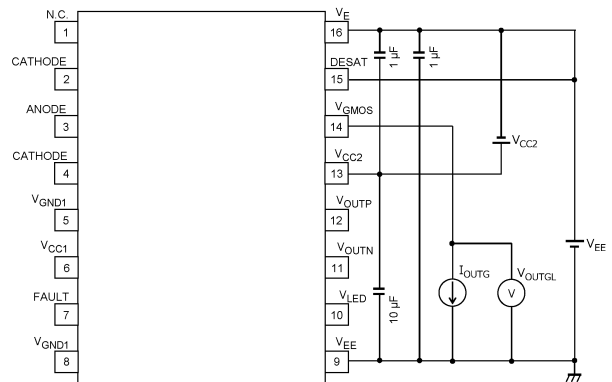


Fig. 13.1.12 V<sub>OUTGL</sub>, R<sub>OUTGL</sub> Test Circuit

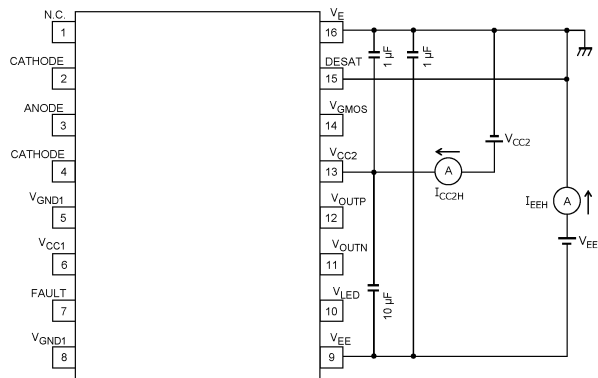


Fig. 13.1.13 I<sub>CC2H</sub>, I<sub>EEH</sub> Test Circuit

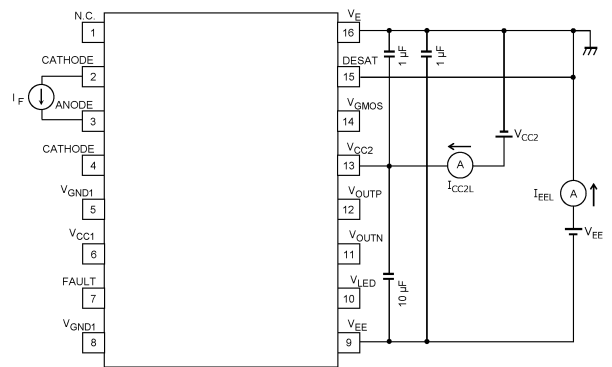


Fig. 13.1.14 I<sub>CC2L</sub>, I<sub>IEEL</sub> Test Circuit



## 13.2. Timing Diagrams

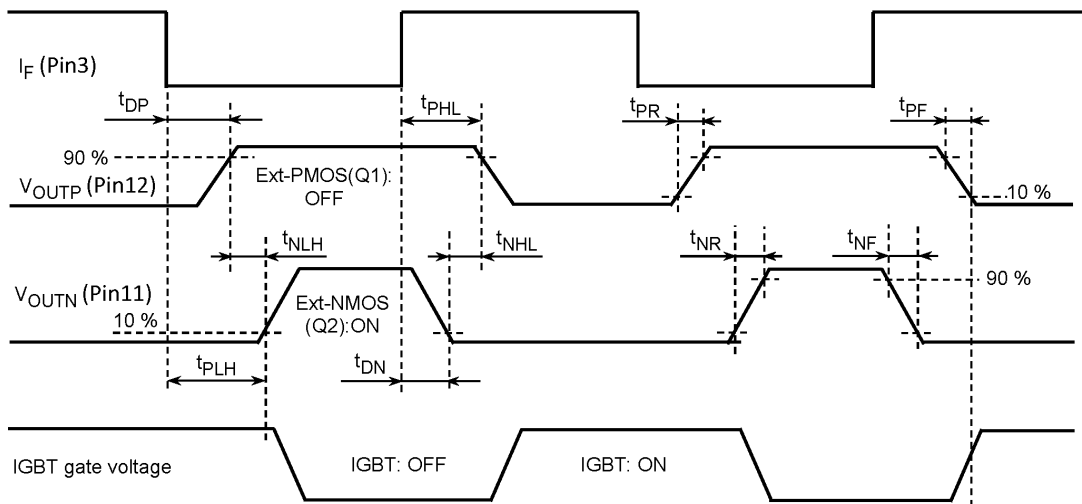


Fig. 13.2.1 Normal State

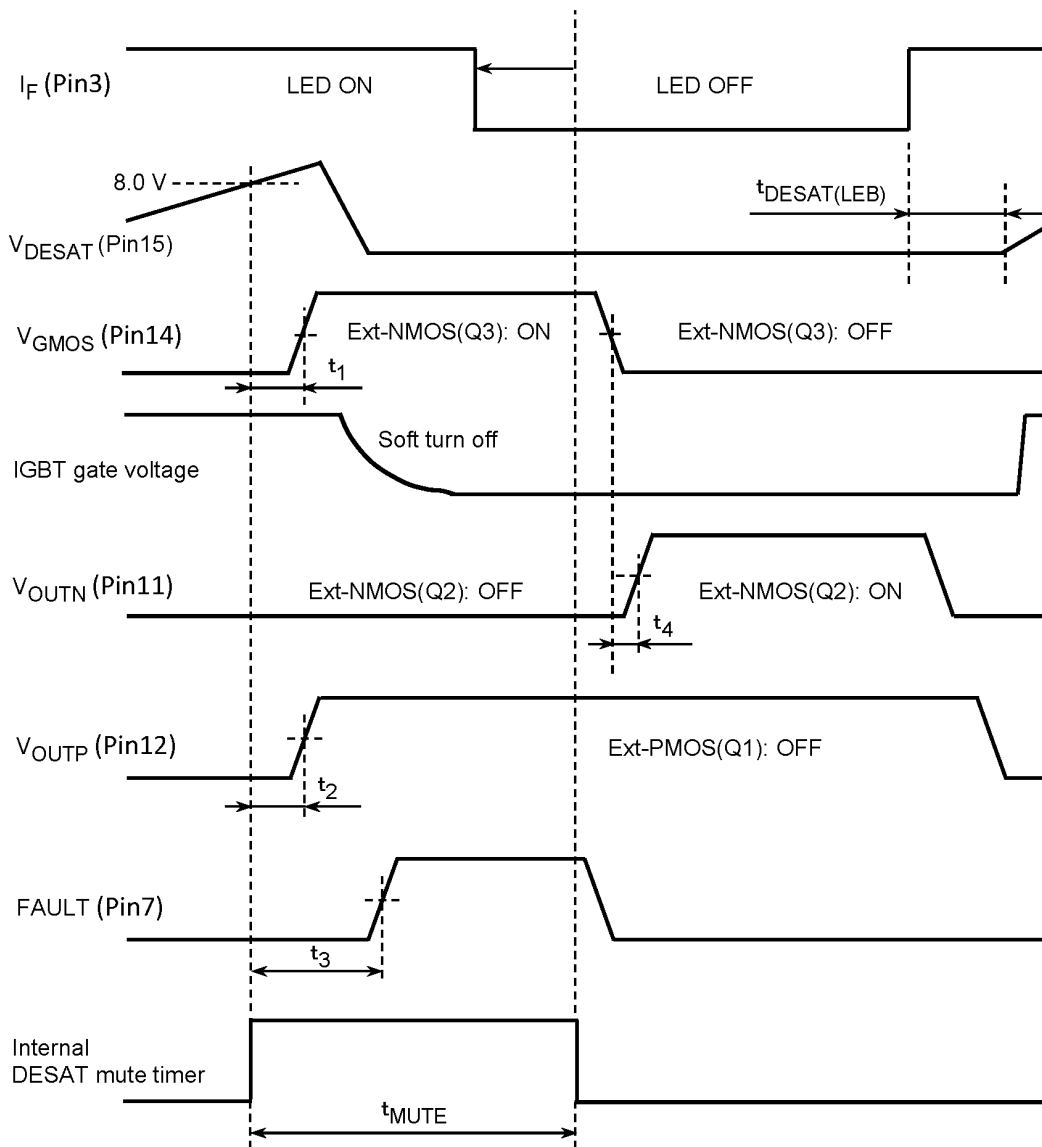
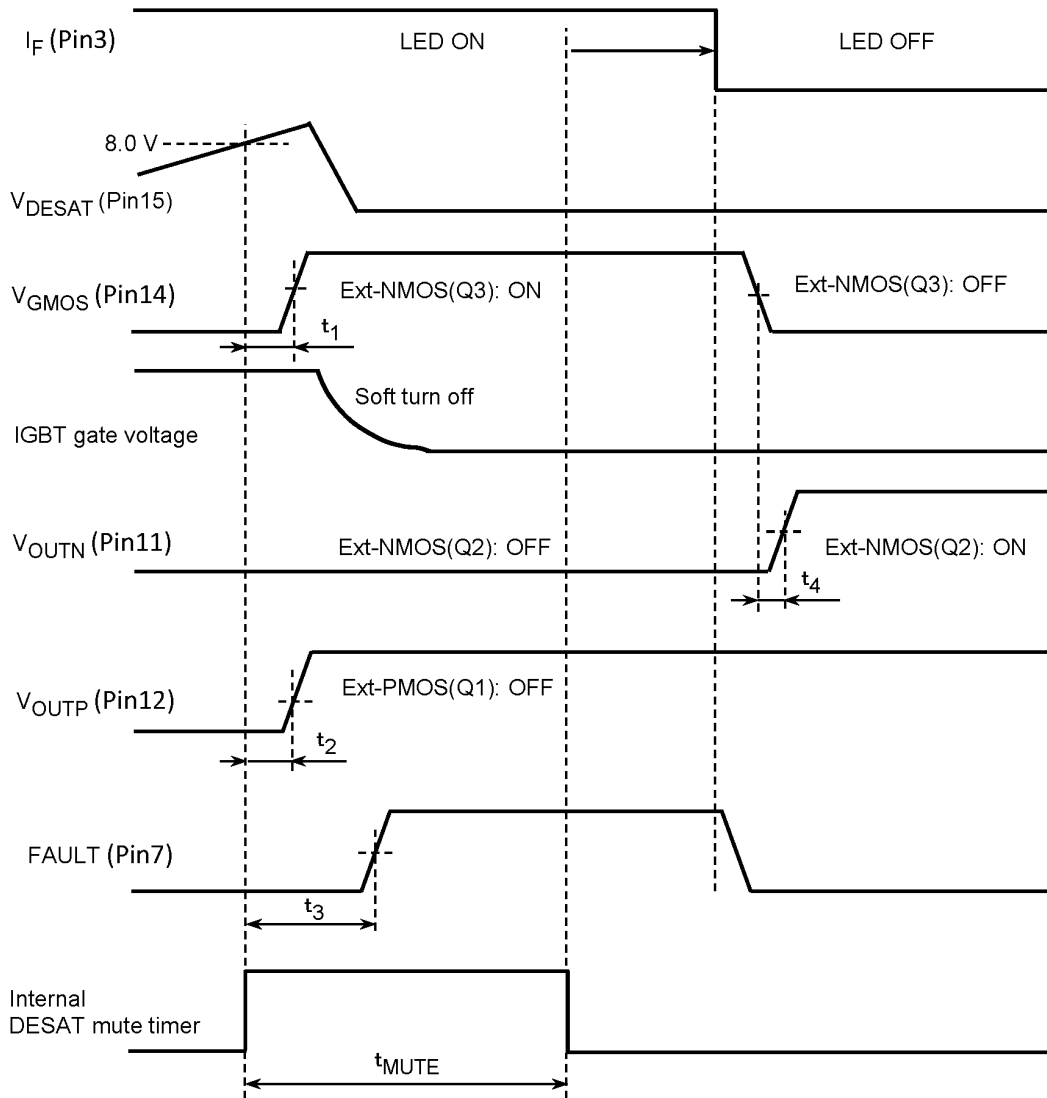
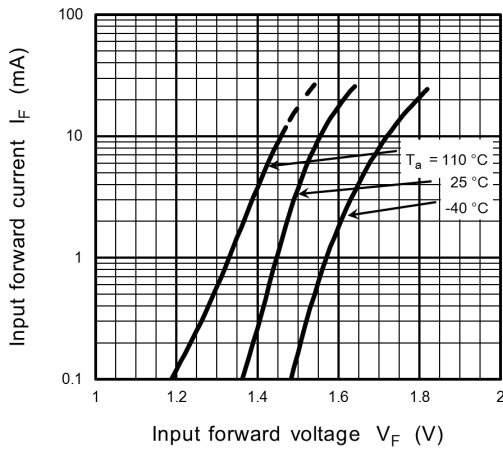


Fig. 13.2.2 DESAT Fault State (the Case that LED is Off within the  $t_{MUTE}$ : Automatic Reset)

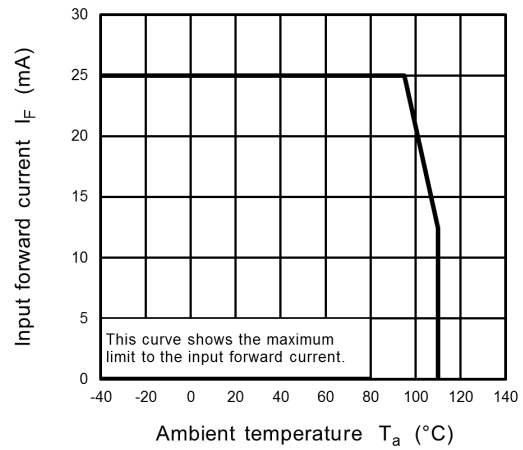


**Fig. 13.2.3 DESAT Fault State (the Case that LED is Off after  $t_{MUTE}$ : Reset by LED Trigger)**

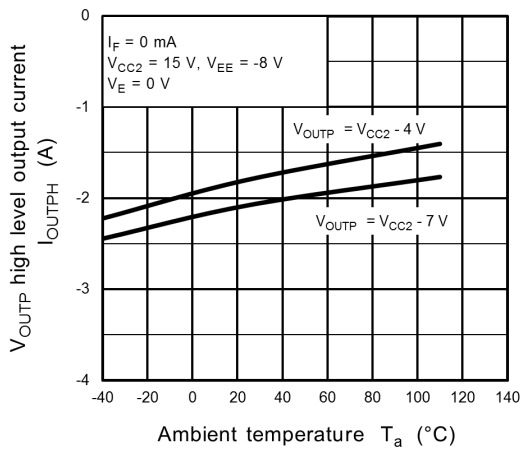
## 13.3. Characteristics Curves (Note)



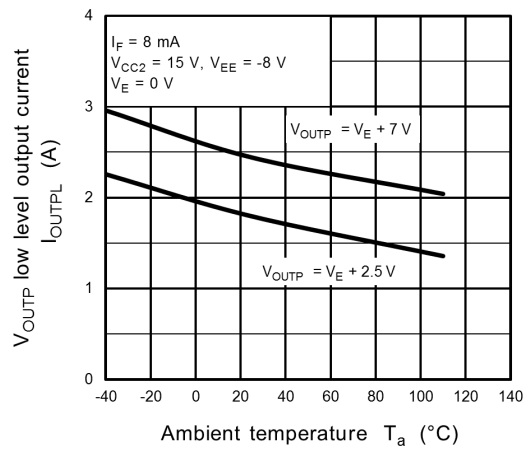
**Fig. 13.3.1  $I_F - V_F$**



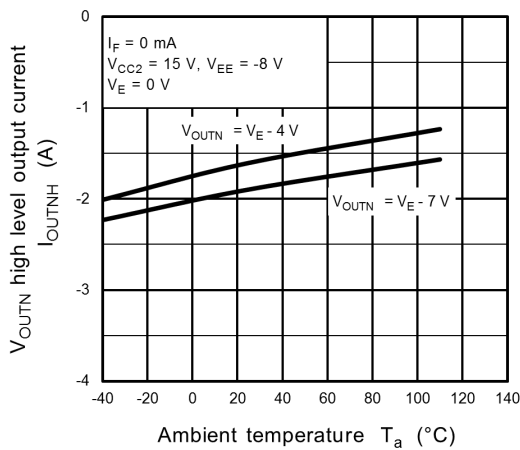
**Fig. 13.3.2  $I_F - T_a$**



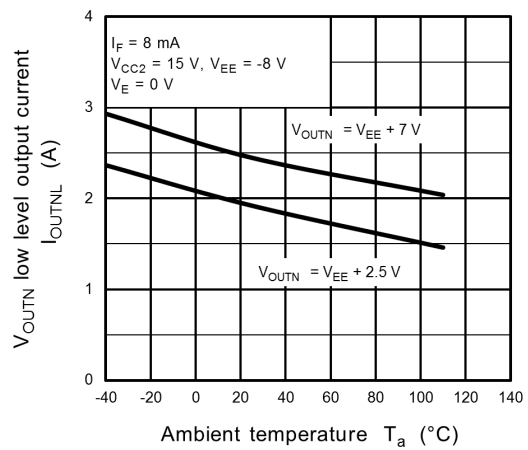
**Fig. 13.3.3  $I_{OUTPH} - T_a$**



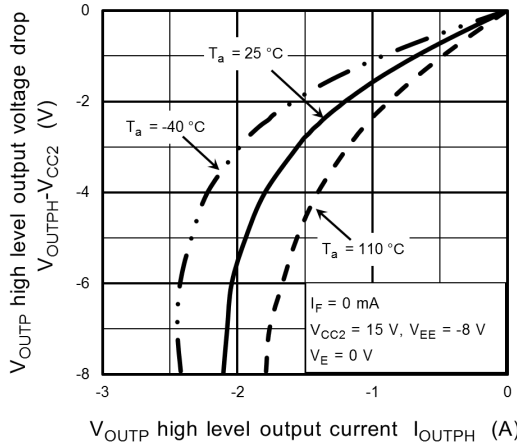
**Fig. 13.3.4  $I_{OUTPL} - T_a$**



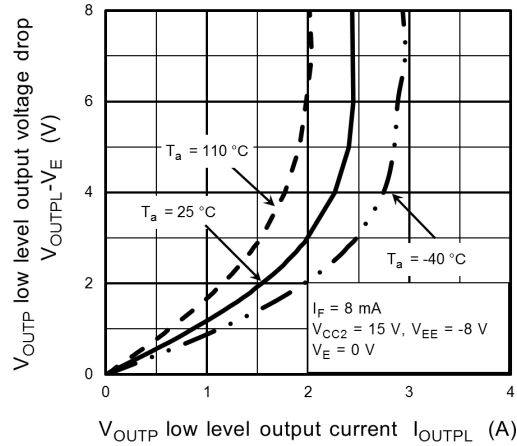
**Fig. 13.3.5  $I_{OUTNH} - T_a$**



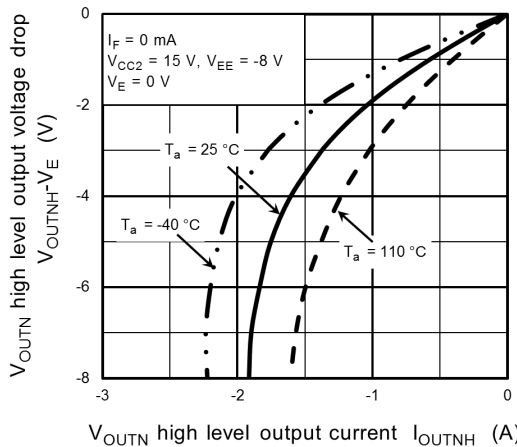
**Fig. 13.3.6  $I_{OUTNL} - T_a$**



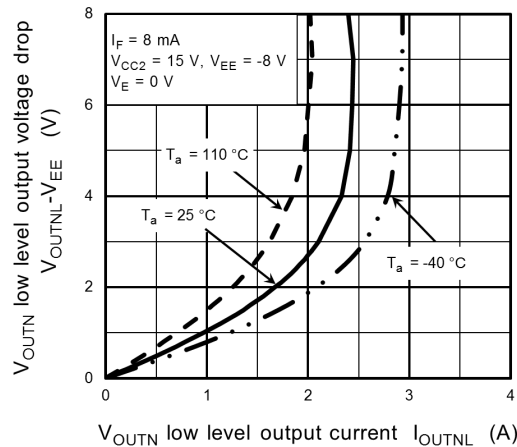
**Fig. 13.3.7**  $(V_{OUTPH} - V_{CC2}) - I_{OUTPH}$



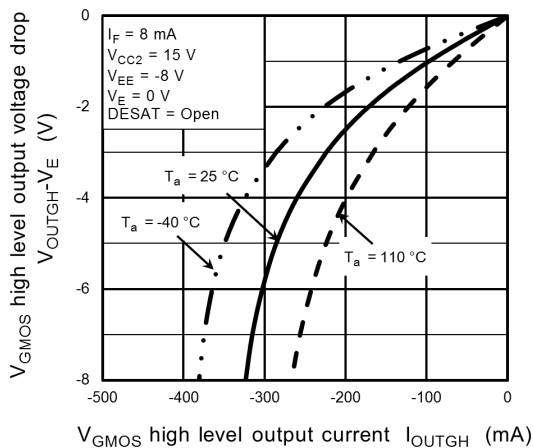
**Fig. 13.3.8**  $(V_{OUTPL} - V_E) - I_{OUTPL}$



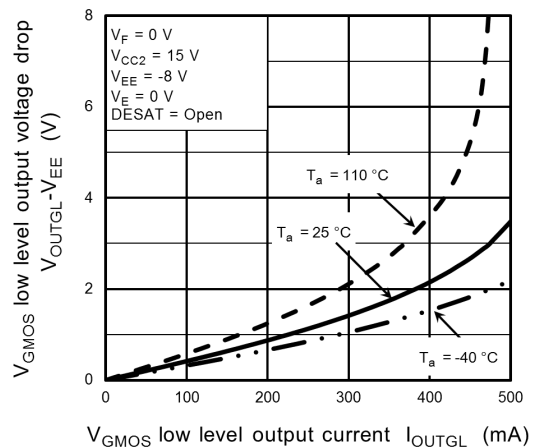
**Fig. 13.3.9**  $(V_{OUTNH} - V_E) - I_{OUTNH}$



**Fig. 13.3.10**  $(V_{OUTNL} - V_{EE}) - I_{OUTNL}$



**Fig. 13.3.11**  $(V_{OUTGH} - V_E) - I_{OUTGH}$



**Fig. 13.3.12**  $(V_{OUTGL} - V_{EE}) - I_{OUTGL}$

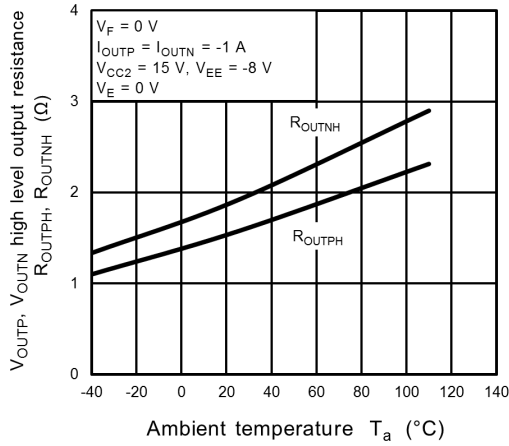


Fig. 13.3.13  $R_{OUTPH}, R_{OUTNH} - T_a$

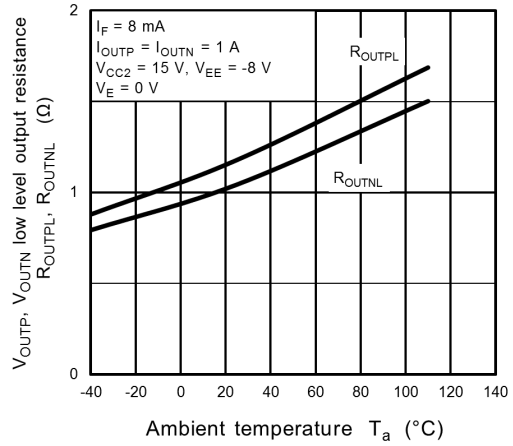


Fig. 13.3.14  $R_{OUTPL}, R_{OUTNL} - T_a$

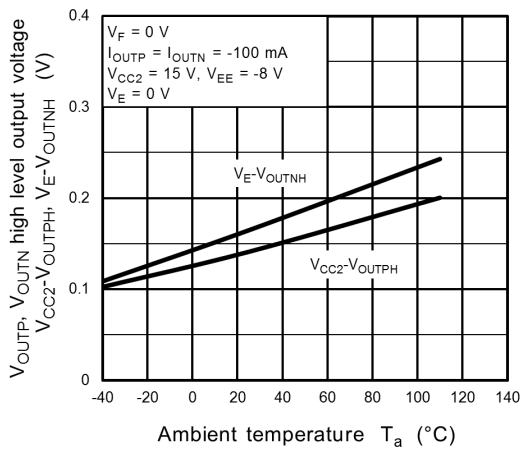


Fig. 13.3.15  $V_{CC2} - V_{OUTPH}, V_E - V_{OUTNH} - T_a$

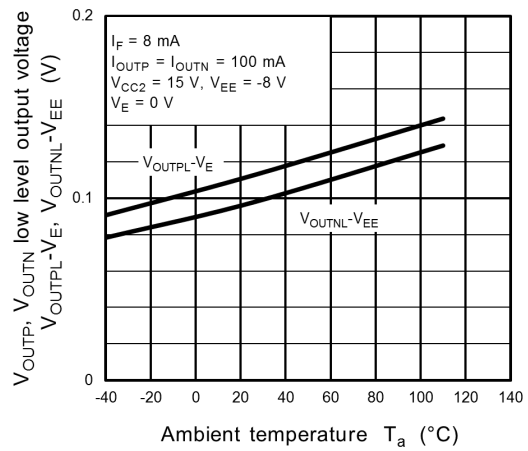


Fig. 13.3.16  $V_{OUTPL} - V_E, V_{OUTNL} - V_{EE} - T_a$

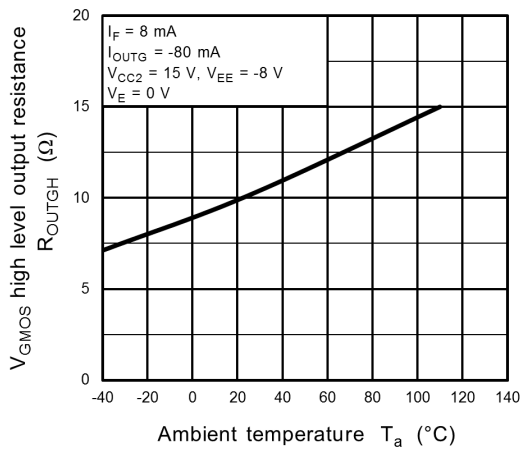


Fig. 13.3.17  $R_{OUTGH} - T_a$

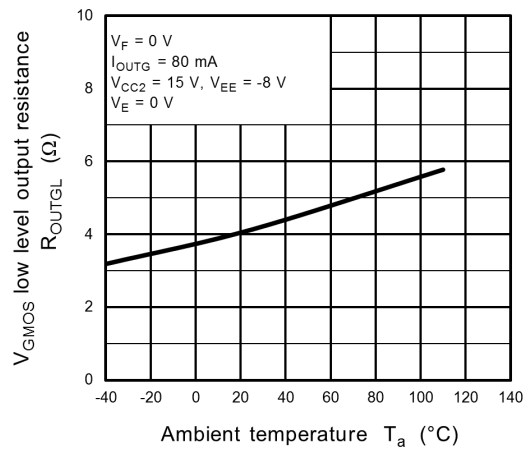


Fig. 13.3.18  $R_{OUTGL} - T_a$

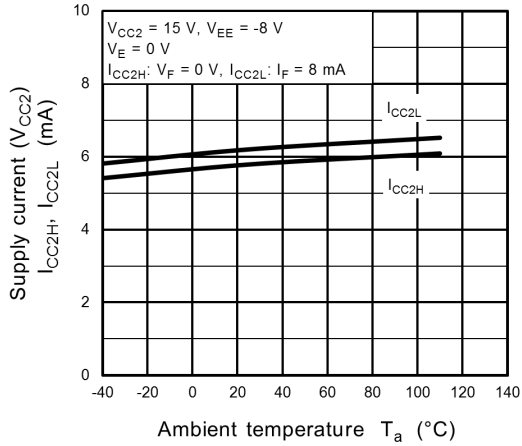


Fig. 13.3.19  $I_{CC2H}, I_{CC2L} - T_a$

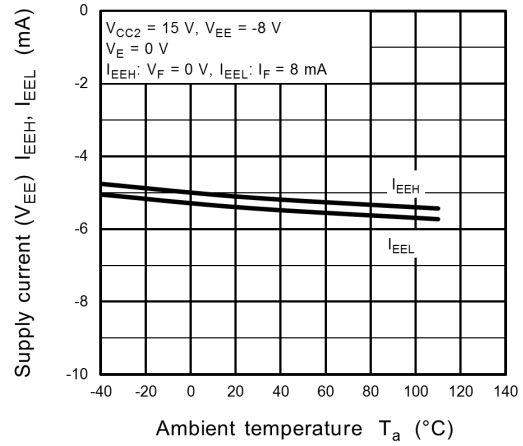


Fig. 13.3.20  $I_{EEH}, I_{EEL} - T_a$

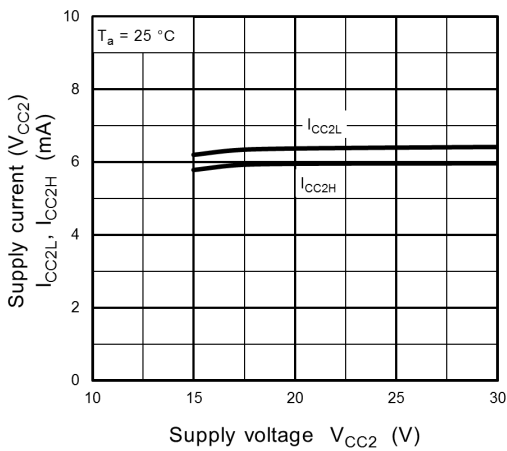


Fig. 13.3.21  $I_{CC2H}, I_{CC2L} - V_{CC2}$

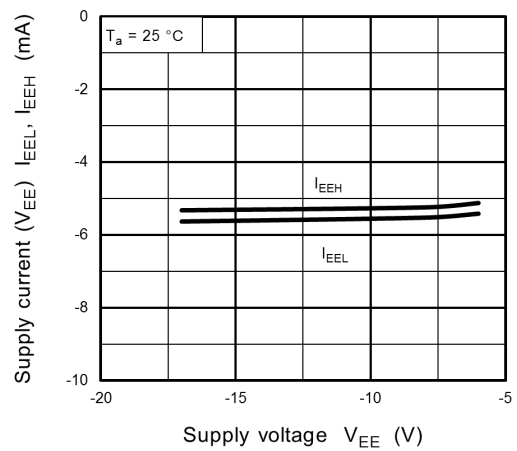


Fig. 13.3.22  $I_{EEH}, I_{EEL} - V_{EE}$

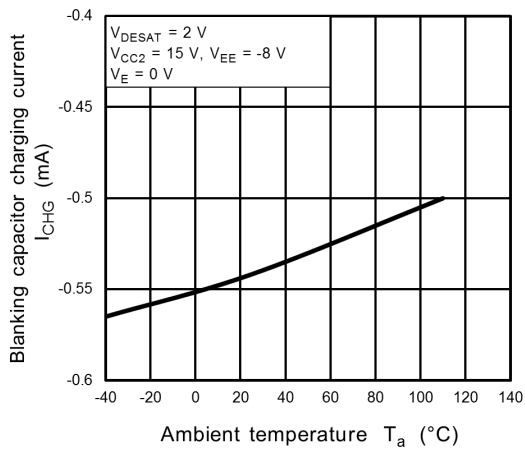


Fig. 13.3.23  $I_{CHG} - T_a$

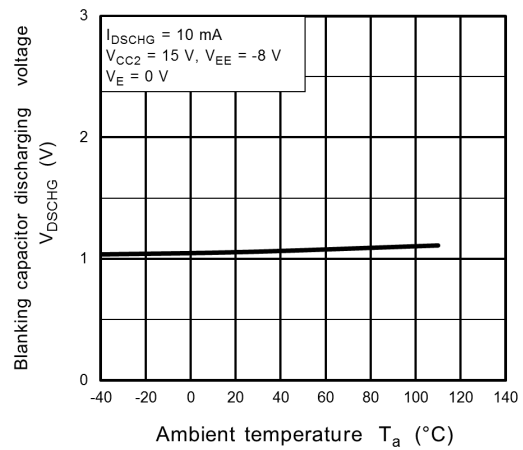
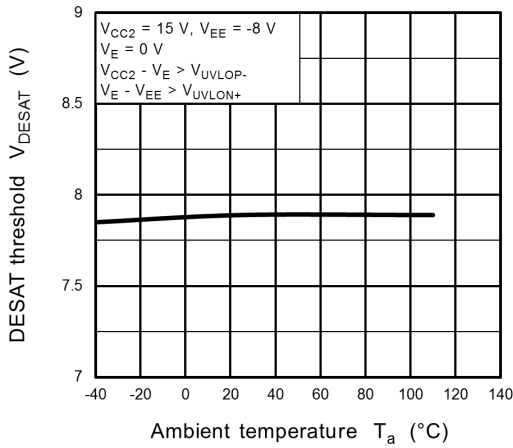
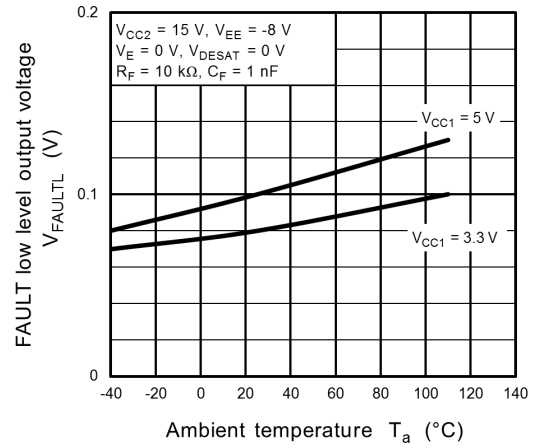


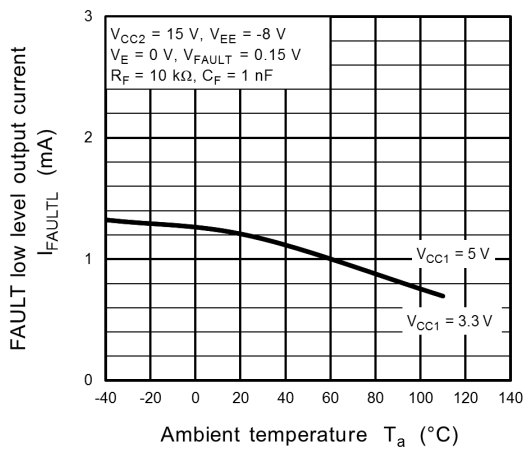
Fig. 13.3.24  $V_{DSCHG} - T_a$



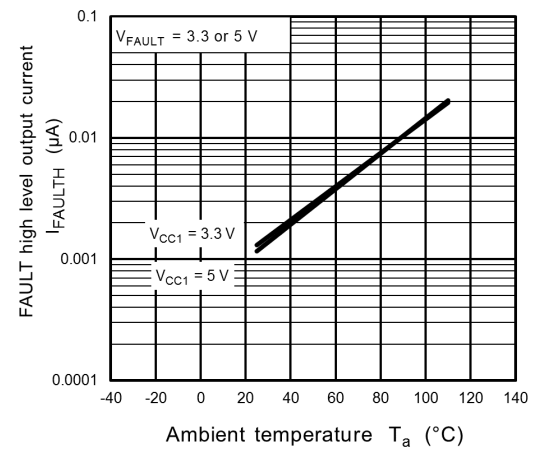
**Fig. 13.3.25**  $V_{DESAT} - T_a$



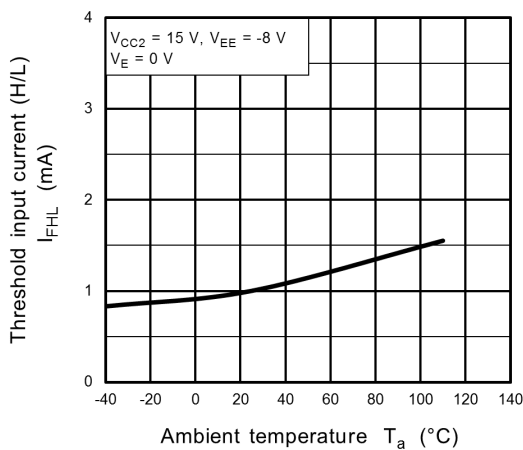
**Fig. 13.3.26**  $V_{FAULTL} - T_a$



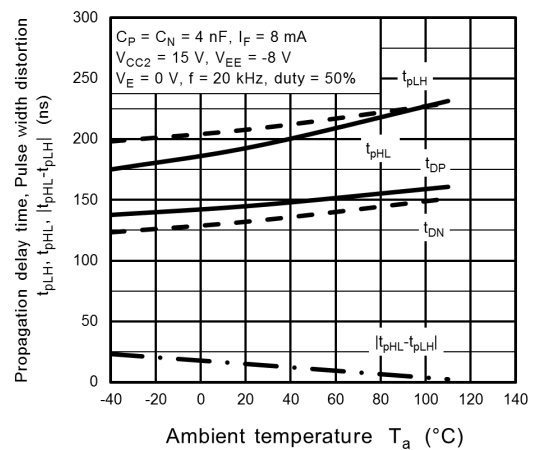
**Fig. 13.3.27**  $I_{FAULTL} - T_a$



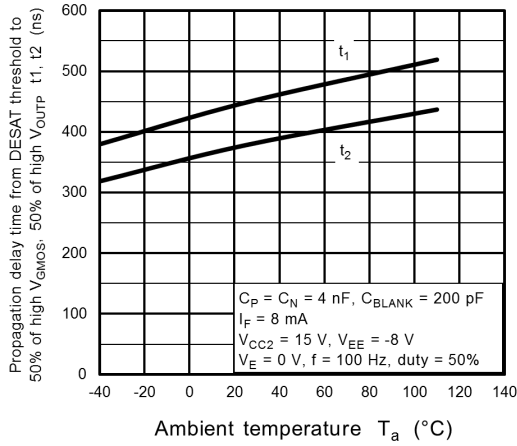
**Fig. 13.3.28**  $I_{FAULTH} - T_a$



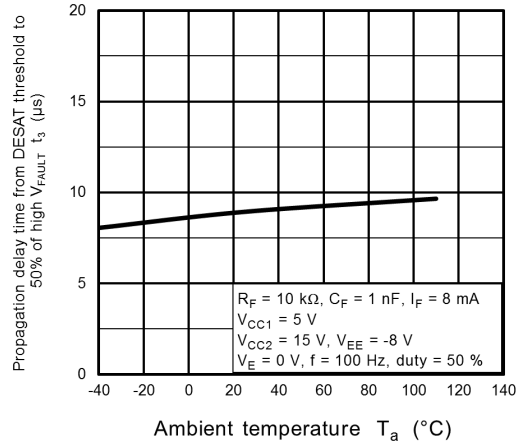
**Fig. 13.3.29**  $I_{FHL} - T_a$



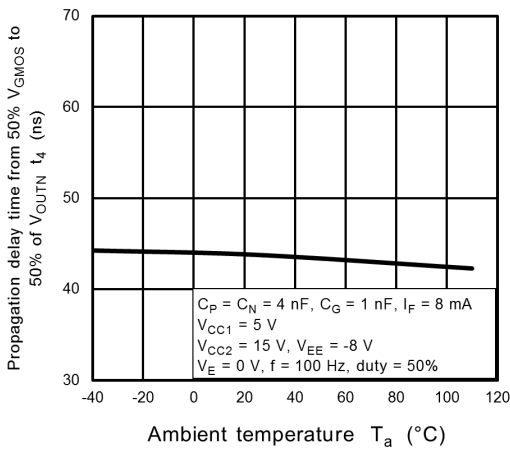
**Fig. 13.3.30**  $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - T_a$



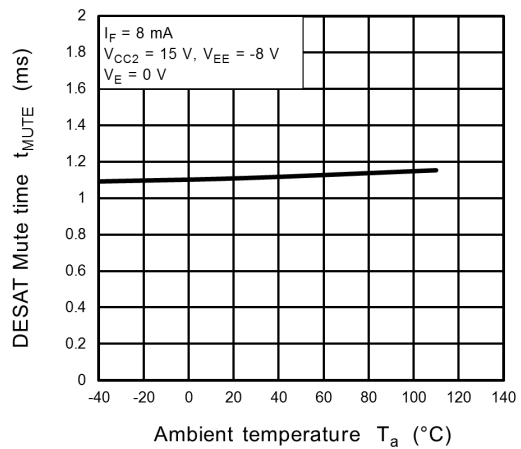
**Fig. 13.3.31  $t_1, t_2 - T_a$**



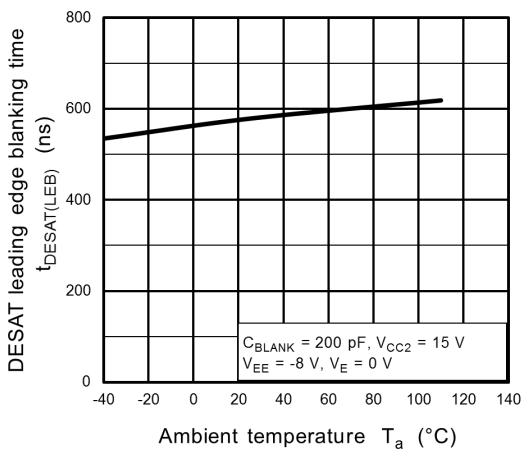
**Fig. 13.3.32  $t_3 - T_a$**



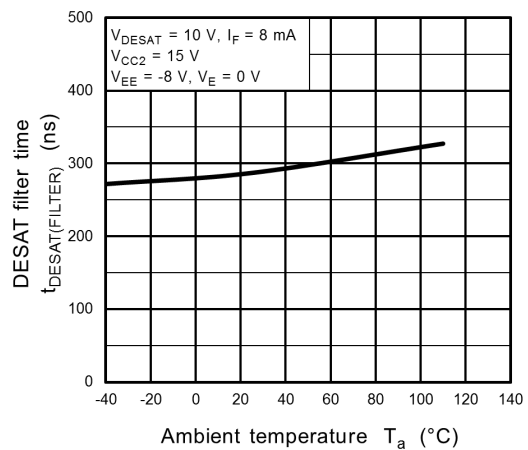
**Fig. 13.3.33  $t_4 - T_a$**



**Fig. 13.3.34  $t_{MUTE} - T_a$**



**Fig. 13.3.35  $t_{DESAT(LEB)} - T_a$**



**Fig. 13.3.36  $t_{DESAT(FILTER)} - T_a$**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 14. Soldering and Storage

### 14.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

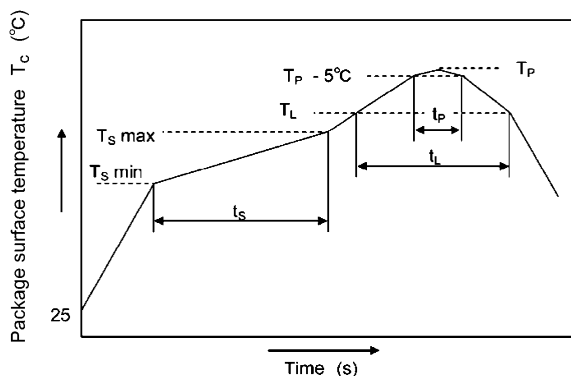
- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.

(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



|  | Symbol | Min | Max | Unit |
|--|--------|-----|-----|------|
| Preheat temperature  | $T_S$  | 150 | 200 | °C   |
| Preheat time   | $t_s$  | 60  | 120 | s    |
| Ramp-up rate ( $T_L$ to $T_P$ )                            |        |     | 3   | °C/s |
| Liquidus temperature                                       | $T_L$  | 217 |     | °C   |
| Time above $T_L$   | $t_L$  | 60  | 150 | s    |
| Peak temperature   | $T_P$  |     | 260 | °C   |
| Time during which $T_c$ is between ( $T_P - 5$ ) and $T_P$ | $t_p$  |     | 30  | s    |
| Ramp-down rate ( $T_P$ to $T_L$ )                          |        |     | 6   | °C/s |

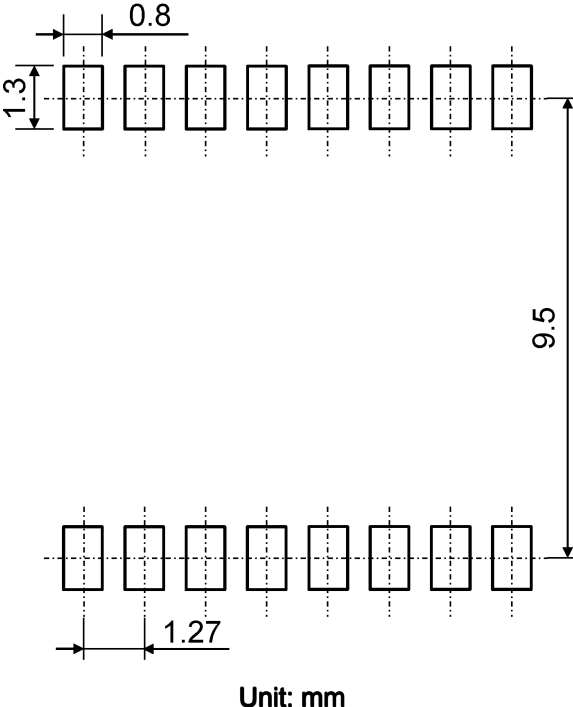
**An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used**

- When using soldering flow  
Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.  
Mounting condition of 260 °C within 10 seconds is recommended.  
Flow soldering must be performed once.
- When using soldering Iron  
Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C  
Heating by soldering iron must be done only once per lead.

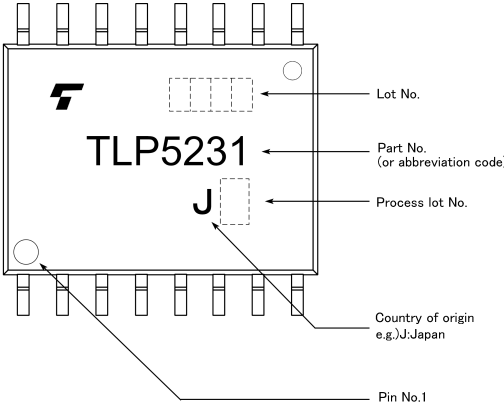
### 14.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

15. Land Pattern Dimensions (for reference only)



16. Marking



## 17. EN 60747-5-5 Option (D4) Specification

- Part number: TLP5231 (**Note 1**)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN 60747.

Example: TLP5231(D4-TP,E)

D4: EN 60747 option

TP: Tape type

E: [[G]]/RoHS COMPATIBLE (**Note 2**)

Note 1: Use TOSHIBA standard type number for safety standard application.

e.g., TLP5231(D4-TP,E → TLP5231

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

| Description   | Symbol   | Rating  | Unit           |
|---|--|---|----------------|
| Application classification<br>for rated mains voltage ≤ 600 Vrms<br>for rated mains voltage ≤ 1000 Vrms   |  | I-IV<br>I-III   | —              |
| Climatic classification   |  | 40 / 110 / 21   | —              |
| Pollution degree  |  | 2   | —              |
| Maximum operating insulation voltage  | VIORM  | 1230  | Vpeak          |
| Input to output test voltage, Method A<br>V <sub>pr</sub> = 1.6 × VIORM, type and sample test<br>t <sub>p</sub> = 10 s, partial discharge < 5 pC  | V <sub>pr</sub>                                      | 1970  | Vpeak          |
| Input to output test voltage, Method B<br>V <sub>pr</sub> = 1.875 × VIORM, 100 % production test<br>t <sub>p</sub> = 1 s, partial discharge < 5 pC  | V <sub>pr</sub>                                      | 2310  | Vpeak          |
| Highest permissible overvoltage<br>(transient overvoltage, t <sub>pr</sub> = 60 s)  | VTR  | 8000  | Vpeak          |
| Safety limiting values (max. permissible ratings in case of fault,<br>also refer to thermal derating curve)<br>current (input current I <sub>F</sub> , P <sub>SO</sub> = 0)<br>power (output or total power dissipation)<br>temperature | I <sub>si</sub><br>P <sub>so</sub><br>T <sub>s</sub> | 400<br>1200<br>175  | mA<br>mW<br>°C |
| Insulation resistance<br>V <sub>IO</sub> = 500 V, T <sub>a</sub> = 25 °C<br>V <sub>IO</sub> = 500 V, T <sub>a</sub> = 100 °C<br>V <sub>IO</sub> = 500 V, T <sub>a</sub> = T <sub>s</sub>  | R <sub>si</sub>                                      | ≥ 10 <sup>12</sup><br>≥ 10 <sup>11</sup><br>≥ 10 <sup>9</sup> | Ω              |

Fig. 17.1 EN 60747 Insulation Characteristics

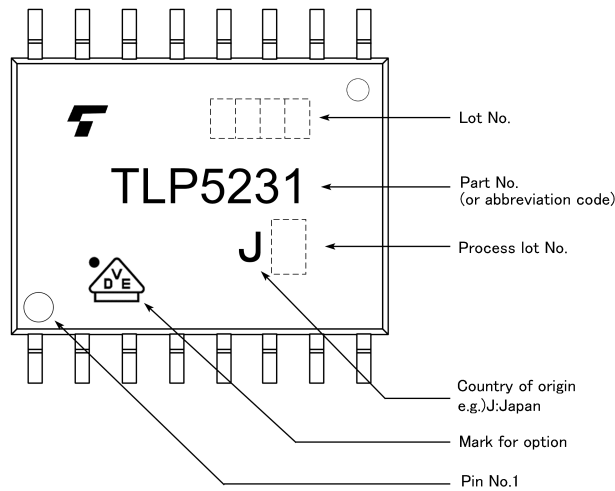
|                              |     |        |
|------------------------------|-----|--------|
| Minimum creepage distance    | Cr  | 8.0 mm |
| Minimum clearance            | Cl  | 8.0 mm |
| Minimum insulation thickness | ti  | 0.4 mm |
| Comparative tracking index   | CTI | 500    |

**Fig. 17.2 Insulation Related Specifications (Note)**

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.



**Fig. 17.3 Marking on Packing for EN 60747**



**Fig. 17.4 Marking Example (Note)**

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.

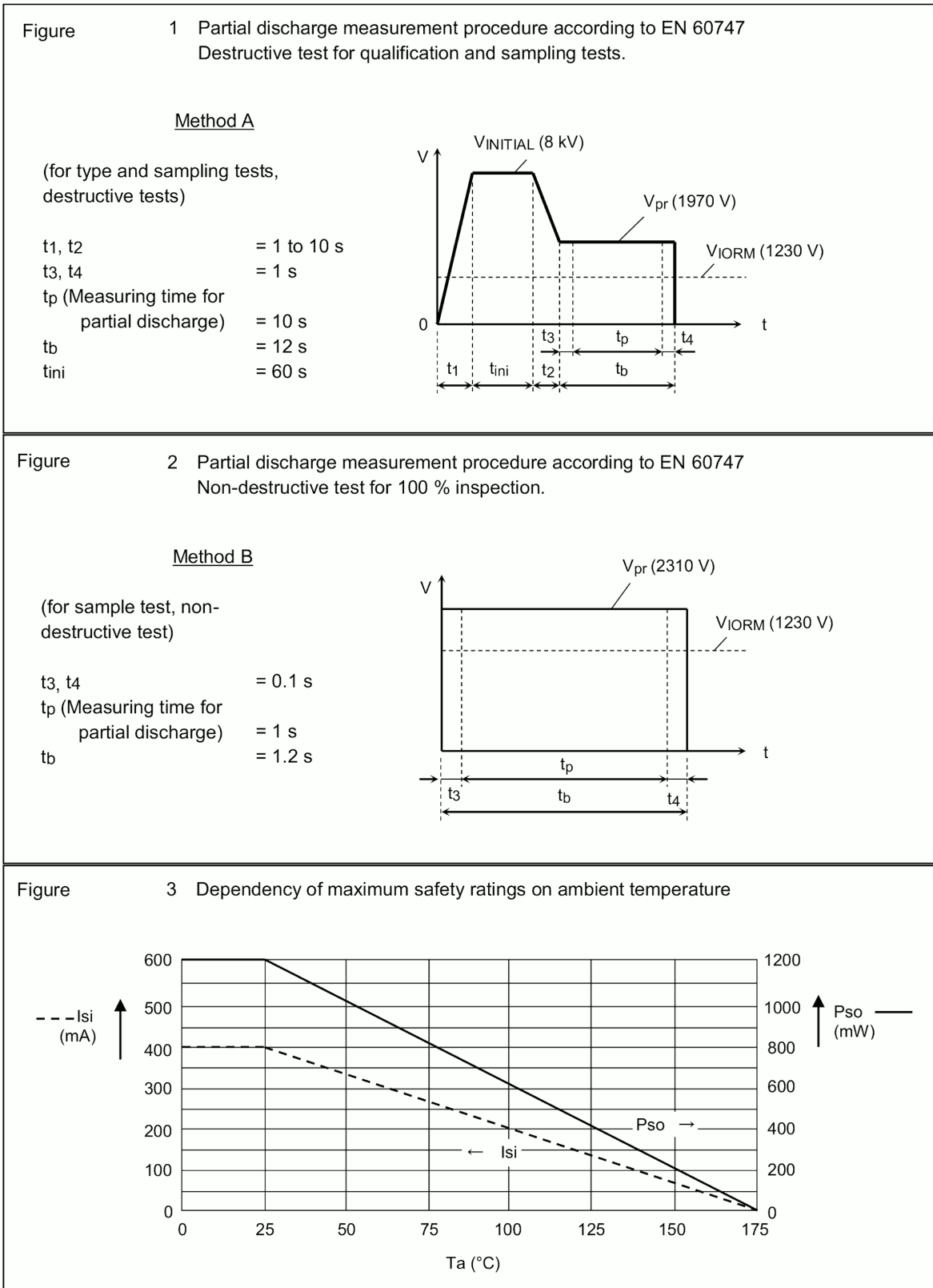


Fig. 17.5 Measurement Procedure

## 18. Ordering Information (Example of Item Name)

| Item Name        | VDE Option   | Packing (MOQ)            |
|------------------|--------------|--------------------------|
| TLP5231(E)       |              | Magazine (50 pcs)        |
| TLP5231(TP,E)    |              | Tape and reel (1500 pcs) |
| TLP5231(D4,E)    | EN 60747-5-5 | Magazine (50 pcs)        |
| TLP5231(D4-TP,E) | EN 60747-5-5 | Tape and reel (1500 pcs) |



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